Stirling Convertor Controller Development at NASA Glenn Research Center

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For nearly two decades, NASA Glenn Research Center (GRC) has been supporting the development of Radioisotope Power Systems (RPS). NASA desires higher conversion efficiency RPS options that are reliable and robust with long life design. Dynamic conversion, such as Stirling and Brayton, offer the potential for higher conversion efficiencies than current RPS but have yet to be demonstrated in a flight application. The RPS program sent out a solicitation to investigate options for dynamic conversion technologies. As a result of this solicitation, four dynamic power convertor (DPC) technologies were selected for design and three are proceeding to the fabrication phase of prototype dynamic convertors. One lesson learned from the Advanced Stirling Radioisotope Generator (ASRG) project is that controller development should be coordinated with the development of a dynamic convertor. As a result of this, NASA GRC has been utilizing hardware from past Stirling convertor projects including that of the ASRG to support controller development for the DPC's. NASA GRC has developed a strong knowledge base on both analog and digital Stirling dynamic power convertor controllers and will continue to expand and apply that knowledge to the DPC's. Over the past 15 years, controllers were developed at GRC, at Lockheed Martin (LM) and by the Johns Hopkins University/Applied Physics Laboratory (JHU/APL). Various generations of the controllers have been developed as lessons were learned through various component and system level tests. Some of the tests performed were fault tolerance, flight acceptance vibration, electromagnetic interference (EMI), spacecraft integration, and extended operation. The fault tolerance test characterized the controller's ability to handle various fault conditions, including high or low bus power consumptions, total open load or short circuit, and replacing a failed controller card while the backup maintains control of the Stirling convertor. The vibration test confirms the controller's ability to control an ASC during launch. The EMI test characterized the AC and DC magnetic and electric fields emitted by the single ASC and if the controller has an impact on the radiated EMI. Spacecraft integration testing in the Radioisotope Power Systems System Integration Laboratory (RSIL) provided insight into the electrical interactions between the representative RPS, its associated control schemes, and realistic electric system loads. The extended operation test allows data to be collected over a period of thousands of hours to obtain long term performance data of the system. This paper describes the history of controller development at NASA GRC, tests performed on these controllers, and lessons learned.

Nomenclature

ACU	=	advanced Stirling convertor control unit
A/D	=	analog to digital
AMSC	=	American Superconductor
APS	=	ASC piston sensor
ASC	=	advanced Stirling convertor
ASRG	=	advanced Stirling radioisotope generator
D/A	=	digital to analog
DASCS	=	dual advanced Stirling convertor simulator
DCC	=	dual convertor controller
DSP	=	digital signal processor
EDU	=	engineering development unit

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EM = engineering model
EMF = electromotor force
GRC = Glenn Research Center
GSE = ground support equipment
FMEA = functional failure modes effects analysis
FPGA = field programmable gate array
FTB = frequency test bed
IEEE = Institute for Electrical and Electronics Engineers
ILN = international lunar network
JHU/APL = the Johns Hopkins University/Applied Physics Laboratory
LAR = linear AC regulator
LM = Lockheed Martin
LMCT = Lockheed Martin/Coherent Technologies
PMAD = power management and distribution system
PWM = pulse width modulation
RMS = root mean square
RPS = radioisotope power system
RSIL = radioisotope power system systems integration laboratory
SCC = single convertor controller
SDL = Structural Dynamics Laboratory
SDM = system dynamic model
SRL = Stirling Research Laboratory
STC = Stirling technology company
TDC = technology demonstration convertor
ZDC = Zener-diode controller

I. Introduction

Free-piston Stirling convertors, that includes an engine coupled to a linear alternator, require a controller to maintain stable operation. During each engine cycle, the load must be modulated to dissipate all the power being produced. If the controller does not dissipate all the power, the excess would flow into the resonating piston motion, increasing amplitude, and ultimately resulting in damage to internal convertor components. Similarly, if the controller dissipated more power than that being produced, the balance would be extracted from the resonating piston motion, ultimately causing a stall of the engine cycle. The controller also provides a regulated user voltage at its output. Typically, to provide DC, the controller rectifies the alternator output, and then modulates the applied load to maintain a specified output voltage. Analog controllers used in the laboratory environment at GRC modulate the load because they are also providing the load. In an actual application, the controller will not modulate the load but rather condition the power.

Since 2003, five Stirling convertor controllers, summarized in Table I, have been tested at NASA GRC and designed under GRC guidance. Each controller was designed for a different application. The controllers include an analog Zener-diode controller (ZDC), an analog Linear AC Regulator (LAR), digital Single Convertor Controller (SCC), digital DCC (Dual Convertor Controller), and a digital Engineering Development Unit (EDU) Advanced Stirling Convertor Control Unit (ACU). The SCC, DCC, and ACU are considered digital controllers because they use field programmable gate arrays (FPGAs) to implement control algorithms and other functionality. The digital controllers use power electronics technology to eliminate the need for tuning capacitors to compensate for alternator inductance. They incorporate high-frequency pulse-width modulated (PWM) switching of an h-bridge to control the convertors[1]. The digital controllers were designed for use with ASCs but the same approach can be used with other convertors. The digital controller functions include[2]:

- rectifying the AC power from the Stirling convertors
- synchronizing the two convertors to reduce disturbance force (DCC and ACU only)
- controlling the convertors' operating frequency and voltage (which then controls the piston amplitude)
- providing power to the spacecraft's DC power bus over a voltage range, with capability to handle over-voltage and under-voltage conditions
- receiving and responding to commands from the spacecraft
- providing telemetry to the spacecraft

- incorporating fault management functionality at the controller box level and integrating into the spacecraft's fault management system.

The digital controllers are all fault tolerant and can autonomously switch from a primary controller to a backup controller. The ability to transfer control of an ASC from a primary controller to a spare should be available at any time. Fault detection requirements for a digital controller include:

- Maintain ASC operation in the event of an internal controller failure.
- Maintain command and telemetry communication between the spacecraft and the controller communication bus.
- Prevent propagation of faults to other cards within the controller.

The analog ZDC and LAR are lab controllers and do not provide the same functions as the digital controllers although they could be modified to include these other functions. In addition, the ZDC and LAR require the use of tuning capacitors to passively correct the power factor. For Stirling convertors with a lower inductance, capacitors could potentially have a large mass and volume and could be unattractive for spacecraft applications. On the other hand, it may be possible to find flight-rated, long-life capacitors for Stirling convertors with a higher inductance. Analog controllers are being considered because they could potentially be simpler to design and more reliable depending on spacecraft requirements.

The ZDC and LAR controller functions include:

- rectifying the AC power from the Stirling convertors
- synchronizing the two convertors to reduce disturbance force
- controlling the convertors' voltage (which then controls the piston amplitude)

Table 1. Comparison of Stirling controllers at GRC.

	Zener-Diode	Zener-Diode	Linear AC Regulator	SCC	ACU	DCC
Design/Manufacturer	GRC/Stirling Technology Company (STC)	GRC	GRC	APL	LMCT	APL
Type of Convertor	TDC	ASC	ASC	ASC	ASC	ASC
# of Convertors	2	2	2	1	2	2
Tuning Cap	Yes	Yes	Yes	No	No	No
Engineering Model	No	No	No	Yes	Yes	Yes
Set Point Control	Potentiometer	Potentiometer	Potentiometer	RS-422	MIL-STD-1553	RS-422
Telemetry	No	No	No	Yes	Yes	Yes
Analog/Digital	Analog	Analog	Analog	Digital	Digital	Digital
Spacecraft Bus Voltage Range	N/A	N/A	N/A	22-36	22-34	22-36
Extended Operation	>110,000	>15,000	No	>36,000	2,000	No
Delivered	2003	2006	2007	2011	2014	2015
AC Input Voltage	Up to 80V	Up to 12 V	Up to 12 V	Up to 15 V	Up to 22 V	Up to 22 V
Application	Laboratory – air	Laboratory – thermal vacuum	ASRG simulator	International Lunar Network (ILN)	ASRG	SCC upgrade

Prior to operation of a controller with actual hardware, there are several steps involved in the development and verification of controller functionality. For the analog controllers, this includes circuit simulations, bench testing with an AC source, and then operation of the controller with actual convertors at full power output. For digital controllers, the development and verification involves additional steps. This includes circuit simulations, testing the controller algorithms and functionality with a software model of the convertor, bench testing with an AC source, operating with a Dual Advanced Stirling Convertor (DASCS) which is described in Section II or a LMCT designed engine simulator, and then operating with the actual convertors at full power output.

II. Stirling Convertors and Support Equipment

This section describes the equipment used to test the controllers. These include the Advanced Stirling Convertor (ASC), EE-35, Technology Demonstration Convertor (TDC), Frequency Test Bed (FTB), the Dual Advanced Stirling Convertor Simulator (DASCS), and test rack support equipment. The EE-35, ASC, and FTB were designed by Sunpower, Inc. The DASCS was designed by the Johns Hopkins University Applied Physics Laboratory (JHU/APL). The TDC was designed by American Superconductor (AMSC), formerly Stirling Technology Company (STC)/Infinia.

A. Stirling Convertors

Over the past 18 years, different types of Stirling convertors have been developed to support RPS-related applications at GRC. From a controller perspective, the main difference between each of these convertors is their alternator parameters and operating frequency as described in Table 2.

Table 2. Summary of Convertor Alternator Parameters.

	RMS Alternator Voltage (V)	RMS Alternator Current (A)	Alternator Power (W)	Operating Frequency (Hz)
TDC	85	0.8	65	82
EE-35	25	1.5	35	106.5
FTB	20	5	75	106
ASC-1	12	7	75	103
ASC-L	12	10	75	102.2
ASC-E3	18	6	75	102.2
DASCS-12	12	7	75	103
DASCS-18	18	6	75	102.2

B. DASCS

The DASCS has been used to support controller design and development since 2011. It was developed using custom-designed circuits, commercial equipment, and a linearized ASC model[3] implemented in software on an off-the-shelf digital signal processor (DSP). Alternator inductance and resistance are modeled with physical components with electrical properties similar to the actual alternator in series with a back emf voltage source.

The DASCS was developed in order to provide a simulator that better represents an ASC. Previous engine simulator designs used an AC source, resistor, and inductor and only modeled electrical performance with no consideration of convertor mechanical behavior. Designers frequently found that their controllers did not function the same with an ASC as with their engine simulator. The impact of controller problems like AC input current sampling noise or spacecraft bus voltage changes on mechanical parameters like piston amplitude could only be investigated using time-consuming testing with a real ASC. In addition, damage to the ASC might occur during such evaluations.

The initial version of the simulator was developed for testing the SCC with a single ASC. Since the single ASC simulator helped to solve numerous problems with the SCC, it was decided to build a DASCS which simulates the operation of a pair of ASCs. The DASCSs simulate both ASCs with alternators in the 12 or 18 V range.

The DASCS has been used to test the SCC, DCC, and the ACU. Several controller tests were first performed with the DASCS prior to operation with ASCs; these tests include full power operation, fault testing, and Radioisotope Power Systems System Integration Laboratory (RSIL) testing. Performing these tests first with the DASCS is a risk-reduction to the ASCs. There have been instances in controller testing with the DASCS where issues were identified and if the test was performed with the ASC instead it could have caused damage to the ASCs.

C. Test Rack

Test racks are used for each of the tests described in this paper and are customized to support each type of controller. Each test rack provides the means for measuring and collecting data for observing operating trends. It

provides the interfaces needed for the controllers and provides mechanisms to ensure the safety of the convertors. Each test article is instrumented to measure output characteristics such as alternator voltage, current, power, and operating frequency. The hot-end of the convertor is heated with electric cartridge heaters. The cold end of the convertor is maintained with a water/glycol bath. Thermocouples are used to monitor temperature. The data system utilizes LabVIEW (National Instruments) hardware and software to acquire data and monitor the test.

To protect the test articles, protection circuits, which can trigger a shutdown in the event of an abnormal condition, monitor the hot-end temperatures and piston amplitudes. The LabVIEW system also monitors critical parameters for potentially unsafe conditions, including high or low charge pressure, high or low hot-end temperature, high pressure vessel temperature, high cold-end temperature, and loss of building power for more than five minutes. If any of these conditions occur, LabVIEW initiates a controlled shutdown of the system.

For operation with the SCC, DCC, and EDU, additional hardware is needed such as a DC electronic load, ground support equipment (GSE) DC power supply, and external shunt resistors. Telemetry is acquired and commands are sent to the controllers via LabVIEW. Commands are sent to:

- Change the voltage applied to the convertor to start piston motion
- Change the convertor operating frequency
- Connect or disconnect from the spacecraft
- Operate with or without a backup controller
- Inject faults (SCC only), enable/disable faults, and monitor faults

III. Stirling Controllers

The background and description of each of the five controllers will be discussed in this section.

D. Zener-Diode

The zener-diode[4] controller is based on a STC design and was modified for use at GRC in 2003. The ZDC was designed for laboratory use only.

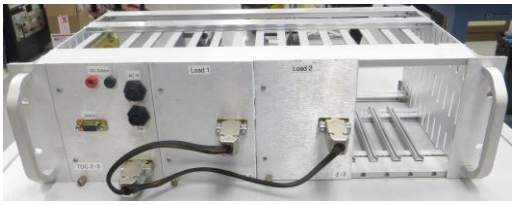

Figure 1. GRC designed ZDC.

The ZDC converts AC from both alternators to DC by a diode bridge and an energy storage capacitor. The loads are then applied in stages to the DC bus. The DC voltage is connected to the operational amplifiers only after it exceeds the breakdown voltage of the Zener-diode. The output of each operational amplifier controls the state of a field effect transistor (FET), which functions to switch a resistance onto the DC bus. The voltage level at which each operational amplifier turns on is controlled by sensing resistors, which are sized so that the trip point of each operational amplifier is slightly higher than the previous one. As the DC voltage rises above the first trip point, the first operational amplifier will turn on, applying its associated resistance to the DC bus. If the DC voltage continues to increase, the next operational amplifier in sequence will turn on, applying more load. This process continues until the DC voltage stops increasing or until all stages are on. As the DC voltage drops, the stages turn off one at a time in the reverse sequence. Because the DC voltage is produced by a rectified sine wave, the cycle of applying loads occurs at twice the convertor operating frequency. The load resistors are sized so that there is sufficient load available to maintain piston amplitude control at maximum convertor power output. The user may change the piston amplitude by adjusting the breakdown voltage of the Zener-diode. Increasing the breakdown voltage of the Zener-diode increases the 'floor' which the DC voltage must reach before any of the loads are activated. Therefore, the piston amplitudes can be increased by increasing the DC voltage. Figure 2 shows a simplified schematic of the controller.

The ZDC has been used to operate several convertor designs and has heritage in the GRC Stirling Research Lab (SRL). The GRC version of the ZDC has been used to operate a pair of Technology Demonstration Convertors (TDCs) in extended operation for over 100,000 hours of operation. An ASC version of the ZDC operated a pair of ASCs in a vacuum chamber for 15,000 hours. A picture of this ZDC is shown in Figure 1. This laboratory controller, as designed, does not have an output stage for a spacecraft but the design can be modified if the need arises in the future.

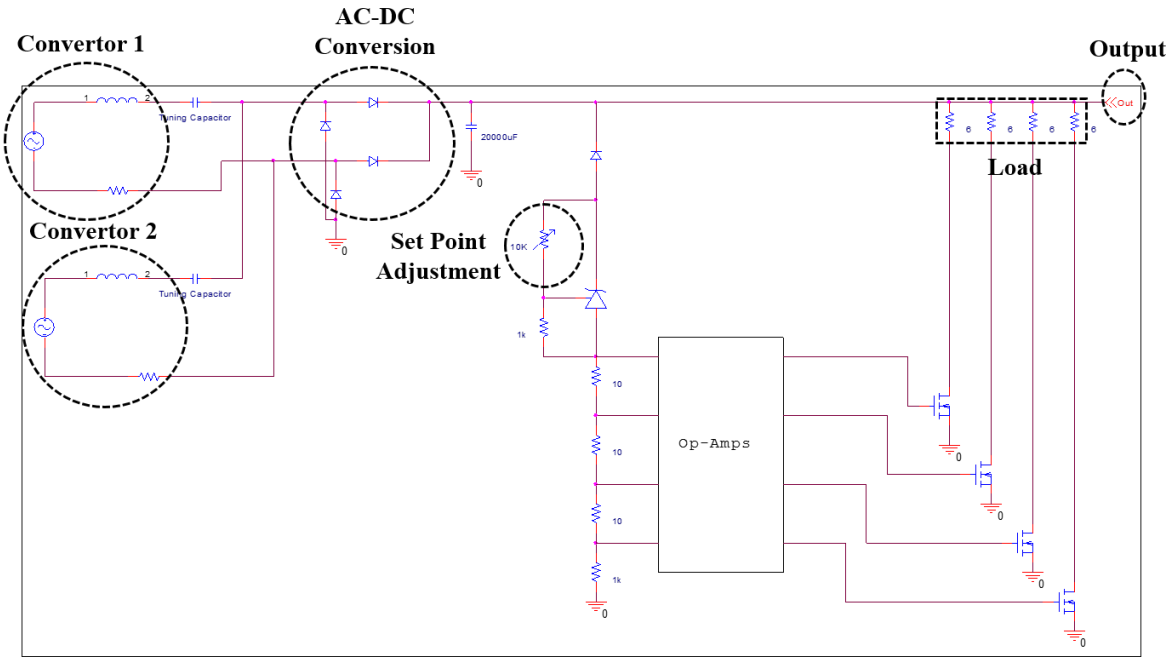

Figure 2. Zener-diode analog controller schematic.

E. Linear AC Regulator

The LAR was designed, in 2006, in support of the ASRG (Advanced Stirling Radioisotope Generator) simulator[5] project. The ASRG simulator consists of two FTBs mounted in a dual-opposed configuration. FTBs are the initial proof-of-concept ASC design before others were manufactured. The ASRG simulator system was designed for integration onto a rover. Figure 3 represents the total system concept for operating, controlling, and powering the rover. As part of this effort, a constant power and Li-ion battery charging circuit were designed to interface with the LAR. These are not described in this paper but are in reference 5. When the rover power exceeds that of the Stirling convertors, the batteries supply the additional power needed. When the constant power circuit detects that more power is required, then the diode becomes forward biased and the batteries start supplying power. The constant power circuit enables the Stirling convertors to continue to maintain full power while the batteries supply the additional power required by the rover.

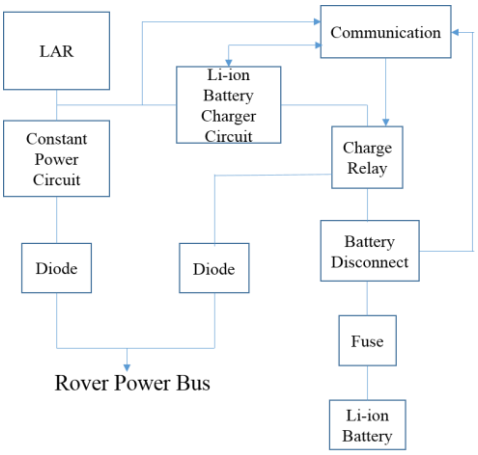

Figure 3. Rover concept block diagram.

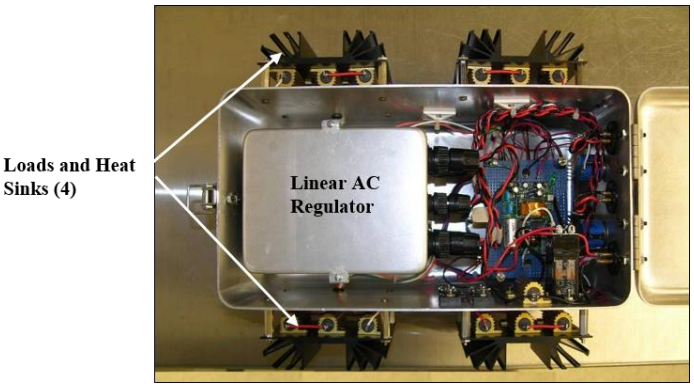

Figure 4. Linear AC regulator.

The LAR, shown in Figure 4, functions much the same way as the ZDC, but applies a load in a directly proportional manner, rather than in discrete steps. As with the ZDC, the AC from both alternators is converted to DC. However, the AC voltage is passed through a separate diode bridge with no energy storage capacitor that would convert it to DC. The rectified AC voltage

is sensed by a voltage divider connected to a single operational amplifier. It generates a voltage proportional to the difference between the divided voltage and the reference voltage. This output is used to drive FETs in their linear range, rather than discrete on-off states. The FETs connect load resistors onto the DC bus, but also dissipate power themselves. The user may change piston amplitude by adjusting the voltage divider that controls the input to the operational amplifier. The motivation behind the design of the LAR is that is has continuously variable loads, which avoids the ON/OFF behavior of the ZDC, but retains the multiple redundant load stages. Figure 5 shows a simplified schematic of the LAR.

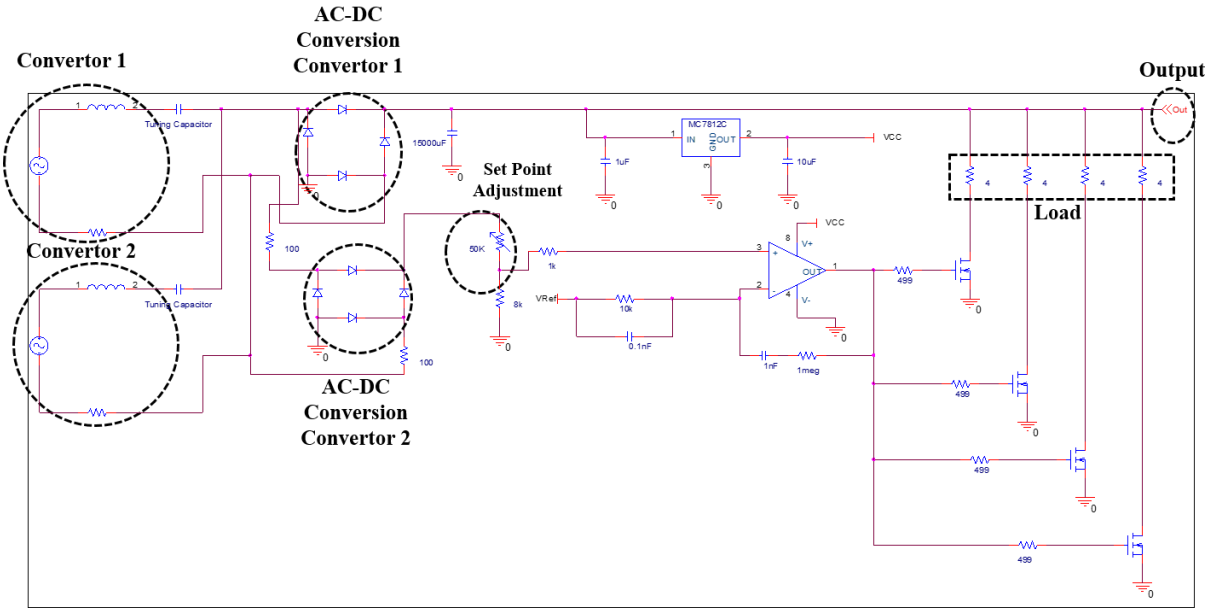

Figure 5. Circuit model of the linear AC regulator analog controller.

Prior to integration with the ASRG simulator, the LAR operated with a pair of EE35 convertors. Following successful integration and operation with the EE35 up to the full combined convertor power output of 130 W_e, the LAR was integrated with the constant power and Li-ion battery charger circuits. This testing was completed on the bench with the Li-ion battery represented by a DC power supply. The testing was successful with the battery (DC power supply providing current) supplying additional power when the LAR reached its maximum power output. After the bench testing of the LAR was complete, it was operated to full power convertor output with the ASRG simulator.

F. SCC

The SCC, shown in Figure 6, was delivered to GRC in 2011. The goal of the SCC task was to design and build a small, efficient, and reliable controller for use with a single ASC in support of the ILN. At the time, the ILN project was studying the feasibility of implementing a multiple-node seismometer network to investigate the internal lunar structure. A single ASC produces approximately 80 W_e and could potentially supply sufficient power for that application. The ILN project was cancelled but the development of the SCC continued.

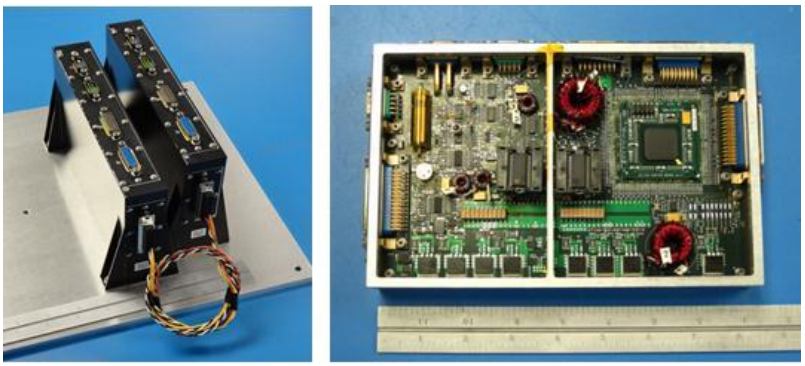

Figure 6. SCC and EM circuit board in the assembly fixture.

The SCC[6] is designed for use with one ASC whereas the other four controllers discussed in this paper operate a pair of Stirling convertors. In addition, the SCC can only operate an ASC with an alternator voltage up to 15 V. It was designed for flight use, but only a mechanically-equivalent, non-flight Engineering Model (EM) was built. Unlike the

ZDC and LAR, the SCC does not require a physical tuning capacitor because it uses power electronics to keep the stator current in phase with the voltage.

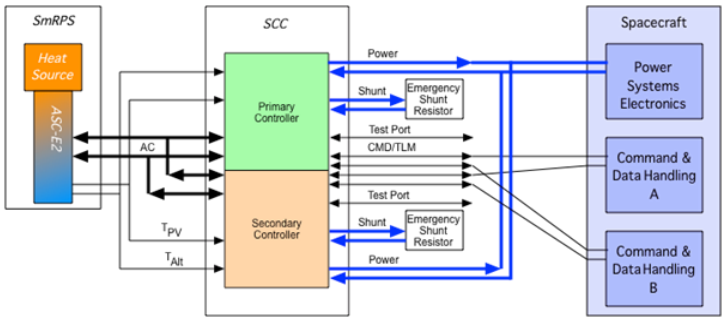

Figure 7. Block Diagram of a typical SCC redundant spacecraft application.

A block diagram of the SCC connected to a convertor and a typical redundant spacecraft is shown in Figure 7. The SCC consists of two identical controller boards packaged in separate chassis. A fault-tolerant[6] SCC consists of two identical boxes, each containing a copy of the same circuit. In typical operation, one box is actively controlling the convertor, while the other is available as a backup in the event of a fault. Each controller board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control a convertor and deliver DC power to the spacecraft.

Power flows from each convertor through an electronic switch for each ASC that acts as an AC circuit breaker. The AC circuit breaker is opened in the event of a fault to isolate the convertor from the failure and allow the redundant board to initiate control. Transient suppression devices on each controller board clamp voltage spikes that may occur when an AC breaker is opened. A field effect transistor (FET) H-bridge is pulse width modulated (PWM) as determined by the control law implemented in the field programmable gate array (FPGA). The H-bridge output is a DC voltage but with a large ripple current. An electromagnetic interference (EMI) filter on the board limits switching noise propagating from the controller to the spacecraft load. When the output regulator/DC breaker FETs are open, convertor power flows to an external shunt resistor controlled using pulse width modulated FET based regulator to maintain a fixed H-bridge output voltage.

The control law inputs and key status analog voltages are digitized by a 12-bit analog to digital converter (A/D) and processed by logic in the FPGA. The control law is implemented digitally by a co-processor in the FPGA. The co-processor contains an Institute of Electrical and Electronics Engineers (IEEE) single precision compliant data path controlled by a finite state machine sequencer programmed to implement the control law algorithm. A 16-bit microcontroller, also implemented in the FPGA, adjusts control law parameters, accepts user commands, and produces status telemetry. A combination of analog circuits, FPGA logic, and microcontroller software monitor DCC operation and detect and correct potential faults. A custom-designed DC/DC converter accepts input power from the spacecraft bus or external source and provides secondary voltages to board circuitry.

The SCC not only provides power to the spacecraft but it also must regulate ASC operation to avoid damage to internal components and maintain safe thermal conditions after fueling. The controller was designed with full redundancy to avoid potential over-heating or damage to the internal convertor structure. During SCC development, a functional failure mode effects analysis (FMEA) was developed to determine possible functional failures in the circuits. The impact of such failures and mechanisms to detect and correct them were identified and implemented in the detailed design. After detecting the H-bridge fault and isolating the failed controller, modeling showed that the backup controller had less than 20 ms to reestablish proper operation of the convertor. Modeling also showed that an open or short must be removed in less than 5 ms to avoid internal damage to convertor components. Analysis and simulation of the methods used to detect and recover from faults without damage to the ASCs as well as the ASC control algorithm are described in reference 7. Some of these faults include:

- Control fault where real alternator voltage significantly differs from the expected value
- Commanded demotion of the active controller
- Output buck regulator FET short/open
- Output buck regulator sync FET short/open
- Commanded A/D value override
- Excessive current into the spacecraft load
- Excessive current from the spacecraft load into the controller
- H-Bridge voltage too low
- Housekeeping voltage too low
- Backup controller power supply overcurrent

Spacecraft power needs may briefly exceed the capacity of the ASC power source. There are many causes of such events; examples include activating thruster valves, sudden momentum wheel speed changes, telemetry downlink transmission, in-rush current surges when activating loads, and bursts of science data collection are among many such possibilities. If auxiliary power is not supplied from another source, the power bus voltage may be pulled too low and trigger a spacecraft fault. A battery frequently acts as the auxiliary power source to ensure that an adequate bus voltage is maintained during these power transients. Alternatively, a large capacitor bank may provide backup power if the expected power transients are short and the energy storage capacity of the capacitor is adequate. Thus, the SCC was required to support either a battery or capacitive power bus spacecraft architecture.

G. DCC

Once the SCC design was completed and tested, JHU/APL began an effort to design a controller for a pair of ASCs, known as the DCC. The DCC, shown in Figure 8, is based on the SCC design. The main difference between the SCC and DCC is that the DCC operates a pair of ASCs. The initial version of the DCC, delivered in 2013, allowed for operation of ASCs with alternator voltages up to 15 V. After testing of this version of the DCC was completed with ASCs, an upgraded version of the DCC, delivered in 2015, was designed that allowed for operation of ASCs with alternator voltages up to 22 V. In order to allow for operation of this higher voltage ASC, a buck regulator was added to the output of the DCC. The H-bridge output is a DC voltage but with a large ripple current. That node is connected through an output buck regulator stage designed to minimize ripple in spacecraft output load current rather than maintain a specific output voltage. The regulator also protects the controller from spacecraft load faults. An additional FET switch in combination with the buck regulator will isolate the load and controller from faults

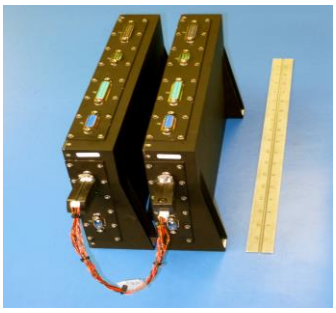

Figure 8. Photograph of the DCC.

A block diagram of the DCC connected to a convertor and a typical redundant spacecraft is shown in Figure 9. One controller board is actively in control of both ASCs, while the other is a hot standby used to recover from a fault. Each controller board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control two convertors and deliver DC power to the spacecraft. DCC capabilities are very similar to the previously mentioned SCC except that two convertors are controlled instead of one.

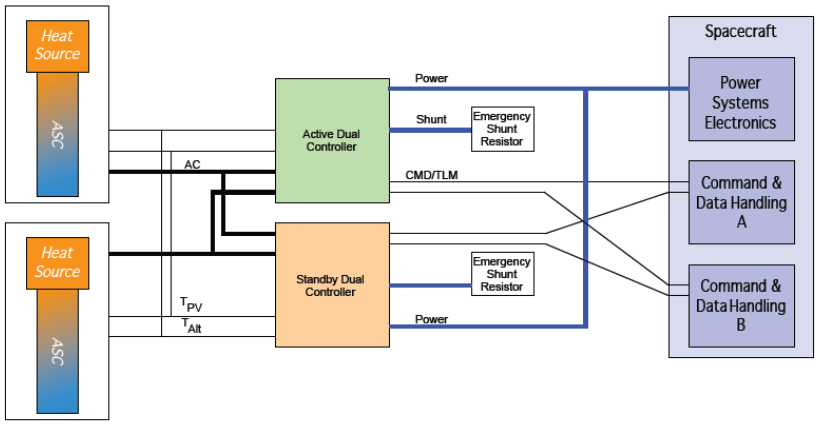

Figure 9. Block Diagram of a typical DCC redundant spacecraft application.

H. EDU/ACU

The ACU was designed in support of the Advanced Stirling Radioisotope Generator (ASRG) project. Several generations of the EDU[8] were built which included EDU1, EDU 2, EDU 2+, EDU 3, and EDU 4. The EDU 4, the most recent version of the ACU, was delivered to GRC in 2014. It controls a pair of ASCs and can operate ASCs with an alternator voltage up to 22 V.

The ACU controls the ASC's piston amplitude and synchronizes them at their operating frequency by means of an AC voltage input to the ASC alternator coil winding. Figure 11 shows a high level block diagram and the ACU interfaces to the ASCs and host spacecraft. The ACU has three controller cards, two cards (designated card 1 and card 2 in Figure

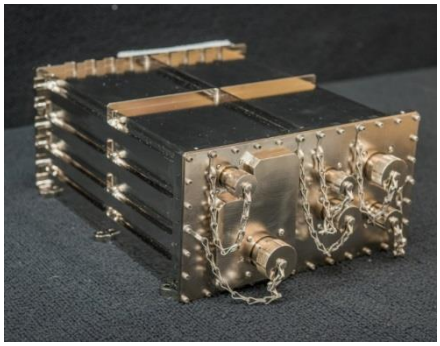

Figure 10. Picture of the EDU 4.

11) to actively control two ASCs and the third card is in hot standby, providing a single-fault tolerant, N+1 redundancy architecture. The controller cards in the ACU also provide independent power factor correction and voltage control to each ASC as well as ASC to ASC phase offset to allow for fine tuning when variations are seen in the ASCs.

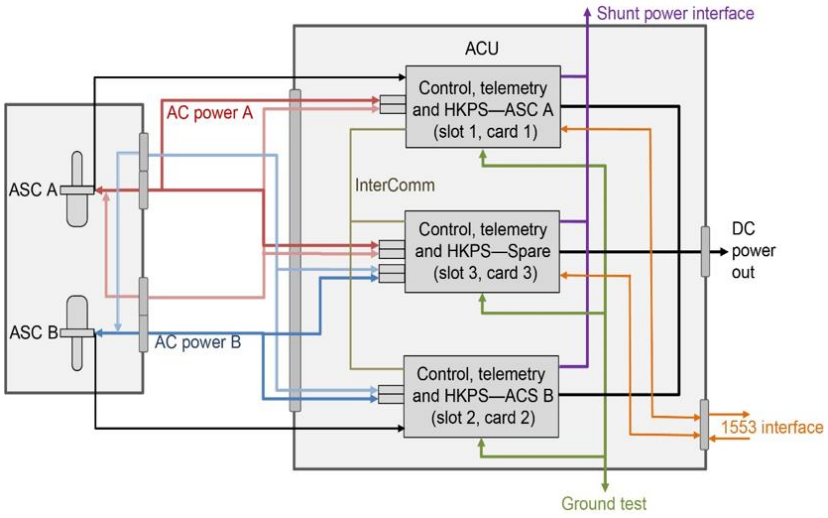

Figure 11. ACU high Level block diagram.

The ACU converts single-phase AC power into DC and sources DC current to the spacecraft by following its bus voltage between 22 and 34 Vdc using a buck converter at the DC Output. Above 34 Vdc, power is disconnected from the spacecraft bus and the converted DC power is shunted to an external shunt; below 22 Vdc, limited current is provided to the spacecraft to assist in the bus voltage recovery.

Operational telemetry and command/control between the spacecraft and ASRG are performed via the redundant MIL-STD 1553B serial bus. The ACU fault handling and transfer of ASC control from an active card to the spare is autonomous, utilizing several fault monitors that are either self-determined or majority voted to activate the failover switch. These faults include:

- **AC power**: detects loss of ASC control
- **Remote terminal address**: detects potential bus contention between the ACU and another remote terminal on the spacecraft MIL-STD-1553 bus or inability to communicate with the ACU.
- **MIL-STD-1553 transceiver +3.3VDC power supply voltage**: detects inability for the spacecraft to communicate with the ACU
- **Intercomm**: detects inability to communicate between controller cards which could lead to inability for the spacecraft to communicate with the ACU, or for a controller card to provide power to the spacecraft or control the ASC.
- **+28VDC local bus voltage**: detects loss of controller card local bus voltage which could lead to the inability for a controller card to provide power to the spacecraft or control the ASC.
- **Host voltage**: detects disagreement on the spacecraft voltage between controllers which could lead to inability to deliver power to the spacecraft
- **Host current**: detects DC Output current errors which could lead to the inability to deliver power to the spacecraft
- **FPGA +3.3V overvoltage**: detects controller card housekeeping power supply issue which could lead to inability for a controller card to provide power to the spacecraft or control the ASC

The ACU also collects telemetry from the ASCs that can be used to monitor the health of the ASCs over time. First, there is a non-redundant ASC Position Sensor (APS) processor on cards 1 and 2 that report the stroke length of each ASC. The ACU also captures a full cycle of the ASC voltage and current waveforms periodically and sends this data through telemetry.

Several features were also put in place to reduce EMI. The H-bridge that produces the ASC voltage utilizes a 3-state switching method instead of the more common 2-state method which reduces the total EMI generated from the H-bridge pulse width modulated (PWM) signal significantly. Next the controller cards are synchronized at the beginning of every ASC cycle. This synchronization signal has several uses with one of the main uses being to apply a phase offset to the PWM signals of each card. Both the AC PWM signal as well as the buck output (DC) PWM signals are offset from card to card to reduce the overall EMI signature.

IV. Stirling Controller Testing

This section discusses testing that has been performed with the SCC, DCC, and ACU. Tests performed with the ZDC and LAR are limited in scope and are therefore not discussed in this section of the paper but are discussed in Section II.D and II.E.

A. SCC

A test series was conducted with the SCC[9], in 2013, which included electromagnetic interference, susceptibility, conducted emissions, fault response, flight acceptance vibration, and extended operation. A summary of each of these tests is described below.

Electromagnetic Interference Testing

The ASC-L was tested, in 2013, for radiated EMI while controlled by an AC bus power supply and then by the SCC to characterize the difference when controlled by the SCC. The SCC and AC bus power supply were located outside the EMI test chamber with the ASC-L mounted inside the test chamber. This testing is based on MIL-STD-461 RE04, RE01, RE02 and RE102.

Test results for the AC magnetic field testing showed that the SCC increased the radiated emissions from the ASC-L marginally (~0.5 dBpT) compared to operation with the AC bus power supply, but the main effect was an introduced spike at 23 kHz, the PWM switching frequency of the SCC, plus harmonics. Test results for the AC electric field testing showed that the SCC decreased the 102.2 Hz dominant spike but increased the 204.4 Hz spike, with associated harmonics. It also injected a 23 kHz spike (due to the PWM switching as mentioned above), and introduced broad-band noise from ~400 kHz through ~15 MHz. Field levels were not significantly different when the ASC-L was controlled with the SCC or the AC bus power supply.

Susceptibility and Conducted Emissions Testing

The SCC was tested for conducted line emissions while operating the ASC-L using test procedures based on MIL-SPEC-461C CE01 & CE03. The majority of peaks were detected at ~204 Hz (2x convertor operating frequency) with 4-5 harmonics, at ~23 kHz (SCC PWM switching frequency) and with harmonics at ~700 kHz. There was no discernible difference in conducted emissions between the different operating modes of the SCC nor on the power vs. return leads. Conducted emissions testing of the SCC showed a large current component at twice the ASC operating frequency. The current is caused by the controller's full wave rectification of the ASC output power. For a capacitive bus based electrical power system, the bus capacitance would smooth the current and minimize emissions. A battery based power system would also reduce emissions but in that case the ripple current would also be equivalent to charge/discharge cycles at a high frequency.

The SCC was subjected to conducted EMI susceptibility testing using test procedures based on MIL-SPEC-461C CS01, CS02 & CS06. To protect the ASC-L hardware against a loss of control event, the DASCS discussed in Section I, was used to provide power to the SCC and a resistive test load was used to dissipate full power during the duration of the test without using an electronic load. During conducted susceptibility testing, there were no noticeable performance effects. Output voltage change, controller latch-up or loss of communication were all monitored for and did not occur.

Fault Testing

The fault detection and correction mechanisms in the controller protect the convertor and spacecraft from damage while recovering from a fault as described in Section II.F. APL designed software that allowed some of these faults to be tested in the laboratory environment:

- Disconnecting from the spacecraft when the bus voltage goes above 36V or below 22V. Once disconnected from the spacecraft, the user must command the SCC to reconnect; this is not done autonomously.
- Emergency shunt PWM FET open to demonstrate that when the PWM FET fails open then the SCC switches to the backup board.
- The external emergency shunt resistor short fault to demonstrate that if there is a short across the SCC external emergency shunt resistor, the SCC switches to the backup board.
- The external emergency shunt FET short while connected to the spacecraft fault demonstrates that if the SCC is connected to the spacecraft and there is a short in the emergency shunt FET, the SCC switches to the backup board.
- H-bridge FET short fault demonstrates that if one of the h-bridge FET's is shorted then the SCC will switch to the backup board.

- H-bridge FET open fault demonstrates that if one of the h-bridge FET's is open then the SCC will switch to the backup board.
- AC breaker open fault test demonstrates that if the AC breaker is open then the SCC switches to the backup board.
- Hot swap demonstrates that a failed controller board can be changed while the other controller board maintains full power operation of the convertors.

The SCC successfully handled the fault conditions[9] listed above while operating an ASC-1.

Flight Acceptance Vibration Testing

The ASC-L was subjected to flight acceptance level vibration testing under SCC control, in 2013, in the Structural Dynamics Lab (SDL) at GRC[11]. The SCC was not on the vibe table. The SCC maintained safe piston margins to flight acceptance levels. At this level of vibration, the ASC-L was producing high current (near 25 A_{rms}) during peak accelerations. This current was near the saturation point of the SCC's current sensor. Due to the high current, the test ended at flight acceptance level and did not proceed to qualification level. The current approached the limits of the SCC's full digitization range. Exceeding that range would cause the control algorithm to process inaccurate input current values and hence risk loss of control. To allow higher external vibration levels, the SCC input alternator current dynamic range should be increased. However, if dynamic range is increased, resolution will be decreased and ASC output power noise may degrade. Hence, an analysis to predict maximum input current while under external vibration should also be performed.

Extended Operation Testing

Extended operation of the SCC with ASC-L was initiated in 2013 and as of June 2018 has accumulated over 36,000 hours of operation. Data is analyzed weekly and no changes in performance have been observed.

B. DCC

RSIL testing

The RSIL is comprised of five major components designed to simulate a prototypical spacecraft powered by a RPS. The major components are: RPS power sources (here a pair of ASCs), a power management and distribution system (PMAD), an energy storage system (bus capacitor, battery or super capacitor), electrical load simulators, and a flight control computer simulation. These components are connected together to simulate a spacecraft's main electrical bus feeding a set of electrical loads all powered by RPS generators. This integrated electrical system tests RPS generators as part of an end-to-end spacecraft system rather than as stand-alone power generators. More information on the RSIL can be found in reference 10.

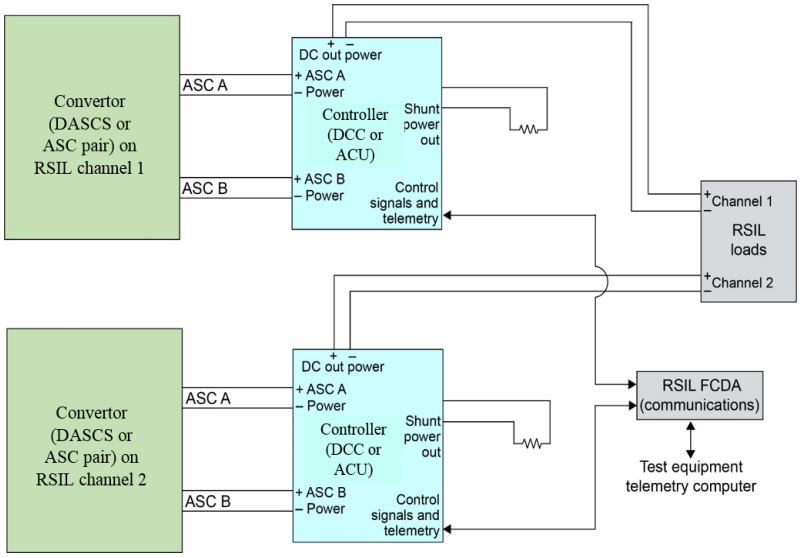

Figure 12. Dual input channel RPS test setup.

The initial version of the DCC completed a testing series with the RSIL in 2015. These test configurations included:

1. Operation with a DASCS to verify the functionality of both the DCC and RSIL on one RSIL channel.
2. Integration with a pair of ASC-1s on one RSIL channel.
3. Operation with two DASCSs operating as parallel inputs (channel 1 and channel 2) to RSIL.

The four main tests included:

1. **Load step**: 2A change in the spacecraft load. This verified that the DCC was able to maintain operation of the convertors during a step change in load.
2. **Load profile**: automated changes in load demand implemented using LabVIEW software. The load profiles were created based on data from several representative missions. The load profile test verified the ability of

the DCC to maintain operation during load demands above and below the power provided by the ASCs. When the RSIL required more power than the RPS could accommodate, the energy storage device (supercapacitor or battery) supplied the additional power. When the RSIL demanded less power than what the source provided, the RSIL shunt regulator unit dissipated the excess power.

3. **Over/Under voltage**: this test verified the DCC's ability to disconnect from the RSIL when out of range from 22-36 V bus voltage for which it was designed.
4. **Short circuit**: verified the RSIL's ability to respond to a short on one of the loads and to verify the DCC maintained operation of the convertors through this event.

A general block diagram describing the setup for the three tests is shown in Figure 12. All testing was performed with the three energy storage configurations in RSIL. The results of the tests are described in reference 10.

Fault Testing

Fault testing was performed with the most recent version of the DCC. The same set of SCC faults described in Section IV and the same test setup were also tested with the DCC since the fault handling functionality of the SCC is the same for the DCC. The DCC successfully handled all fault conditions. During the testing, it was learned that the power delivered to the spacecraft was 9 W less than expected. Troubleshooting is underway to determine the root cause of this power loss.

C. EDU/ACU

Testing[13] with the ACU in RSIL completed the same test sequence in the same test configurations as the DCC mentioned in section IV. B. There were three main differences in these tests compared to the DCC testing.

1. The load step changes were performed with constant power and constant resistance loads whereas the DCC used constant current loads for this test.
2. The load profiles were performed at bus voltages of 26, 28, and 32 V whereas the DCC testing only completed load profiles at 28 V.
3. The short circuit tests were performed with constant power and constant resistance loads whereas the DCC short circuit testing was performed with a constant current laod.

To mimic integration of a controller with a spacecraft, the convertors were brought to full power operation with the ACU dissipating power in external shunt resistors. Then the ACU's DC output harness was connected to the RSIL and the ACU command was sent to connect to RSIL thereby simulating connecting to a spacecraft.

The results of the RSIL testing for configurations 1 and 3 are described in reference 11. The RSIL testing with ASC-1s (configuration 2) was performed in May 2018 and the data is still being analyzed. RSIL testing revealed several issues resulting in lessons learned or necessitate further development:

1. ASC power required for dead bus recovery
2. DC output current spike during dead bus recovery
3. grounding impact on a spacecraft
4. alternator harnessing impedance requirement due to ASCs with different alternator voltages

Lesson learned 1 and 2 are described in reference 11. In a real application, the ACU would operate a pair of ASCs for up to 3 years before launch and after they are fueled. During this time, the ACU will provide its DC power to an electronic load in a GSE test rack. Once the spacecraft is ready for the ASCs, the ACU is disconnected from the electronic load in the GSE and commanded to dissipate the DC power in an external shunt resistor. Once integration is complete with the spacecraft, the ACU is then commanded to provide power to the spacecraft and is no longer dissipating its power in the external shunt.

To replicate the real application, the DC power provided by the ACU is dissipated in an electronic load in a test support rack. When RSIL is ready to accept the power from the ACU, the ACU is commanded to dissipate power it its external shunt resistors. The ACU DC output cable is then disconnected from the electronic load in the ACU test support rack and connected to the RSIL bus. Once this connection is complete, the ACU is commanded to connect to the RSIL. During testing, when the EDU's output harness was connected to RSIL, 1553 communication was lost and there were several fault indicators. It was determined that there was a voltage differential between the RSIL and the ACU DC output harness. From this it was determined that there was a grounding issue within the test support rack. The EDU uses both the DC output and external power supply as ground references. When the DC output harness is disconnected, it relies on the external power supply ground. It was determined that the grounding of the external power supply was open from the external power supply to the rack ground. This was corrected and the testing was able to commence. This lesson learned can be applied when considering integration with the GSE that will be used in the real application.

The EDU 4 had only operated ASCs with an alternator of 22 V. An effort was underway to understand the capabilities of the ACU and therefore plans were made to operate the ACU with ASCs with a 12 V alternator. Initially, testing was performed with a DASCS-12 as a risk reduction to the ASCs. During testing with the DASCS, the ASC power factor dropped below 0.5 and the ACU was only able to operate up to a power level of approximately 50 W. Troubleshooting revealed that the ACU algorithm expects a minimum resistance on its input. The resistance of the ASCs with 12 V alternators is lower than those with a 22 V alternator. The resistance of the AC harness was increased and testing with the DASCS and then a pair of ASCs with 12 V alternators was performed. This lesson learned is valuable when considering controller designs that can operate more than one type of Stirling convertor.

V. Conclusion

This paper described the five analog/digital controllers tested and developed either at GRC or under GRC guidance over the past 15 years to support various Stirling convertor applications. Requirements, convertor control, fault implementation, and tests completed varied amongst the controllers. Tests completed with the controllers provided lessons learned that can be implemented in future Stirling convertor controller designs and test setups.

Acknowledgments

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