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Cryogenic Parametric Characterization of Gallium Nitride Switches

Marcelo C. Gonzalez, Lee W. Kohlman, and Andrew J. Trunek
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October 2018

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Summary

This report presents the parametric characterization results of four GaN field-effect transistor (FET) devices from three manufacturers, one of which is a cascode device, and compares those results to a Si power metal-oxide-semiconductor field-effect transistor (MOSFET) and a SiC power MOSFET. The devices were first characterized at ambient temperature, then at cryogenic temperatures down to –196 °C (LN_2 temperature), and finally at ambient temperature again in the event that the device parameters were permanently affected by the cryogenic temperatures. In general, the results indicate that the GaN devices show significant improvement overall at cryogenic temperatures in the parameters characterized, such as on-resistance and leakage currents, compared to the Si and SiC devices. The results show that the SiC device tested should not be used at cryogenic temperatures due to the significant increase in on-resistance. The results also show that the GaN and Si parameters characterized were either not affected by the cryogenic temperatures or changed by no more than ±20 percent post LN_2 submersion. The device that exhibited the most parametric change post LN_2 submersion was the SiC power MOSFET in its leakage currents.

Nomenclature

ADC	analog-to-digital converter
CV	capacitance voltage
DUT	device under test
FET	field-effect transistor
LNG	liquid natural gas
MOSFET	metal-oxide-semiconductor field-effect transistor
PCB	printed circuit board
PPE	personal protective equipment
SMT	surface mount

Symbols

BV_{dss}	drain-to-source breakdown voltage
C_{ds}	drain-to-source capacitance
C_{gd}	gate-to-drain capacitance
C_{gs}	gate-to-source capacitance
C_{iss}	input capacitance
C_{oss}	output capacitance
C_{rss}	reverse transfer capacitance
D	drain
f	frequency
G	gate
I_d	drain current
I_{ds}	drain-to-source current
I_{dss}	drain-to-source leakage current
I_{gs}	gate-to-source current
I_{gssf}	forward gate-to-source leakage current
I_{gssr}	reverse gate-to-source leakage current
$R_{ds(on)}$	drain-to-source on-resistance
R_g	gate resistance
S	source
V_{ds}	drain-to-source voltage
V_{gs}	gate-to-source voltage
$V_{gs(th)}$	gate-to-source threshold voltage

1.0 Introduction

NASA is currently pursuing aeronautics research in hybrid electric vehicles to improve aircraft fuel efficiency in order to keep pace with increasing air travel demands, which are projected to double in 20 years. Other factors driving this research are energy sustainability, fuel cost volatility, and projected air travel cost increase. One area of interest is in the use of cryogenic fuels, such as liquid natural gas (LNG) and LH_2, to power the aircraft and cool the electric motors and motor drivers (inverters) for improved efficiency. Results by other researchers investigating both Si and GaN field-effect transistor (FET) devices indicate that performance improvements are possible with cryocooling (Refs. 1 and 2). Furthermore, GaN promises significant performance advantages in terms of efficiency and power density over Si as discussed in References 3 and 4.

The performance characteristics of GaN, Si, and SiC switches were evaluated at temperatures from ambient to LN_2 temperature, taking advantage of the temperature gradient that exists above the LN_2 inside the Dewar for temperatures in between. A total of eight parameters were characterized versus temperature and these include the switches' drain-to-source on-resistance ($R_{ds(on)}$), gate-to-source threshold voltage ($V_{gs(th)}$), forward gate-to-source leakage current (I_{gssf}), reverse gate-to-source leakage current (I_{gssr}), drain-to-source leakage current

(I_{dss}), input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}). Attempts were made to measure the drain-to-source breakdown voltage (BV_{dss}), but this was eliminated from the list of parameters for GaN and SiC due to device failures. The experimental setup is described in Section 2.0 and the results and analysis are discussed in Section 3.0. Lastly, conclusions are drawn based on the results in section 4.0.

2.0 Experimental Setup

Accurate parametric characterization of semiconductor components, for example metal-oxide semiconductor field-effect transistors (MOSFETs) and diodes, requires the use of specialized testing equipment such as a state-of-the-art curve tracer (e.g., the 2600–PCT–4B from Keithley) coupled with a high-voltage biasing module and a capacitance-voltage (CV) measurement module (e.g., the PCT–CVU from Keithley) in order to be able to characterize the devices from very low currents (e.g., picoamps) to high currents and from low voltages (microvolts) to high voltages (kilovolts) with high accuracy. Typically a curve tracer is sold with a device test fixture that seamlessly connects to the curve tracer to test two- and three-terminal devices. However, the device test fixture is not designed nor intended for use at cryogenic temperatures, forcing the researcher to develop a custom solution to test devices at these very cold temperatures.

One such solution is shown in Figure 1, which shows a small Dewar, a custom-made motorized dipping mechanism with the device under test (DUT) in the Dewar, and an interface panel to connect the DUT to the curve tracer. This solution enables testing at LN_2 temperature (–196 °C) when the device is immersed and at temperatures above LN_2 temperature by taking advantage of the temperature gradient due to LN_2 vapor that exists above the liquid inside the Dewar. The motorized mechanism allows for safe lowering and raising of the DUT into and out of the cryogenic fluid, eliminating accidental contact with LN_2 or extremely cold parts, via control switches at a safe distance from the Dewar. The Dewar is also prevented from tipping over by the vertical fins as shown in Figure 1.

The DUT was attached to the dipping mechanism via a printed circuit board (PCB) for surface-mount (SMT) devices as shown in Figure 2(a) or a cryorated G10 board for through-hole devices as shown in Figure 2(b). The PCB or G10 board was secured to the dipping mechanism by using two screws when it was swiveled away from the Dewar.

Three GaN devices, one cascode GaN device, one Si device, and one trench-type (vertical) SiC device, 10 samples each, were selected and prepared for testing. The three GaN devices are SMT type and required a PCB for testing (Figure 3(a)). The cascode GaN device, Si, and SiC devices are through-hole TO–247 package devices. The through-hole device was secured to the G10 board with a screw (Figure 3(b)). All the samples were prepared by using cryocompatible solder, Teflon-insulated (Chemours) wire, and an type E thermocouple mounted on the body of the semiconductor switches with cryocompatible thermal epoxy. The thermocouple was connected to a datalogger to collect temperature data. The DUT was connected to the curve tracer via banana plugs on the DUT leads and banana jacks on the interface panel.

A small portable Dewar was used to collect about 2 L of LN_2 from an LN_2 tank. The small amount of LN_2 was slowly poured into the dipping Dewar, with the motorized dipping mechanism swiveled to the side, until the LN_2 was about 5 in. from the Dewar rim. Since LN_2 is at an extremely cold temperature, proper personal protective equipment (PPE) must be used when handling the LN_2 (Ref. 5). Components that have been dipped in LN_2 are allowed to reach room temperature before handling.

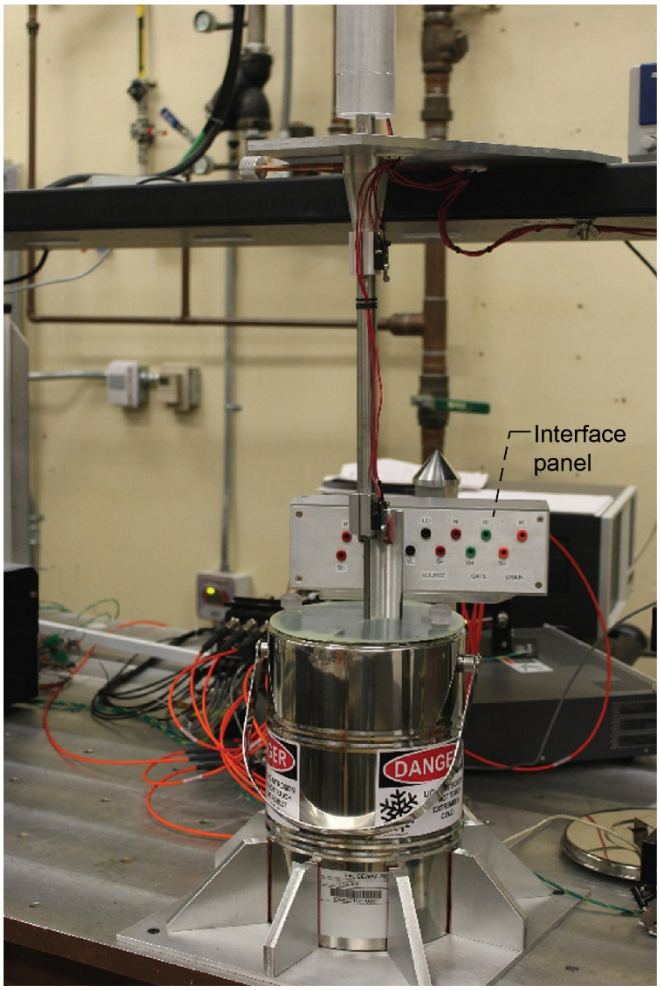


Figure 1.—Cryogenic device test fixture.

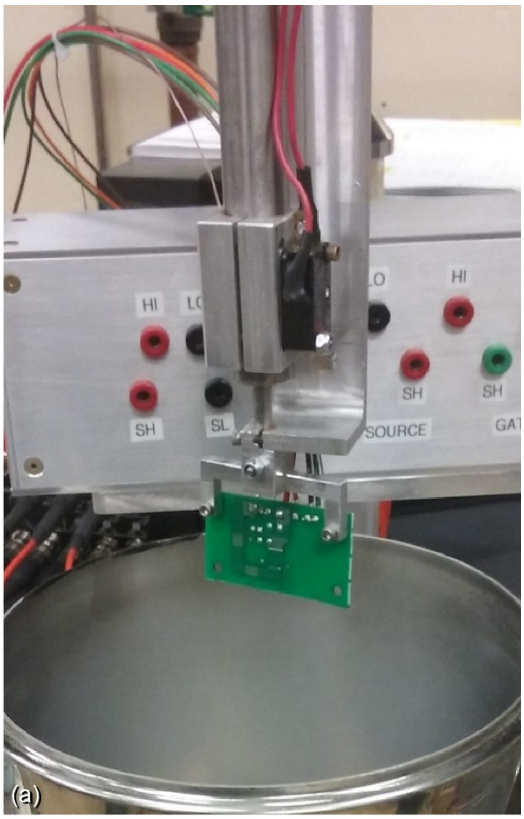
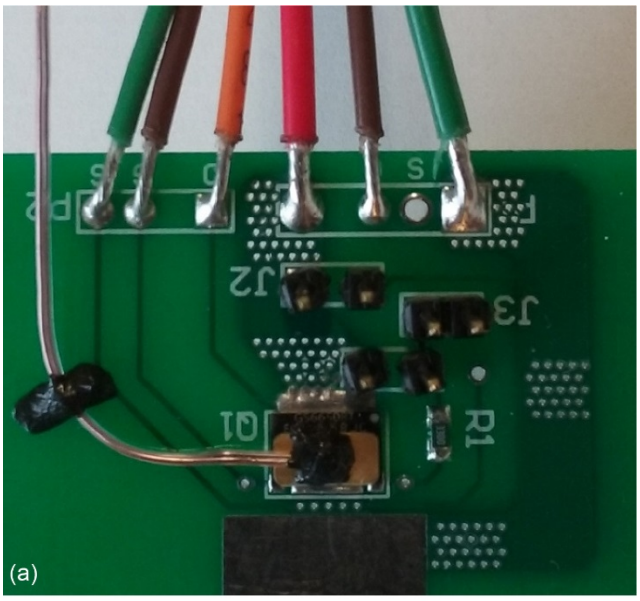


Figure 2.—Cryogenic device over test fixture.
(a) Surface-mount printed circuit board.
(b) Through-hole G10.



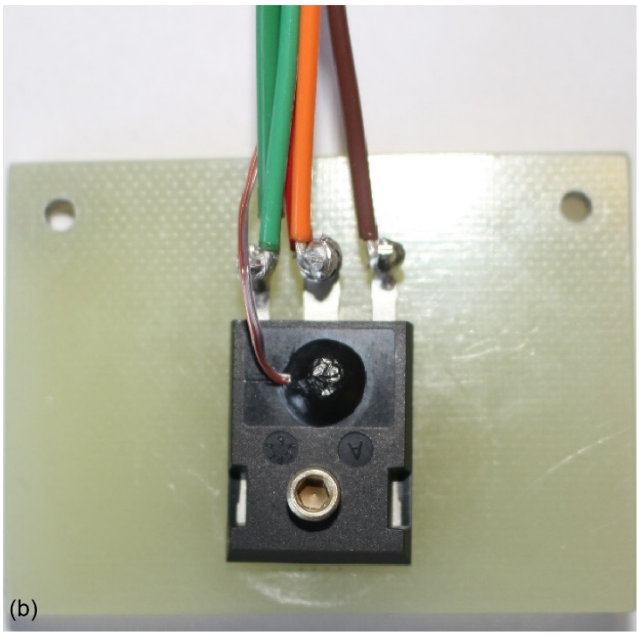


Figure 3.—Devices. (a) Surface mount. (b) Through hole.

In order to avoid premature failure of devices due to thermal shock, the DUT was allowed to reach thermal stability while incrementally lowering or raising the dipping mechanism. The operator uses the DUT temperature displayed by the datalogger to determine if the device has reached thermal stability before slowly and incrementally lowering or raising the DUT. Once the target temperature was reached, the Dewar covers were installed (Figure 1) and characterization data taken with the curve tracer. Figure 4 depicts a representative temperature profile from room temperature down to LN_2 temperature and back to room temperature. The graph shows that three data points were taken with two above LN_2 temperature at

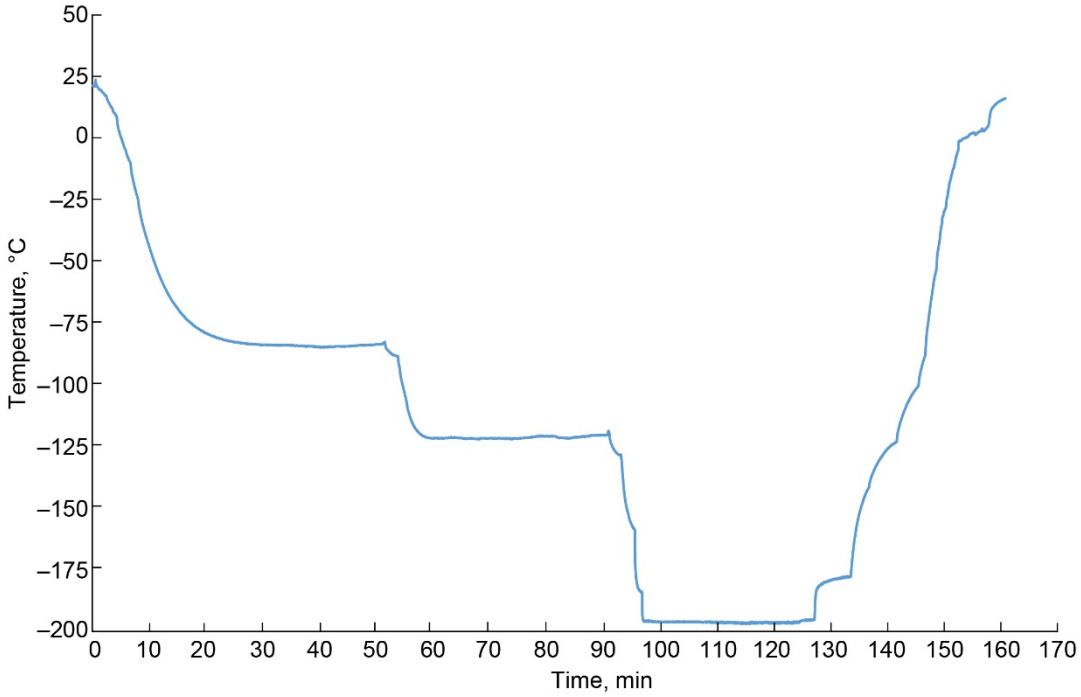


Figure 4.—Representative device under test thermal profile.

approximately –84.5 and –121 °C. Note that it takes about 30 min to take the desired characterization data with the curve tracer for each temperature data point, and that for most samples, only two temperature data points were taken, eliminating the first data point, due to time limitations.

3.0 Results

A total of 60 samples, comprising GaN, Si, and SiC, were prepared for characterization. Each was subjected to characterization at ambient temperature, at two or three cryogenic temperatures, and at ambient temperature again. The latter was done to determine if permanent changes or damage occurred as a result of the device being exposed to the extremely cold temperatures during testing. As discussed previously, eight typical characterization parameters were selected for testing. These parameters are generally classified into three categories: on-state parameters ($R_{ds(on)}$, $V_{gs(th)}$, I_{gssf}, and I_{gssr}) with gate-to-source voltage (V_{gs}) applied, off-state parameters (I_{dss} and BV_{dss}) with no V_{gs} applied, and device capacitance (C_{iss}, C_{oss}, and C_{rss}). The results for each parameter are presented in its corresponding subsection.

3.1 On-Resistance

The on-resistance of a semiconductor FET has various contributing components as reported in References 6 to 9. It is measured by applying a fixed V_{gs} voltage and a known drain-to-source current (I_{ds}). The I_{ds} current can also be swept to produce an on-resistance sweep. The on-resistance is computed by the curve tracer by taking the ratio of the drain-to-source voltage to the drain-to-source current (V_{ds}/I_{ds}). Figure 5 shows a simplified drawing of the curve tracer configuration and Figure 6 displays sample on-resistance sweeps. The gate resistor is of a value ≤1 kW. Note that remote sensing for V_{ds} is used for this test due to the large I_{ds} current. Also note that the Si device's on-resistance is significantly higher than the GaN and trench-type SiC devices. Please refer to Appendix A for device parameters and test conditions and Appendix B for on-resistance comparison.

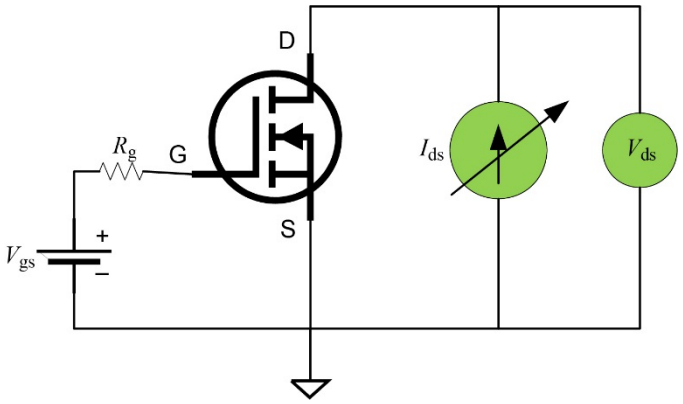


Figure 5.—On-resistance test configuration. Where D is drain, G is gate, I_{ds} is drain-to-source current, R_g is gate resistance, S is source, V_{ds} is drain-to-source voltage, and V_{gs} is gate-to-source voltage.

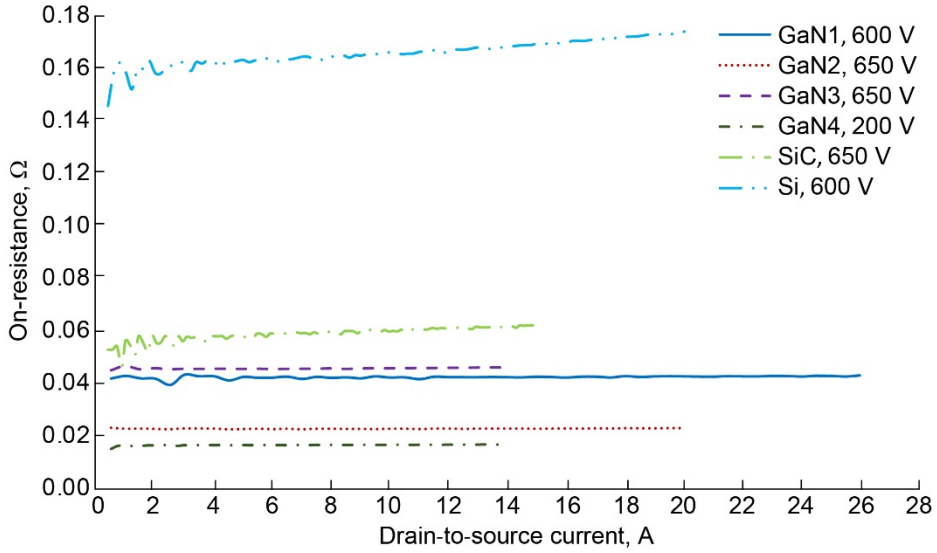


Figure 6.—Sample device on-resistance sweeps.

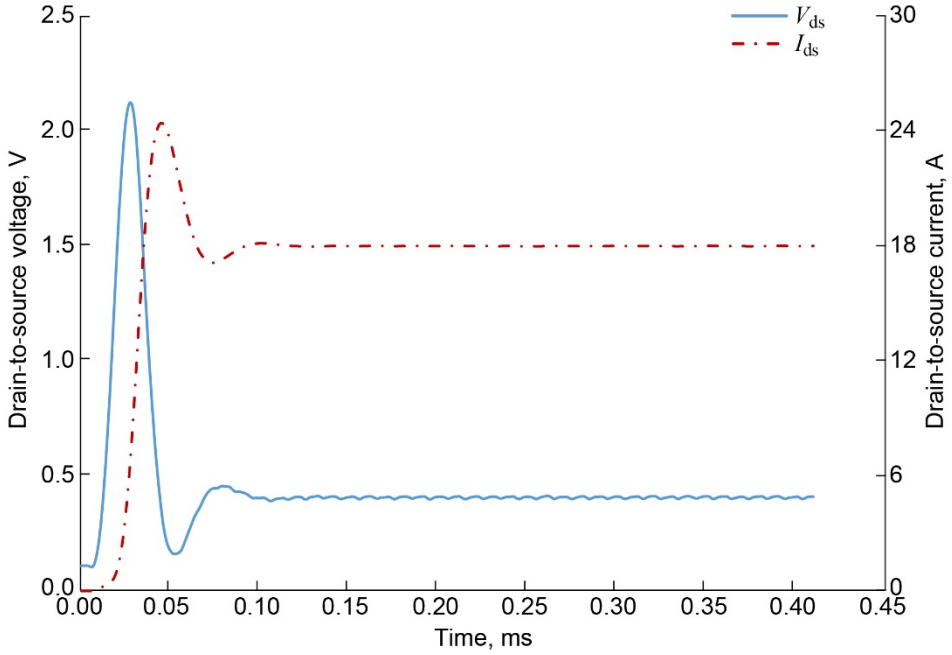


Figure 7.—Drain-to-source current (I_{ds}) pulse transient. Where V_{ds} is drain to source voltage.

Due to the relatively large I_{ds} currents at which $R_{ds(on)}$ is measured, self-heating becomes a concern, especially for the small GaN SMT devices. As a result, the I_{ds} is pulsed during testing at a very small duty ratio of around 1 percent and the measurement is taken when the pulse transient has settled. The settling time and thus the pulse width is determined by using the curve tracer's built-in high-speed analog-to-digital converter (ADC) to capture the transient to determine when to take the measurement (Ref. 10). This conveniently eliminates the need to use oscilloscopes and voltage and current probes. Pulse transient data was taken for each device model to ensure the pulse width was large enough (see Figure 7 for an example) and the duty ratio was low enough (typically 1 percent) to avoid self-heating (Ref. 11). Note that for the resistance sweep, the I_{ds} steps were significantly smaller, depending on the number of data points desired from 0 A to the desired I_{ds} current dictated by the device datasheet.

The temperature-dependent $R_{ds(on)}$ for each sample is the average of 10 readings performed by the curve tracer, and the reported $R_{ds(on)}$ for each device model is the average of the

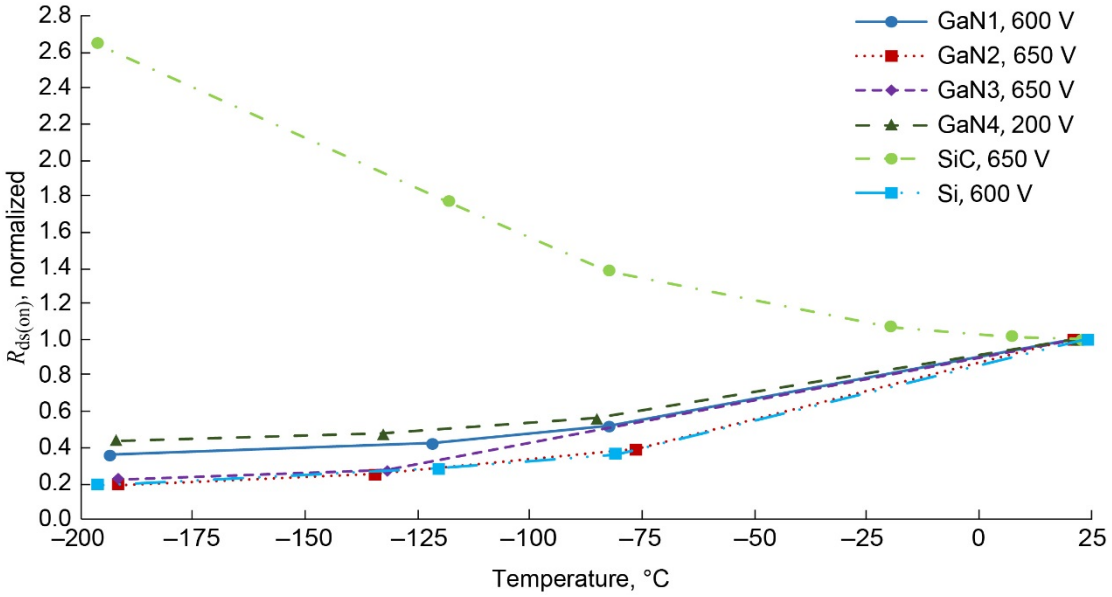


Figure 8.—Normalized drain-to-source on-resistance ($R_{ds(on)}$) for GaN, SiC, and Si devices.

10 samples computed in a spreadsheet. In some cases, less than 10 readings were averaged due to some devices failing during testing. Discussion of the cause(s) of device failures is beyond the scope of this paper. These values were then normalized to the ambient temperature values pre-LN_2 submersion and are shown in Figure 8. It is important to note that for GaN and Si, most of the $R_{ds(on)}$ drop occurs in the first 100 °C temperature drop. GaN1 in the graphs is the cascode GaN device. The resistances drop between approximately 60 to 80 percent at LN_2 temperature. On the contrary, the SiC device exhibited a significant increase in on-resistance with decreasing temperature, primarily due to the effect known as carrier freezeout (Refs. 12 and 13). The on-resistance versus temperature of this device agrees very well with data reported in Reference 12, showing a minimum around 300 K.

3.2 Gate Threshold Voltage

The gate-to-source threshold voltage, $V_{gs(th)}$, is the minimum voltage needed to turn on the device, that is, when drain-to-source current starts flowing (Refs. 6 to 9). The threshold voltage is measured by sweeping the same voltage across the gate-to-source and drain-to-source until a desired drain-to-source current is obtained, which can range from hundreds of microamps to milliamps, depending on the device. The curve tracer configuration for this test is shown in Figure 9 and a sample $V_{gs(th)}$ sweep is shown in Figure 10. It is evident from the latter figure that GaN devices have lower $V_{gs(th)}$ than Si and SiC devices. This requires careful design of the gate drive circuit to avoid unwanted or inadvertent device turnon that could result in device failure.

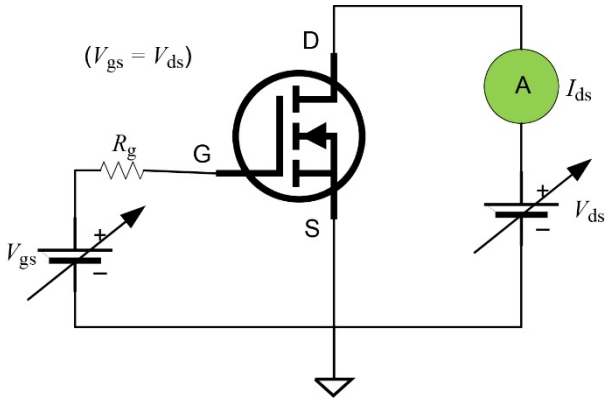


Figure 9.—Gate (G) threshold test configuration. Where D is drain, I_{ds} is drain-to-source current, R_g is gate resistance, S is source, V_{ds} is drain-to-source voltage, and V_{gs} is gate-to-source voltage.

The curve tracer is configured to sweep the V_{gs} and V_{ds} voltages together, that is, V_{gs} = V_{ds}, and measures the threshold value from the data at the drain current specified in the datasheet by using extrapolation of the data if necessary. The value is then entered into a spreadsheet where it is averaged for each of the six devices tested. The results were then graphed and shown in Figure 11 by using values normalized to the ambient temperature value.

The data shows that for GaN2 to GaN4, the threshold voltage either stays constant (GaN3), decreases (GaN2), or increases (GaN4) by about 10 percent at LN_2 temperature. Since GaN devices have lower threshold and gate drive voltages compared to SiC and Si, a change of ±10 percent is a good result. If the threshold voltage is too low, the device could turn on due to noise

or transients. On the contrary, if the threshold voltage increases significantly, it may not be possible to turn the device fully on into saturation or stay in saturation due to the low maximum gate voltage of 5 to 6 V. GaN1 is a cascode device with an Si MOSFET at its gate. As a result, cascode GaN devices can be driven with higher gate voltages. Its threshold voltage shows a similar increase to the Si device of around 30 percent, whereas the Si device exhibits around 40 percent. The threshold voltage for the SiC device almost doubles at –196 °C, showing a higher temperature dependence than Si and GaN (Ref. 13).

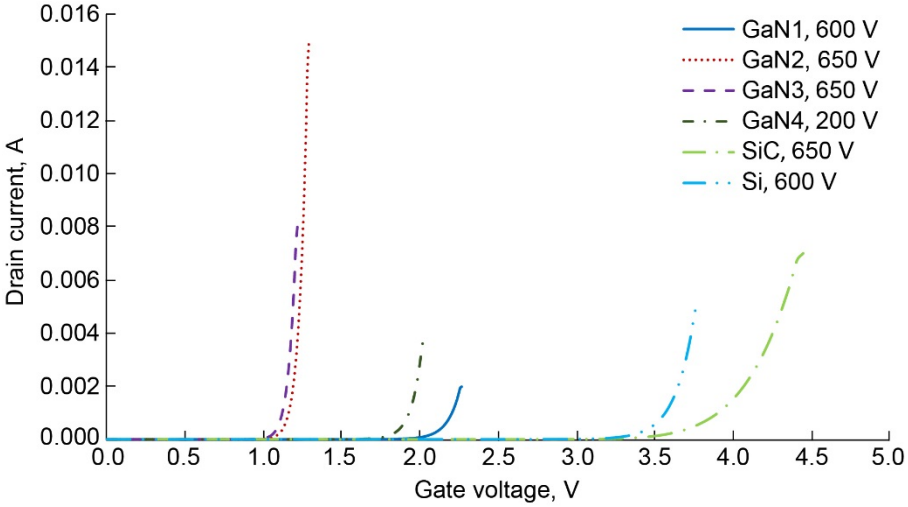


Figure 10.—Sample gate-to-source voltage sweeps.

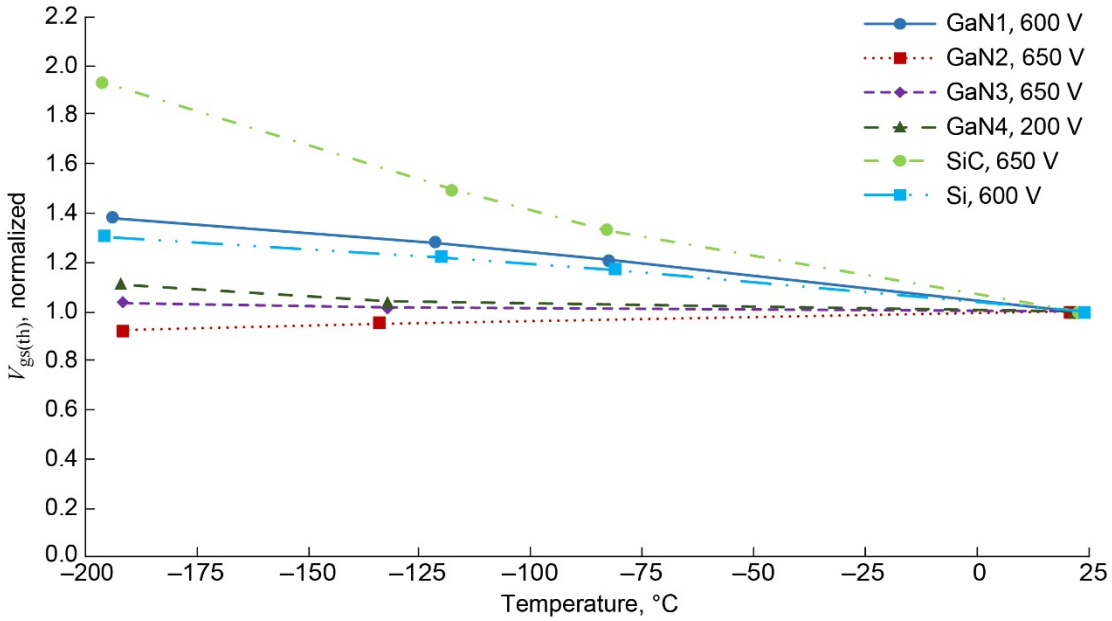


Figure 11.—Normalized gate-to-source threshold voltage ($V_{gs(th)}$) for GaN, SiC, and Si devices.

3.3 Gate-to-Source Leakage Current

The gate-to-source leakage current is gate current that flows when the drain is shorted to the source and the gate voltage is typically set at or close to its plus or minus maximum value (Refs. 6 to 8). Both the forward leakage current (I_{gssf}; $V_{gs} > 0$ V) and reverse leakage current (I_{gssr}; $V_{gs} < 0$ V) were measured. Ideally, the leakage currents would be 0 A but, in practicality, the currents are nonzero but small in the tenths of milliamp to picoamp range for the devices tested. The I_{gssf} test configuration diagram is shown in Figure 12. For I_{gssr}, a negative V_{gs} voltage is applied. Shorting of the drain to source can be done manually at the interface panel or by providing a zero-voltage bias with the curve tracer. The latter was used for these tests. The leakage current value recorded for each device is the average of ≥25 readings, automatically computed by the curve tracer. These values were then entered into a Microsoft® Excel® spreadsheet where the average value of the 10 samples was computed for each device model. With the exception of the cascode GaN device shown in Figure 13, all the remaining GaN devices showed a marked decrease in I_{gssf} (Figure 14) and I_{gssr} (Figure 15) of as much as 70 percent at LN_2 temperature. The cascode GaN showed a significant increase in I_{gssf} and a moderate decrease in I_{gssr} of a little over 30 percent. Both the SiC and Si devices showed an increase or minor decrease in I_{gssf} and I_{gssr} with a decrease in temperature (Figure 13 and Figure 16).

GaN devices, unlike Si and SiC, do not have a gate oxide layer since oxide growth is not an option (Ref. 14). As a result, the gate leakage current for GaN devices is higher in the microamp and even milliamp range as compared to the nanoamp range for Si and SiC.

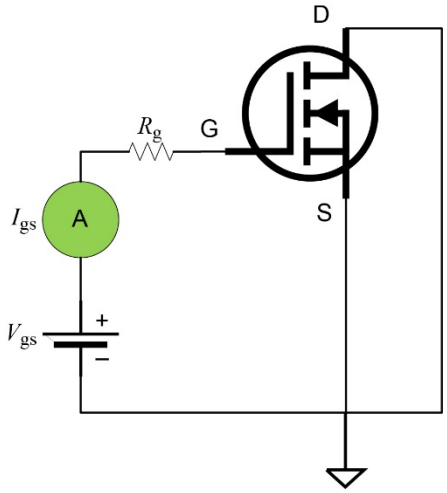


Figure 12.—Gate leakage test configuration. Where D is drain, I_{gs} is gate-to-source current, R_g is gate resistance, S is source, and V_{gs} is gate-to-source voltage.

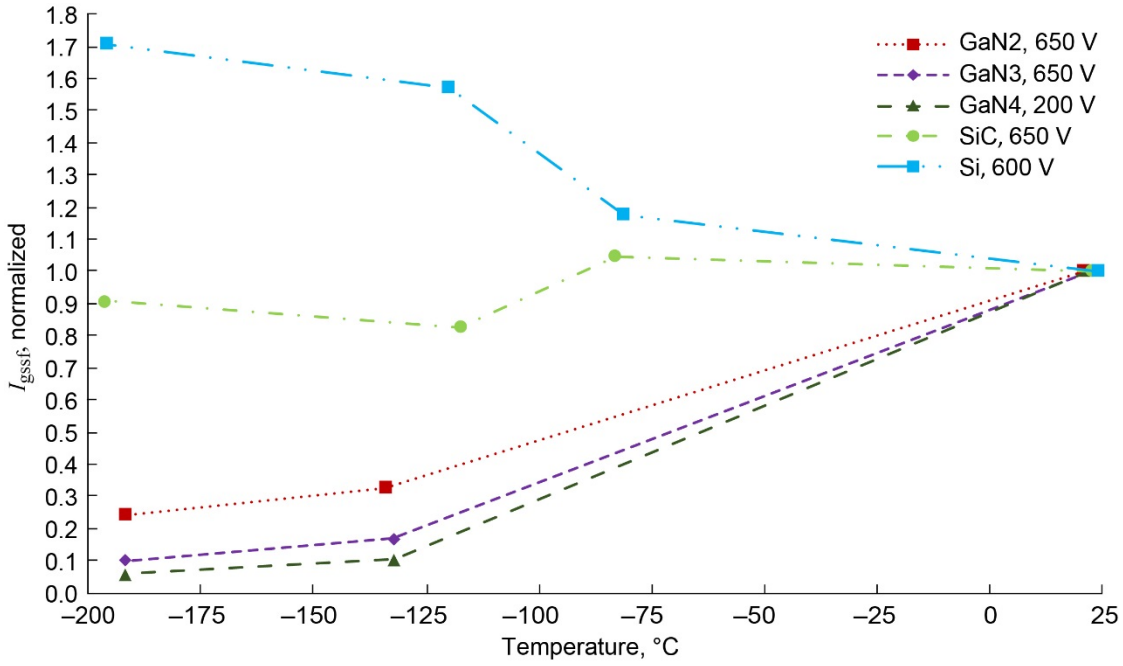


Figure 13.—Forward gate-to-source leakage current (I_{gssf}) for GaN cascode device.

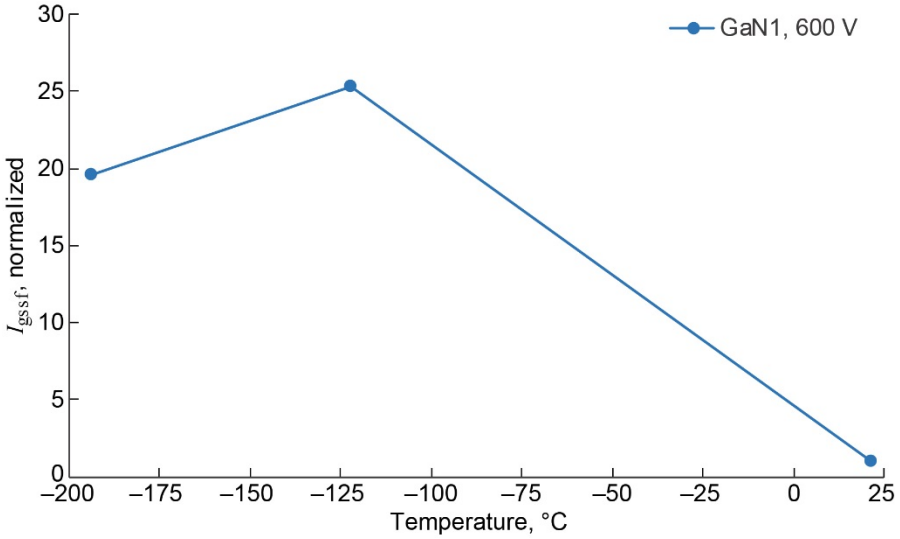


Figure 14.—Forward gate-to-source leakage current (I_{gssf}) for GaN, SiC, and Si devices.

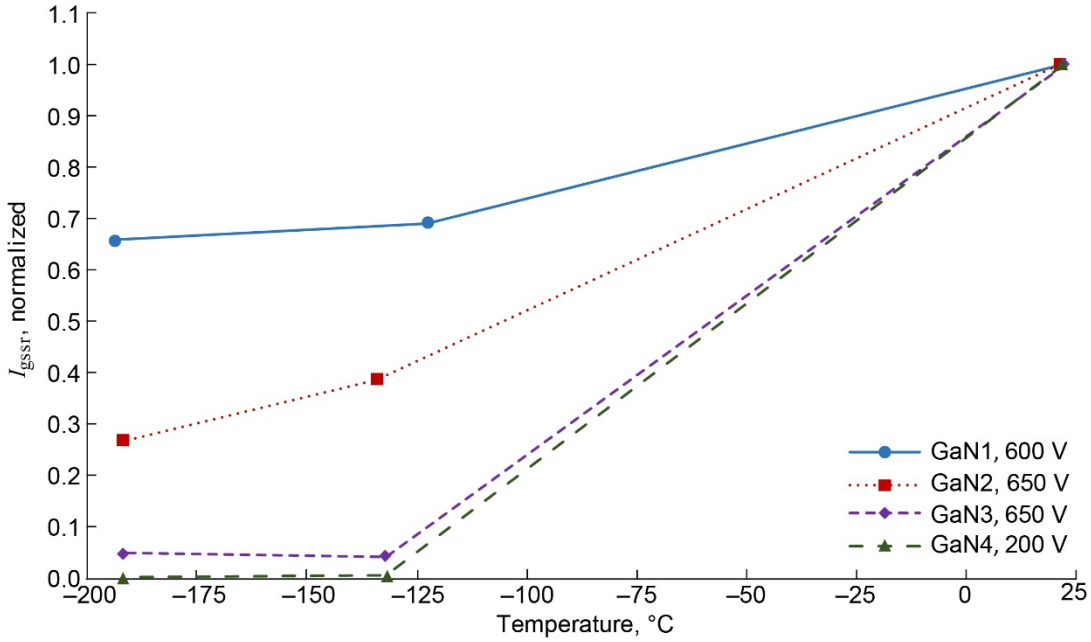


Figure 15.—Gate-to-source reverse leakage current (I_{gssr}) for GaN devices.

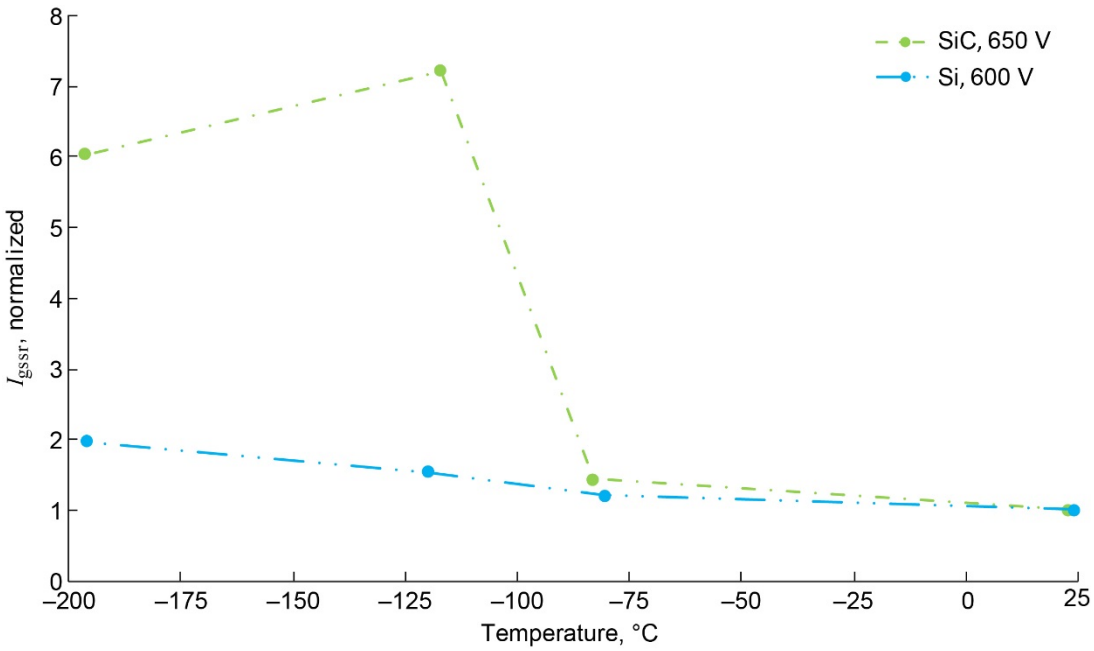


Figure 16.—Gate-to-source reverse leakage current (I_{gssr}) for SiC and Si devices.

3.4 Drain-to-Source Leakage Current (I_{dss}) and Drain-to-Source Breakdown Voltage (BV_{dss})

The drain-to-source leakage current, I_{dss}, is measured with the gate tied to the source or the gate-to-source bias set to 0 V via the curve tracer and the drain-to-source voltage (V_{ds}) set to 100 percent of the rated voltage (Refs. 7, 8, and 10). For this test, the gate was tied to the source at the interface panel to minimize inadvertent turnon of the device due to dV/dt transients, and the V_{ds} voltage was swept from 0 V to the rated voltage. See Figure 17 for the test configuration and Figure 18 for sample I_{dss} sweeps at ambient temperature. The latter shows that the SiC and Si devices have the lowest drain-to-source leakage current sweeps with the GaN4 device (lower voltage device) having the highest leakage.

The normalized I_{dss} versus temperature is shown in Figure 19. The data shows that the cascode device's (GaN1) leakage current essentially remains constant while the remaining GaN devices and the SiC device show moderate to significant drops. The most significant decrease is for the GaN3 and GaN4 devices, over 90 percent, below –130 °C.

Note that I_{dss} data for the Si device is not shown. The reason for this is that the I_{dss} for this device is measured at 600 V, but the breakdown voltage drops below 600 V as the temperature drops. The breakdown voltage is measured with the same configuration as in Figure 17. The difference is that for BV_{dss}, the V_{ds} voltage is increased until a target drain current given in the datasheet is met. Figure 20 shows the BV_{dss} results for the Si device, indicating that it linearly drops to about 80 percent

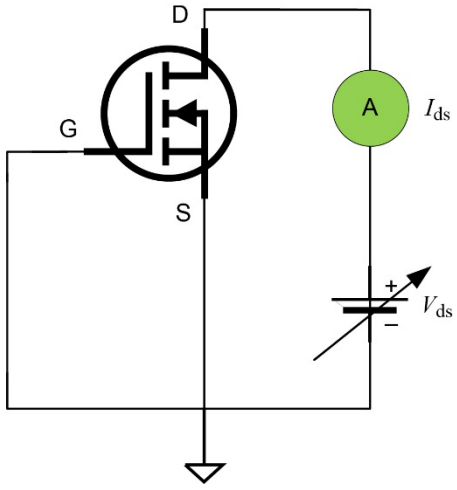


Figure 17.—Drain (D) leakage test configuration. Where G is gate, I_{ds} is drain-to-source current, S is source, and V_{ds} is drain-to-source voltage.

of its ambient temperature value at LN_2 temperature. Breakdown voltages versus temperature were not measured for the GaN and SiC devices due to device failures experienced during initial testing. Inadvertent turnon during the V_{ds} sweep is suspected as the cause of failure. These lateral GaN devices do not have a body diode, as in traditional silicon MOSFETs, and as a result, they do not possess a physical avalanche mechanism and there are no reverse recovery losses. Instead, they have a dielectric breakdown voltage similar to a capacitor and typically have much higher breakdown voltages than their V_{ds} rated value, as much as 30 percent or more (Ref. 15).

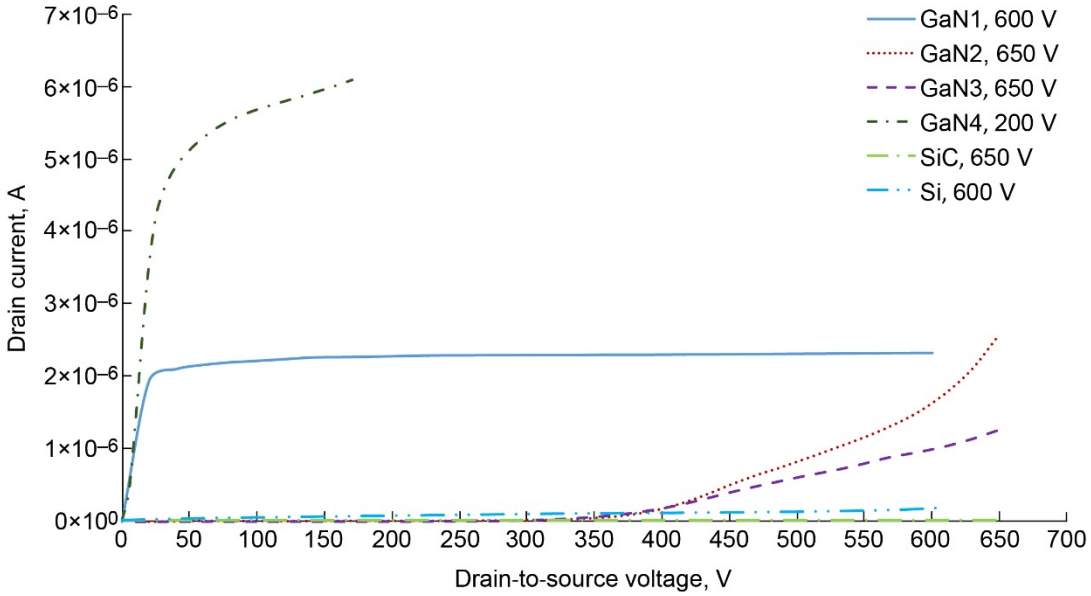


Figure 18.—Sample drain-to-source leakage current sweeps. Gate-to-source voltage (V_{gs}) = 0 V.

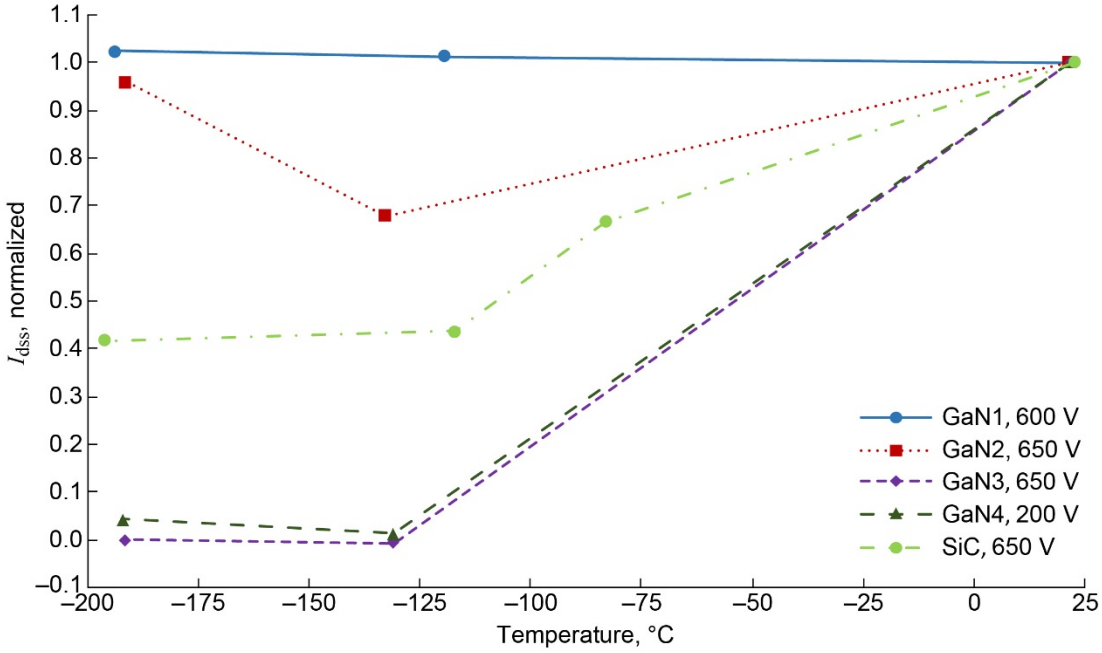


Figure 19.—Drain-to-source leakage current (I_{dss}) for GaN and Si devices.

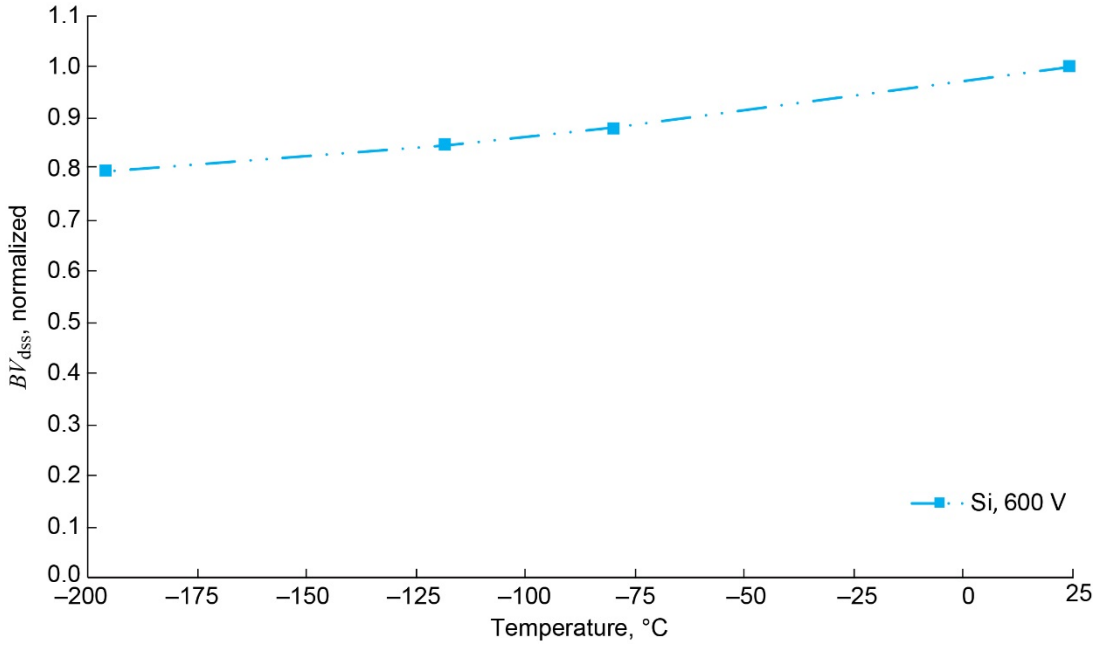


Figure 20.—Drain-to-source breakdown voltage (BV_{dss}) for Si device.

3.5 Input, Output, and Reverse Transfer Capacitance

The input capacitance (C_{iss}) is the sum of the gate-to-source capacitance (C_{gs}) and the gate-to-drain capacitance (C_{gd}). The output capacitance (C_{oss}) is the sum of C_{gd} and the drain-to-source capacitance (C_{ds}). The reverse transfer capacitance (C_{rss}) is simply $C_{gd.}$ A simple diagram of the component-level capacitances is presented in Figure 21. The configuration for CV measurements is more involved and not included in this report. If interested, however, please refer to Reference 11 for the Keithley curve tracer test configurations.

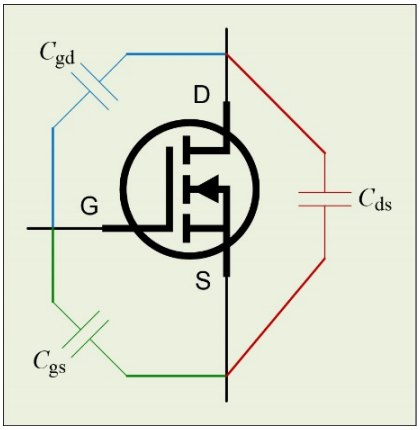


Figure 21.—Metal-oxide-semiconductor field-effect transistor component-level capacitance. Where C_{ds} is drain-to-source capacitance, C_{gd} is gate-to-drain capacitance, and C_{gs} is gate-to-source capacitance.

Figure 22 shows sample plots for C_{iss} and C_{oss} for GaN, SiC, and Si devices at ambient temperature. Note that for the Si device, the plot only extends about 25 V even though the device is rated at 600 V. The reason is that the manufacturer specifies the component-level capacitances at 25 V. The GaN and SiC devices are specified at values (400 and 500 V, respectively) below the rated voltage but at significantly higher voltages than the Si device. Also, the GaN device has, in general, lower C_{iss} and C_{oss} compared to the SiC and Si devices with the Si device having the highest values. C_{rss} data was not plotted due to the difficulty in measuring accurate absolute values. Of these devices, the GaN device is an SMT part and both the SiC and Si devices are TO–247 through-hole packages, resulting in higher capacitance.

Normalized data for C_{iss}, C_{oss}, and C_{rss} versus temperature are shown in Figure 23 to Figure 25, respectively. The data show that, in general, the capacitance values remain constant or drop less than 10 percent, down to –196 °C. The exception being the SiC C_{iss}, shown in Figure 23, with a drop of slightly over 20 percent at –196 °C. As a result, switching losses due to device capacitance will show minimal to negligible improvement at cryogenic temperatures (Refs. 16 and 17). The data also validate that device capacitances have little to no dependence on temperature, even down to cryogenic values (Ref. 8).

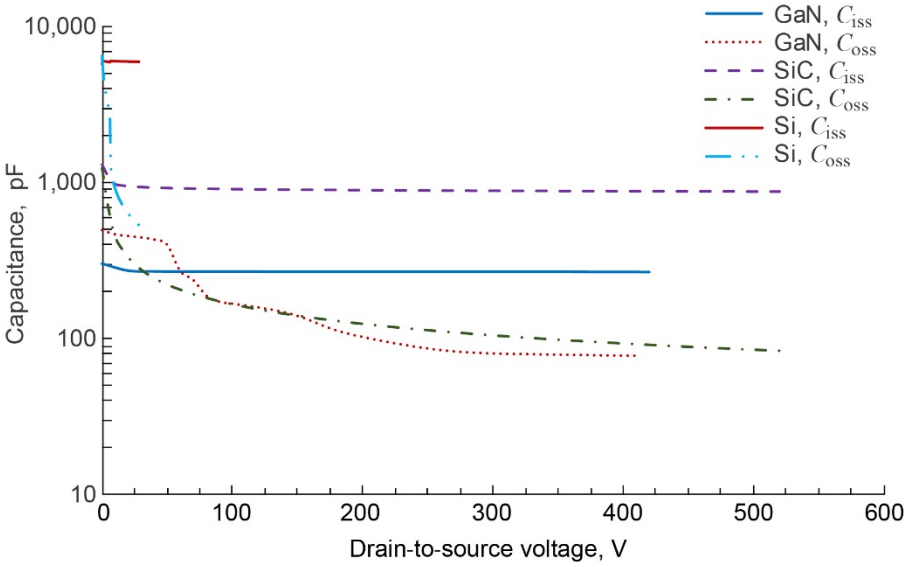


Figure 22.—Sample input and output capacitance sweeps.

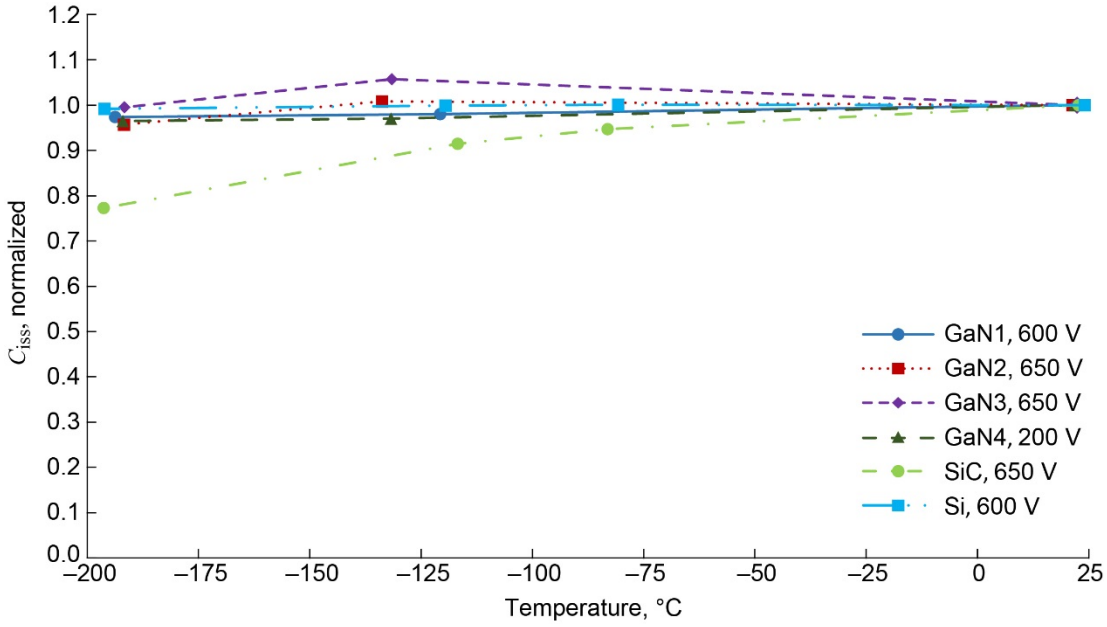


Figure 23.—Normalized input capacitance (C_{iss}).

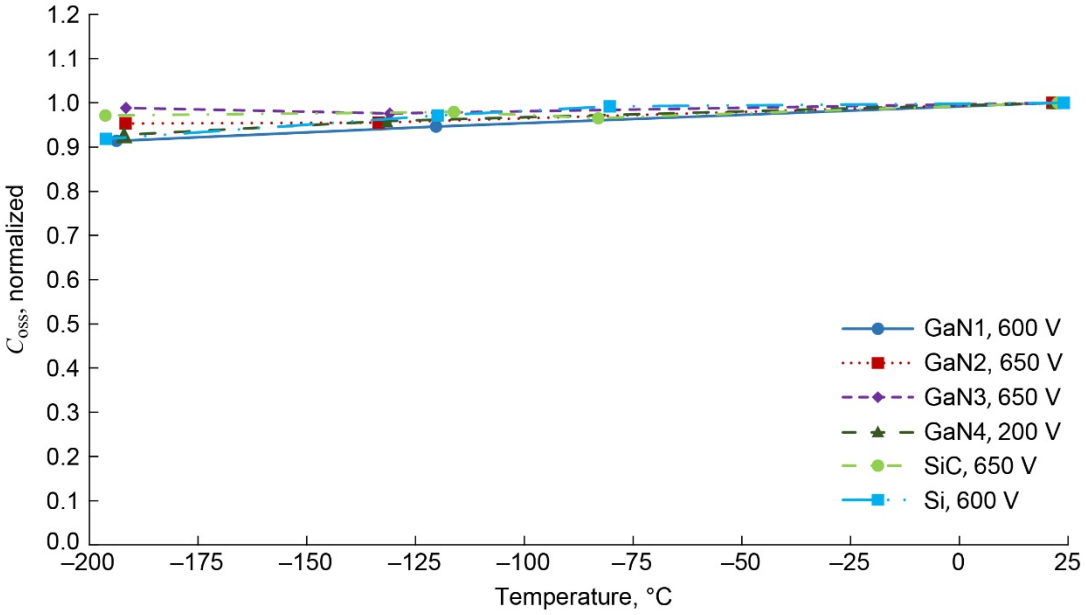


Figure 24.—Normalized output capacitance (C_{oss}).

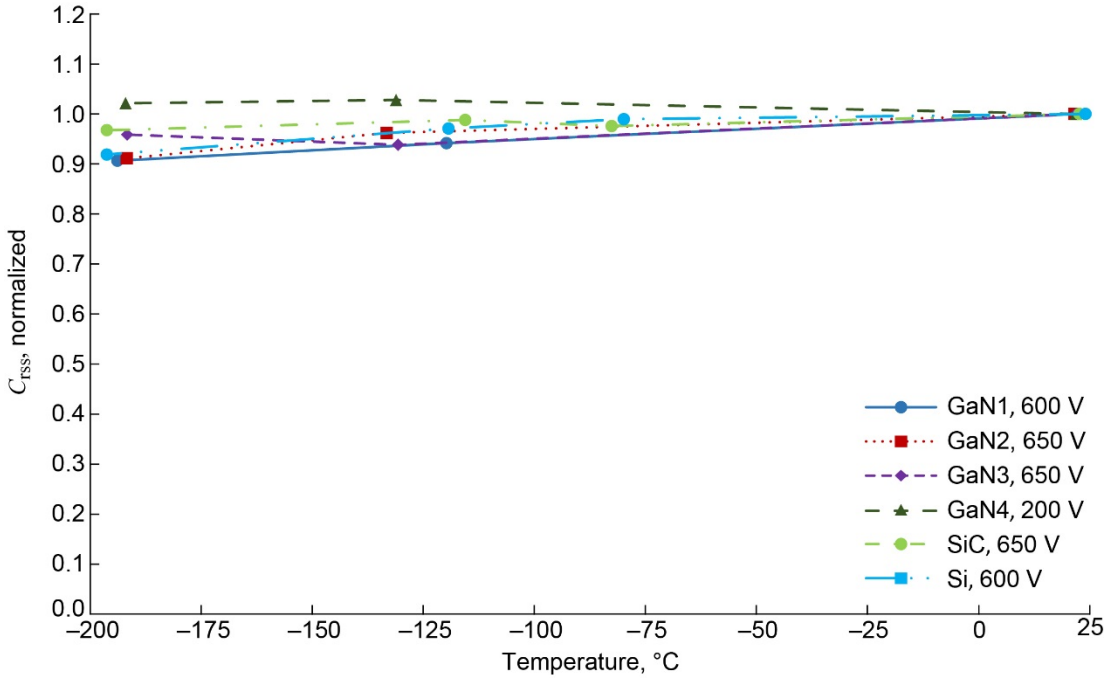


Figure 25.—Normalized reverse transfer capacitance (C_{rss}).

3.6 Post- to Pre-LN_2 Submersion Test Comparison

Ambient test data was retaken after the device was submerged in LN_2 and compared to the ambient data taken prior to LN_2 submersion. The post-LN_2 submersion data was divided by the pre-LN_2 data and graphed (Figure 26 to Figure 31). A value of 1.0 indicates that the parameter did not change after LN_2 submersion, a value less than 1.0 means that the parameter decreased, and a value higher than 1.0 means that the parameter increased after submersion. A forensic determination for the root cause of changes observed in parametric values is beyond the scope of this effort.

Of the six devices tested, the cascode GaN device (Figure 26) showed the least change in its parameters and the SiC device (Figure 30) exhibited the most change in its parameters due to LN_2 submersion. The other devices' parameter changes were within ±20 percent. The parameters that exhibited the most change are the drain-to-source and gate-to-source leakage currents, and some of that change might be attributed to the difficulty in measuring such small currents with values as low as picoamps. On the contrary, the on-resistance, gate-to-source threshold voltage, and device capacitance parameters showed little to no change in value after being exposed to the cryogenic temperatures.

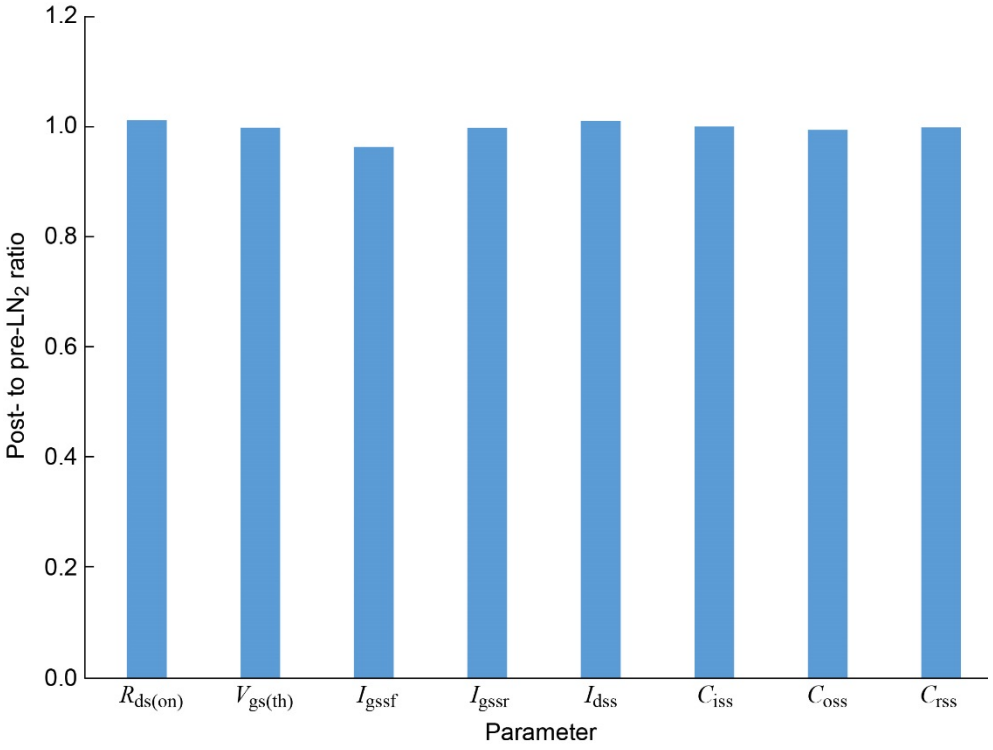


Figure 26.—GaN1 ratio of post-LN_2 to pre-LN_2 parameter change. Where C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

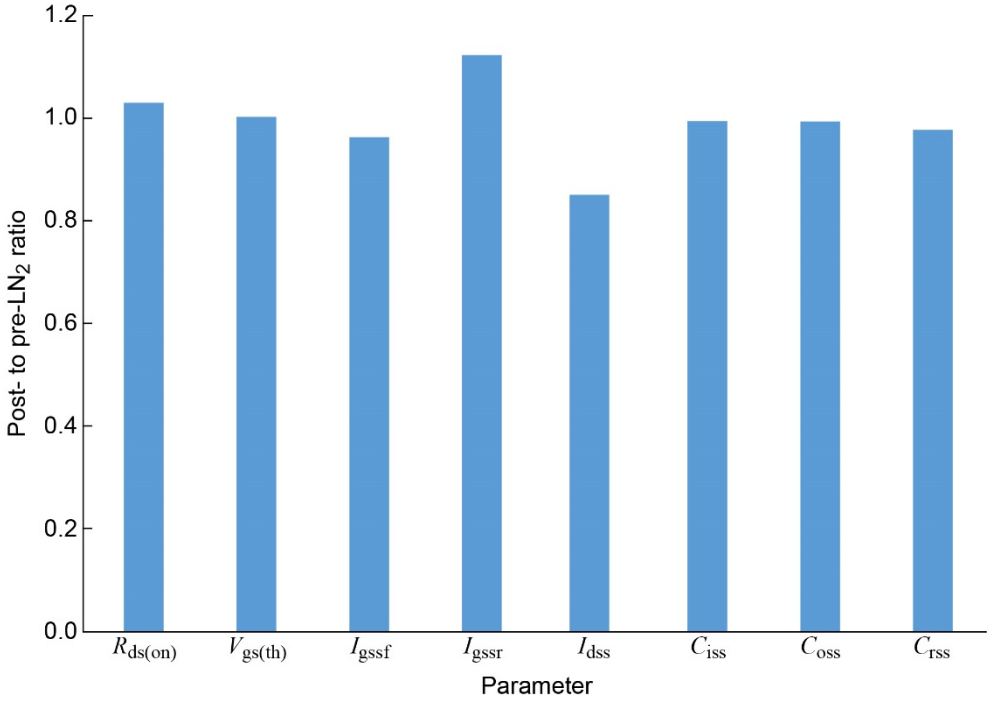


Figure 27.—GaN2 ratio of post-LN_2 to pre-LN_2 parameter change. Where C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

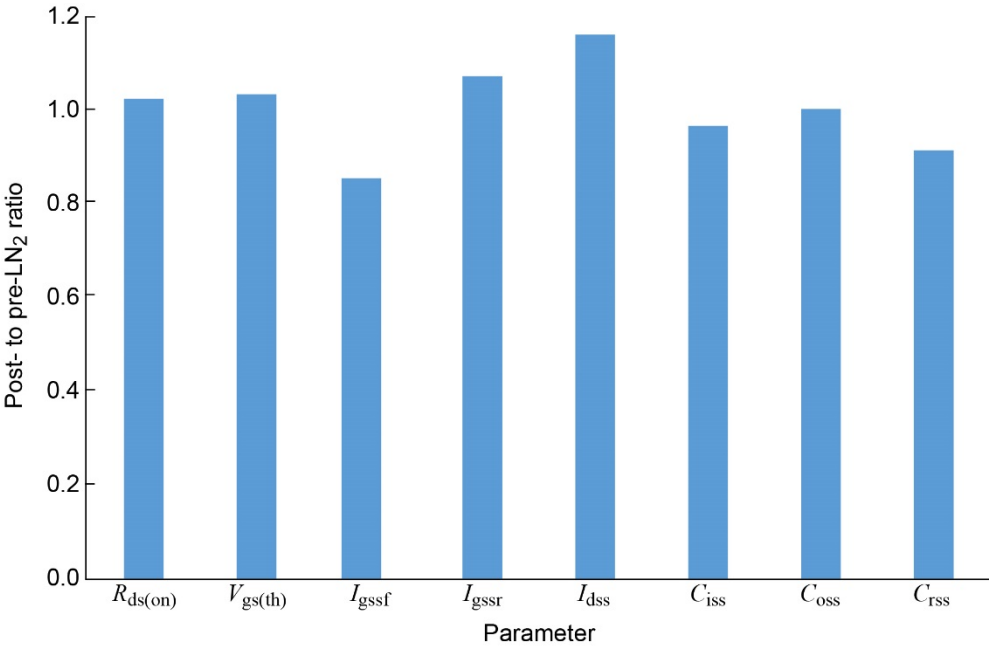


Figure 28.—GaN3 ratio of post-LN_2 to pre-LN_2 parameter change. Where C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

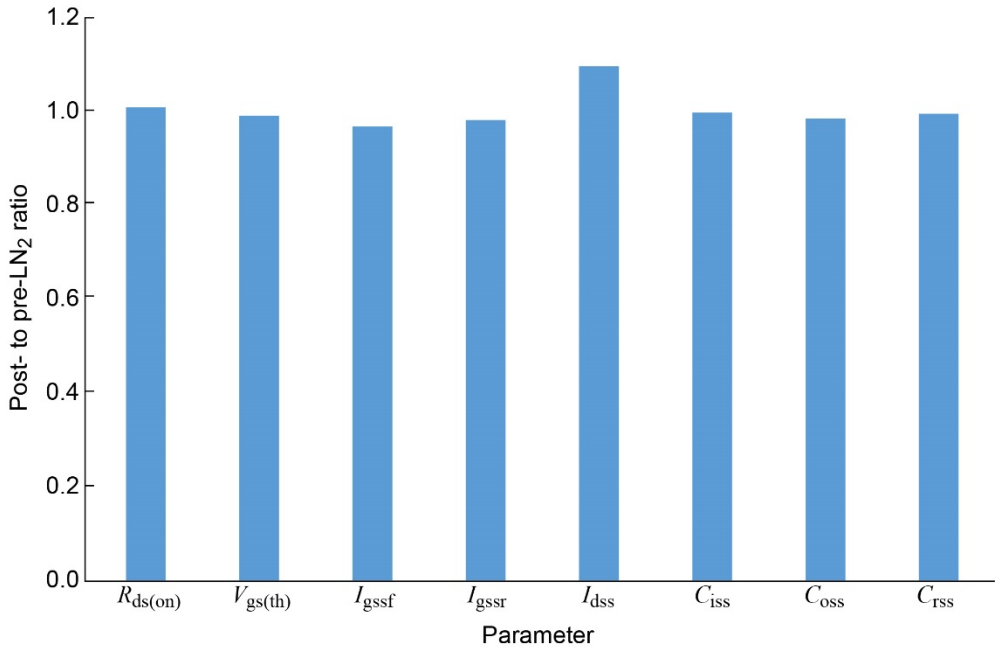


Figure 29.—GaN4 ratio of post-LN_2 to pre-LN_2 parameter change. Where C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

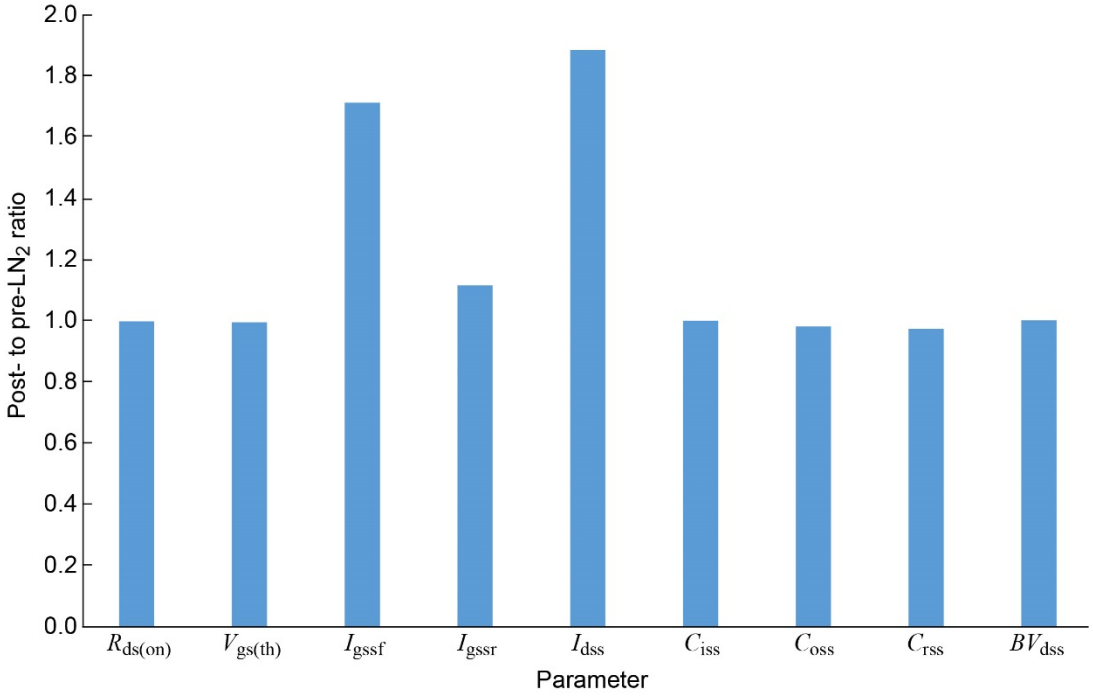


Figure 30.—SiC ratio of post-LN_2 to pre-LN_2 parameter change. Where BV_{dss} is drain-to-source breakdown voltage, C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

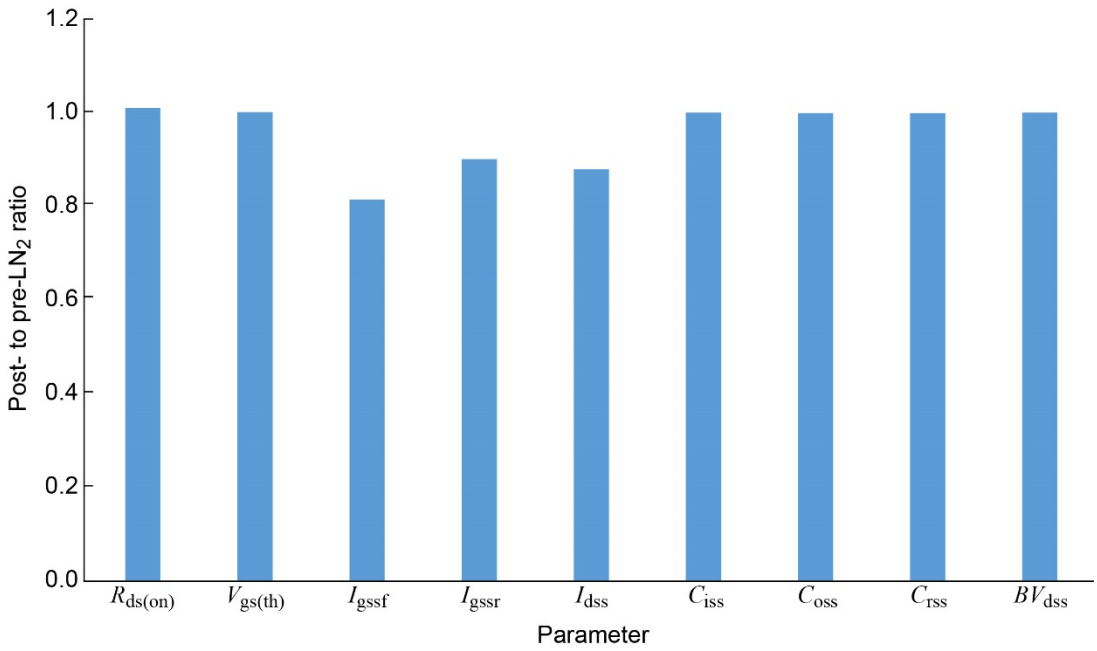


Figure 31.—Si ratio of post-LN_2 to pre-LN_2 parameter change. Where BV_{dss} is drain-to-source breakdown voltage, C_{iss} is input capacitance, C_{oss} is output capacitance, C_{rss} is reverse transfer capacitance, I_{dss} is drain-to-source leakage current, I_{gssf} is forward gate-to-source leakage current, I_{gssr} is reverse gate-to-source leakage current, $R_{ds(on)}$ is drain-to-source on-resistance, and $V_{gs(th)}$ is gate-to-source threshold voltage.

4.0 Conclusion

Three GaN devices, one cascode GaN device, one SiC device, and one Si device, 10 samples each, were subjected to parametric characterization at ambient and cryogenic temperatures down to LN_2 temperature (–196 °C). The results show that the on-resistance decreases significantly, by approximately 60 to 80 percent, for GaN and Si but increases significantly, by approximately 160 percent, for SiC primarily due to the effect known as carrier freezeout. It is important to note that for GaN and Si, most of the on-resistance decrease occurs in the first 100 °C temperature drop. These changes would lead to a significant drop in on-resistance losses, thus improving efficiency. However, the Si device has a larger on-resistance at ambient temperature compared to the SiC and GaN wide bandgap devices. In terms of the gate-to-source threshold voltage, the GaN devices showed the least change of about a 10-percent increase or decrease, followed by the cascode GaN and Si devices with about a 40-percent increase, and the SiC device with over a 90-percent increase. GaN devices have relatively low maximum gate-to-source voltage (V_{gs}) of around 6 to 7 V compared to cascode GaN, Si, or SiC (>18 V), so a 10-percent change is a welcome result. A major drawback of the GaN devices is the low V_{gs} and that they can be easily damaged in application if the gate drive circuit is not carefully designed to clamp the V_{gs} transient voltages to below the maximum rating.

The data for leakage current measurements show mixed results that may be partly attributed to the very low leakage values that needed to be measured. However, in general, leakage currents decrease for GaN devices but increase for cascode GaN, Si, and SiC devices. Note that the drain-to-source leakage current for the Si device was not measured since its drain-to-source breakdown voltage decreased with decreasing temperature. Also, the drain-to-source breakdown voltage for the GaN, cascode GaN, and SiC devices was not measured due to the high rate of device failure during attempted measurements.

The capacitance measurement results confirm the fact that device capacitances are essentially not temperature dependent. The results show that the capacitances varied by no more than 10 percent, except for the SiC input capacitance (C_{iss}), which decreased by a little over 20 percent. Finally, post-LN_2 submersion measurements show that the device parameters for all the devices were not significantly affected by the cryogenic temperatures with the exception of the drain-to-source leakage current (I_{dss}) and forward gate-to-source leakage current (I_{gssf}) of the SiC device. Based on these results, GaN devices are able

to operate at cryogenic temperatures and show marked improvements in their measured parameters, indicating the potential for increased efficiency gains and high power density at ambient and cryogenic temperatures.

Note that the results presented are for only the samples tested and may not be representative of all GaN, SiC, and Si devices, especially for GaN since it is a technology that is far from reaching maturity.

Appendix A.—Device Datasheet Parameters and Test Conditions

This appendix contains the device parameters and test conditions, which are sourced from the device datasheets (Table I to Table IX).

TABLE I.—DRAIN-TO-SOURCE ON-RESISTANCE, $R_{ds(on)}$

Device	Typical at 25 °C, mW	Max. at 25 °C, mW	Test condition at 25 °C
GaN1, 600 V	52	63	V_{gs}[a] = 8 V, I_d[b] = 24 A
GaN2, 650 V	27	Not stated	V_{gs} = 6 V, I_d = 18 A
GaN3, 650 V	55	Not stated	V_{gs} = 6 V, I_d = 9 A
GaN4, 200 V	18	25	V_{gs} = 5 V, I_d = 12 A
SiC, 650 V	60	78	V_{gs} = 18 V, I_d = 13 A
Si, 600 V	Not stated	190	V_{gs} = 10 V, I_d = 18 A

[a]Gate-to-source voltage.
[b]Drain current.

TABLE II.—GATE-TO-SOURCE THRESHOLD VOLTAGE, $V_{gs(th)}$

Device	Typical at 25 °C, V	Max. at 25 °C, V	Test condition at 25 °C
GaN1, 600 V	2.1	2.6	V_{ds}[a] = V_{gs}[b], I_d[c] = 0.7 mA
GaN2, 650 V	1.4	Not stated	V_{ds} = V_{gs}, I_d = 12 mA
GaN3, 650 V	1.4	Not stated	V_{ds} = V_{gs}, I_d = 6 mA
GaN4, 200 V	1.4	2.5	V_{ds} = V_{gs}, I_d = 3 mA
SiC, 650 V	Not stated	5.6	V_{ds} = V_{gs}, I_d = 6.67 mA
Si, 600 V	Not stated	5.0	V_{ds} = V_{gs}, I_d = 4 mA

[a]Drain-to-source voltage.
[b]Gate-to-source voltage.
[c]Drain current.

TABLE III.—FORWARD GATE-TO-SOURCE LEAKAGE CURRENT, I_{gssf}

Device	Typical at 25 °C	Max. at 25 °C	Test condition at 25 °C
GaN1, 600 V	Not stated	100 nA	V_{gs}[a] = 18 V, V_{ds}[b] = 0 V
GaN2, 650 V	80 mA	Not stated	V_{gs} = 6 V, V_{ds} = 0 V
GaN3, 650 V	40 mA	Not stated	V_{gs} = 6 V, V_{ds} = 0 V
GaN4, 200 V	1 mA	3 mA	V_{gs} = 5 V, V_{ds} = 0 V
SiC, 650 V	Not stated	100 nA	V_{gs} = 22 V, V_{ds} = 0 V
Si, 600 V	Not stated	200 nA	V_{gs} = 30 V, V_{ds} = 0 V

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.

TABLE IV.—REVERSE GATE-TO-SOURCE LEAKAGE CURRENT, I_{gssr}

Device	Typical at 25 °C, mA	Max. at 25 °C	Test condition at 25 °C
GaN1, 600 V	Not stated	–100 nA	V_{gs}[a] = –18 V, V_{ds}[b] = 0 V
GaN2, 650 V	–80	Not stated	V_{gs} = –6 V, V_{ds} = 0 V
GaN3, 650 V	–40	Not stated	V_{gs} = –6 V, V_{ds} = 0 V
GaN4, 200 V	–50	–150 mA	V_{gs} = –4 V, V_{ds} = 0 V
SiC, 650 V	Not stated	–100 mA	V_{gs} = –4 V, V_{ds} = 0 V
Si, 600 V	Not stated	–200 mA	V_{gs} = –30 V, V_{ds} = 0 V

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.

TABLE V.—DRAIN-TO-SOURCE LEAKAGE CURRENT, I_{dss}

Device	Typical at 25 °C, mA	Max. at 25 °C, mA	Test condition at 25 °C
GaN1, 600 V	4	40	V_{gs}[a] = 0 V, V_{ds}[b] = 600 V
GaN2, 650 V	4	Not stated	V_{gs} = 0 V, V_{ds} = 650 V
GaN3, 650 V	2	Not stated	V_{gs} = 0 V, V_{ds} = 650 V
GaN4, 200 V	50	150	V_{gs} = 0 V, V_{ds} = 160 V
SiC, 650 V	1	10	V_{gs} = 0 V, V_{ds} = 650 V
Si, 600 V	Not stated	100	V_{gs} = 0 V, V_{ds} = 600 V

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.

TABLE VI.—DRAIN-TO-SOURCE BREAKDOWN VOLTAGE, BV_{dss}

Device	I_d at 25 °C, A	Min. at 25 °C, V	Test condition at 25 °C
GaN1, 600 V	36	600	V_{gs}[a] = 0 V, I_d[b] = Not provided
GaN2, 650 V	60	650	V_{gs} = 0 V, I_d = 1 mA
GaN3, 650 V	30	650	V_{gs} = 0 V, I_d = 1 mA
GaN4, 200 V	22	200	V_{gs} = 0 V, I_d = 200 mA
SiC, 650 V	39	650	V_{gs} = 0 V, I_d = 1 mA
Si, 600 V	36	600	V_{gs} = 0 V, I_d = 250 mA

[a]Gate-to-source voltage.
[b]Drain current.

TABLE VII.—INPUT CAPACITANCE, C_{iss}

Device	Typical at 25 °C, pF	Max. at 25 °C, pF	Test condition at 25 °C
GaN1, 600 V	2,200	Not stated	V_{gs}[a] = 0 V, V_{ds}[b] = 400 V, f[c] = 1 MHz
GaN2, 650 V	525	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN3, 650 V	260	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN4, 200 V	380	540	V_{gs} = 0 V, V_{ds} = 100 V, f = 1 MHz
SiC, 650 V	852	Not stated	V_{gs} = 0 V, V_{ds} = 500 V, f = 1 MHz
Si, 600 V	5,800	Not stated	V_{gs} = 0 V, V_{ds} = 25 V, f = 1 MHz

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.
[c]Frequency.

TABLE VIII.—OUTPUT CAPACITANCE, C_{oss}

Device	Typical at 25 °C, pF	Max. at 25 °C, pF	Test condition at 25 °C
GaN1, 600 V	115	Not stated	V_{gs}[a] = 0 V, V_{ds}[b] = 400 V, f[c] = 1 MHz
GaN2, 650 V	134	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN3, 650 V	65	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN4, 200 V	240	320	V_{gs} = 0 V, V_{ds} = 100 V, f = 1 MHz
SiC, 650 V	55	Not stated	V_{gs} = 0 V, V_{ds} = 500 V, f = 1 MHz
Si, 600 V	570	Not stated	V_{gs} = 0 V, V_{ds} = 25 V, f = 1 MHz

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.
[c]Frequency.

TABLE IX.—REVERSE TRANSFER CAPACITANCE, C_{rss}

Device	Typical at 25 °C, pF	Max. at 25 °C, pF	Test condition at 25 °C
GaN1, 600 V	19.0	Not stated	V_{gs}[a] = 0 V, V_{ds}[b] = 400 V, f[c] = 1 MHz
GaN2, 650 V	4.0	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN3, 650 V	2.0	Not stated	V_{gs} = 0 V, V_{ds} = 400 V, f = 1 MHz
GaN4, 200 V	1.8	2.7	V_{gs} = 0 V, V_{ds} = 100 V, f = 1 MHz
SiC, 650 V	24.0	Not stated	V_{gs} = 0 V, V_{ds} = 500 V, f = 1 MHz
Si, 600 V	30.0	Not stated	V_{gs} = 0 V, V_{ds} = 25 V, f = 1 MHz

[a]Gate-to-source voltage.
[b]Drain-to-source voltage.
[c]Frequency.

Appendix B.—Drain-to-Source On-Resistance ($R_{ds(on)}$) Comparison of 600- and 650-V Si, SiC, and GaN Devices

This appendix contains the drain-to-source on-resistance comparison of the 600- and 650-V Si, SiC, and GaN devices (Figure 32).

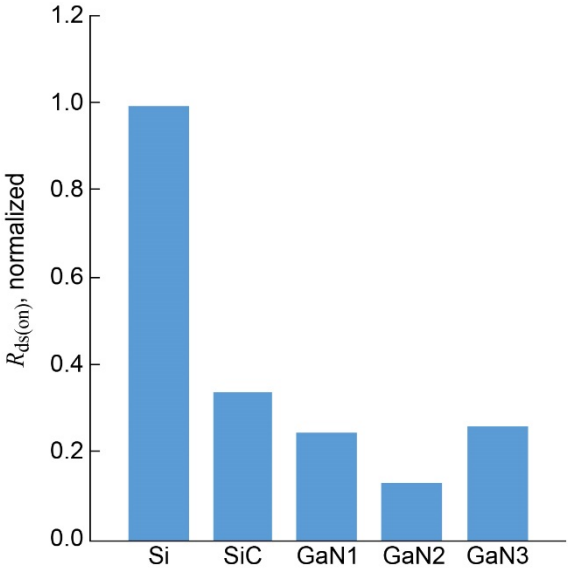


Figure 32.—Drain-to-source on-resistance comparison for 600- and 650-V Si, Sic, and GaN devices.

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