National Aeronautics and Space Administration



Getting SiC Power Devices Off the Ground: Design, Testing, and Overcoming Radiation Threats

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Abbreviations & Acronyms



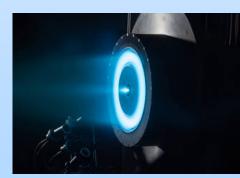
Acronym	Definition		Acronym	Definition
GCR	Galactic Cosmic Ray		SEE	Single-Event Effect
I _D	Drain Current		Si	Silicon
I _G	Gate Current		SiC	Silicon Carbide
I _R	Reverse-Bias Leakage Current		SOA	Safe Operating Area
ICSCRM	International Conference on Silicon Carbide and Related Materials		TAMU	Texas A&M University cyclotron facility
JFET	Junction Field Effect Transistor		TID	Total Ionizing Dose
LBNL	Lawrence Berkeley National Laboratory cyclotron facility		VDMOS	Vertical Double-diffused MOSFET
MOSFET	Metal Oxide Semiconductor Field Effect Transistor		V _{DS}	Drain-Source Voltage
RHA	Radiation Hardness Assurance		V_{GS}	Gate-Source Voltage
RHBD	Radiation Hardened By Design		V _R	Blocking Voltage
SEB	Single-Event Burnout			

Outline



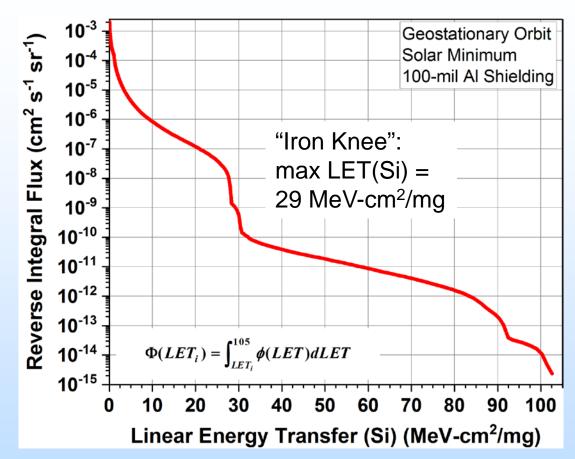
• Part 1: Design

- Understanding single-event effects susceptibility of SiC power devices through heavy-ion test data on different device types
- Part 2: Testing
 - Additional findings from heavy-ion test conditions
- Part 3: Overcoming Radiation Threats
 - Putting design insights into action: radiation hardening of a 1200 V SiC MOSFET
 - Radiation Hardness Assurance conclusions



Solar Electric Propulsion image courtesy of NASA

Heavy-Ion Environment



SEE radiation requirements are derived in part by the environment specified as a function of linear energy transfer (LET) in silicon; SiC test results therefore are in LET(Si)



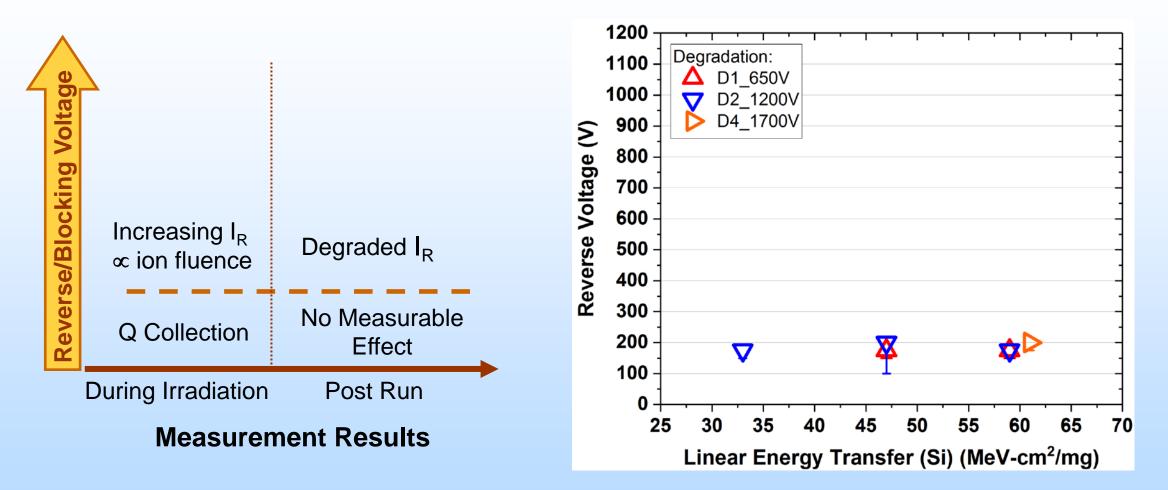
PART 1: DESIGN



SINGLE EVENT EFFECTS: LEARNING FROM DIODE DESIGNS

Schottky Diode Effects: Degradation

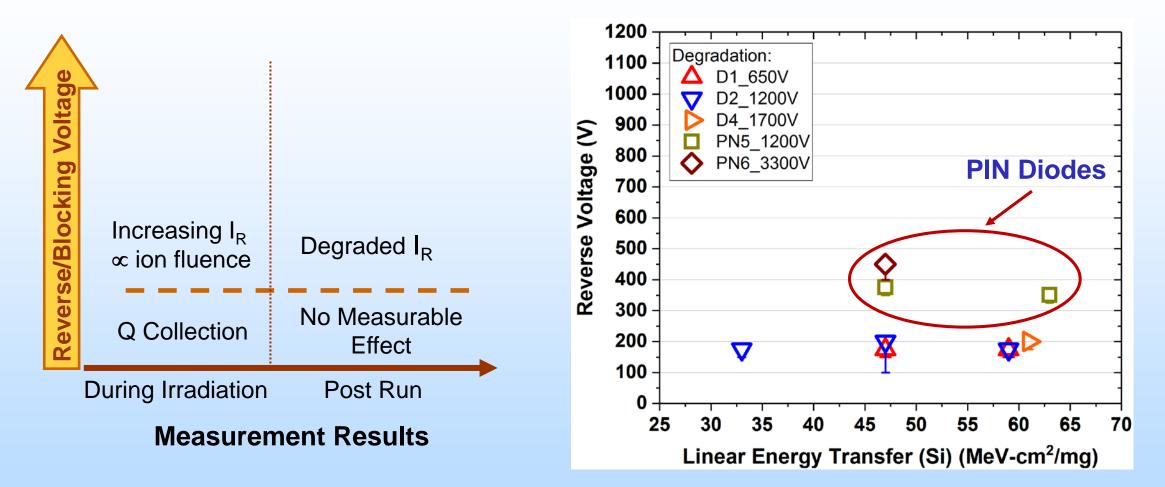




Onset V_R for degradation is similar for 650 V – 1700 V Schottky diodes: Electric field may not be a primary factor

Schottky vs. PIN Diode Effects: Degradation

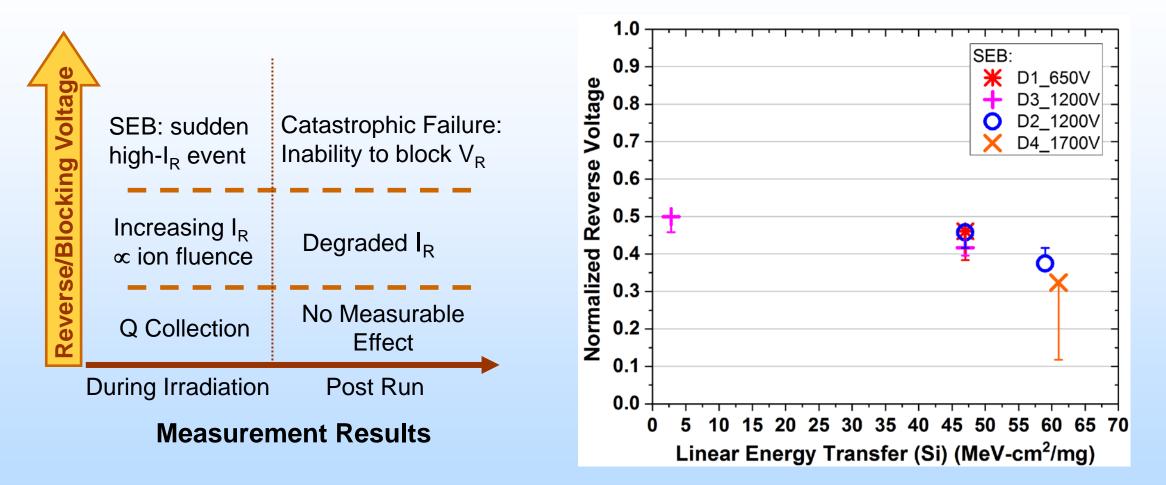




Onset V_R for degradation is higher for PIN diodes: The Schottky contact may contribute an additional mechanism

Schottky Diode Effects: SEB

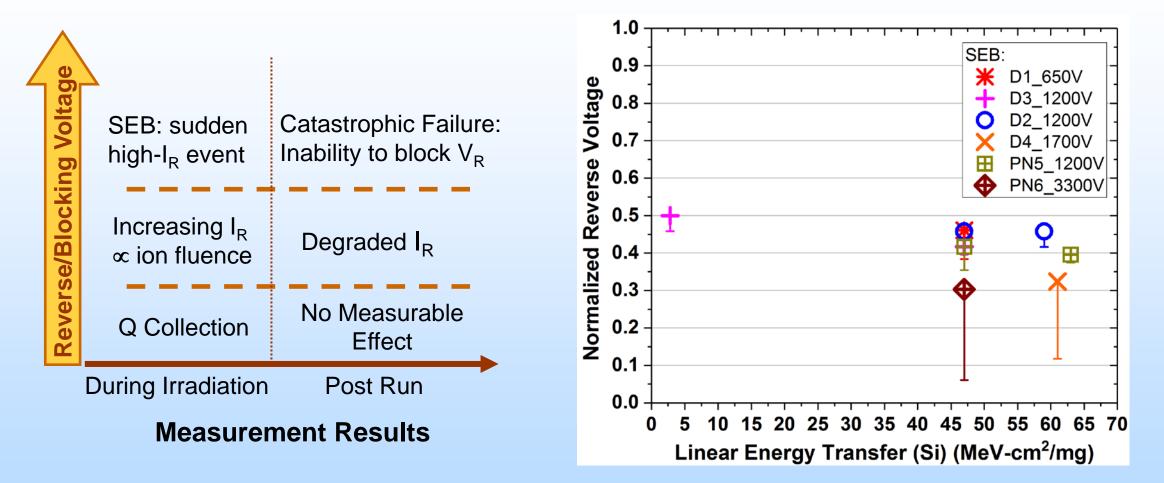




650 V – 1700 V Schottkys show SEB at similar fraction of rated V_R : Electric field dependent

Schottky vs. PIN Diode Effects: SEB





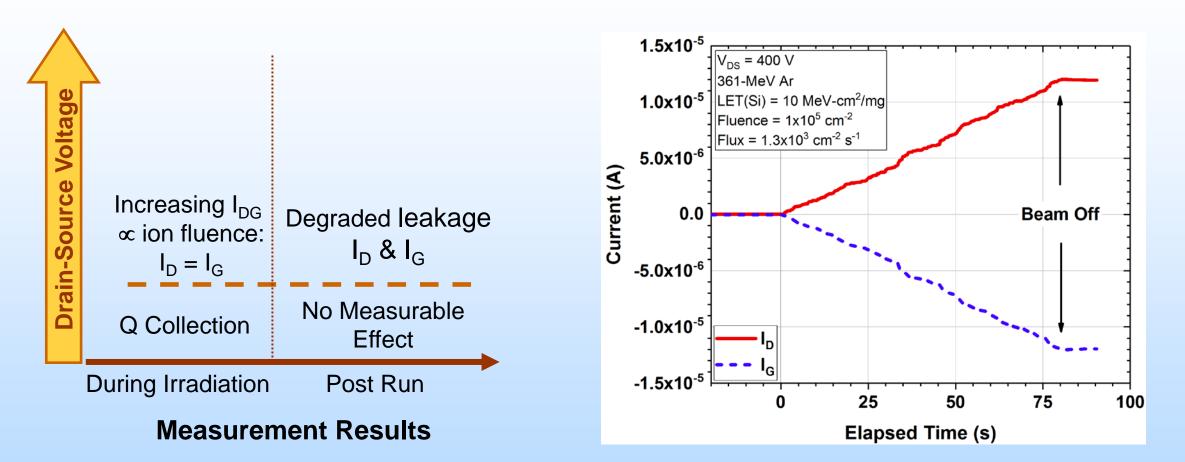
No difference between Schottky and PiN diodes for normalized SEB onset voltage



SINGLE EVENT EFFECTS: LEARNING FROM JFET DESIGNS

JFET Effects as a Function of V_{DS} at Fixed off V_{GS}: Degradation

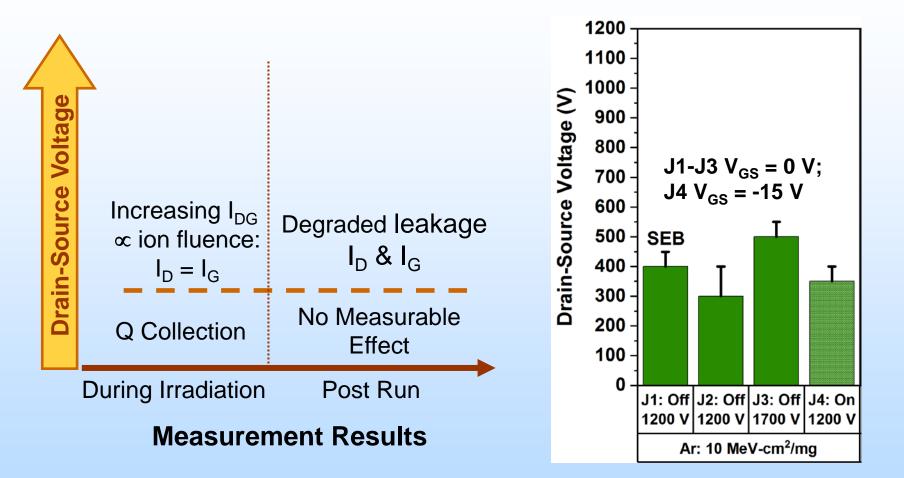




Degradation in normally-on and normally-off JFETs in this study is always drain-gate leakage, suggesting a trench design

JFET Effects as a Function of V_{DS} at Fixed off V_{GS}: Degradation

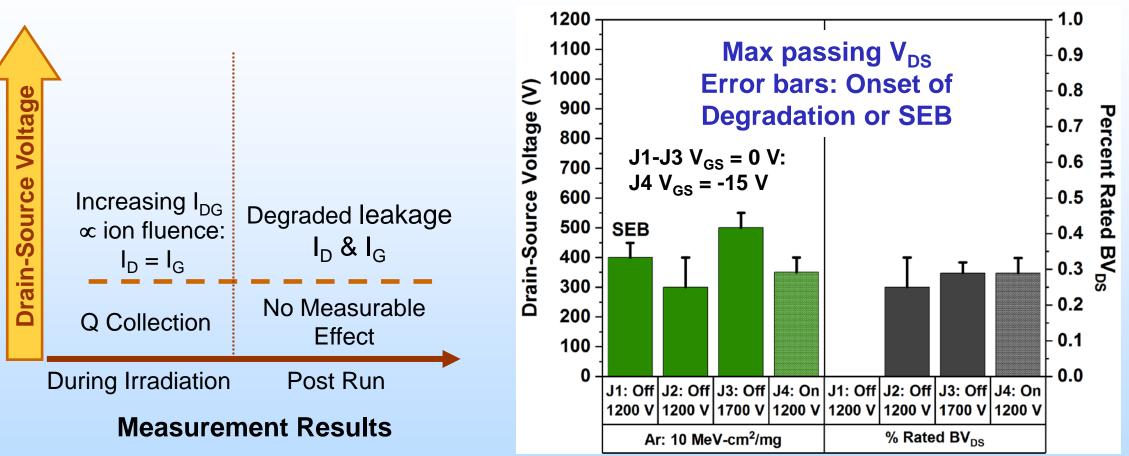




Columns: no effects Error bars: Onset of degradation or SEB

Onset V_{DS} for degradation is similar for normally-on and (non-cascaded) normally–off JFETs

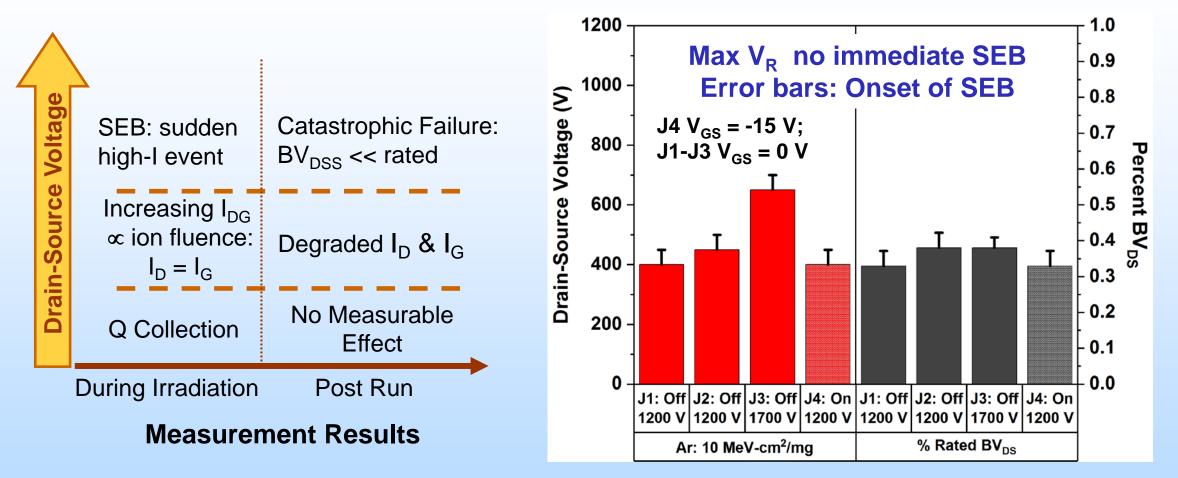
JFET Effects as a Function of V_{DS} at Fixed off V_{GS}: Degradation



1200 V & 1700 V JFETs have similar normalized onset V_{DS}: Greater field dependence of degradation mechanism vs. diodes (due to gate involvement or to lower LET?)

JFET Effects as a Function of V_{DS} at Fixed off V_{GS}: SEB



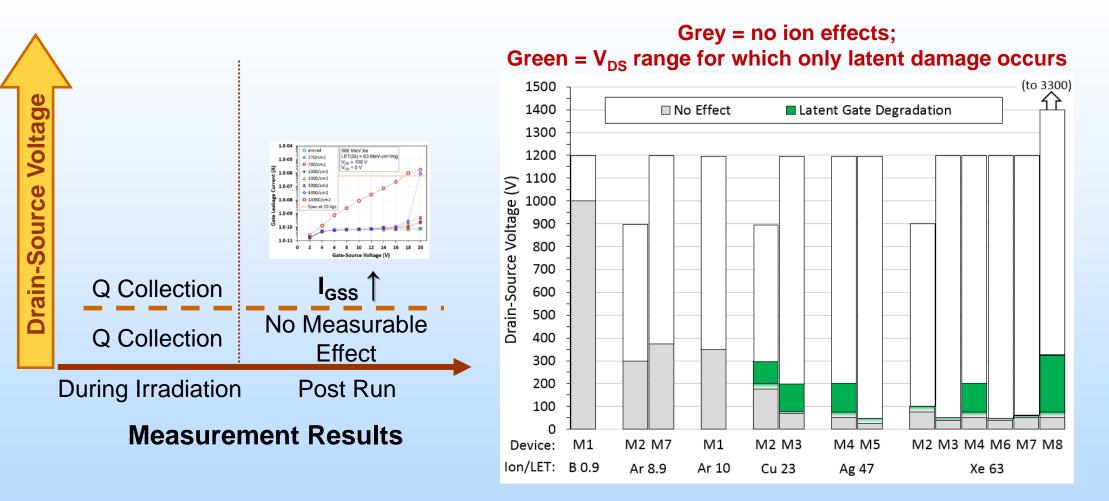


1200 V – 1700 V JFETs show SEB at similar fraction of rated V_{DS} Normally-on similar to normally-off JFET susceptibility



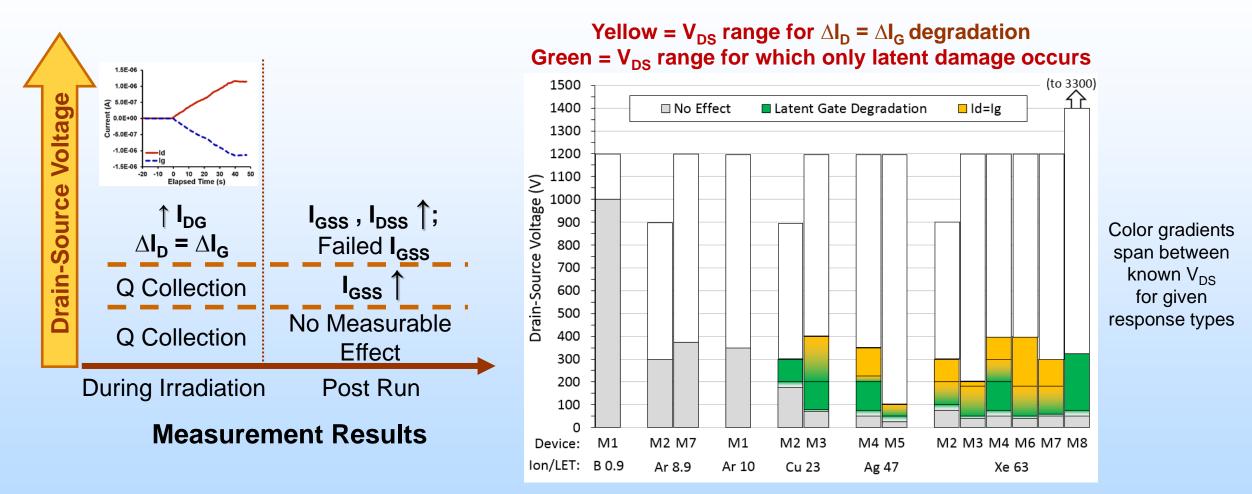
SINGLE EVENT EFFECTS: LEARNING FROM MOSFET DESIGNS

MOSFET Effects as a Function of V_{DS} at V_{GS} = 0 V: Latent Gate Damage



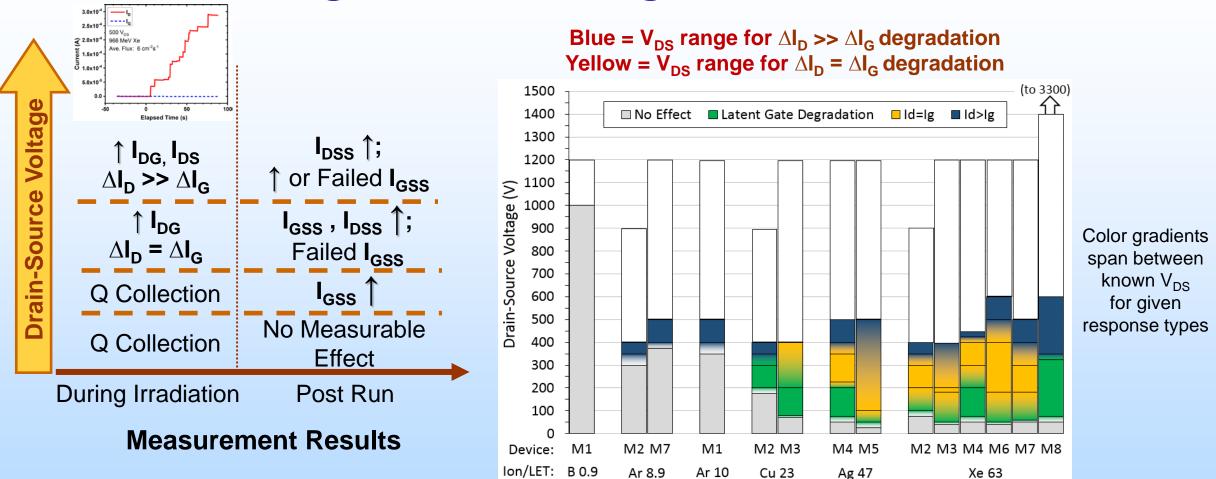
No latent damage to gate from low LET/light ions; Onset is independent of MOSFET voltage rating at higher LETs

MOSFET Effects as a Function of V_{DS} at $V_{GS} = 0$ V: Degradation During Beam Run



Not all MOSFETs exhibit drain-gate leakage current degradation: Design techniques may eliminate this vulnerability

MOSFET Effects as a Function of V_{DS} at V_{GS} = 0 V: Degradation During Beam Run

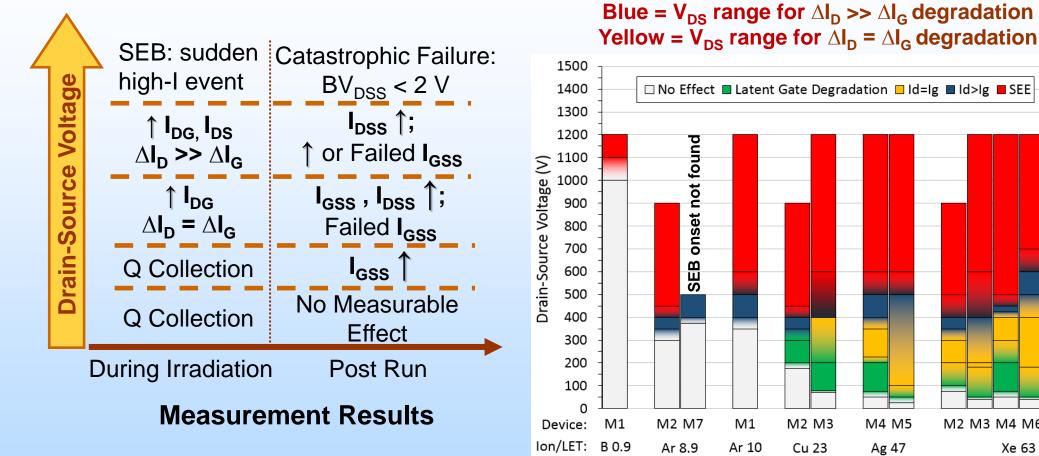


I_{DS} degradation least influenced by electric field and ion LET: linked to material properties??

MOSFET Effects as a Function of V_{DS} at $V_{GS} = 0$ V: **SEB**

Red = V_{DS} range for SEB





Color gradients span between known V_{DS} for given response types

(to 3300)

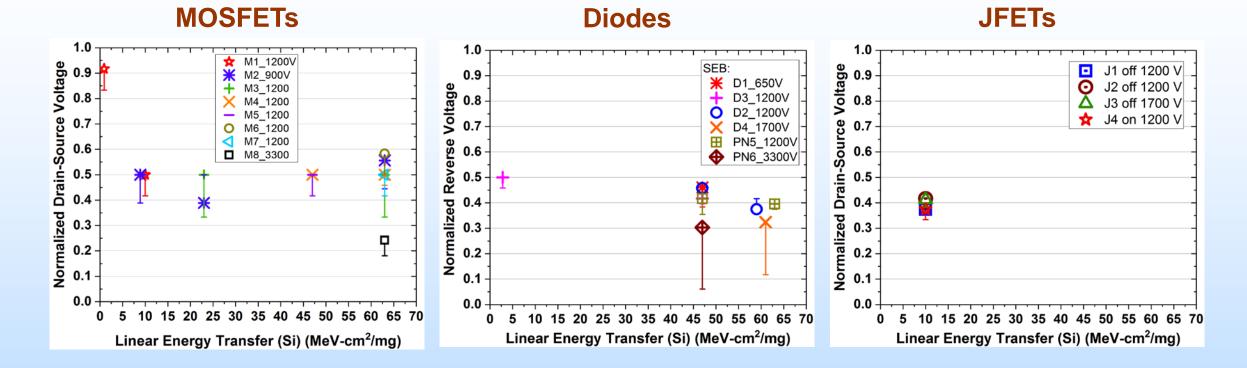
M2 M3 M4 M6 M7 M8

Xe 63

SEB vulnerability at LET(Si) < 1 MeV-cm²/mg Vulnerability saturates before the GCR flux "iron knee"

Normalized Onset Voltage for Immediate SEB: Comparison of Device Types





Onset for SEB similar across device types: ~40% to 50% of rated V; Use of real breakdown voltage would strengthen similarity across devices of different ratings

Summary of Design Insights

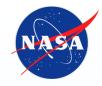


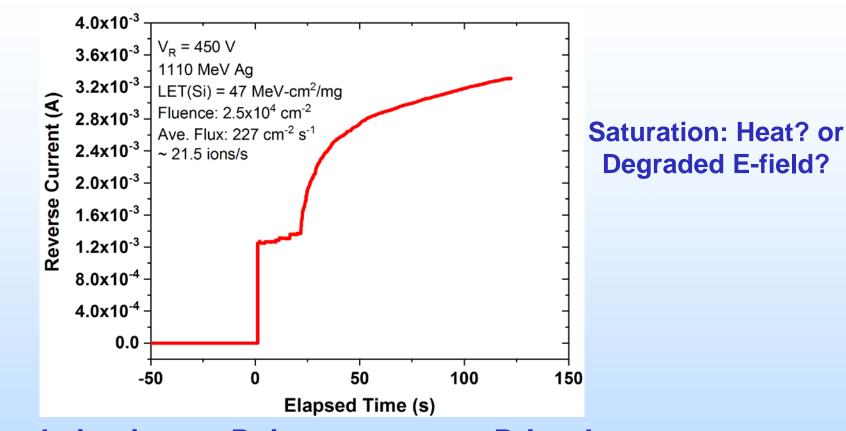
- SEB susceptibility similar across all device types suggesting common mechanism
 - E-field dependent
 - Saturated onset at ~40% 50% of rated voltage
- Schottky contact increases susceptibility of I_R degradation but not SEB
- I_R and I_{DS} degradation in diodes & MOSFETs may be most linked to material properties
 - Minimal E-field dependence
 - Susceptibility saturates at low LETs (< 10 MeV-cm²/mg)
- JFET I_{DG} degradation, however, shows field dependence
 - No difference between normally-on and normally-off designs
- MOSFET I_{DG} degradation is design-dependent expected to be easiest effect to eliminate
 - Does not occur at low LETs / lighter ions
- MOSFET latent gate damage susceptibility occurs in all designs at very low V_{DS}
 - Onset by ~100 V_{DS}
 - Does not occur at low LETs / lighter ions
 - Expected to be the most difficult heavy-ion effect to eliminate



PART 2: TESTING

Test Challenge: Identification of SEB SOA



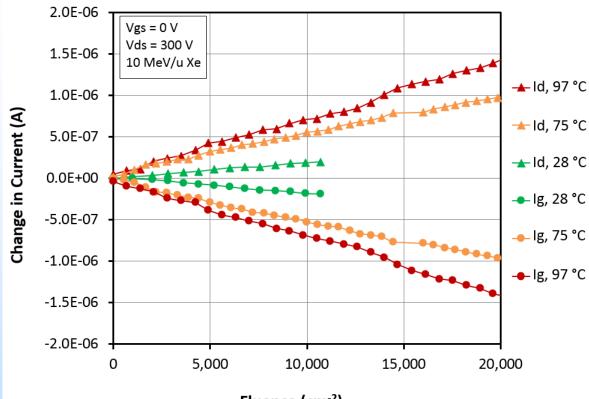


Degradation is non-Poisson process: Prior damage can impact effect of next ions. Threshold for SEB can be affected, preventing accurate identification of "SEB-safe" region of operation*.

*see Kuboyama, IEEE Trans. Nucl. Sci. 2006.

Testing: Temperature Effects





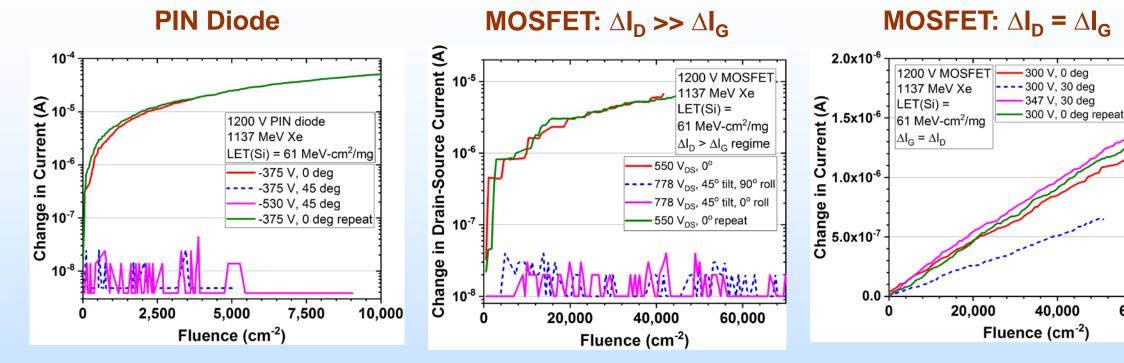
Fluence (cm⁻²)

Rate of leakage current degradation in 1200-V power MOSFET increases with increasing temperature. Because SiC dopants may not be fully ionized at room temperature, important to test at application temperature!

Testing: Angle Effects



60,000



- Diode & MOSFET (in △I_D >> △I_G regime): Strong angle effect
 - At given V_R / V_{DS} , no degradation at 45°
 - Matching vertical component of E-field has no impact: Cosine law not followed

- MOSFET (in △I_D = △I_G regime): Follows cosine law
 - Path length through gate likely dominates angle effect (Vertical field reduced with angle)

Summary of Testing Insights



- We may not be able to reliably define the SEB safe-operating area
 - Appropriate test fluence may not be achievable before damage influences SEB susceptibility
 - No longer a true "single-event effect" due to effect of prior ion strikes
- Temperature influences rate of current degradation
 - Application temperature testing may be required
- Strong angle responses will help reduce on-orbit susceptibility
 - May also make rate calculations difficult

• Lighter ions/lower LETs will reveal nuances between designs

Responses saturate quickly

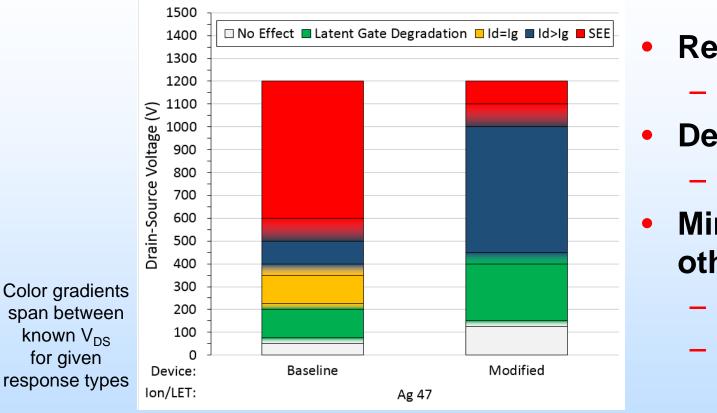




PART 3: OVERCOMING RADIATION THREATS

Radiation Hardness by Design: 1200 V MOSFET





Reduced SEB susceptibility

- Thicker epilayer
- Degradation of I_{DG} eliminated
 - Drain neck width reduction
- Minimal change in onset of other degradation effects:
 - $-\Delta I_D >> \Delta I_G$
 - latent gate damage

After Zhu, X., et al., 2017 ICSCRM

Continued research and development efforts are necessary to understand residual degradation mechanisms!

Summary & RHA Conclusions



- SEB safe operating area is difficult to reliably define
 - Susceptibility quickly saturates before the high-flux iron knee of the GCR spectrum
 - Mission orbit will have less influence on risk
- Application-specific temperature testing may be necessary
 - Dopants not fully ionized at room temperature
 - Effects of temperature on SEB susceptibility must be established
- Some degradation mechanisms may persist despite RHBD efforts
 - Impact on device long-term reliability must be established
- Radiation hardening comes with a cost
 - As with Si power MOSFETs, electrical performance will suffer from hardening techniques
- Lighter ion/lower LET tests will reveal nuances between designs and aid on-orbit degradation predictions
 - Responses are saturated at LETs dictated by typical mission destructive-SEE radiation requirements
 - LET should be specified in terms of LET(Si) but penetration range must be for SiC
- Characterization data should include identification of voltage conditions at which different effects occur
 - Richer dataset will include how susceptibility to these effects changes with ion species/LET