INTEGRATION OF MULTILEVEL SUPERCONDUCTING BURIED WIRING LAYERS WITH TRANSITION-EDGE SENSOR DETECTORS FOR LARGE SCALE ARRAYS

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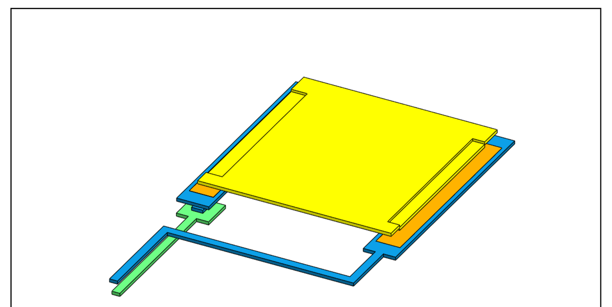
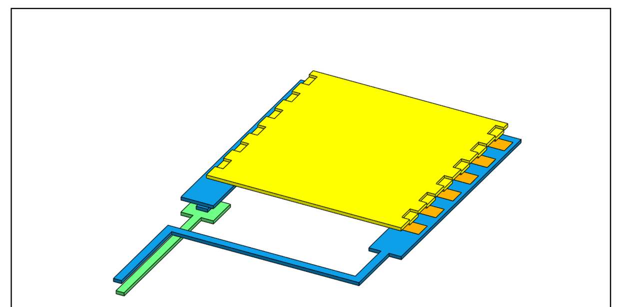
ABSTRACT

Lynx, one of the four mission concepts under consideration for the next Astrophysics Decadal Review, will include a microcalorimeter array consisting of more than 100,000 pixels in a compact arrangement with absorber pitch as small as 25 microns. In order to realize the desired array scale, fine-pitch multi-level superconducting wiring with high yield, compatible with rapid expansion of our hydra absorber designs, is essential. We have demonstrated a method of integrating transition edge sensor (TES) microcalorimeters with suitable multi-level buried wiring, fabricated at MIT Lincoln Laboratory using advanced tools dedicated to superconducting circuit fabrication. The TES Mo/Au bilayer is deposited on a high-quality oxide surface created by chemical-mechanical polishing, allowing tight specifications on the TES superconducting transition and link conductivity to be achieved even though the process order has been inverted. The TESs contact the top-level niobium wiring through vias etched through silicon dioxide down to the topmost wiring layer. We discuss the overall fabrication process, as well as the behavior of sensors with different via designs, proximity structures, and lateral sizes. An initial iteration of the integrated fabrication process indicates that microcalorimeters fabricated in this way should meet mission specifications using a Mo/Au bilayer with a reasonable critical temperature below 100 mK, which we also achieved.

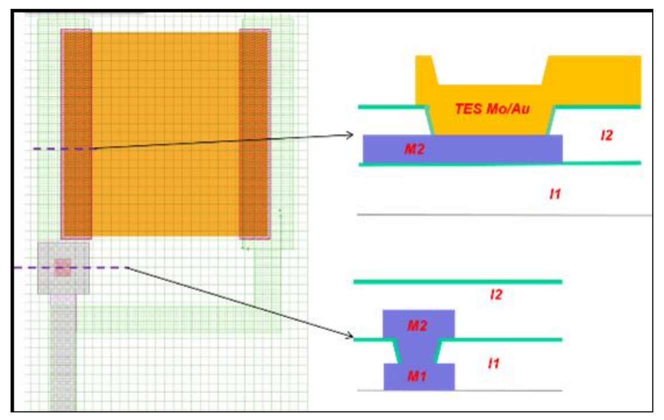
TES STRUCTURE AND VIA CONTACTS

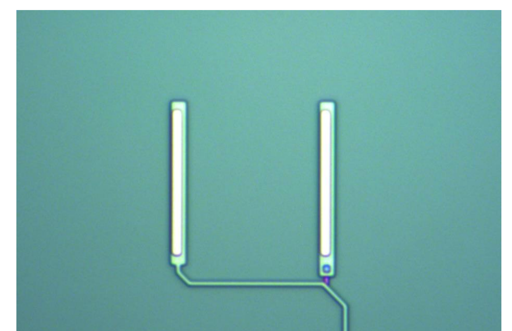


Via Design 1



Via Design 2





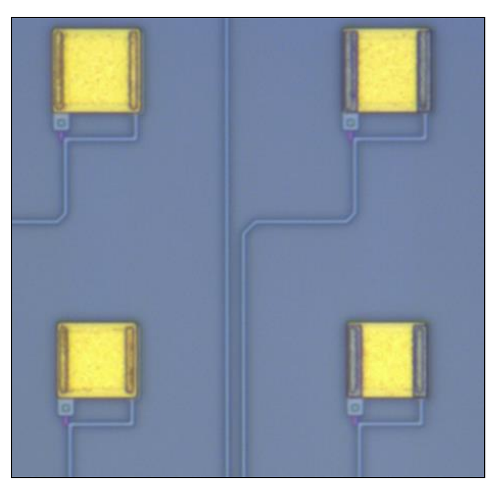
After liftoff of interface layer (Via Design 1)

- Fine-pitch buried wiring permits the hydra connections to overlay the TES wiring. The approach will allow fabrication of a dense array consisting of 100,000 absorbers that can be read out using only 4000 channels.
- The wiring layers were fabricated by collaborators at MIT Lincoln Laboratory using existing processes developed for multilevel JJ circuits.
- A technique for contacting the Mo/Au TES to the top M2 wiring layer through a planarized I2 insulating layer is required. We investigated two methods of creating these via contacts.

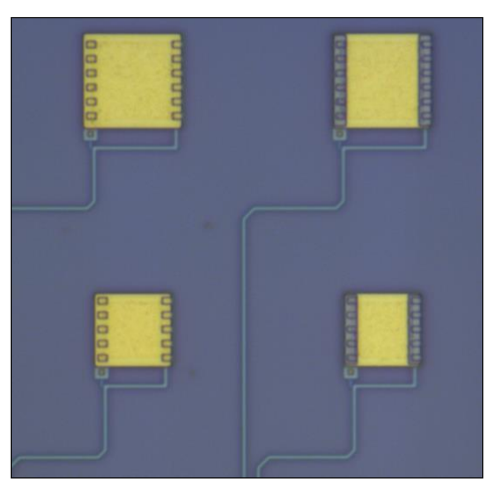
The process flow consisted of the following steps:

i. *Pattern and etch through I2 SiO_2 layer, stopping on M2. (Method 1 only)*
ii. *Pattern for interface layer liftoff.*
iii. *Ion mill followed by deposition of a thin Ti-Au interface layer.*
iv. *Liftoff of the interface layer.*
v. *Deposition of Mo/Au TES layer.*
vi. *Patterning and ion mill definition of TES.*

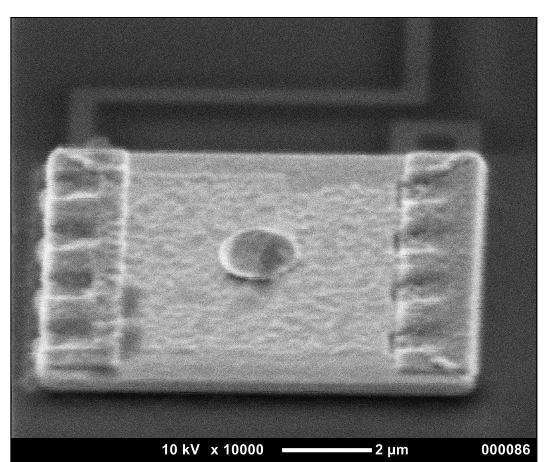
FIRST ITERATION



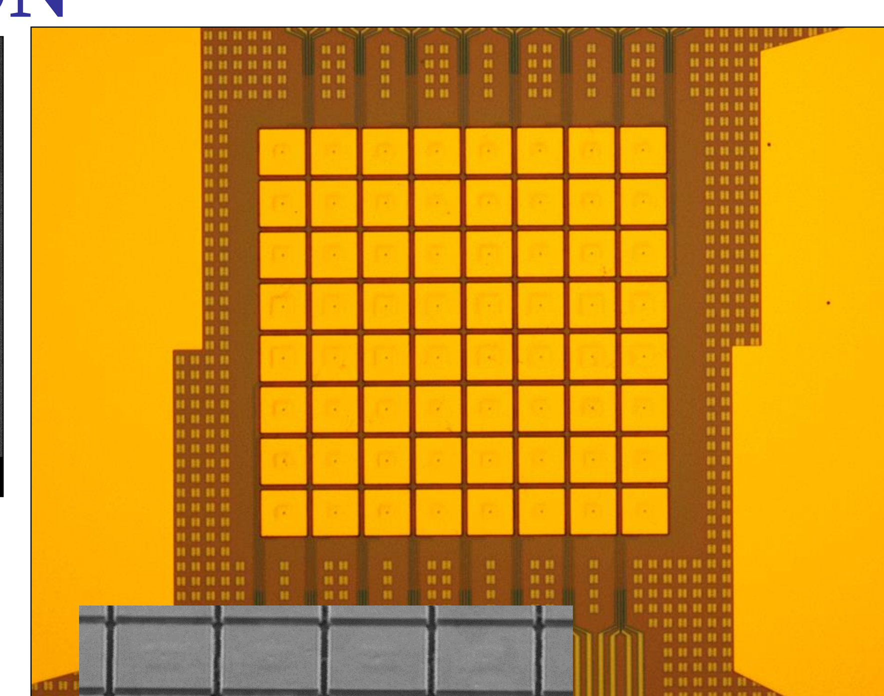
Via Design 1

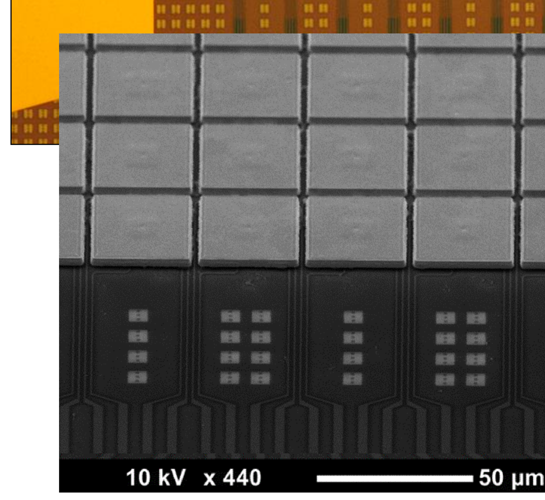


Via Design 2



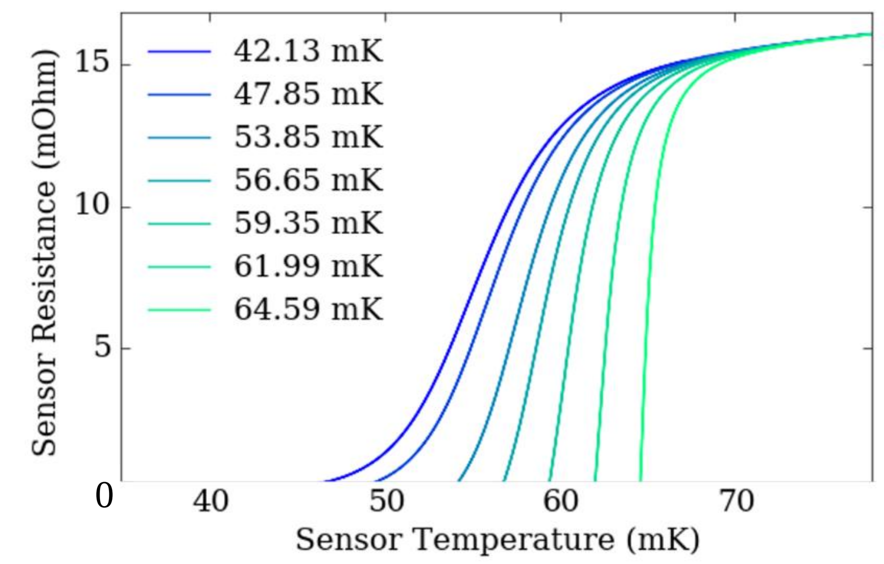
Via Design 2 with Nb patch and stem

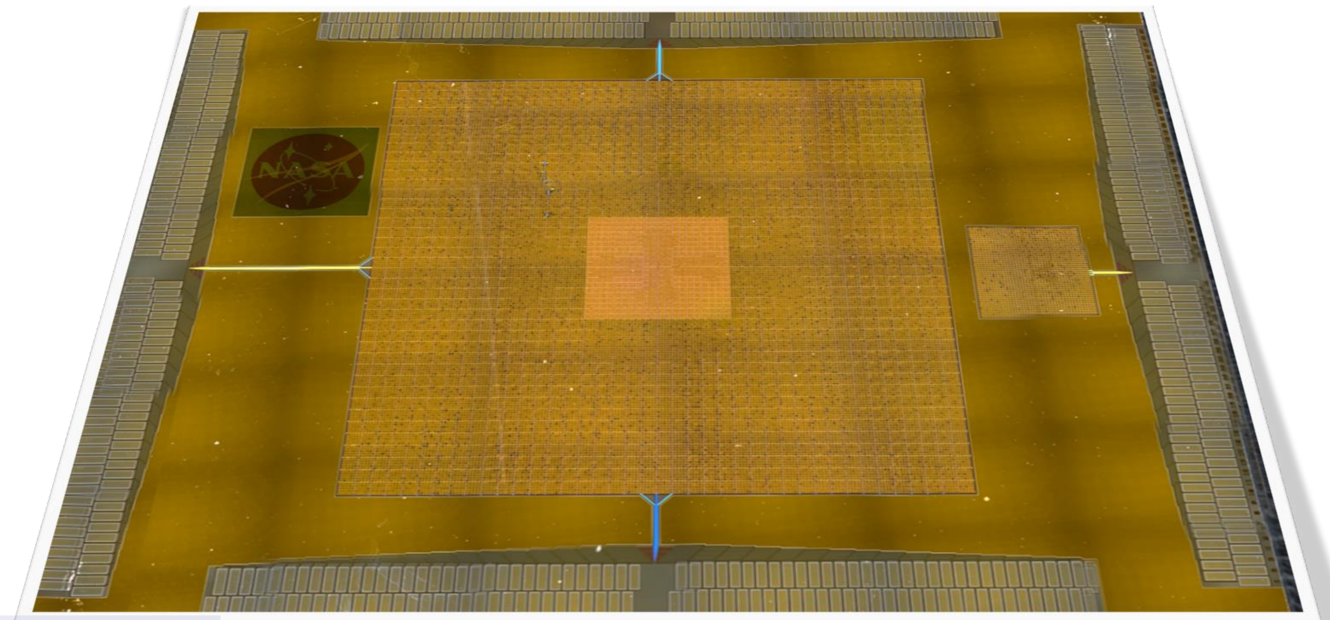




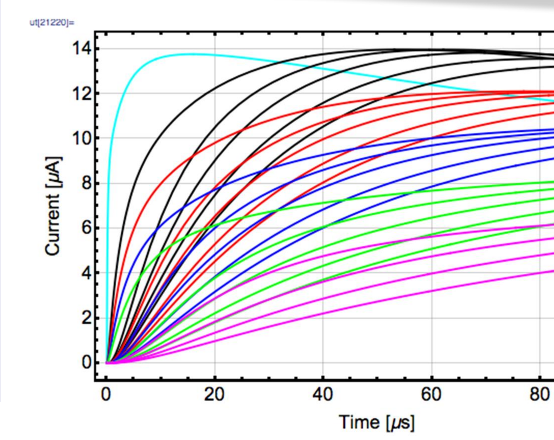
- The first iteration produced 64-element arrays including lateral TES dimensions of 7, 8, 9 and 12 microns.
- The design leverages the SOLAR-E work published in 2016. (A hard copy of that report is available.)
- Half of the devices included a niobium "patch" layer over the via region that mimics the SOLAR-E structure. The motivation is to maintain a high critical current through the TES-M2 via.
- The detectors incorporate electroplated gold absorbers 4 microns thick on round 1 µm stems. A SOLAR-E detector with this design demonstrated an energy resolution of 1.47 eV at 6 keV, to our knowledge the best ever reported.

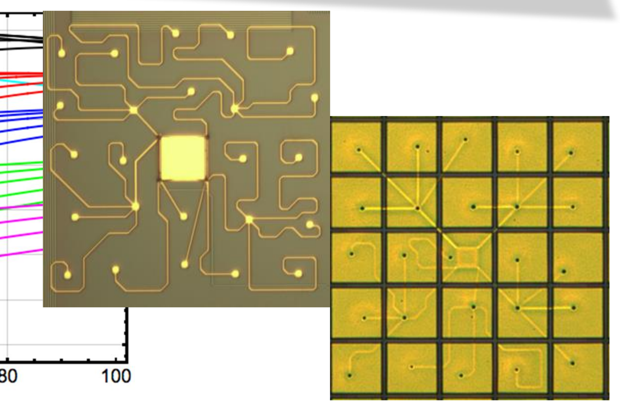
SECOND ITERATION: LYNX PROTOTYPE



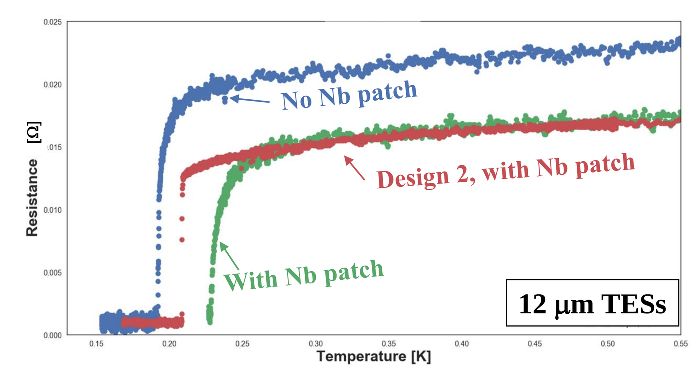


- Fabricated a single array of 47,500 elements featuring 25-element hydras.
  a. 10,000 pixel inner high-resolution array with 25 µm pitch. Outer portion on 50 µm pitch.
- Operating temperature in desirable range between 50 – 60 mK.
  a. Intrinsic T_C of Mo/Au bilayer was 85 mK.
  b. Low-excitation measurement of TES device showed T_C = 115 mK.
  c. TES dimension (20 µm) reduced the influence of leads upon the device operating temperature.
- Hydra links 1 µm wide gold thin film (300 nm thick) patterned by liftoff.

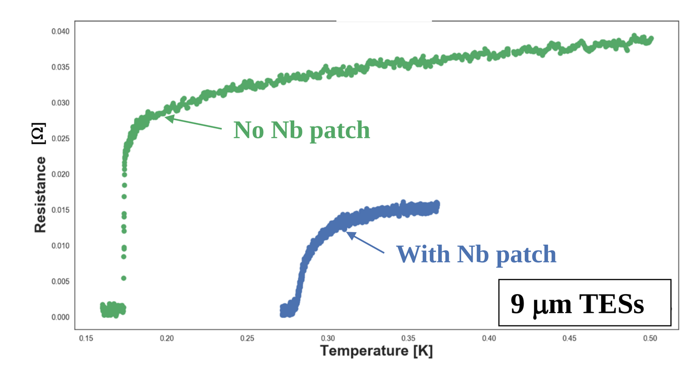




FIRST ITERATION CHARACTERIZATION



Via Design 1 & comparison



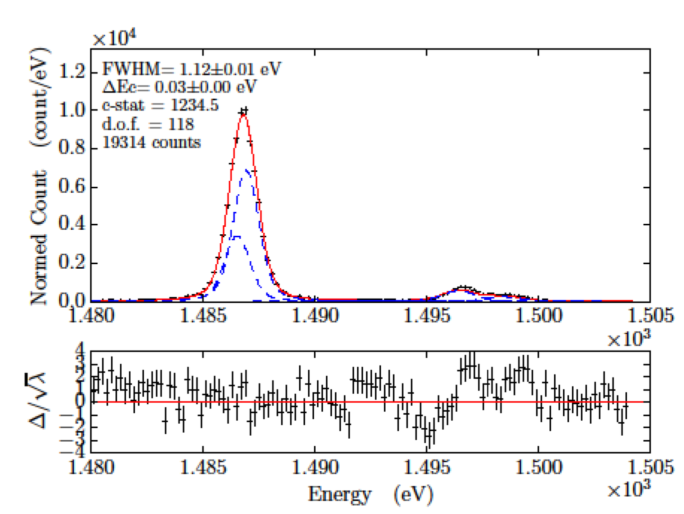
Via Design 2

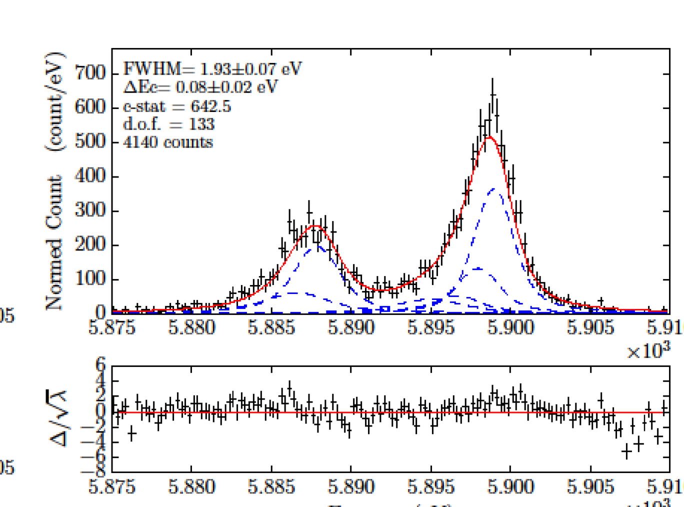
Size (µm)	R_n (mΩ)	T_C (mK)	Nb Patch
7		700	
7	14	730	Y
8		470	
8	20	500	N
9	20	500	N
9	20	520	N
12	14	500	Y
12	14	500	Y

Low-Excitation Measurement

- Intrinsic T_C of Mo/Au bilayer was about 200 mK. Increased Tc due to the Nb patch was observed, which is consistent with the SOLAR-E results.
- The experiment demonstrated that the series via resistance was about 20 mΩ for Design 1, and 7 mΩ for Design 2. The result is consistent with the different via areas, though not strictly proportional.
- The R(T) curves agreed for 12 µm devices with different via designs when both possessed the Nb patch, which short-circuited the via resistance.
- Zero-bias measurement using SQUID electronics shows elevated critical temperature for all sizes – moreso for 7 µm TES – with no discernible impact due to Nb patch.

FIRST ITERATION X-RAY TESTING RESULTS





- Using an 8 µm TES with via Design 1, we report an energy resolution of 1.12 eV for Al Kα and 1.93 eV for Mn Kα, as shown.
- The initial results indicate that a detector with a critical temperature of 65 mK utilizing a 1 micron thick absorber would demonstrate a desirable energy resolution of 0.2 eV at 1 keV.
- X-ray testing of Lynx prototype devices (from the second iteration) is underway.