National Aeronautics and Space Administration

High-Performance Spaceflight Computing (HPSC) Project Overview

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Acronym List

AMBA	ARM Advanced Microcontroller Bus Architecture	DRAM	Dynamic Random Access memory	GPU	Graphics Processing Unit
ASIC	Application Specific Integrated Circuit	DTRA	Defense Threat Reduction Agency	GSFC	Goddard Space Flight Center
BSP	Board Support Package	ECC	Error Correction Coding	HEOMD	Human Exploration and Operations Directorate
BW	Bandwidth	EEPROM	Electrically Erasable Programmable Read-Only Memory	HPPS	High Performance Procerssing Subsystem
CCN	Cache Coherent Network	FCR	Fault Containment Region	HPSC	High Performance Spaceflight Computing
CFS	Core Flight Software	FPGA	Field Programmable Gate Array	I2C	Inter-Integrated Circuit
CPU	Central Processing Unit	FPU	Floating Point Unit	IDE	Integrated Development Environment
C&DH	Command and Data Handling	FSW	Flight Software	ISA	Instruction Set Architecture
CDR	Critical Design Review	Gbd	Gigabaud	ISI	Information Sciences Institute
DARPA	Defense Advanced Research Projects Agency	Gb/s	Gigabits Per Second	JPL	Jet Propulsion Laboratory
DDR	Double Data Rate	GB/s	Gigabytes Per Second	JTAG	Joint Test Action Group
DECTED	Double Error Correct Triple Error Detect	GHz	Gigahertz	KHz	Kilohertz
DMEA	Defense Microelectronics Activity	GNC	Guidance Navigation and Control	Kpps	Kilo Packets Per Second
DMIPS	Dhrystone Million Instructions per Second	GOPS	Giga Operations Per Second	LET	Linear Energy Transfer

Acronym List

Mbps	Megabits Per Second	PERFECT	Power Efficiency Revolution For Embedded Computing Technologies	SpW	SpaceWire
MCM	Multi Chip Module	QoS	Quality of Service	SRAM	Static Random Access memory
MeV	Million Electron Volt	RHBD	Radiation Hardened By Design	SRIO	Serial RapidIO
MHz	Megahertz	RTOS	Real Time Operating System	SSED	Solid-State Electronics Development
MRAM	Magnetoresistive Random Access Memory	RTPS	Real Time Processing Subsystem	SSR	Solid State Recorder
MT/s	Million Transfers per Second	S/C	Spacecraft	STMD	Space Technology Mission Directorate
mW	Milli Watt	SCP	Self Checking Pair	TID	Total Ionizing Dose
NASA	National Aeronautics and Space Administration	SCS	Secure Computing Solutions	TTE	Time Triggered Ethernet
NGSP	Next Generation Space Processor	SEE	Single Event Effects	TTGbE	Time Triggered Gigabit Ethernet
nm	Nanometer	SerDes	Serializer Deserializer	TMR	Triple Modular Redundancy
NVRAM	Nonvolatile Random Access memory	SIMD	Serial Instruction Multiple Data	TRCH	Timing Reset Configuration and Health
PCB	Printed Circuit Board	SMD	Science Mission Directorate	XAUI	10 Gigabit Media Independent Interface)
PCIe	Peripheral Component Interconnect Express	SOI	Silicon On Insulator	UART	Universal Asynchronous Receiver/Transmitter
PDR	Preliminary Design Review	SPI	Serial Peripheral Interface	VMC	Vehicle Management Computer

Outline

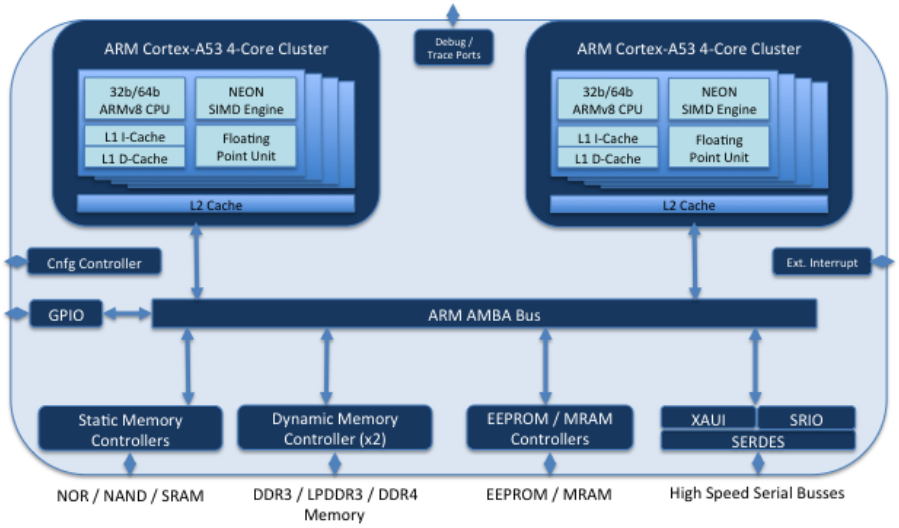
- HPSC Overview
- HPSC Contract
- Key Requirements
- Chiplet Architecture
- HPSC System Software and Middleware
- NASA HPSC Use Cases
- HPSC Ecosystem

High Performance Spaceflight Computing (HPSC) Overview

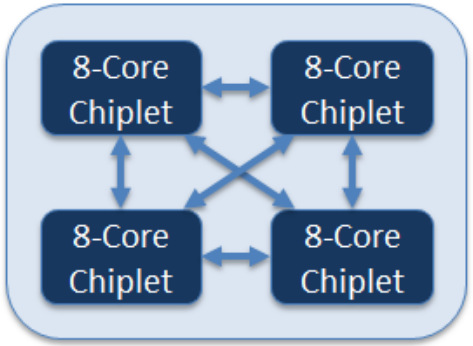
- The goal of the HPSC program is to dramatically advance the state of the art for spaceflight computing
- HPSC will provide a nearly two orders-of-magnitude improvement above the current state of the art for spaceflight processors, while also providing an unprecedented flexibility to tailor performance, power consumption, and fault tolerance to meet widely varying mission needs
- These advancements will provide game changing improvements in computing performance, power efficiency, and flexibility, which will significantly improve the onboard processing capabilities of future NASA and Air Force space missions
- HPSC is funded by NASA's Space Technology Mission Directorate (STMD), Science Mission Directorate (SMD), and the United States Air Force
- The HPSC project is managed by Jet Propulsion Laboratory, and the HPSC contract is managed by NASA Goddard Space Flight Center (GSFC)

HPSC Reference Architecture

- Initially provided in the Request for Proposal, a reference design features power-efficient **ARM 64-bit processor cores (8)** and on-chip interconnects scalable **and** extensible in MCM (Multi-Chip Module) or on PCB (Printed Circuit Board) via XAUI and SRIO (Serial RapidIO) 3.1 high-speed links
  - Multi-Chiplet configurations (tiled or cascaded) provide increased processing throughput and/or increased fault tolerance (e.g. each Chiplet as separate fault containment regions, NMR)
  - Chiplets may be connected to other XAUI/SRIO devices
    - e.g. FPGAs, GPUs, or ASIC co-processors
- Supports multiple hardware-based and software-based fault tolerance techniques



HPSC "Chiplet" Reference Design



Multi-Chiplet Configuration

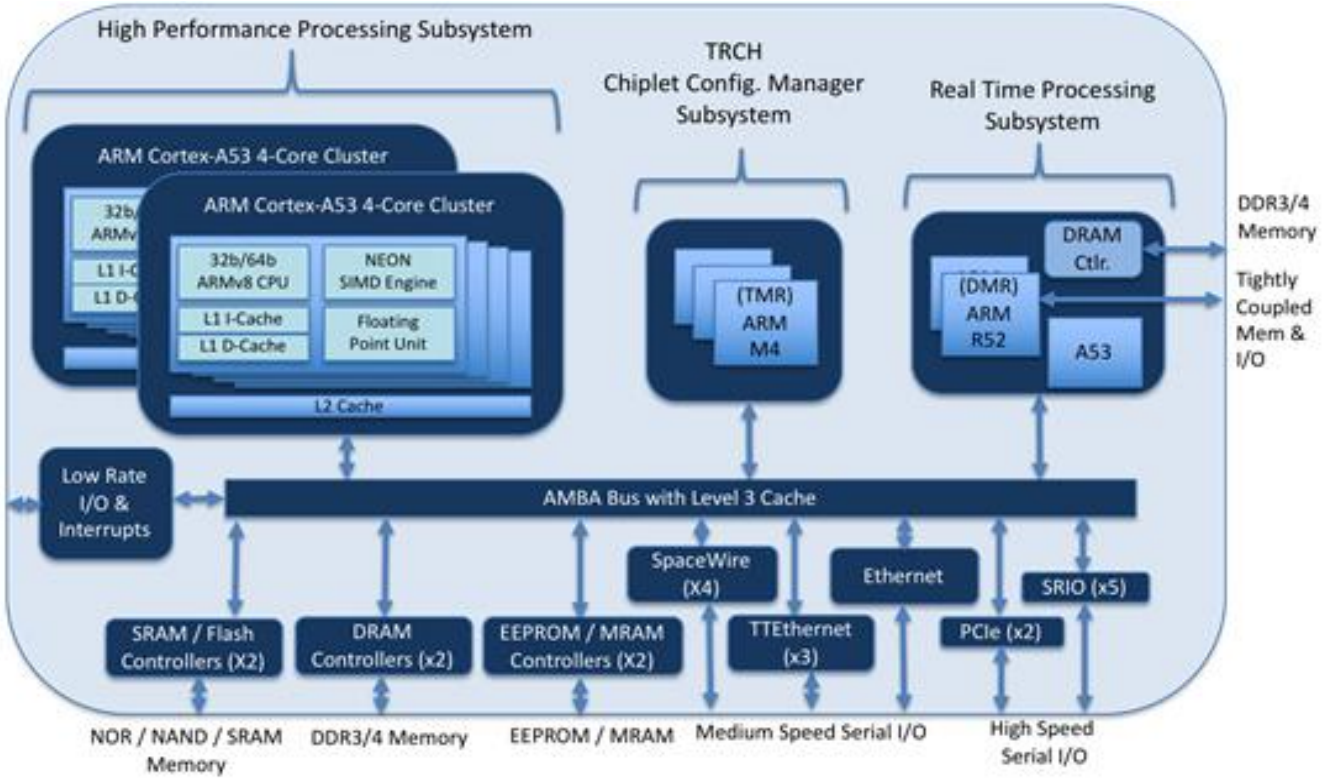
To be presented at Radiation Hardened Electronics Technology (RHET) Conference, Phoenix, AZ, November 5-8, 2018.

HPSC Contract

- Following a competitive procurement, the HPSC cost-plus fixed-fee contract was awarded to Boeing
- Under the base contract, Boeing will provide:
  - Prototype radiation hardened multi-core computing processors (Chiplets), both as bare die and as packaged parts
  - Prototype system software which will operate on the Chiplets
  - Evaluation boards to allow Chiplet test and characterization
  - Chiplet emulators to enable early software development
- Five contract options have been executed to enhance the capability of the Chiplet
  - On-chip Level 3 cache memory
  - Dual real-time processors
  - Dual Time Triggered Ethernet (TTE) interfaces
  - Dual SpaceWire interfaces
  - Package amenable to spaceflight qualification
- Contract deliverables are due April 2021

Chiplet Architecture

- With the contract options awarded and the preliminary design completed, the Chiplet architecture has evolved from the original reference architecture



HPSC Chiplet Architecture

HPSC Chiplet Program Overview
Program Structure & Schedule

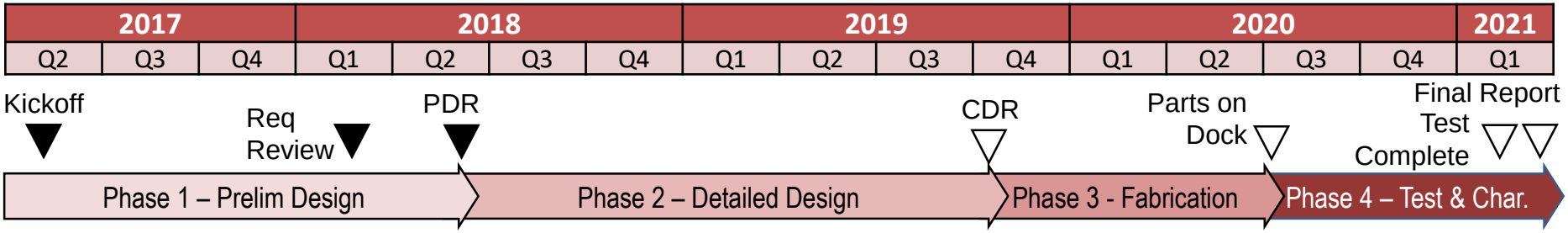
- **Tasks (WBS Level 1)**

1.0 Management
2.0 System Engineering
3.0 Chiplet Development
4.0 System Software Development
5.0 Evaluation Board Development
6.0 Test and Characterization

- **Phases**

Phase	Duration	Period of Performance
1. Preliminary Design	14 months	March 2017 through May 2018
2. Detailed Design	17 months	June 2018 through October 2019
3. Fabrication	9 months	November 2019 through July 2020
4. Test & Characterization	9 months	August 2020 through April 2021

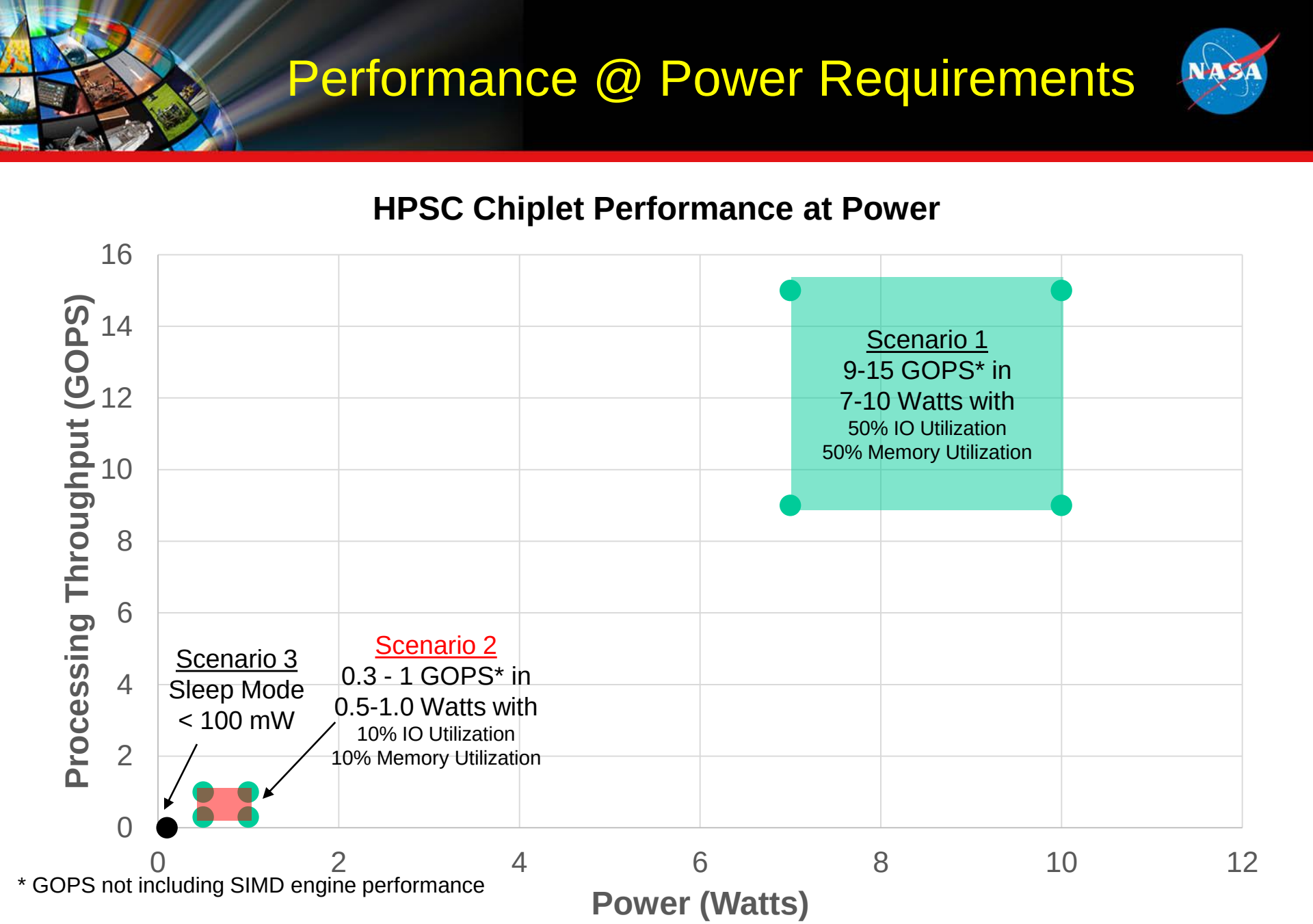
- **Schedule**



Key Requirements Summary

Processor Cores	• High Performance Processing Subsystem (HPPS): 8 ARM Cortex-A53 cores with floating point & Single Instruction Multiple Data (SIMD) engine. Performance & power on next slide • Real Time Processing Subsystem (RTPS) with single A53 and dual Cortex-R52 cores
Memory Interfaces	• 3 DDR3/4: 2 for A53 clusters, 1 for RTPS • 4 SRAM/NVRAM • Enhanced error correction (ECC) to operate through bit upsets and whole memory device failures
IO Interfaces	• 6 SRIO 3.1, 2 PCIe Gen2 serial IO • Ethernet, SpaceWire, Time Triggered Ethernet (TTE), SPI, UART, I^2C, GPIO
Power scaling	Able to dynamically power down/up cores, subsystems, & interfaces via software control
Fault tolerance	Able to autonomously detect errors & log errors, prevent propagation past established boundaries, and notify software
Trust & Assured Integrity	• DMEA-accredited Trusted supply chain • Free of malicious insertions / alterations
Temperature	-55C to 125C

Performance @ Power Requirements



* GOPS not including SIMD engine performance

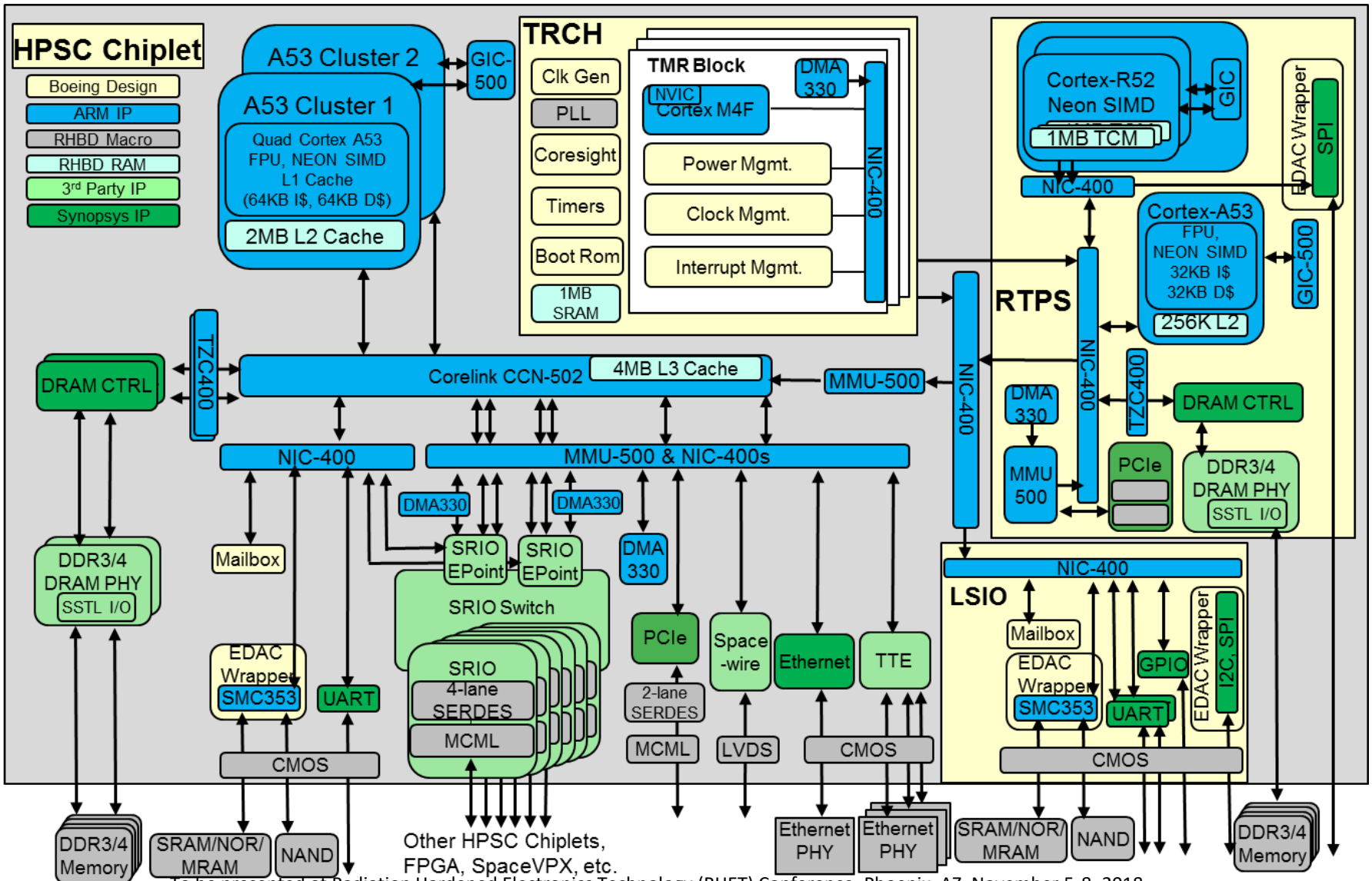
Key Requirements Summary

Total Ionizing Dose (TID)	Strategic radiation hardness for Air Force applications
Prompt Dose Immunity	
Dose Rate Survivability	
Latchup Immunity	LET ≥ 90 MeV-cm^2/mg
Single-Event Upset (SEU) (Adams 90% WC GEO)	• HPPS (A53 Array): ≤ 1E-3 errors/device-day • RTPS: ≤ 1E-4 errors/device-day • TRCH: ≤ 1E-5 errors/device-day
Single-Event Upset (SEU) (WC Solar Flare)	• HPPS (A53 Array): ≤ 1E-1 errors/device-min • RTPS: ≤ 1E-2 errors/device-min • TRCH: ≤ 1E-3 errors/device-min
Reliability	≥ 100,000 power-on hours
Software	• Multicore operating systems (Linux & RTOS) • Development tools (compilers, debuggers, etc) • Board Support Packages (BSPs) • APIs for fault tolerance, power management
Emulators	• Software-based quick emulator • FPGA-based cycle-accurate emulator

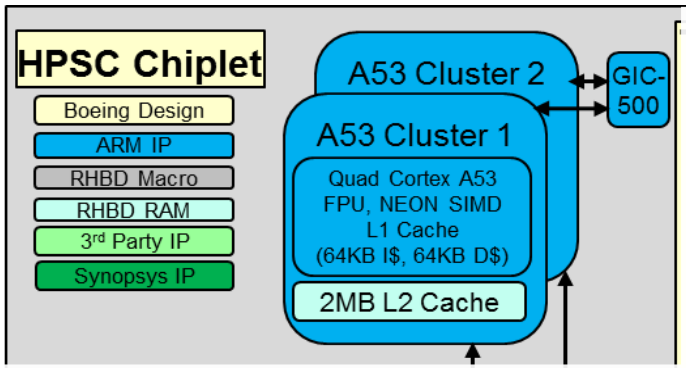
HPSC Chiplet Program Overview Approach

- **Develop Chiplet using Boeing's RHBD 32nm SOI design & fabrication flow, which provides:**
  - High-performance library and mixed-signal macros
  - Strategic radiation hardness
  - Single-Event-Effects (SEE) mitigations optimized for power efficiency
  - Assured integrity
- **Employ core competencies of team comprised:**
  - Boeing Solid-State Electronics Development (SSED)
  - Boeing Secure Computing Solutions (SCS)
  - Boeing Space & Launch
  - USC Information Sciences Institute (ISI)
  - University of Michigan ARM Research Center
- **Utilize silicon-proven IP:**
  - ARM, Globalfoundries, Synopsys, Praesum, and Uniquify
- **Leverage tens of millions of dollars of Government and Boeing investments in related technology areas:**
  - DTRA RHBD3, AFRL/NASA Next NGSP, MAESTRO, DARPA PERFECT, etc.

HPSC Chiplet Architecture



Chiplet Architecture: High-performance Cores



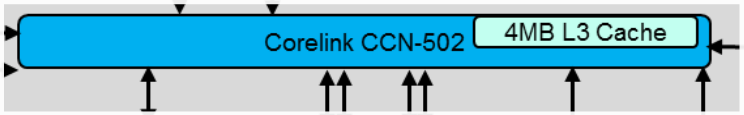
Two (2) ARM Cortex-A53 MPCore Clusters

- **High-Performance Processing Subsystem (HPPS)**
- **Four (4) cores per cluster**
- **ARMv8 64-bit ISA**
- **Up to 800 MHz frequency**
  - **Peak 1840 Dhrystone MIPS (DMIPS) per core @ 800MHZ**
  - **Peak 7360 DMIPS/Quad Cluster, Total of 14,720 DMIPS**
- **64 KByte L1 instruction and data cache per core**
- **2 MByte L2 Cache per quad cluster**
- **Floating Point Unit (FPU) per core**
- **NEON SIMD engine per core**
  - **8-bit mode: Peak 12.5 GOPS/NEON, Total 100 GOPS**
  - **16-bit mode: Peak 6.25 GOPS/NEON, Total 50 GOPS**
  - **32-bit mode: Peak 3.125 GOPS/NEON, Total 25 GOPS**

Chiplet Architecture: Interconnect

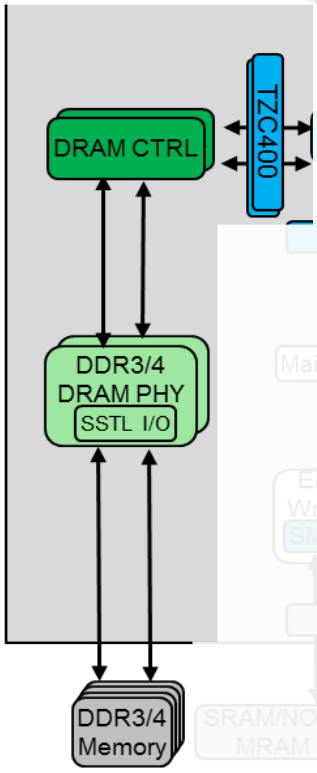
ARM CoreLink CCN-502

- Cache-coherent ring based interconnect
- AMBA5 Coherent Hub Interface protocol
  - Optimized for ARM v8 64-bit ISA
- 4 MB L3 Cache



- Advanced Power Management Features
- 60 GB/s internal interconnect bandwidth @ 1GHz
- Supports ECC, Quality of Service (QoS), QoS Virtual Networks, and ARM TrustZone security

Chiplet Architecture: DRAM Interfaces



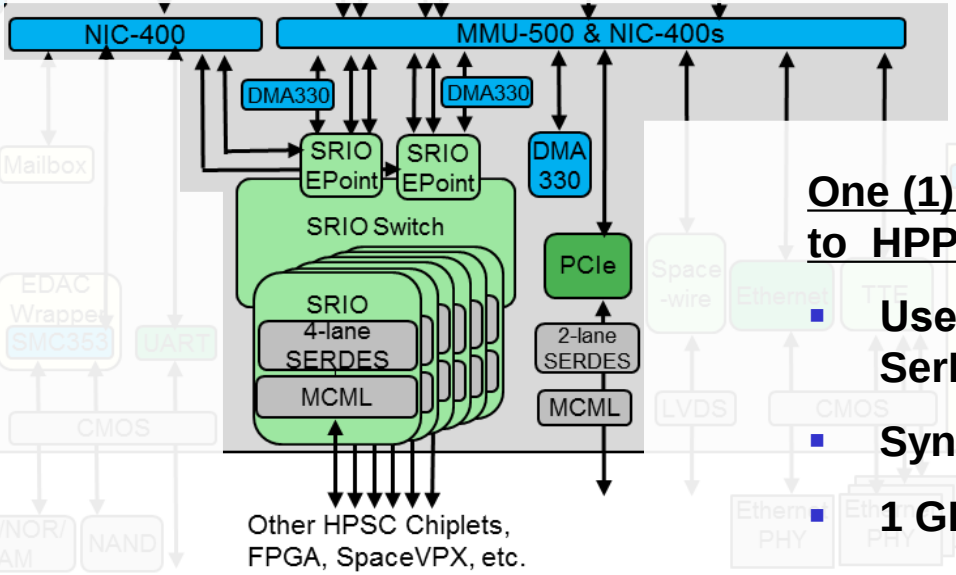
Two (2) DDR3/4 SDRAM Interfaces for HPPS

- **Speeds up to 1600 Megatransfers/second (MT/s)**
- **Synopsys DDR3/4 Controller**
- **Uniquify PHY (uses Boeing RHBD cells)**
- **ARM TCZ-400**
  - **Extends TrustZone security and QoS to external interface**
- **Robust ECC allows operation through loss of a whole memory device**
- **Provides up to 25.6 GB/s of bandwidth**

Chiplet Architecture: Serial I/O Interfaces

Six (6) Serial RapidIO® (SRIO) 3.1 ports

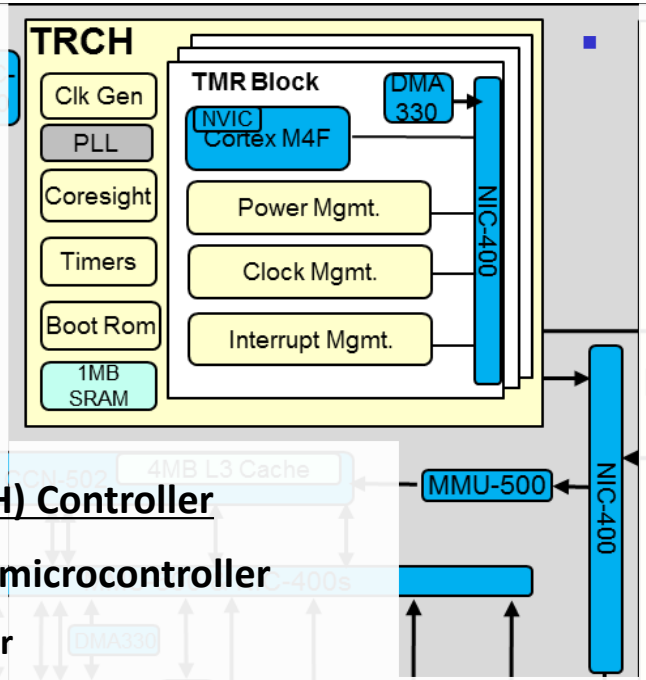
- **Four (4) lanes per port, each lane up to 10.3125 GBd full-duplex**
- **Uses Boeing's 32nm RHBD SerDes macro**
- **Supports high-speed serial connections to:**
  - **Other Chiplet devices**
  - **Expansion FPGA**
  - **Protocol conversion**
- **Provides up to 59.1 GB/s of Serial I/O bandwidth**



One (1) PCIe Gen2 port dedicated to HPPS

- **Uses Boeing's 32nm RHBD SerDes macro (2 lanes)**
- **Synopsys PCIe Controller**
- **1 GB/s Bandwidth**

Chiplet Architecture: TRCH Controller



Timing, Reset, Config, & Health (TRCH) Controller

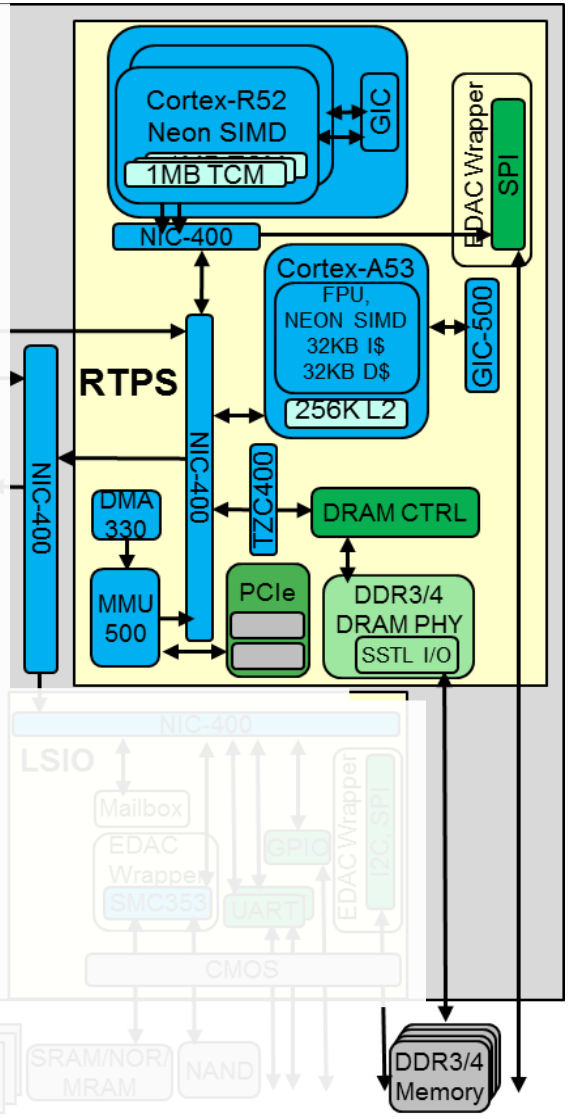
- **Built around a small Cortex-M4F microcontroller**
  - **Low power and small form factor**
  - **More flexibility than a finite state machine approach**
  - **TMRed for maximal fault tolerance**
  - **1 MB Tightly-Coupled Memory (TCM) SRAM with Double-Error Correct, Triple-Error Detect (DECTED) ECC**

- **Provides the following Chiplet functionality:**
  - **Boot Sequencing**
  - **Power-On-Reset**
  - **Clock Generation**
  - **Power Management**
  - **Configuration Control**
  - **Sleep Mode (< 50mW)**
  - **Health Monitoring / Fault Management**
  - **Built-in-Self-Test, eFuse**
  - **Timers and Synchronization Control**
  - **Interrupt handling and distribution**

Chiplet Architecture: Realtime Processing Subsystem

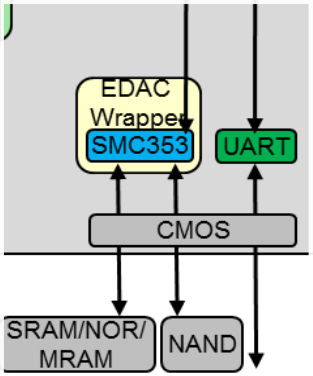
Realtime Processing Subsystem (RTPS)

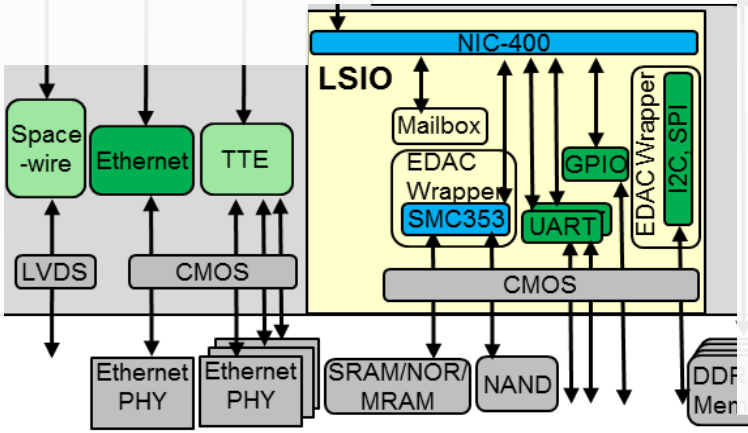
- **Single Cortex-A53 core managing two (2) Cortex-R52 Realtime cores (ARM v8 64b)**
  - **Supports virtualization and time & space partitioning / ARINC 653, as well as realtime performance needs**
- **RTPS Dedicated Memory & IO interfaces:**
  - **One (1) DDR3/4 interface**
  - **One (1) PCIe Gen2 interface**
  - **One (1) SPI interface**
- **R52 cores provide:**
  - **ARM's highest level of safety features, including Dual-Core Lock Step (DCLS) operation**
  - **Up to 600 MHz frequency**
  - **Peak 1296 Dhrystone MIPS (DMIPS) per core @ 600MHZ**
  - **Floating Point Unit (FPU), NEON SIMD engine, and 1 MB Tightly Coupled Memory per core**
- **A53 core provides:**
  - **Peak 1380 Dhrystone MIPS (DMIPS) @ 800MHZ**
  - **32 KB L1, 256 KB L2 Caches**



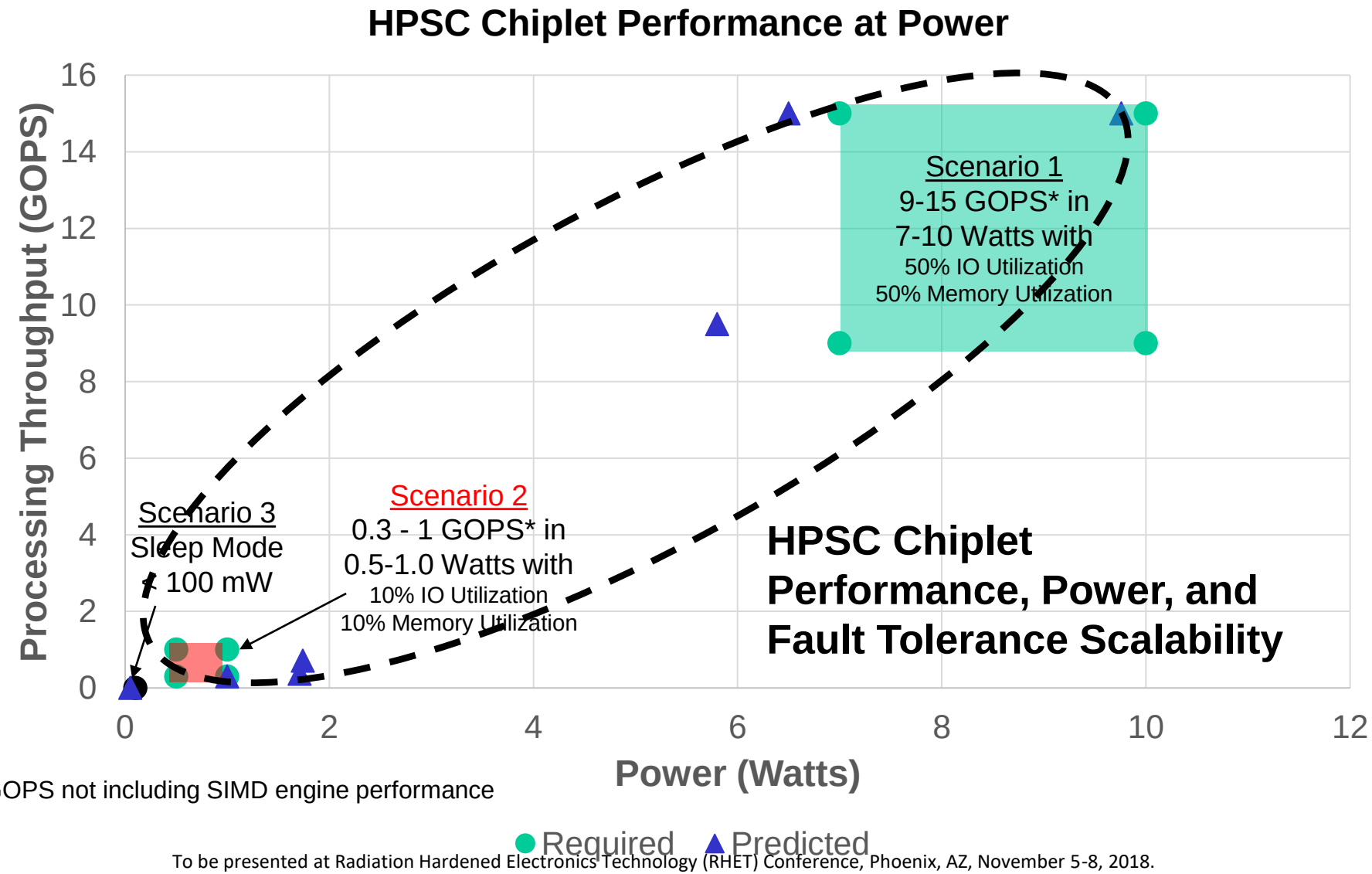
Chiplet Architecture: Other IO Interfaces

- **Two (2) 10/100/1000 Ethernet Interfaces**
- **3-Port Time-Triggered Ethernet (TTE) interface**
  - Can operate as a single TMRed port for fault tolerance
- **2-Port Spacewire Interface**
- **UART, SPI, and I²C interfaces**
- **SRAM and NVRAM (NAND/NOR Flash, MRAM) interfaces**
- **ARM CoreSight trace and debug, JTAG debug interfaces**
- **GPIO (single-ended and LVDS)**





Performance @ Power Predictions



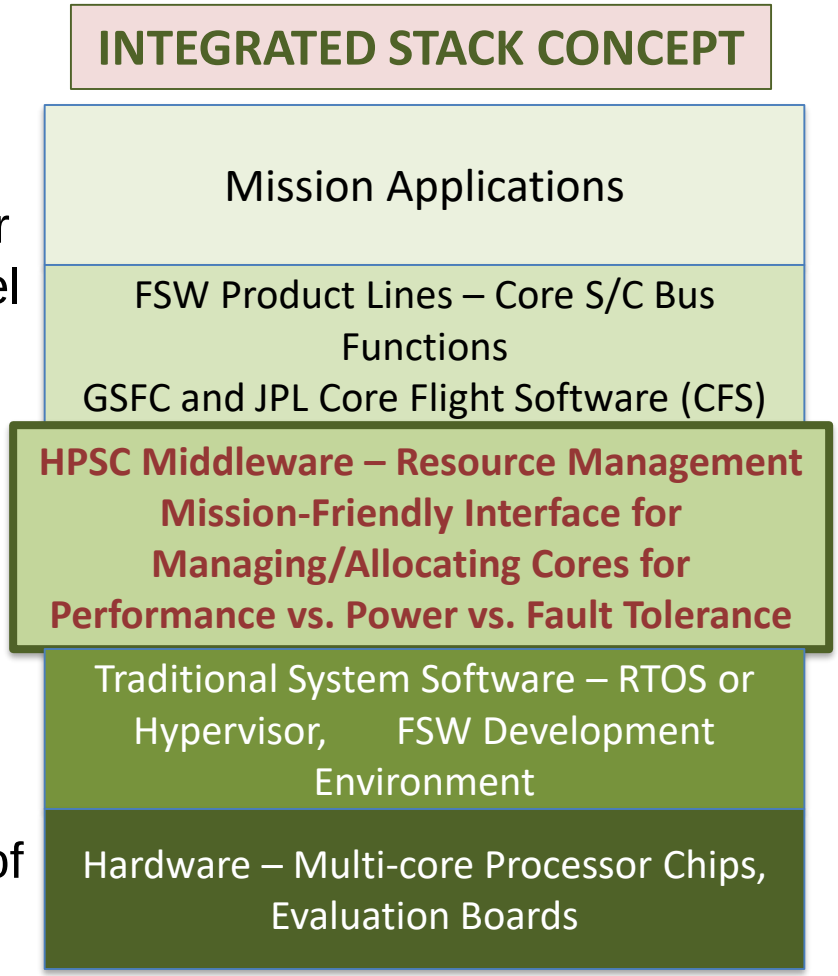
* GOPS not including SIMD engine performance

HPSC System Software

- **The HPSC Chiplet inherits a large complement of existing open source software including:**
  - Libraries, operating systems, compilers, and debuggers.
- **We're able to leverage much of this software unmodified.**
- **The HPSC System Software effort largely encompasses 4 thrusts:**
  1. Board support packages for Linux and RTOS;
  2. Development tools (e.g., compilers, debuggers, IDEs);
  3. Software-based fault tolerance; and
  4. Chiplet emulators.
- **Our goal is to build a sustainable software ecosystem to enable full lifecycle software development.**

HPSC Middleware

- AFRL is funding JPL and NASA GSFC to develop HPSC Middleware
- Middleware will provide a software layer that provides services to the higher-level application software to achieve:
  - Configuration management
  - Resource allocation
  - Power/performance management
  - Fault tolerance capabilities of the HPSC chiplet
- Serving as a bridge between the upper application layer and lower operating system or hypervisor, the middleware will significantly reduce the complexity of developing applications for the HPSC chiplet



HPSC Use Cases – Rovers and Landers

Rover

Compute Needs
- Vision Processing
- Motion/Motor Control
- GNC/C&DH
- Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault detection/recovery

- **System Metrics**
- 2-4 GOPs for mobility(10x RAD750)
- >1Gb/s science instruments
- 5-10GOPs science data processing
- >10KHz control loops
- 5-10GOPS, 1GB/s memory BW for model based reasoning for planning

Lander

Compute Needs
- Hard Real time compute
- High rate sensors w/zero data loss
- High level of fault protection/ fail over

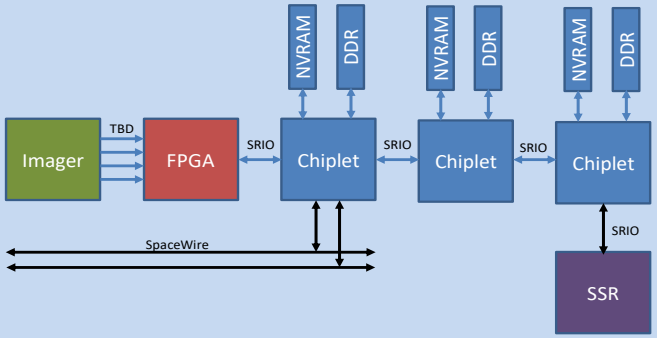
- **System Metrics**
- >10 GOPs compute
- 10Gb/s+ sensor rates
- Microsecond I/O latency
- Control packet rates >1Kpps
- Time tagging to microsecond accuracy

HPSC Use Cases - High Bandwidth Instruments and SmallSats/Constellations

High Bandwidth Instrument

Compute Needs
- Soft real time
- Non-mission critical
- High rate sensors
- Large calibration sets in NV memory

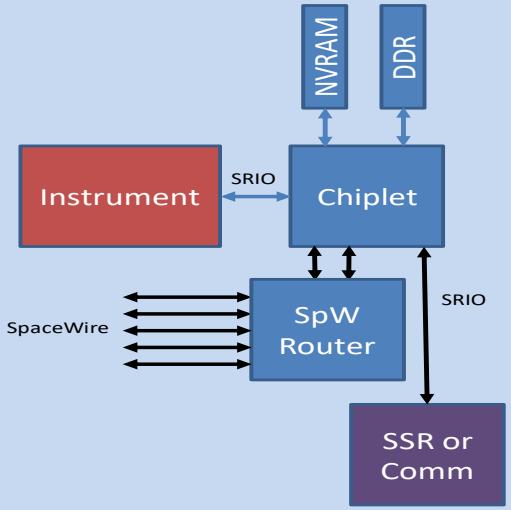
- **System Metrics**
- 10-20 GOPs compute
- >10GB/s memory bandwidth
- >20Gbps sensor IO data rates



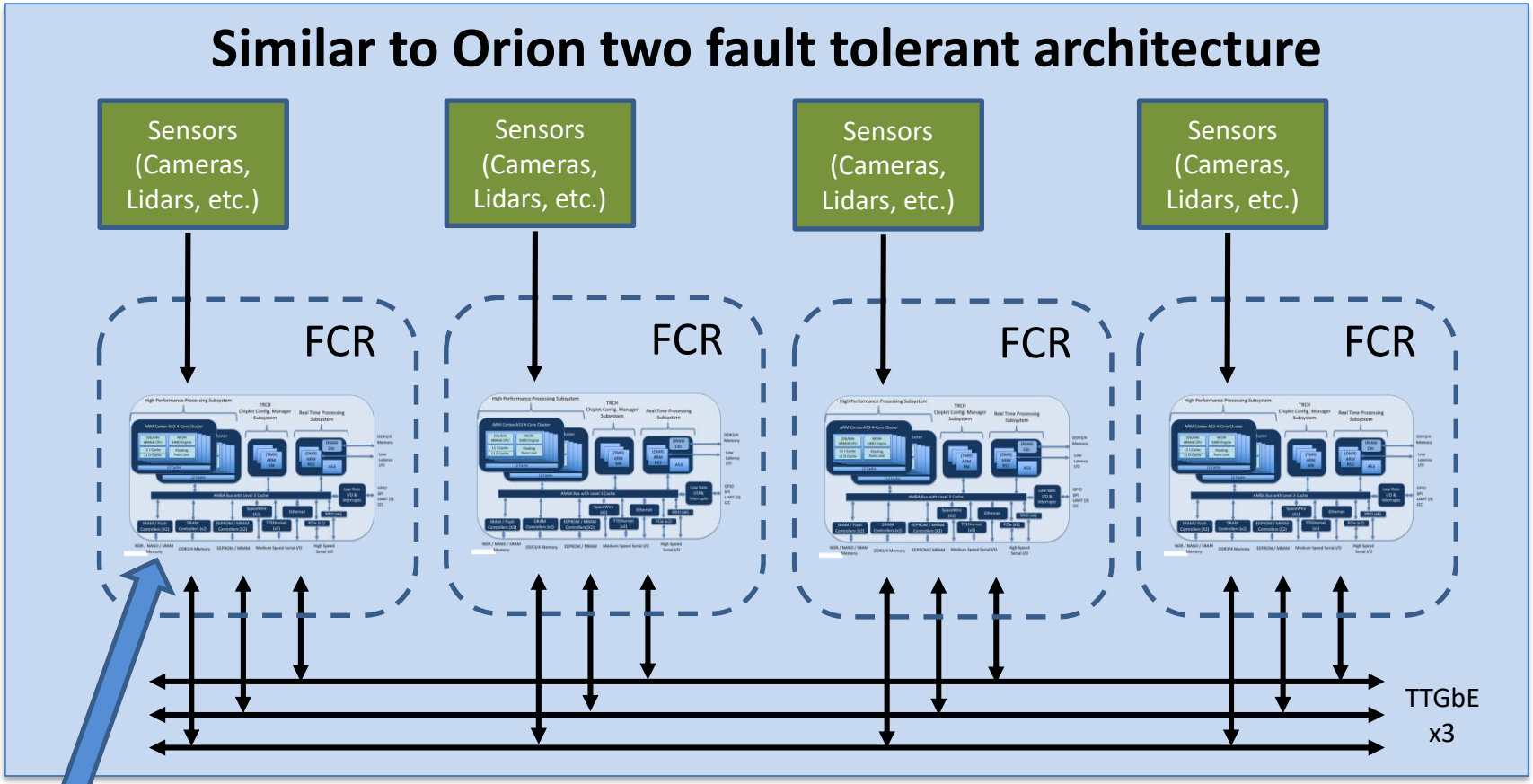
Smallsat

Compute Needs
- Hard and Soft real time
- GNC/C&DH
- Autonomy and constellation(cross link comm)
- Sensor data processing
- Autonomous science

- **System Metrics**
- 2-5Gbps sensor IO
- 1-10GOPs
- 1GB/s memory bandwidth
- 250Mbps cross link bandwidth



HPSC Use Cases – HEO Habitat/Gateway



- A single HPSC exceeds the performance metrics of a Orion Vehicle Management Computer (VMC)
- A VMC contains three Self-Checking Pairs (SCP)

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Broader HPSC Ecosystem

- Beyond the HPSC Chiplet, System Software, and Middleware developments, further investments can implement a robust HPSC avionics ecosystem
  - Advanced Spaceflight Memory
  - Increased RTOS Support
  - Multi-Output Point-Of-Load Converters
  - Coprocessors (GPU, Neuromorphic, etc.)
  - Special Purpose Chiplets (Security Chiplet, etc.)
  - Advanced Packaging (Multiple Chiplets in a Package)
  - Single Board Computers

Conclusion

- As illustrated by the NASA use cases, our future missions demand the capabilities of HPSC
- Improved spaceflight computing means enhanced computational performance, energy efficiency, and fault tolerance
- With the ongoing HPSC development, we are well underway to meeting future spaceflight computing needs
- The NASA-developed Middleware will allow the efficient infusion of the HPSC chiplet into those missions
- Further investments can implement a full HPSC avionics ecosystem

Acknowledgements: Rich Doyle (JPL), Rafi Some (JPL), Jim Butler (JPL), Irene Bibyk (GSFC), Jonathan Wilmot (GSFC), and Jon Ballast (Boeing) for diagrams and use case definitions