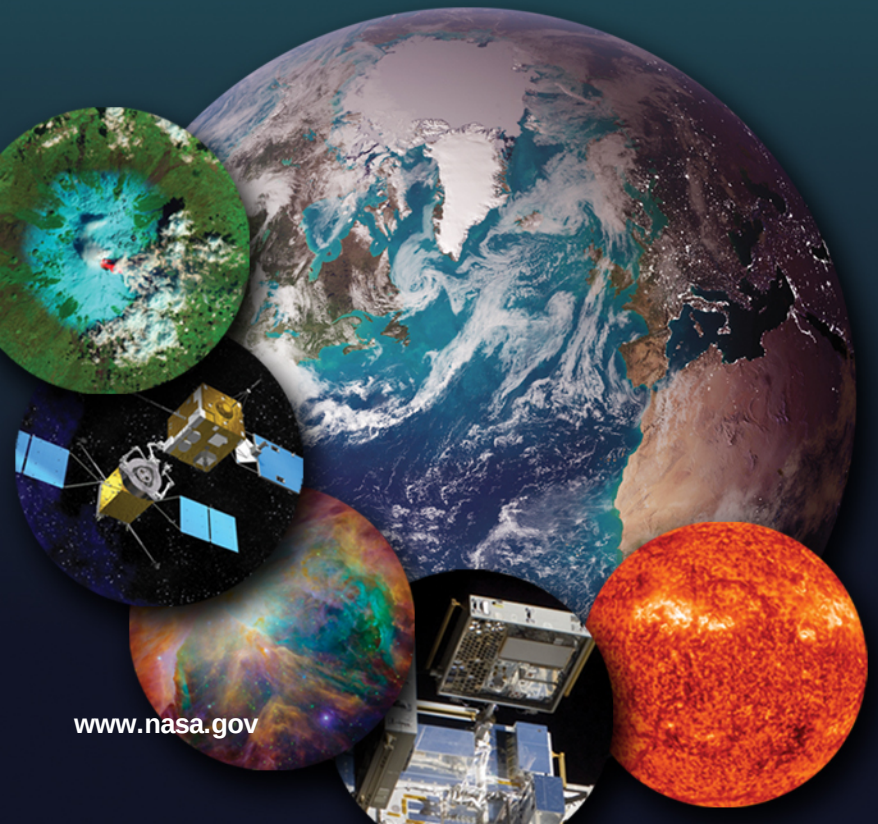
National Aeronautics and Space Administration

SpaceCube: A Family Of Reconfigurable Hybrid On-Board Science Data Processors



Thomas P. Flatley
Head, Science Data Processing Branch
Software Engineering Division
NASA - Goddard Space Flight Center
Greenbelt, MD USA

November 2018

SpaceCube

www.nasa.gov

Background

The Challenge

The next generation of NASA science and exploration missions will require "order of magnitude" improvements in on-board computing power …

Mission Enabling Science Algorithms & Applications

- Autonomous Operations
- Real-time Event / Feature Detection
- Real-time Sensing and Control
- On-Board Data Volume Reduction
- Real-time Image Processing
- On-Board Product Generation
- On-Board Classification
- Real-time "Situational Awareness"
- "Intelligent Instrument" Data Selection / Compression
- Real-time Calibration / Correction
- Inter-platform Collaboration
- Distributed Measurement Missions

Our Approach

- The traditional path of developing radiation hardened flight processor will not work … they are always one or two generations behind
- Use the latest radiation-tolerant* processing elements to achieve 10x to 100x improvement in "MIPS/watt" (for the same size/weight/power)
- Accept that radiation induced upsets may happen occasionally and just deal with them appropriately … any level of reliability can be achieved via smart system design

*Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation induced destructive failures (latch-up)

Our Solution

SpaceCube: a high performance reconfigurable science / mission data processor based on Xilinx Virtex FPGAs

- Hybrid processing … CPU, DSP and FPGA logic
- Integrated "radiation upset mitigation" techniques
- SpaceCube "core software" infrastructure (cFE/cFS and "SpaceCube Linux", with Xenomai)
- Small "critical function" manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

*Note: SpaceCube 2.0 and SpaceCube Mini can be populated with either commercial Virtex 5 FX130T parts or radiation hardened Virtex 5 QV parts … offering system developers the option of trading computing performance for radiation performance

Being Reconfigurable …

… equals BIG SAVINGS (both time and money)

During mission development and testing

- **Design changes without PCB changes**
- **"Late" fixes without breaking integration**

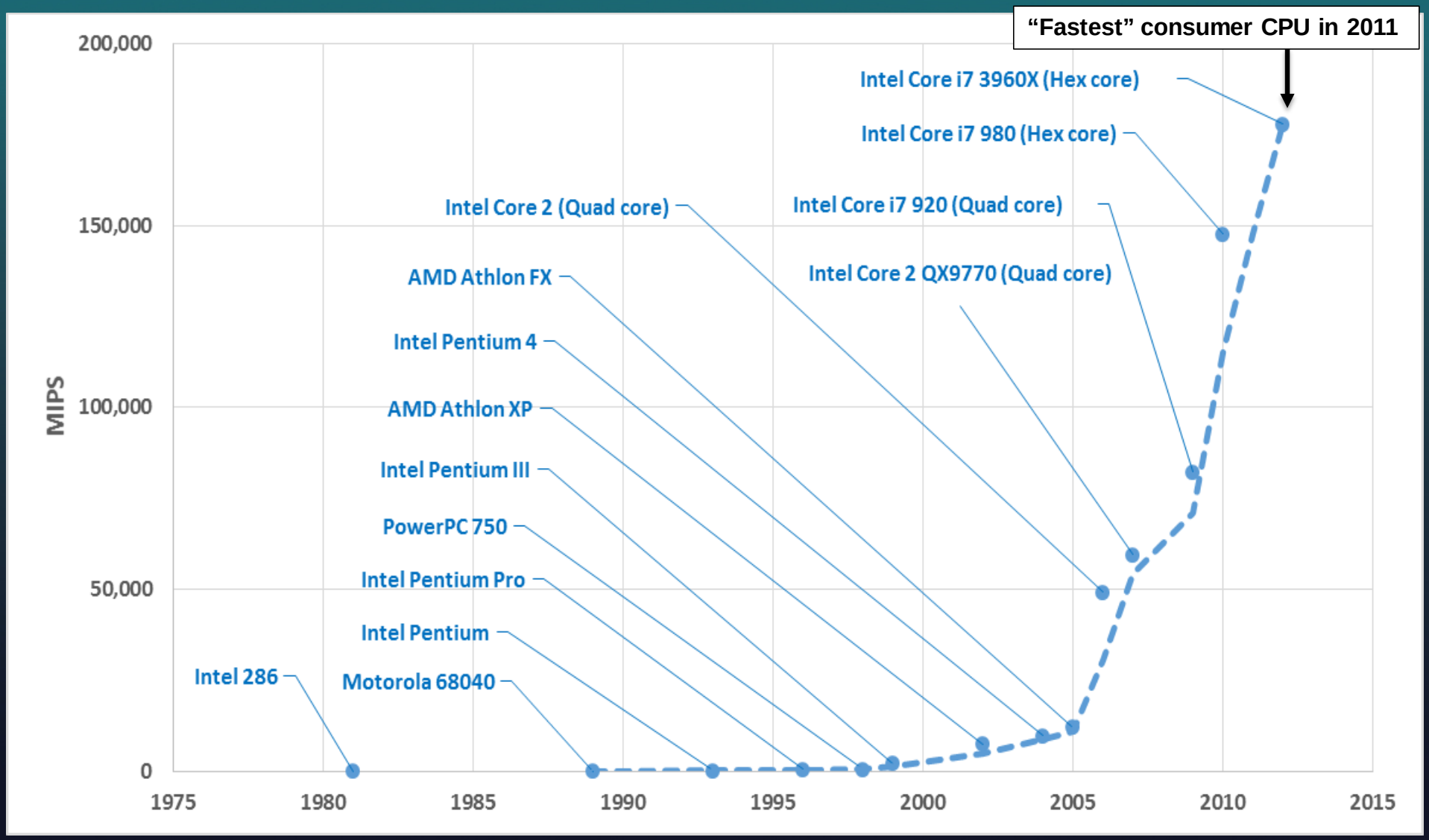
During mission operations

- **On-orbit hybrid algorithm updates**
- **Adaptive processing modes**
  - **- hi-reliability vs. high-performance**
  - **- intelligently adapt to current environment**

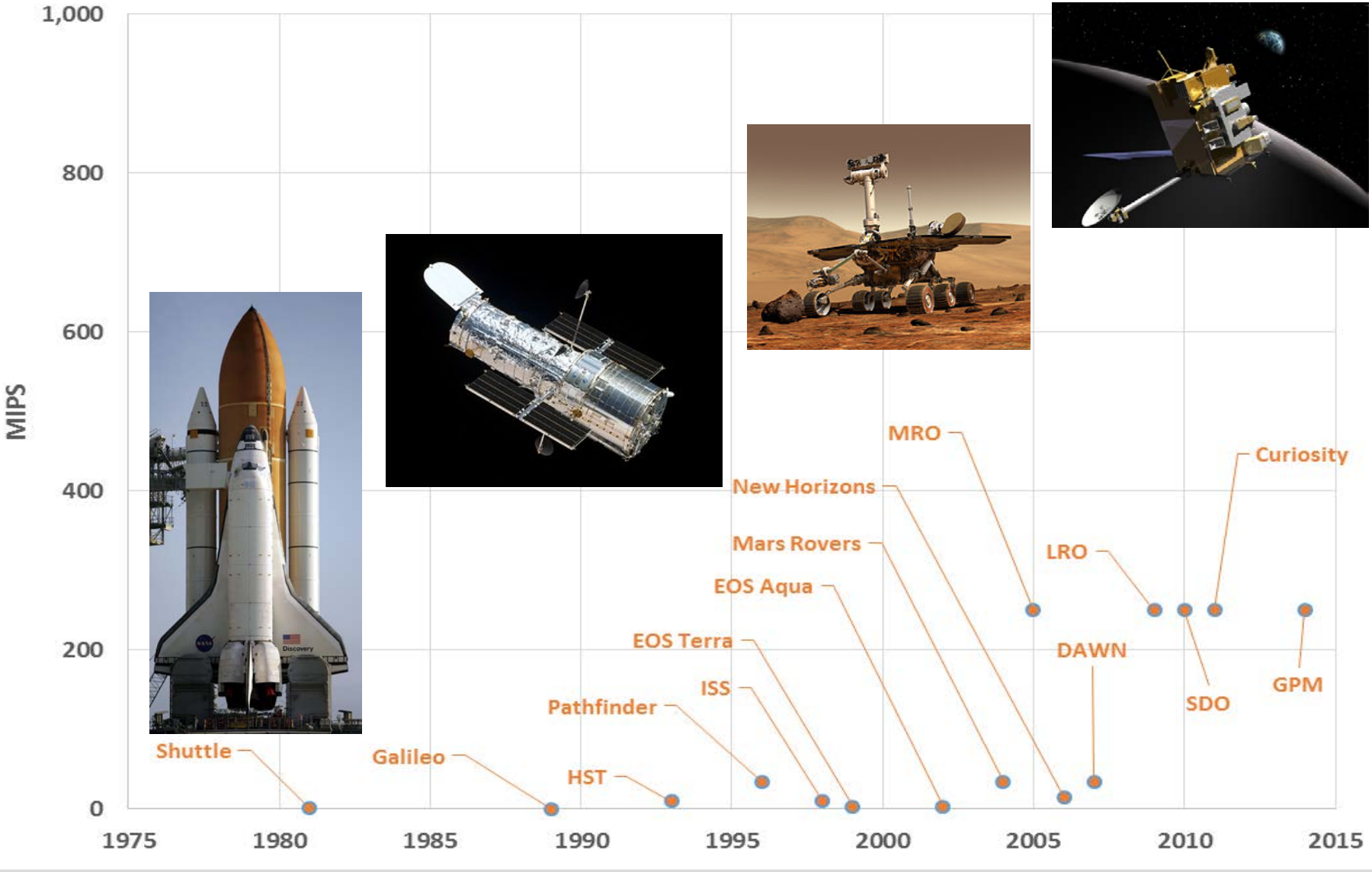
From mission to mission

- **Same avionics reconfigured for new mission**

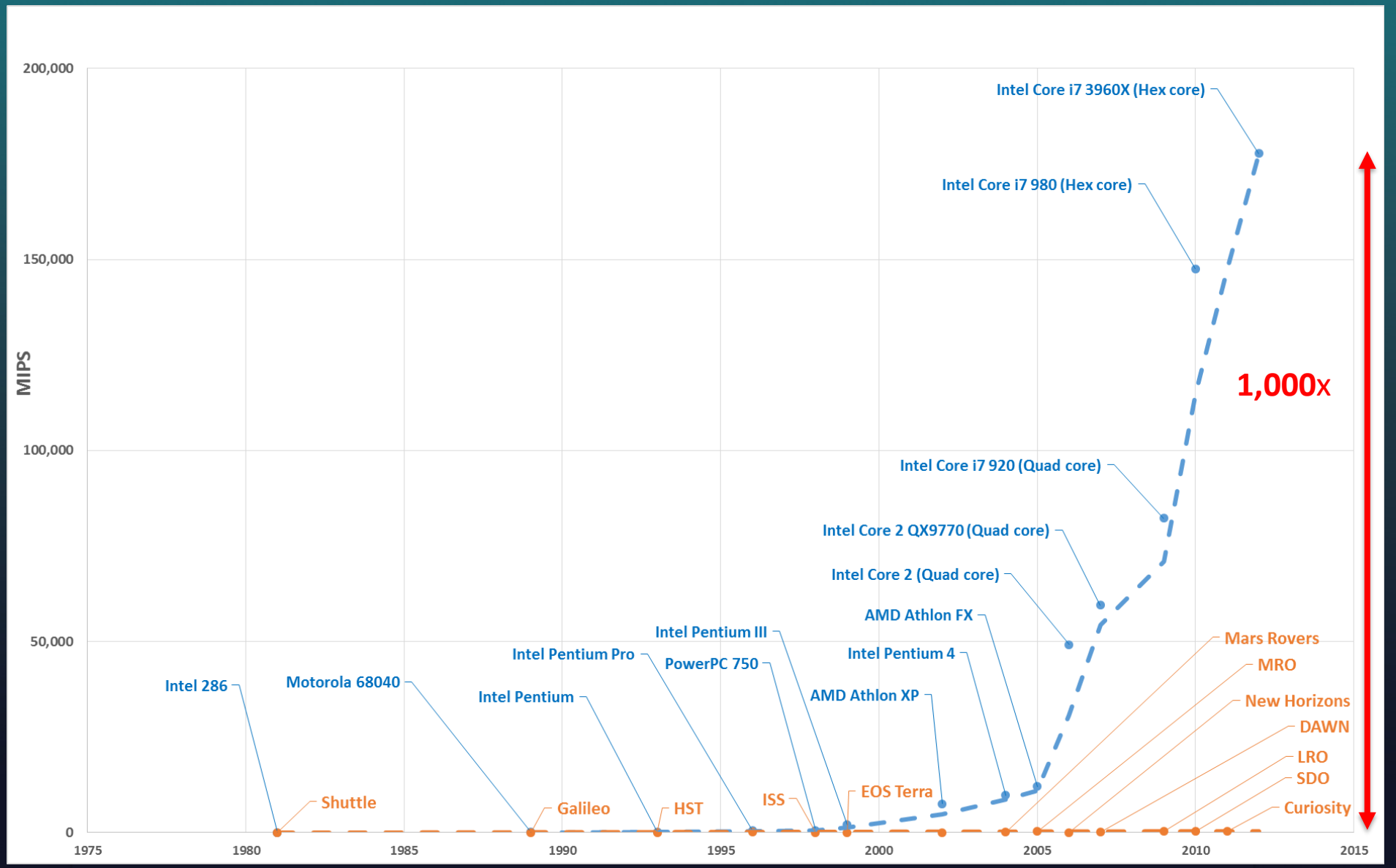
Commercial Processor Trend



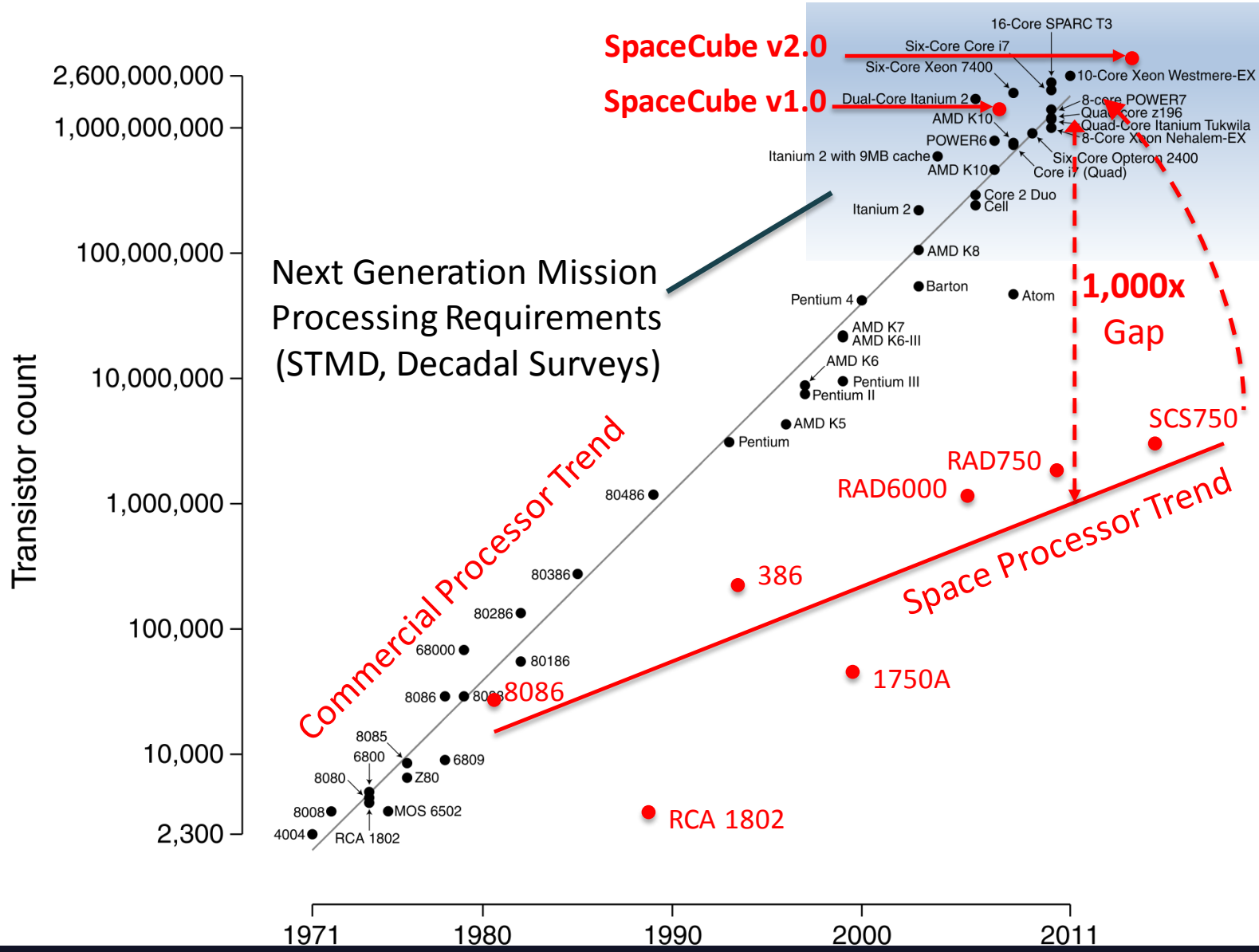
Space Processor Trend



Processor Trend Comparison

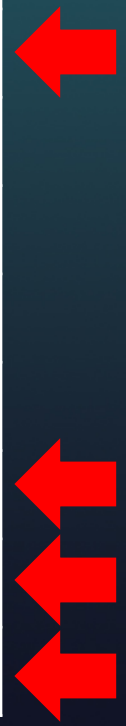


SpaceCube Closes the Gap



Processor Comparison

Processor	MIPS	Power	MIPS/W
MIL-STD-1750A	3	15W	0.2
RAD6000	35	15W	2.33
RAD750	300	15W	20
LEON 3FT	75	5W	15
LEON3FT Dual-Core	250	10W	25
BRE440 (PPC)	230	5W	46
Maxwell SCS750	1200	25W	48
SpaceCube 1.0	3000	7.5W	400
SpaceCube 2.0	6000	10W	600
SpaceCube Mini	3000	5W	600



SpaceCube 1.0 vs RAD750

25 RAD750 6U Processor Cards



=

1 SpaceCube Processor Card



Single String Box

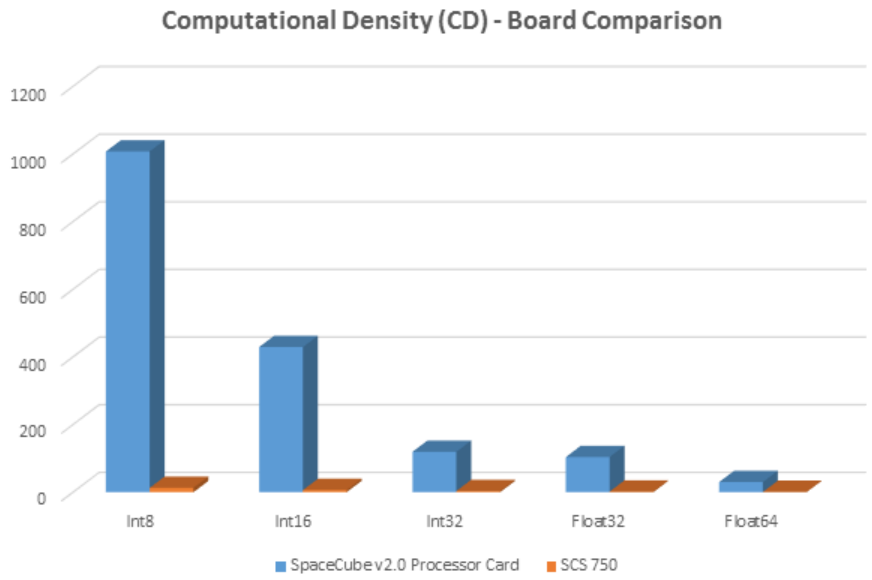
Power	600W
Weight	100-lbs
Volume	48.6 cu-ft

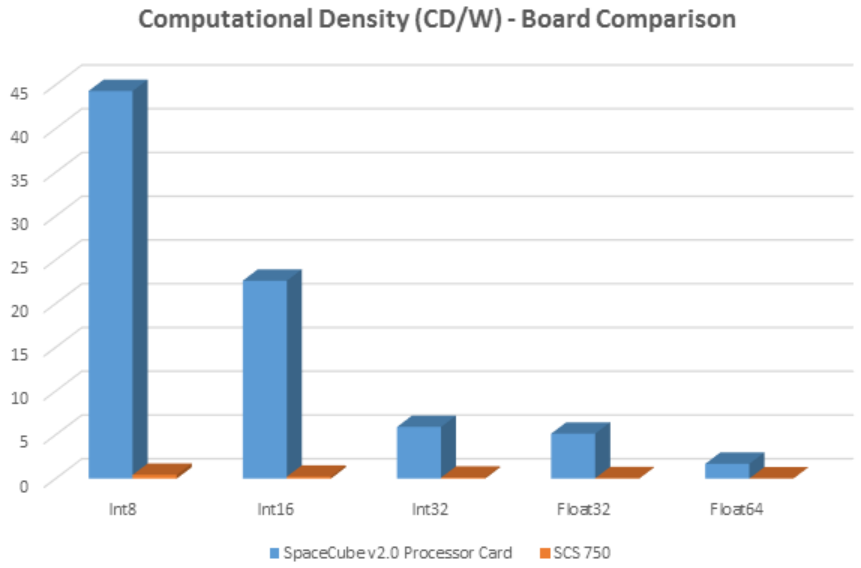
Dual Redundant Box

Power	37W
Weight	7.5-lbs
Volume	1.2 cu-ft

SpaceCube 2.0 vs SCS750 (per NSF CHREC)

Board Comparison





	CD (GOPS)					CD/W (GOPS/W)					EMB (GB/s)	IOB (GB/s)
Processor	Int8	Int16	Int32	Float32	Float64	Int8	Int16	Int32	Float32	Float64		
SpaceCube v2.0 Processor Card	1007.44	429.14	119.34	103.86	29.92	44.3	22.62	5.91	5.14	1.7	32	218.32
SCS 750	12.8	6.4	3.2	1.6	0.8	0.44	0.22	0.11	0.05	0.03	6.4	6.4

Notes:

- Power for PowerPC 750fx is ~9.7Watts max. However, for 3x PowerPC 750fx processors it's 29.1 Watts. No performance gain, but triple the power consumption lowers CD/W.
- Computational Density doubled for SpaceCube v2.0 (2x Xilinx FPGAs)

- Computational Density numbers for Xilinx Virtex-5QV FX130 FPGA from:
  - "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics" Tyler M. Lovelly and Alan D. George University of Florida, Gainesville, Florida 32611
- Computational Density numbers for PowerPC 750FX from:
  - NSF SHREC Device Metrics (Fixed Logic Device) IBM PowerPC 750FX, Evan Wiliam Gretok

Performance Comparisons

Computational Density (CD) & CD per Watt

Processor	CD (GOPS)					CD/W (GOPS/W)				
	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP
Honeywell HXRHPPC	0.08	0.08	0.08	0.08	0.04	0.01	0.01	0.01	0.01	0.01
BAE Systems RAD750	0.27	0.27	0.27	0.13	0.13	0.05	0.05	0.05	0.03	0.03
Cobham GR712RC	0.08	0.08	0.08	0.03	0.03	0.05	0.05	0.05	0.02	0.02
Cobham GR740	1.00	1.00	1.00	1.00	1.00	0.67	0.67	0.67	0.67	0.67
BAE Systems RAD5545	3.73	3.73	3.73	1.86	1.86	0.19	0.19	0.19	0.09	0.09
Boeing Maestro	11.99	11.32	10.19	12.74	12.74	0.54	0.51	0.46	0.57	0.57
Ramon Chips RC64	102.40	102.40	30.72	19.20	0.00	12.80	12.80	3.84	2.40	0.00
BAE Systems RADSPEED	14.17	11.81	6.44	**70.83**	**35.42**	0.94	0.79	0.43	4.72	2.36
Xilinx Virtex-5QV FX130	**503.72**	**214.57**	**59.67**	51.93	14.96	44.30	22.62	5.91	5.14	1.70
Xilinx Zynq-7020	283.3	152	46.29	40.57	12.63	**60.41**	**36.91**	**10.72**	**7.83**	**3.06**

SPFP = Single-Precision Floating Point
DPFP = Double-Precision Floating Point

Results assume an operations mix of 50% additions and 50% multiplications

CHREC
NSF Center for High-Performance Reconfigurable Computing

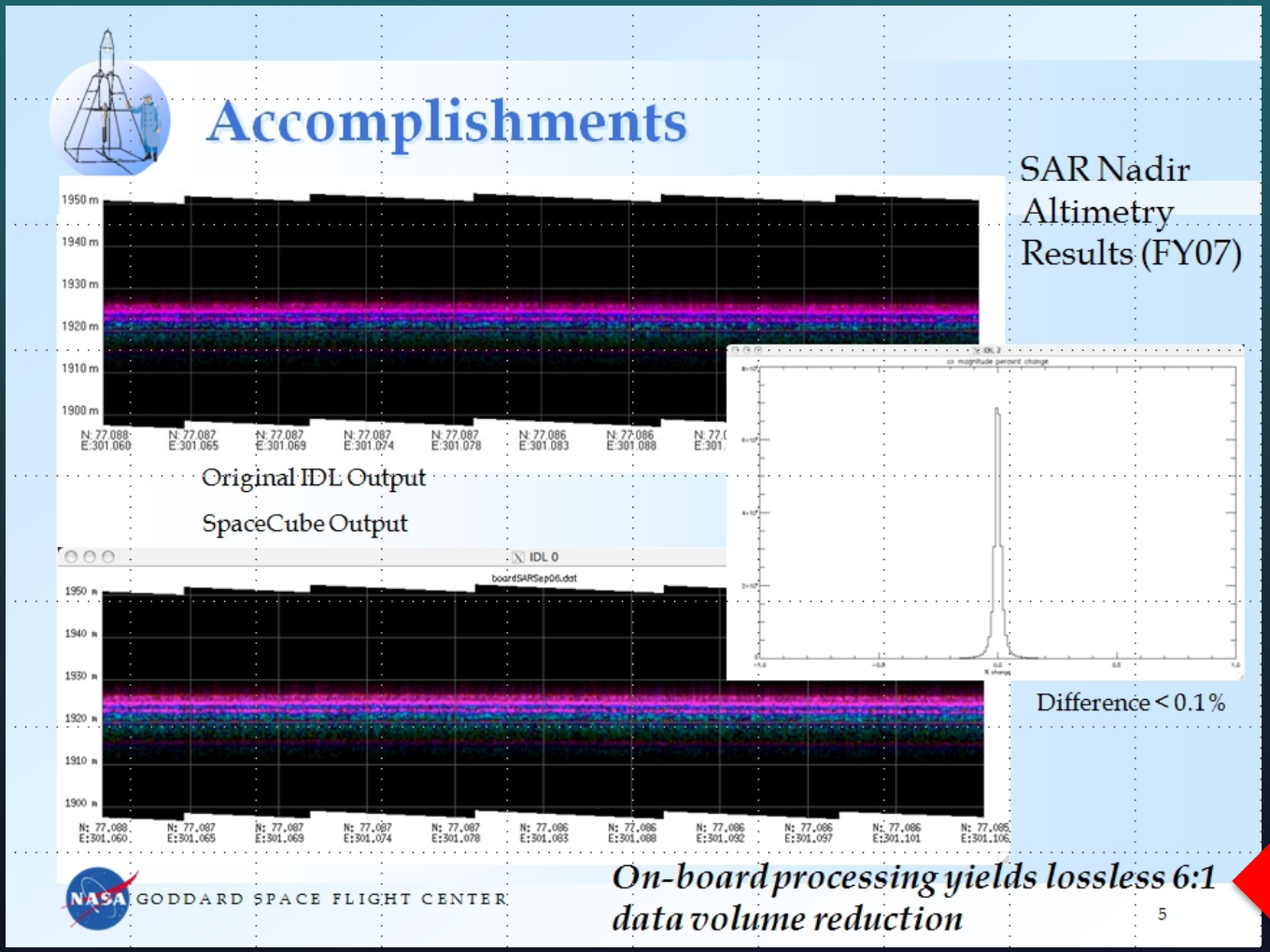
Applications

Algorithm Acceleration

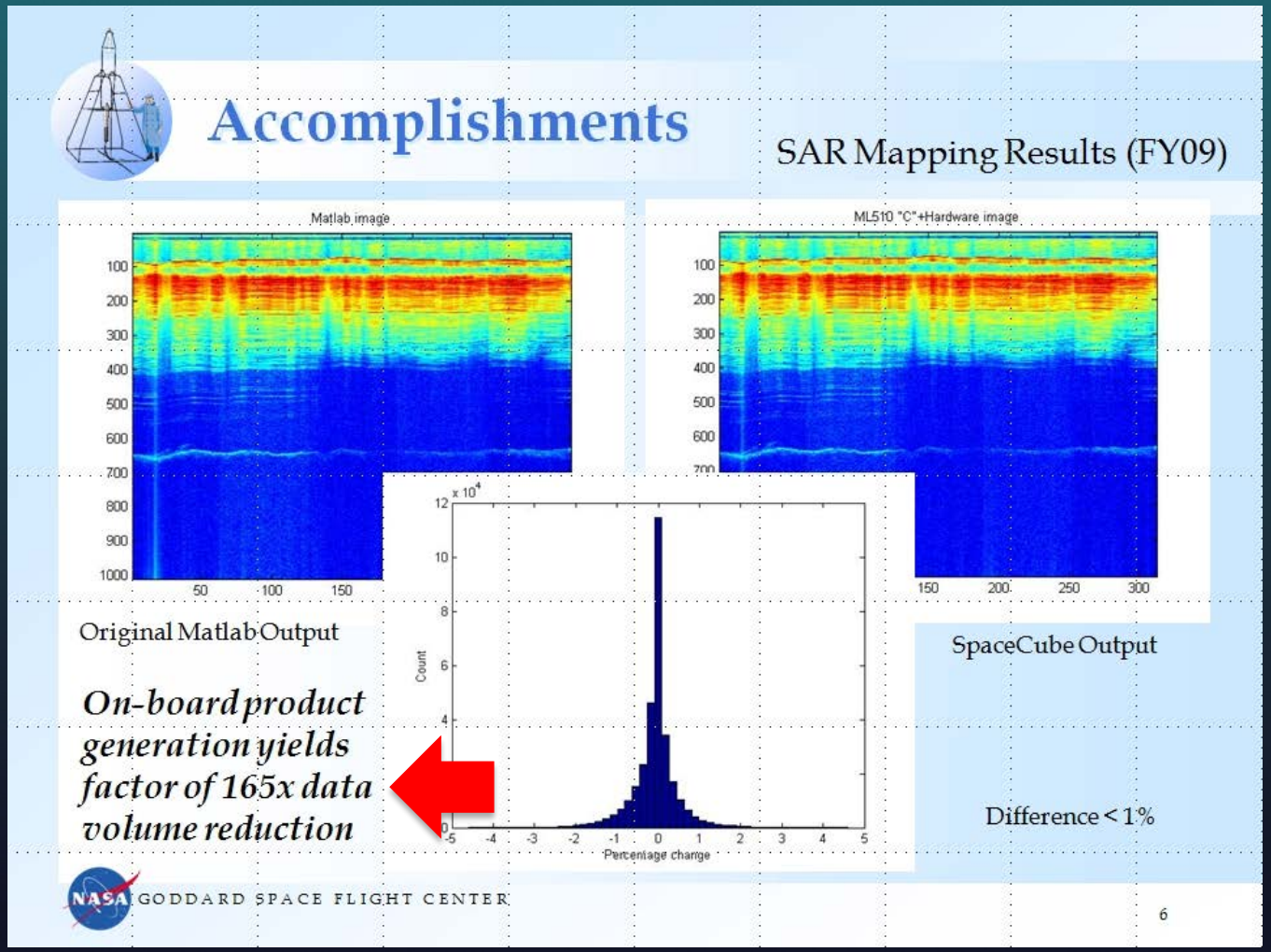
Application	Xilinx Device	Acceleration vs CPU
SAR Altimeter	Virtex-4 FX60	**79x** vs PowerPC 405 (250MHz, 300 MIPS)
RNS GNFIR FPU, Edge	Virtex-4 FX60	**25x** vs PowerPC 405 (250MHz, 300 MIPS)
HHT EMD, Spline	Virtex-1 2000	**3x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)
Hyperspectral Data Compression	Virtex-1 1000	**2x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)
GOES-8 Ground System Sun correction	Virtex-1 300E	**6x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)

- ❑ All functions involve processing large data sets (1MB+)
- ❑ All timing includes moving data to/from FPGA
- ❑ **SpaceCube 2.0 is 4x to 20x more capable than these earlier systems**

On-Board Data Reduction

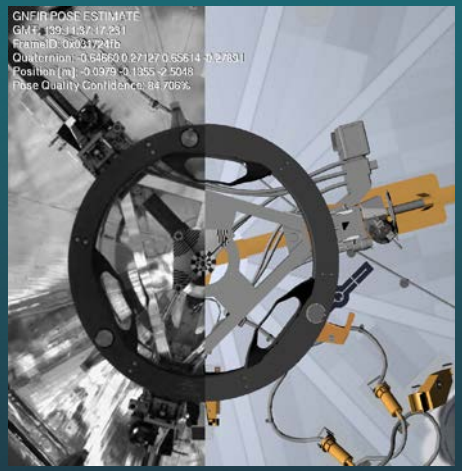


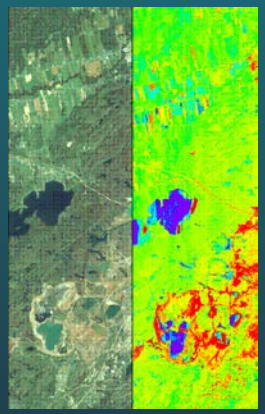
On-Board Data Reduction (cont.)



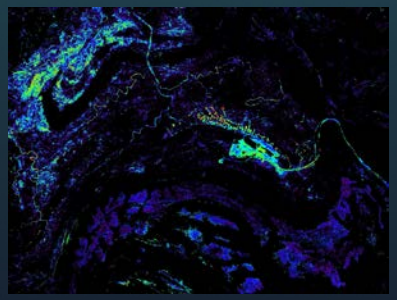
On-Board Product Generation

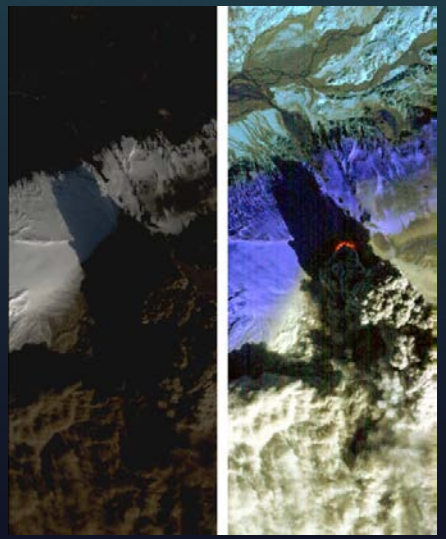


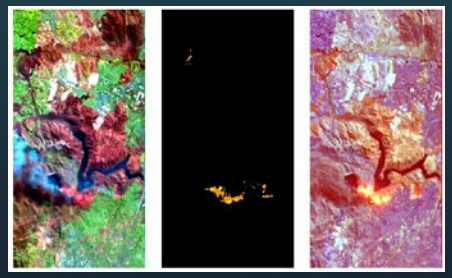


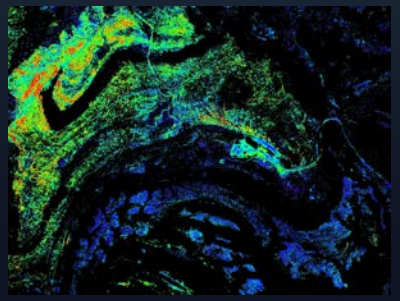


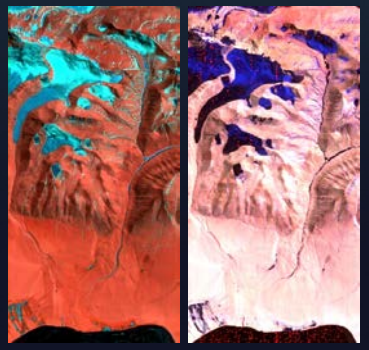
- Classification
- Product Generation
- Event Detection
- Atmospheric Correction

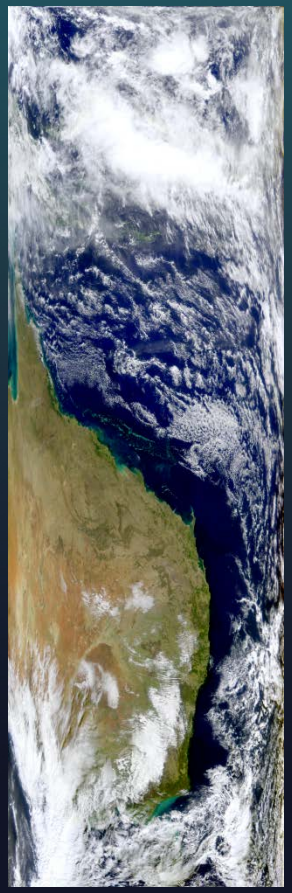


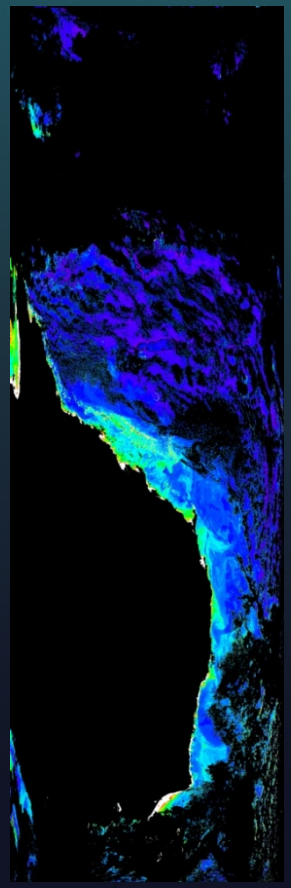








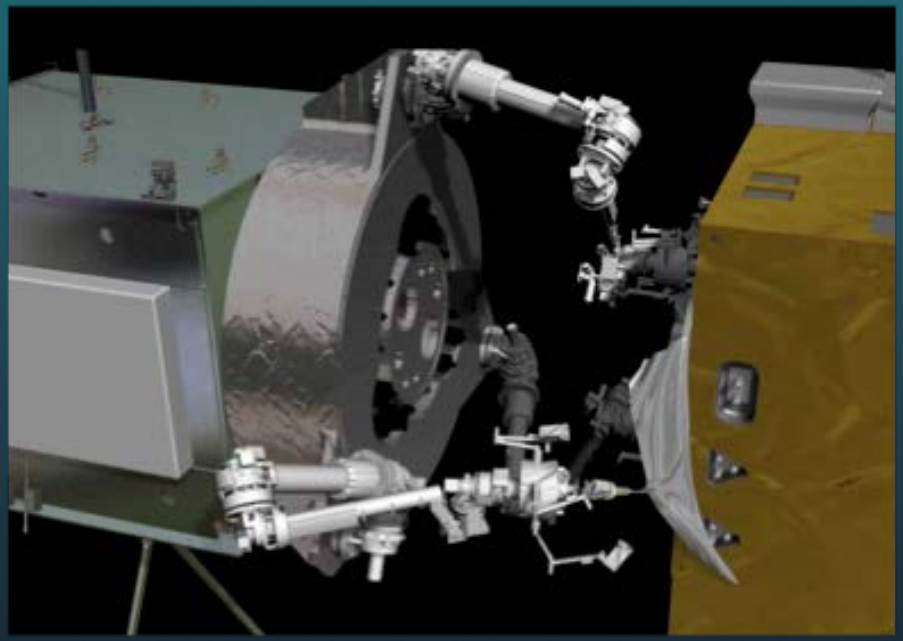




Robotic Satellite Servicing

- **Autonomous rendezvous & docking**
- **Robotic servicing**







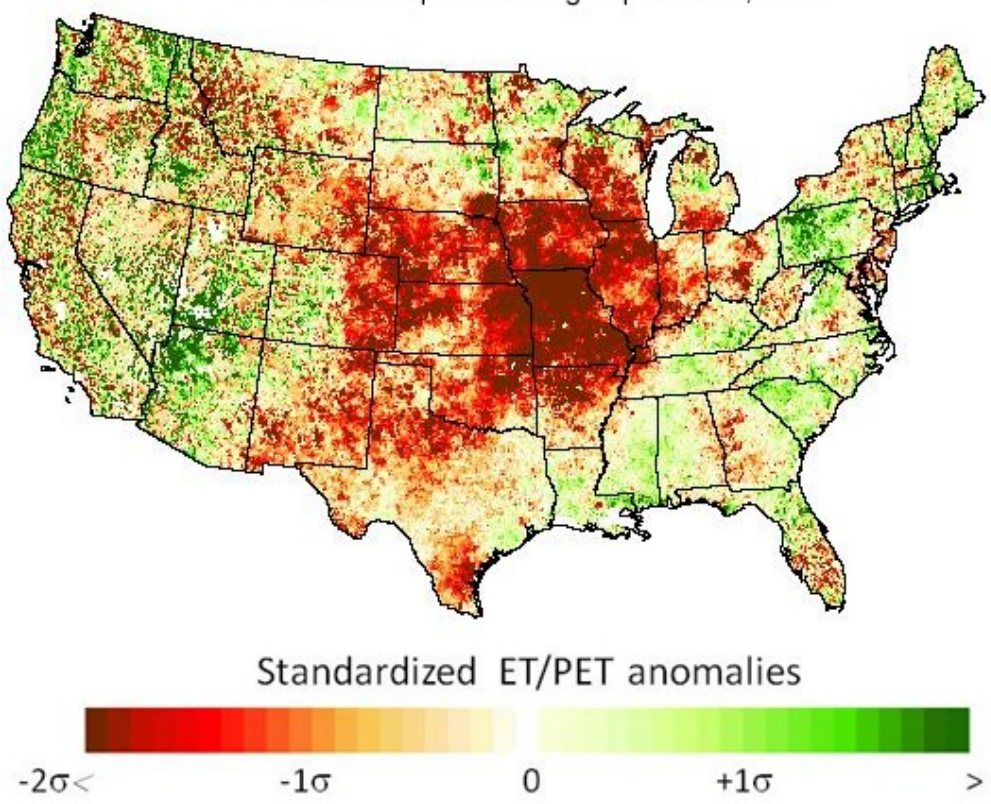
- Inspect
- Refuel
- Repair
- Replace
- Relocate

Imaging Spectrometers

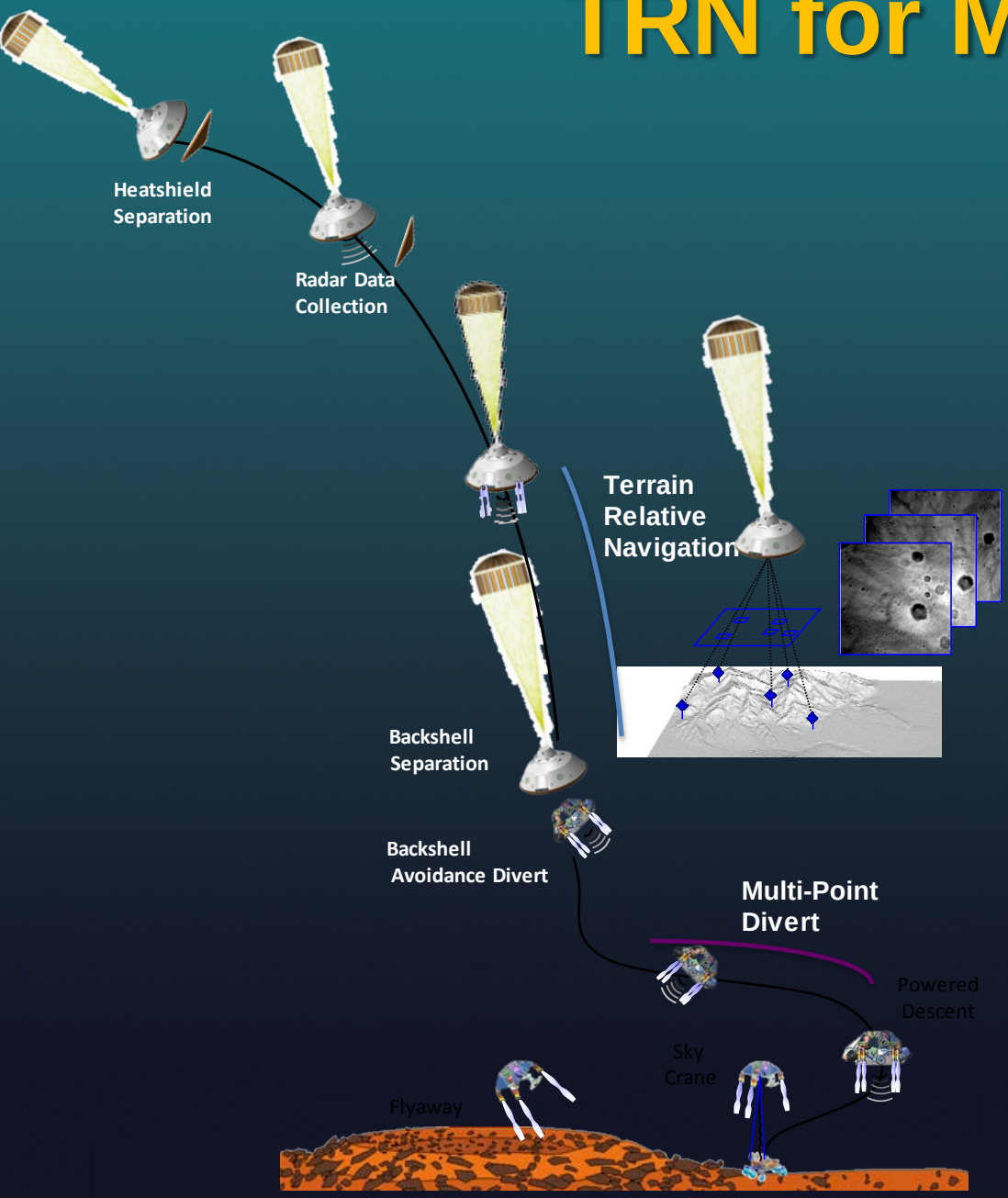


Image Credit: HyspIRI Mission Concept Team

- Direct broadcast
- Real-time products
- Data volume reduction
- Adaptive processing
- Sensor webs



TRN for Mars Missions



Terrain Relative Navigation (TRN)

- Works by taking images during parachute descent and matching them to an onboard map
  - Uses a dedicated compute element and camera
  - Yields a position solution
- Performs terrain relative navigation while the spacecraft is priming the descent engines
- Executed by the Lander Vision System (LVS)

Multi-Point Divert

- Uses position solution and list of safe landing locations to select a landing target
- Augments original MSL backshell avoidance divert (requires slightly higher backshell separation altitude)
- Lives within MSL fuel and control authority constraints

Credit: JPL Mars EDL Team

More Rover Applications?

Fast traverse

Terrain mapping (while driving)

Background science (while driving)

Entry/Descent/Landing documentation (video)

- Landing
- Parachute release
- Sky Crane

On-board processing for efficient use of downlink





Image Credit: JPL / MSSS MARDI Team

Real-time Mars Terrain Analysis

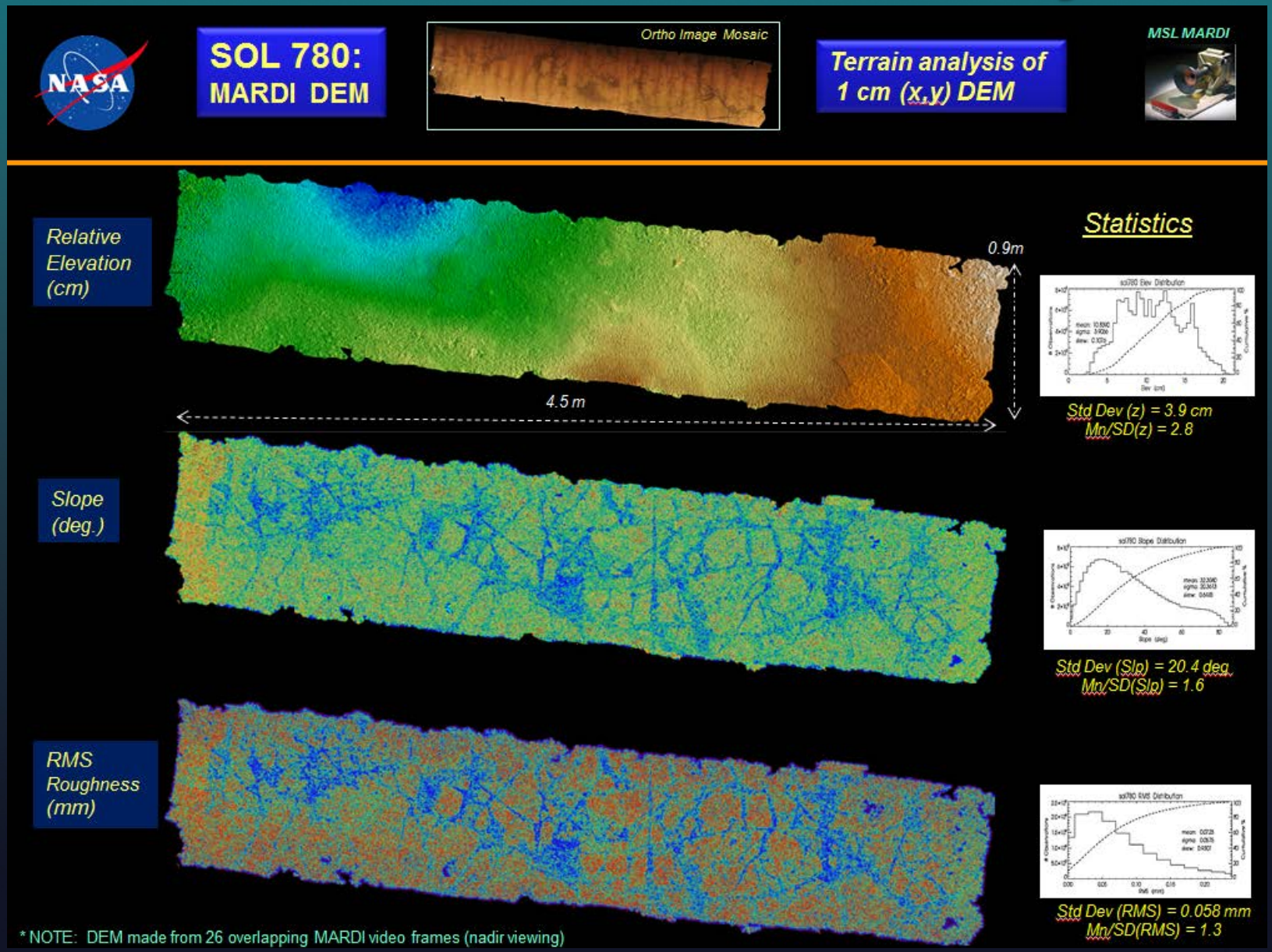
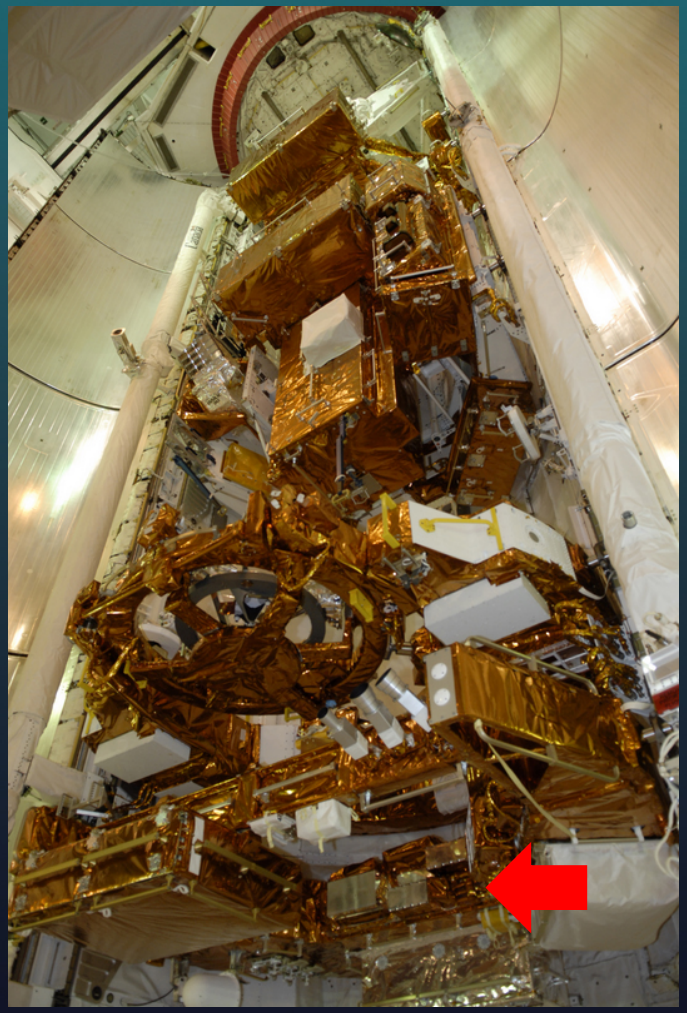


Figure by Garvin for MSL Science team: MARDI-based DEM derived from sidewalk video imaging mode data collection on the 22 m drive to "Book Cliffs" illustrating the power of fixed-nadir video imaging for terrain analysis of Mars in support of engineering (geotechnical) assessments.

Flight Demonstrations

On-Board Image Processing



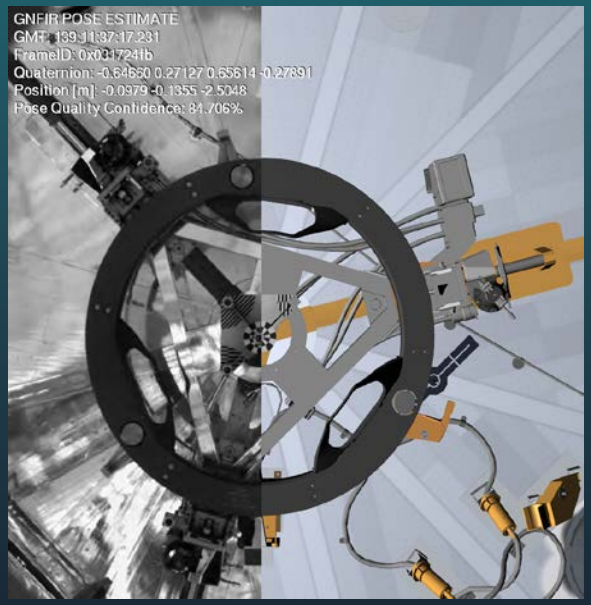
STS-125 Payload Bay

Long Range Camera on Rendezvous



Flight Image RNS Tracking Solution

Short Range Camera on Deploy



Flight Image RNS Tracking Solution

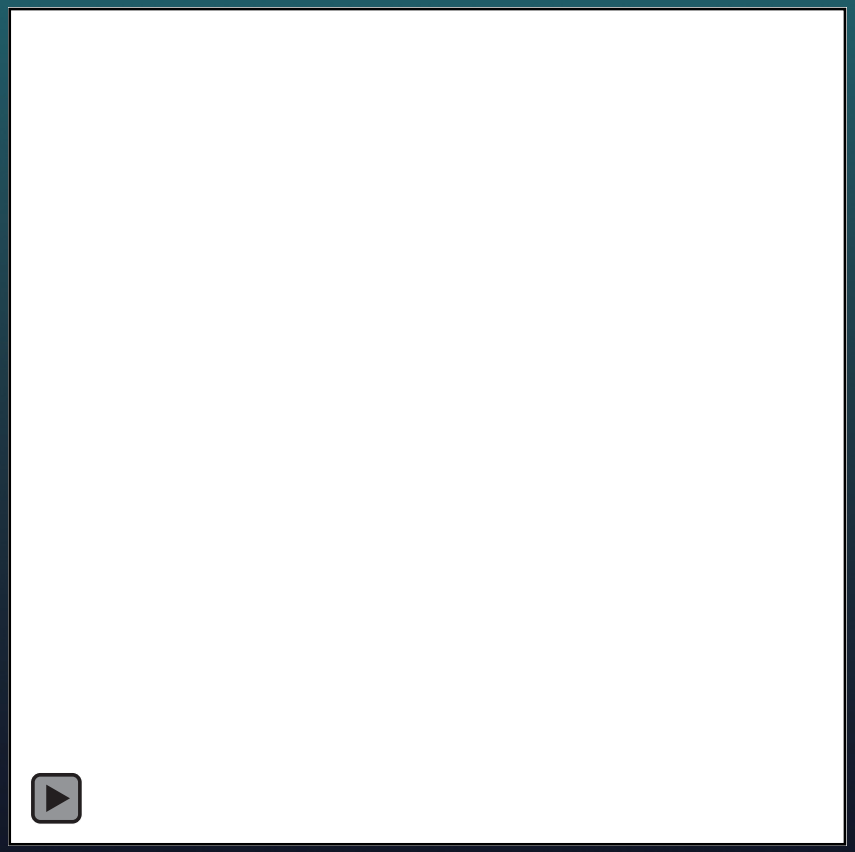
HST-SM4

GSFC SpaceCube 1.0a - Hubble SM 4 (May 2009):

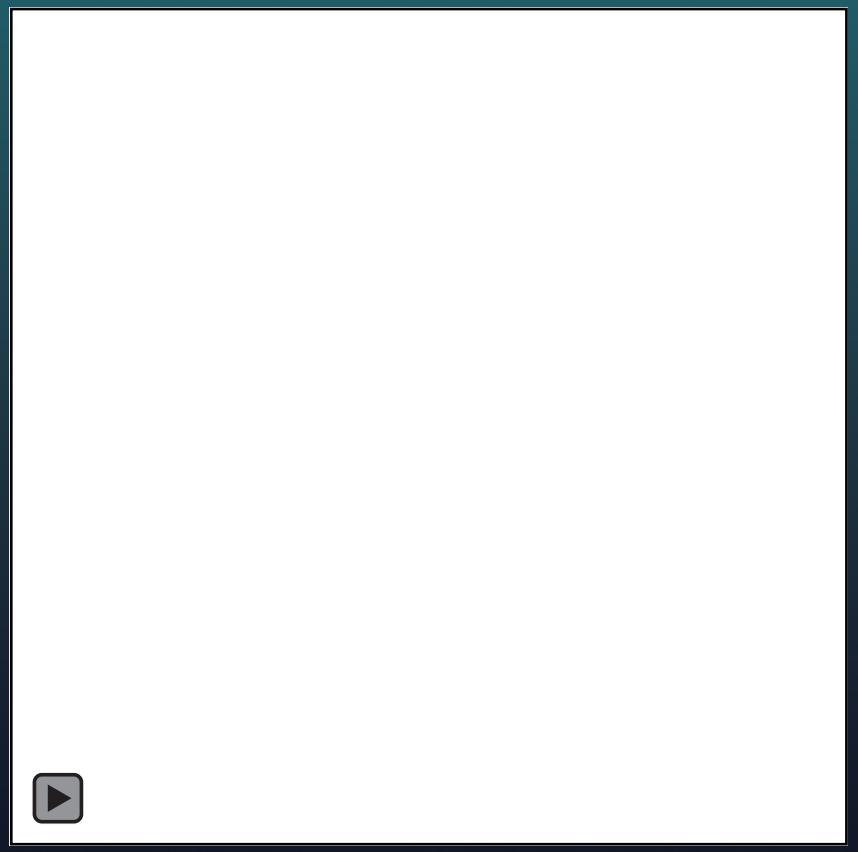
- Autonomous Rendezvous and Docking Experiment
- Hosted camera AGC and two Pose algorithms

On-Board Image Processing

→ Successfully tracked Hubble position and orientation in real-time operations
→ FPGA Algorithm Acceleration was required to meet 3Hz loop requirement



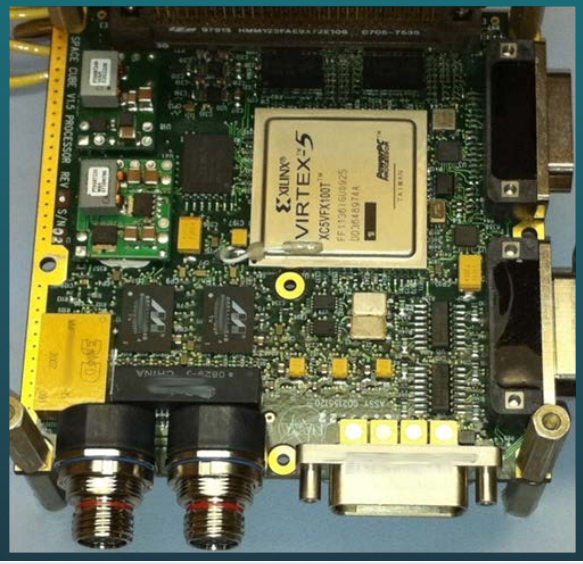
Rendezvous



Deploy (Docking Ring)

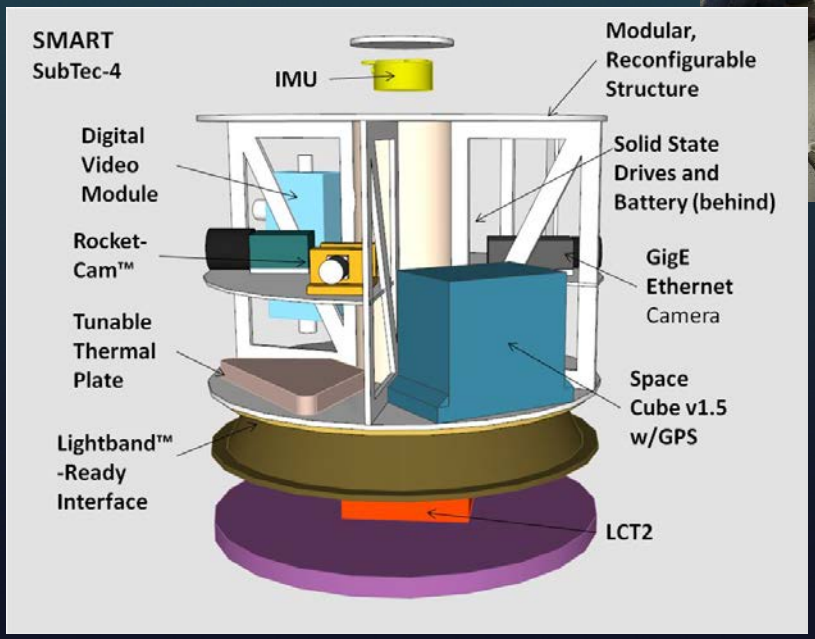
→ Typical space flight processors are 25-100x too slow for this application

SMART Sounding Rocket Experiment

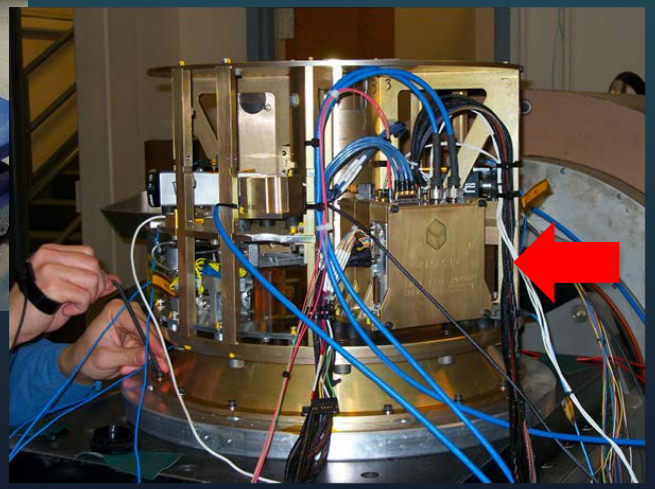












SpaceCube 1.5 on the SMART sounding rocket payload (SubTec-5, launched June 2011):

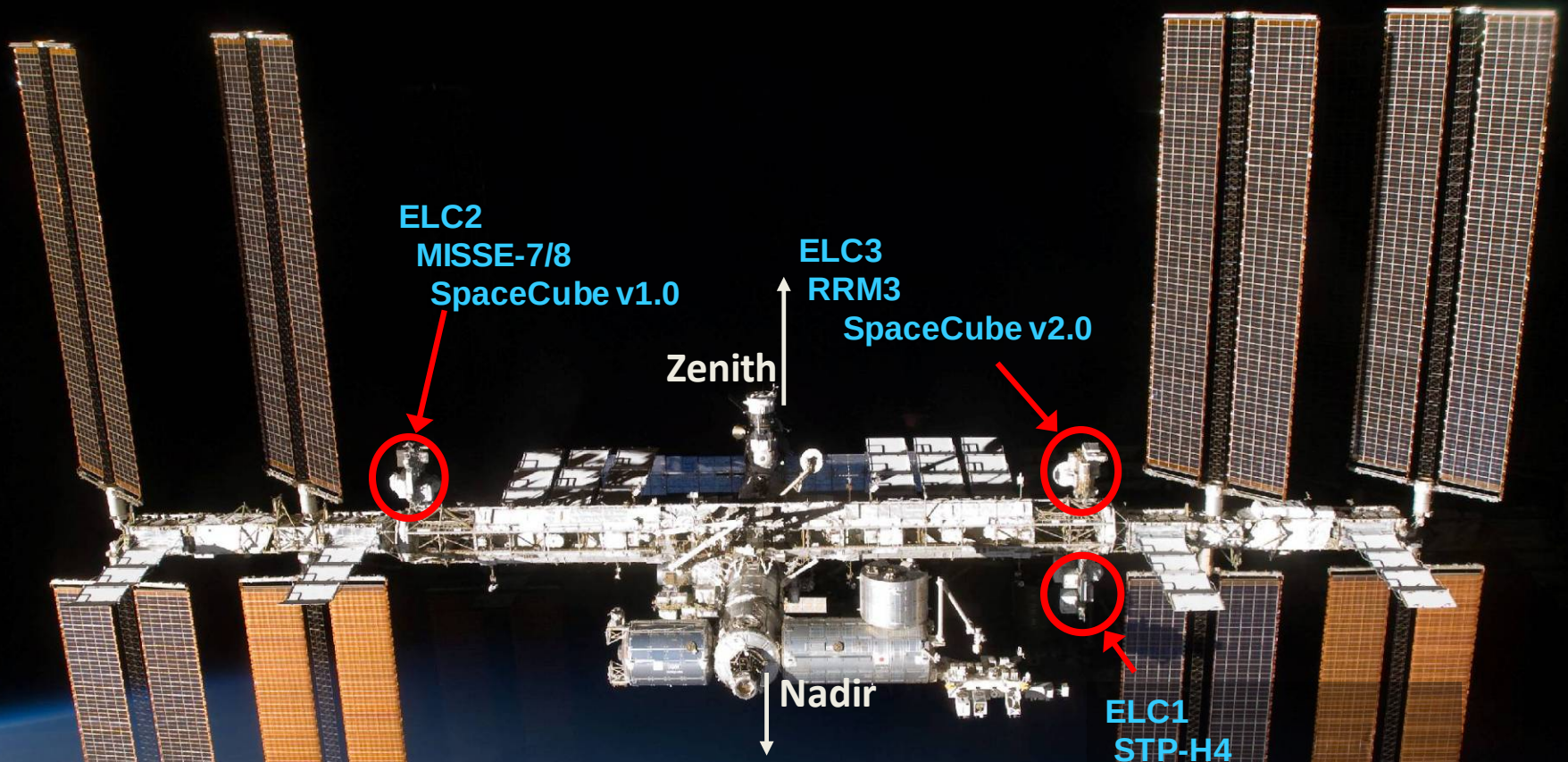
- **Multi-function avionics**
- **Collaboration with ORS**

SMART Video



SpaceCube 1.5 - SMART GigE Camera Clip
NASA Wallops Flight Facility - June 10, 2011

SpaceCube on the ISS



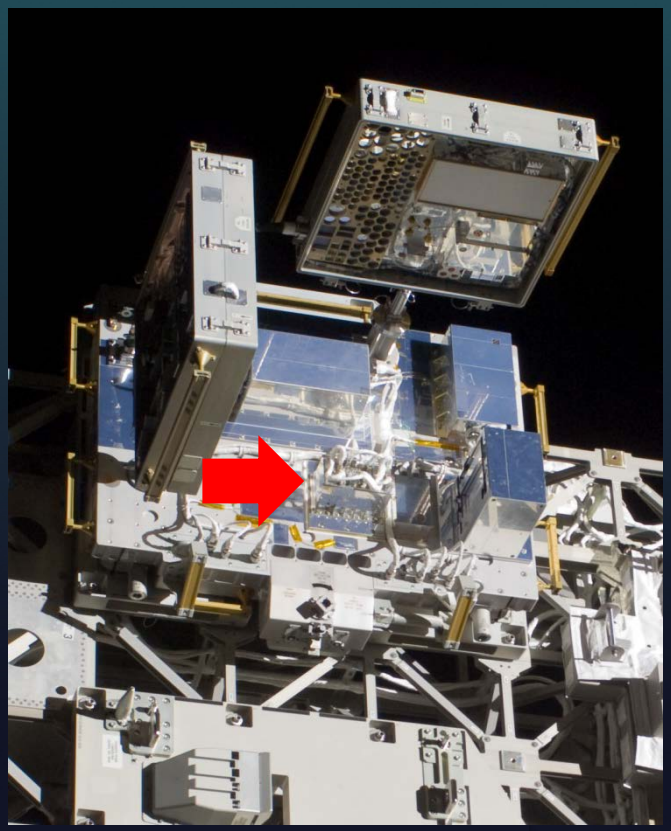
ISS Flying Towards You

Image Credit: DoD Space Test Program

SpaceCube Upset Mitigation



GSFC SpaceCube 1.0b (Nov 2009):
- "Radiation Hardened by Software" Experiment (RHBS)
- Autonomous Landing Application
- Collaboration with NRL and the DoD Space Test Program (STP)

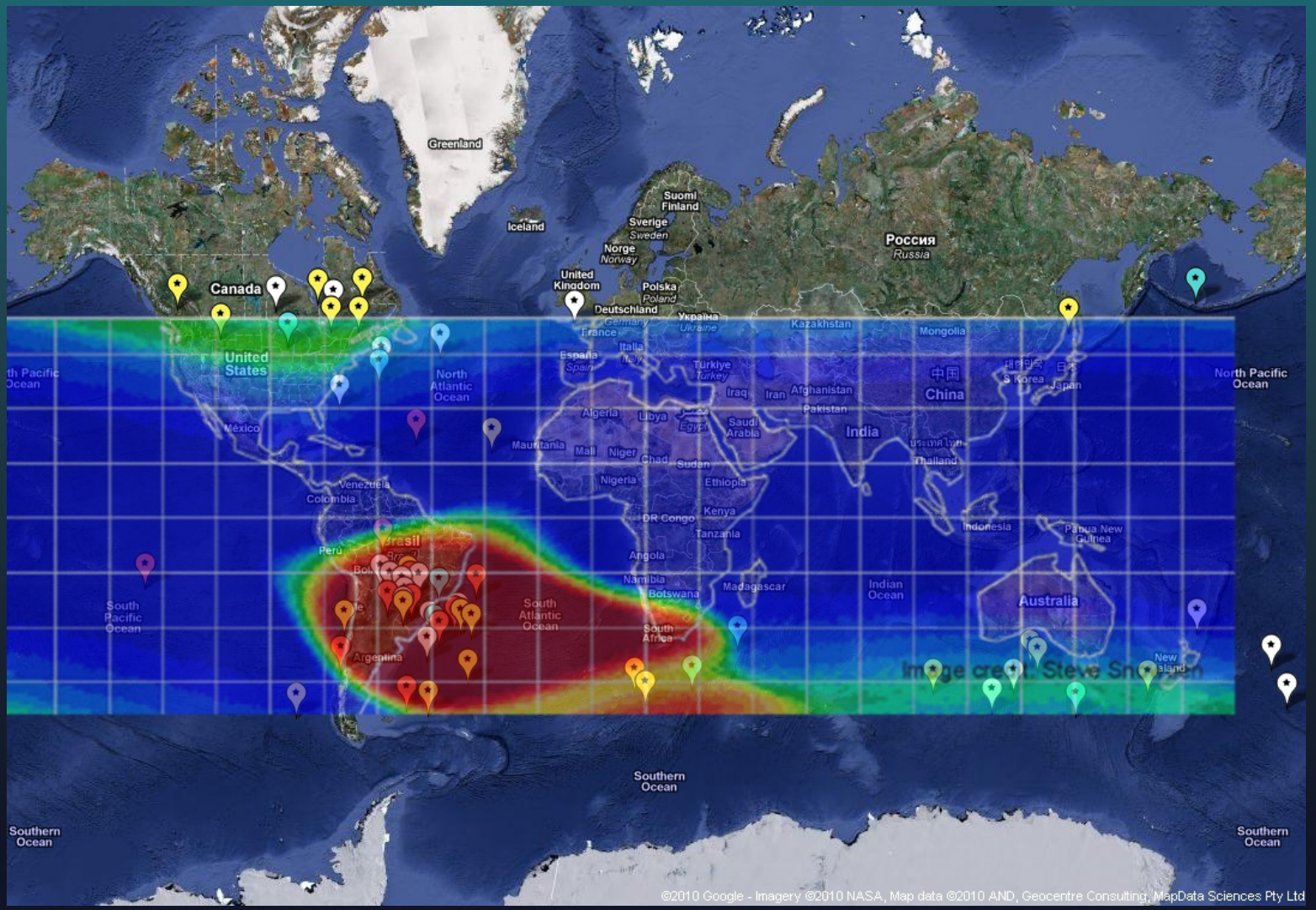


Orbit	ISS
Days in orbit	1800+
Total SEUs detected & corrected	200+
Total SEU-induced resets	6
Total SEU-induced reset downtime	30 min
Total processor availability	99.99%

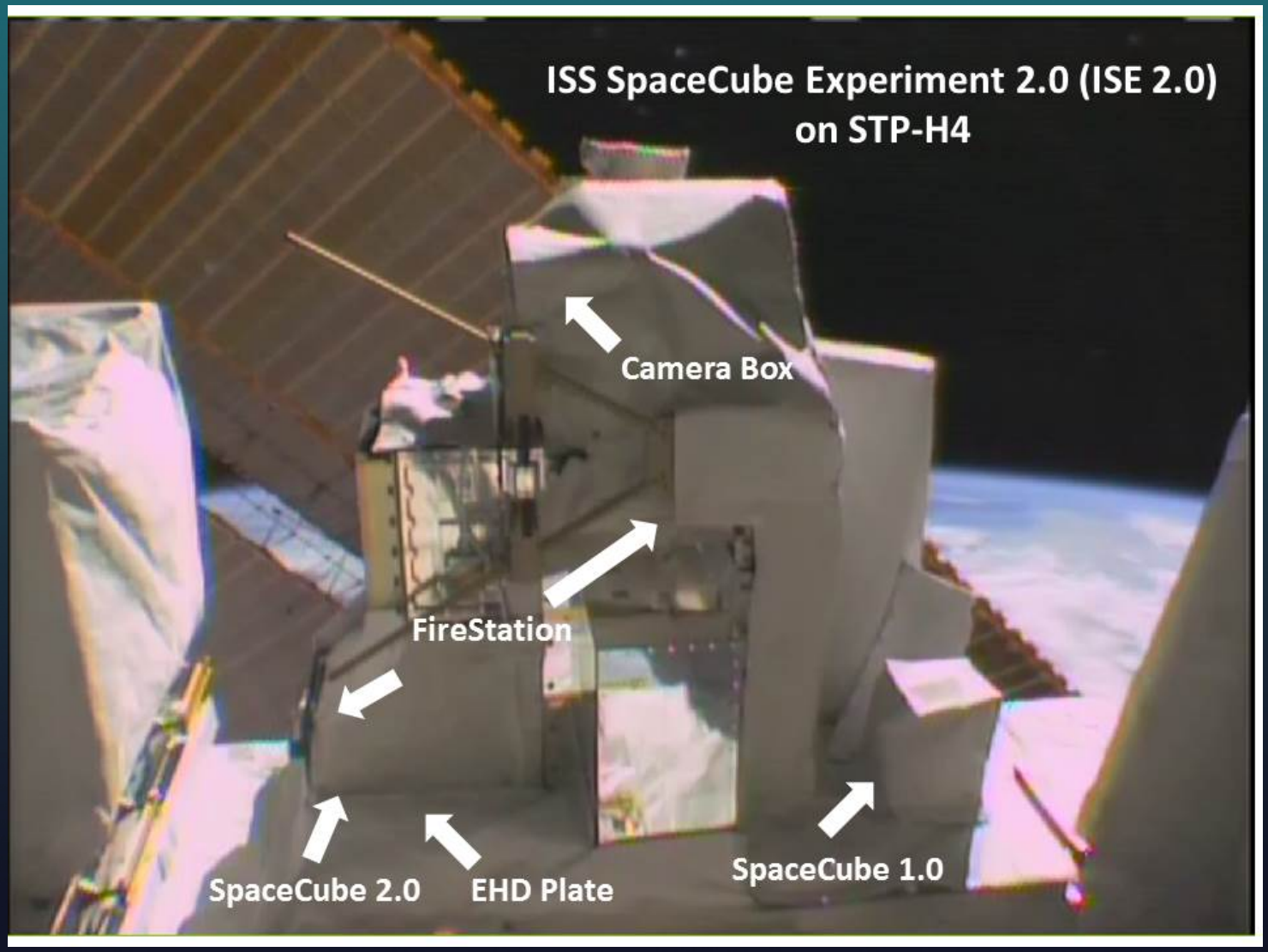
On-Orbit Upset Locations



On-Orbit Upset Locations

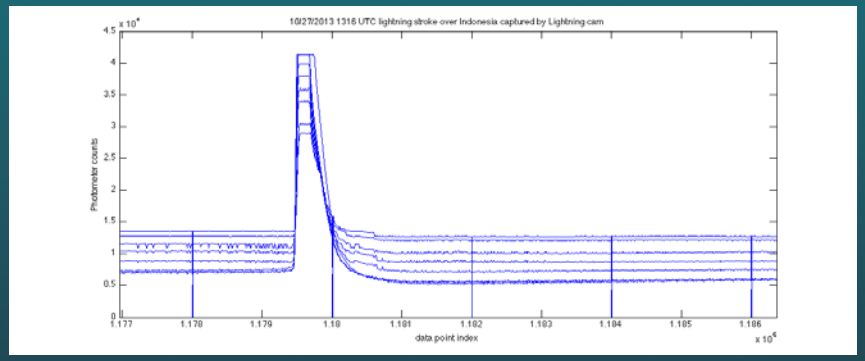


ISE 2.0 on ISS – August 2013

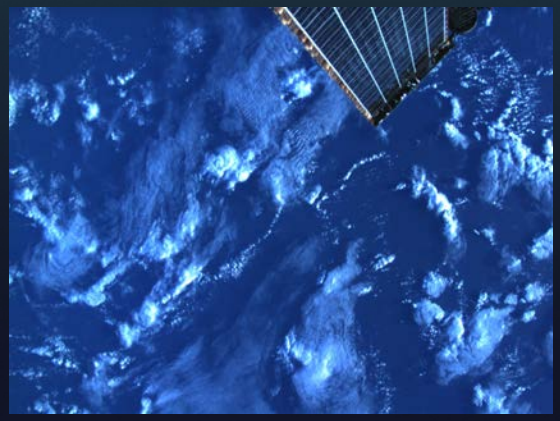


ISE 2.0 Sample Data & Images



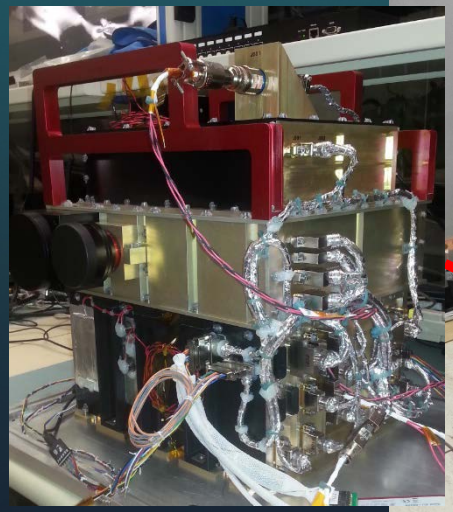






ISEM on STP-H5 ISS Payload

ISEM, SpaceCube Mini



ISEM Stack Includes:
- SpaceCube Mini
- FP Spectrometer
- EHD Pump
- CSP & Camera

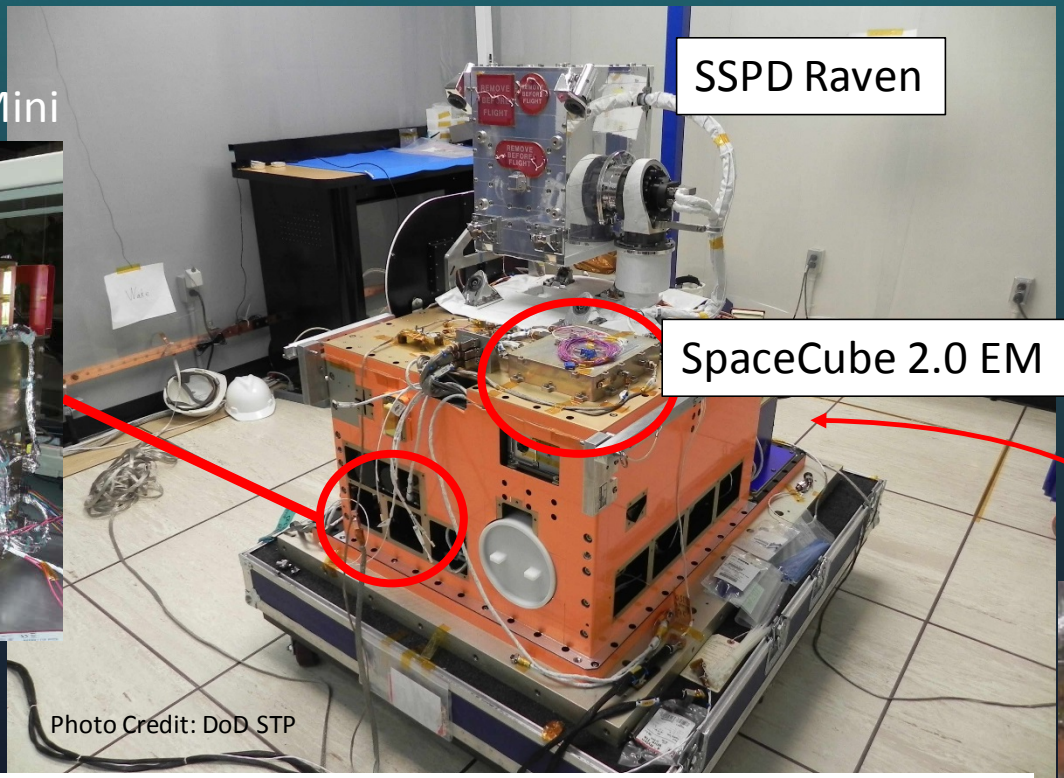


Photo Credit: DoD STP

Raven Suite Includes:
- SpaceCube 2.0
- Visible Camera
- IR Camera
- Lidar

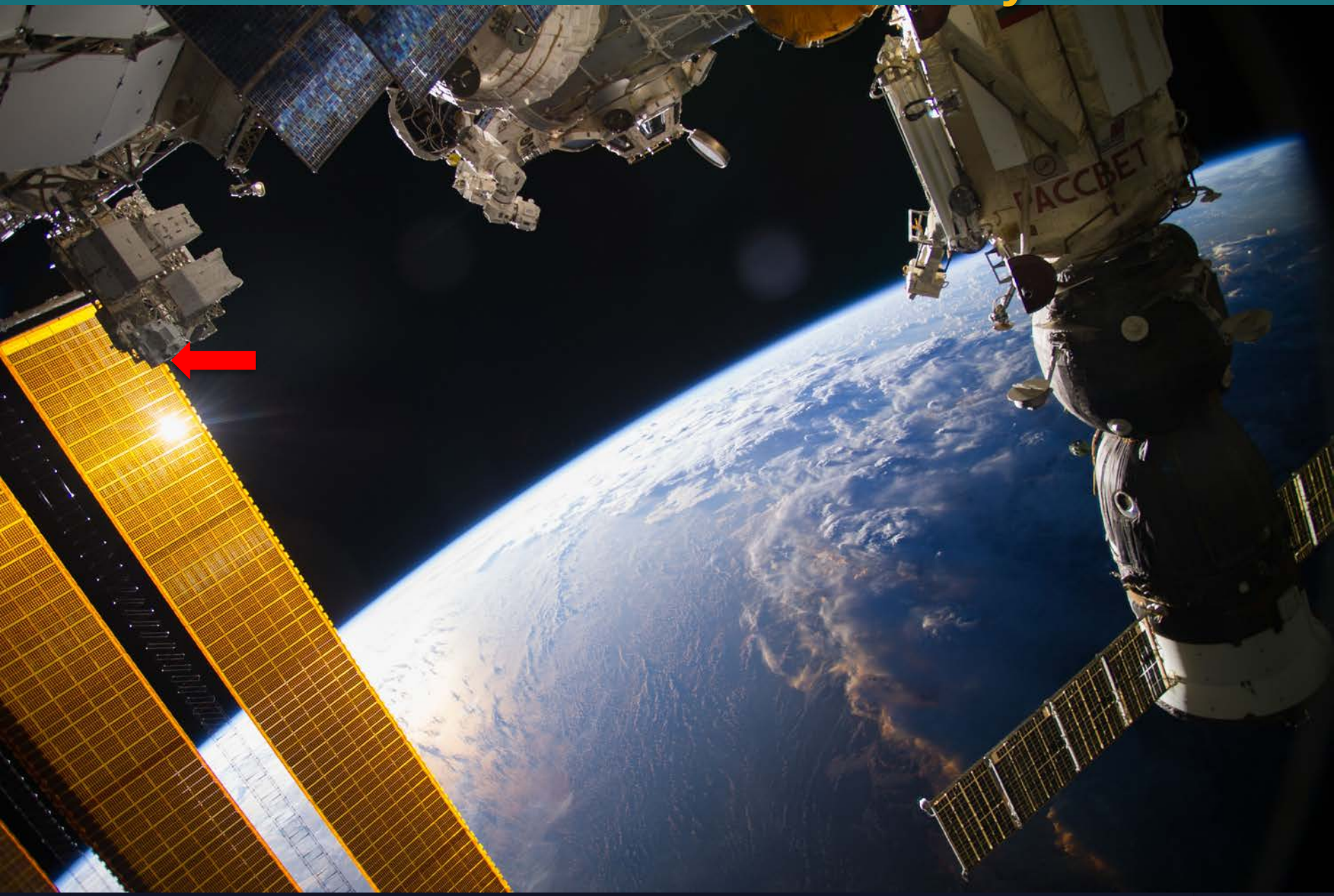
SpaceCube 1.0 CIB



The Space Test Program-H5 (STP-H5) external payload, a complement of 13 unique experiments from seven government agencies, is integrated and flown under the management and direction of the Department of Defense's Space Test Program.

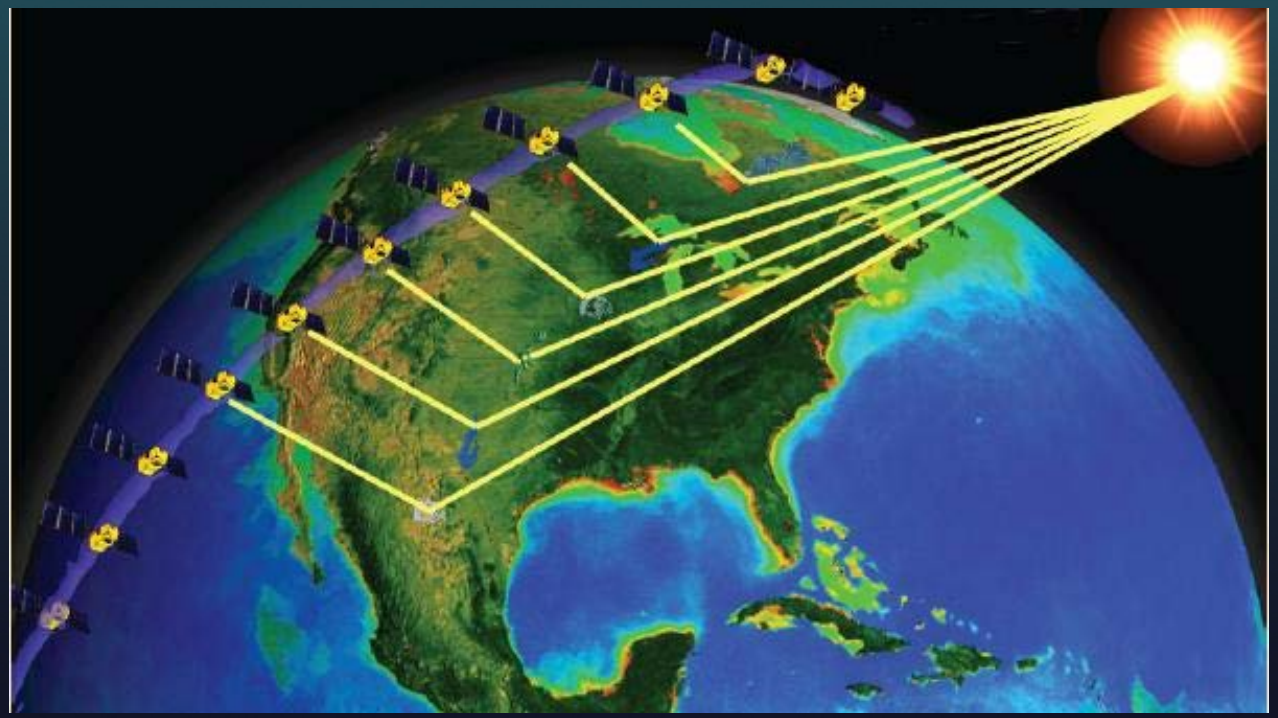
Installed on ISS February 27, 2017

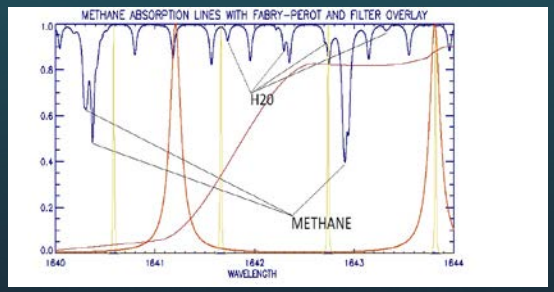
STP-H5 Installed on ISS - February 2017

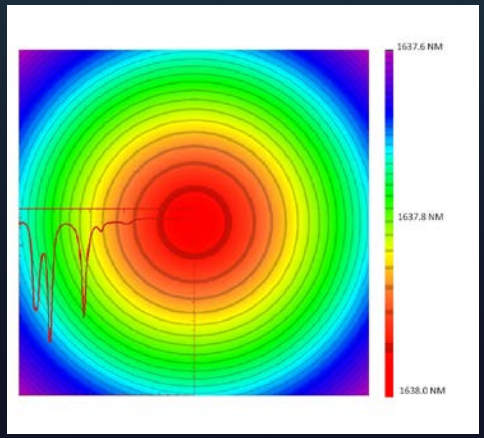


ISEM FPS Science

- Continuous Atmospheric Methane Measurements From ISS
- Fabry-perot Spectrometer Measures Absorption By Atmospheric Gases In Sunlight Reflected Off The Earth
- Demonstrating 900:1 Downlink Data Volume Reduction



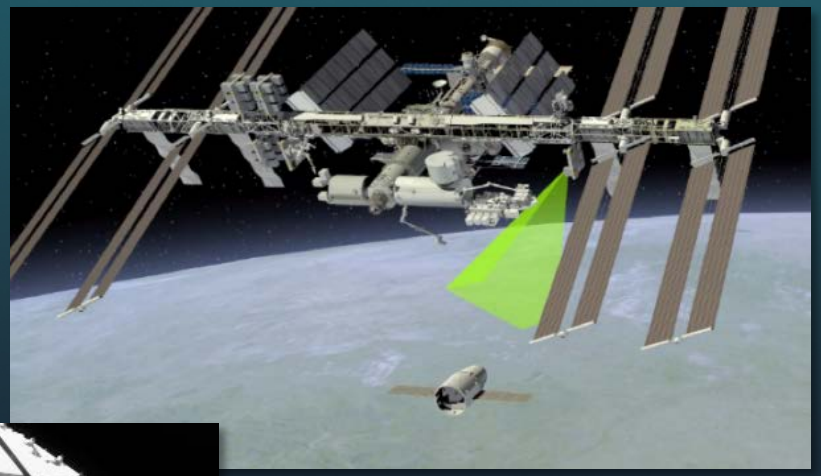




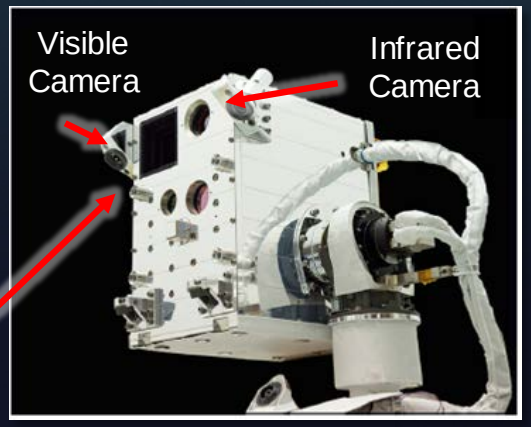
Raven Experiment Overview

Raven is a technology demonstration experiment on the Space Test Program-Houston 5 (STP-H5) payload, launched to the ISS on the SpaceX CRS-10 mission in February, 2017. During its two year mission on ISS, it will advance the state-of-the-art in NASA's relative navigation capabilities.

- Raven contains three sensors (visible, infrared, lidar), a high-performance & reliable computing platform (SpaceCube) and advanced machine vision algorithms
- Raven tracks visiting vehicles to ISS, developing an "off-the-shelf" relative navigation capability for NASA







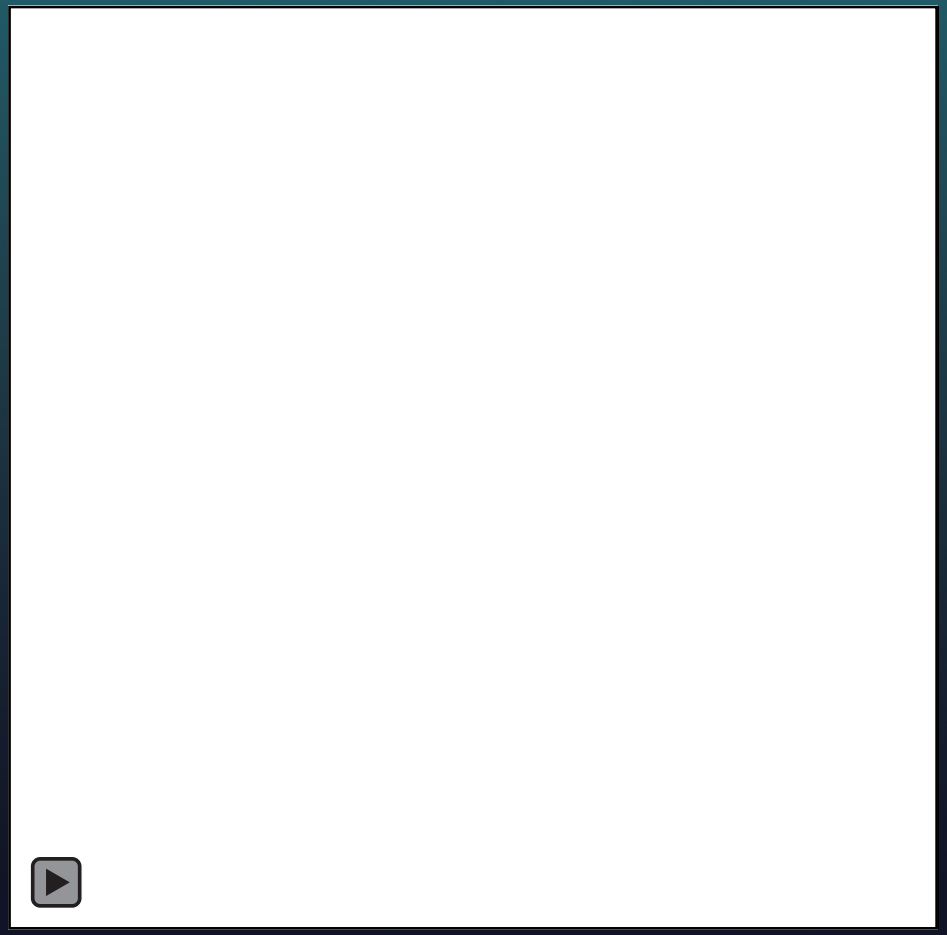
Raven
(Deployed Configuration)

Raven – Sample Data

Raven is currently generating valuable science that is reducing the risk for future NASA missions that require rendezvous and proximity operations systems

Dragon Tracking (VisCam)





Raven demonstrated successful on-board vehicle tracking during SpaceX CRS-10 departure

SpaceCube Evolution and Current Research

SpaceCube Family Overview

1.0





2009 STS-125
2009 MISSE-7
2013 STP-H4
2016 STP-H5
2018 STP-H6

1.5



2012 SMART (ORS)

2.0-EM



2013 STP-H4
2016 STP-H5

2.0-FLT





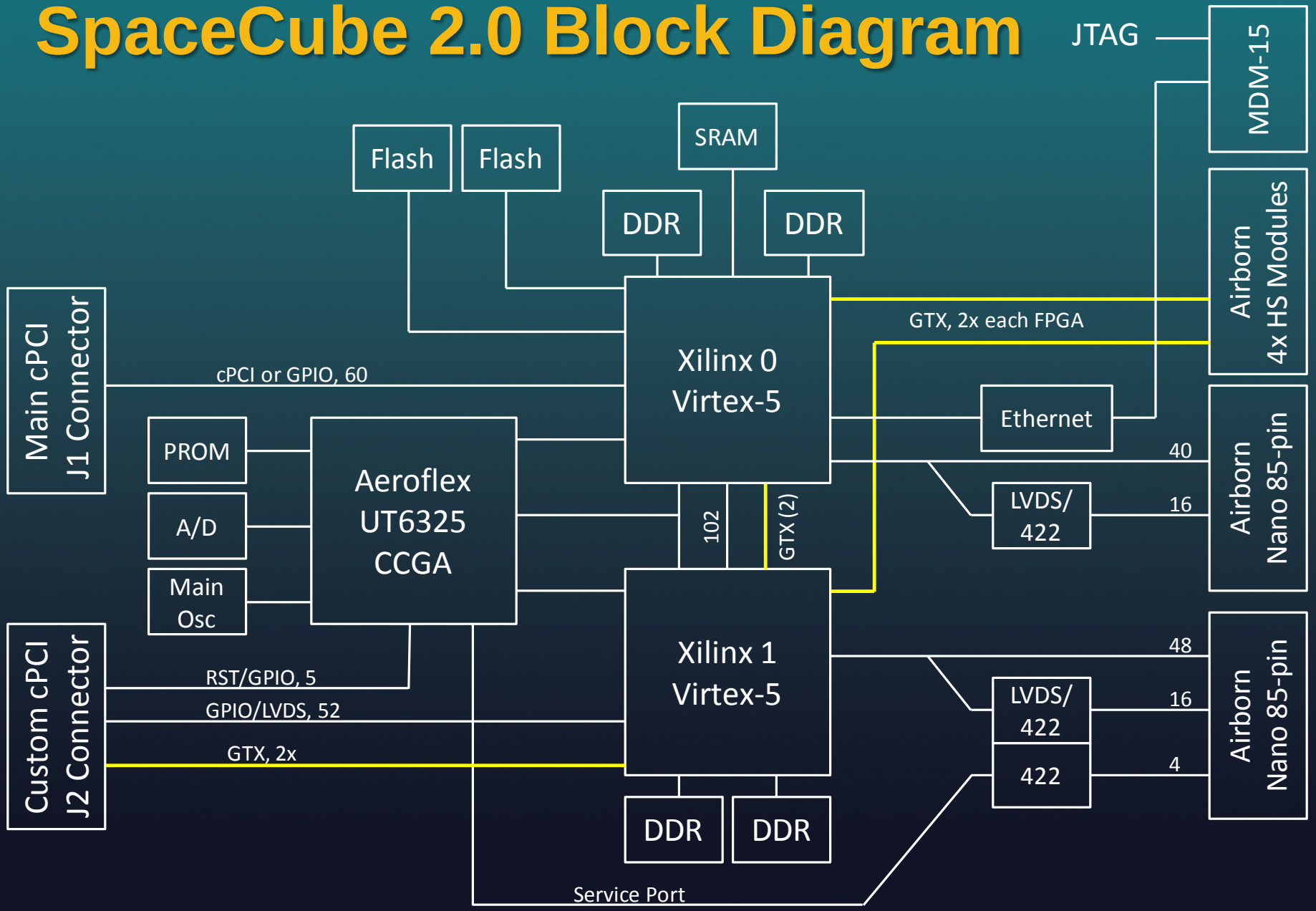
2018 RRM3
2018 STP-H6 (NavCube)
2018 NEODaC
2020 Restore-L
Many NASA proposals

2.0 Mini



2016 STP-H5, UVSC-GEO, Many proposals

SpaceCube 2.0 Block Diagram



SpaceCube 2.0 Highlights



Heritage

- GOAL: close the gap with commercial processors while retaining reliability
- Started in 2006 at GSFC as IR&D
- **42+ Xilinx device-years on orbit**
- 22 Xilinxs in space by 2017
- 8 systems in space by 2018
- Various R&D efforts on hardware acceleration

- Powerful hybrid data processing in a compact 3U size
- Parallel data processing:
  - FPGA + DSP + Processor(s)
- **SpaceCube can move 3,000x more data than a sequential processor per clock cycle**

SpaceCube is a Mission-Enabling Technology

- **Currently TRL-8**
- Leverages 10+ years of design heritage and operation experience
- **$10M+ of NRE**
- Adopted by SSPD for all missions
- **IPC 6012B Class 3/A PWB Reliability**
- Modular: 9 Mission-Unique I/O cards
- **Run-Time Reconfigurable**

Xilinx Virtex-5 FPGA



SpaceCube v2.0



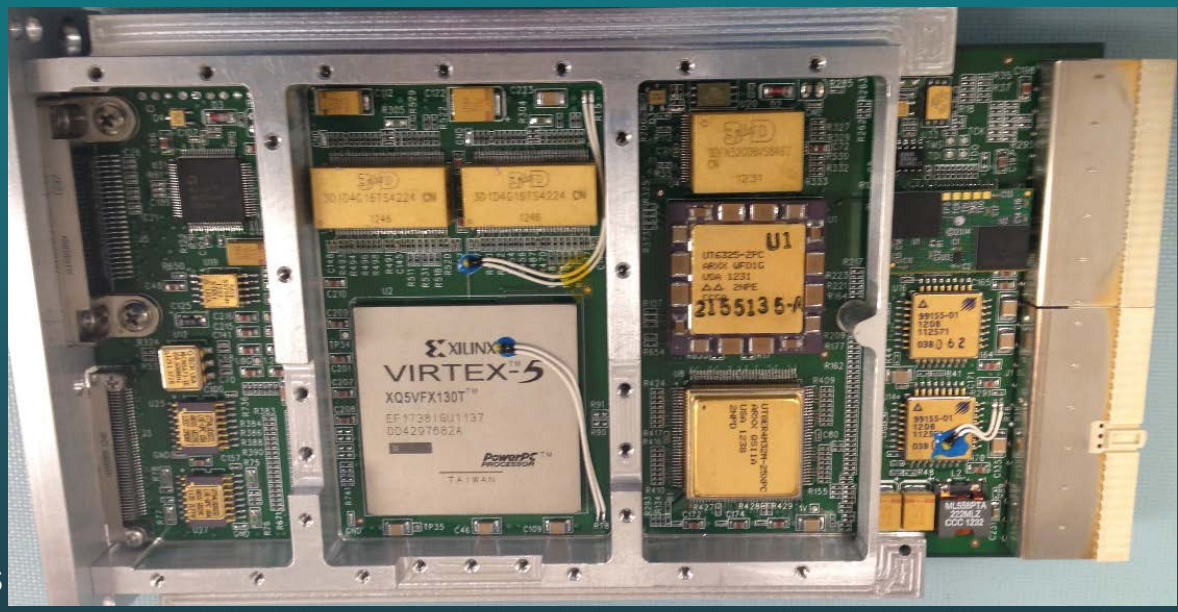
SpaceCube 2.0 Processor Card

Power Draw: 6-15W

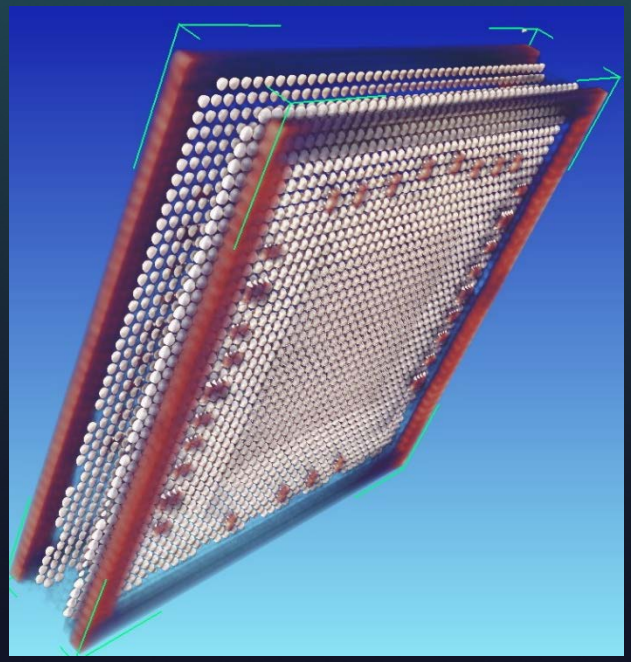
Weight: 0.98-lbs

22 Layers, Via-in-Pad

IPC 6012B Class 3/A



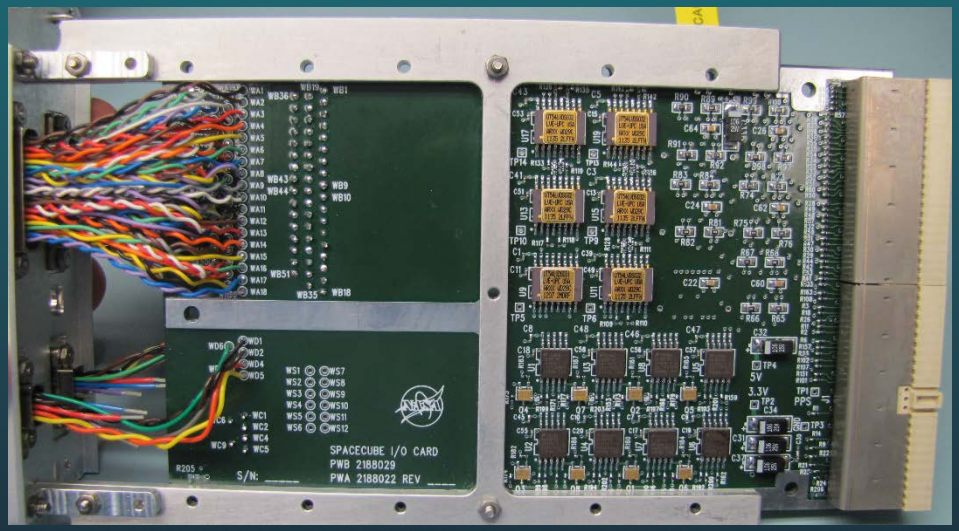
- 2x Xilinx Virtex-5 (QR) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 4x 512MB DDR SDRAM
- 2x 4GB NAND Flash
- 16-channel Analog/Digital circuit for system health
- Optional 10/100 Ethernet interface
- Gigabit interfaces: 4x external, 2x on backplane
- 12x Full-Duplex dedicated differential channels
- 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Mechanical support for heat pipes and stiffener for Xilinx devices



2014 Mentor Graphics "Most innovative design worldwide in the Military/Aerospace sector"

Mission-Unique I/O Card Examples

Restore-L Video/Spacecraft Interface Card



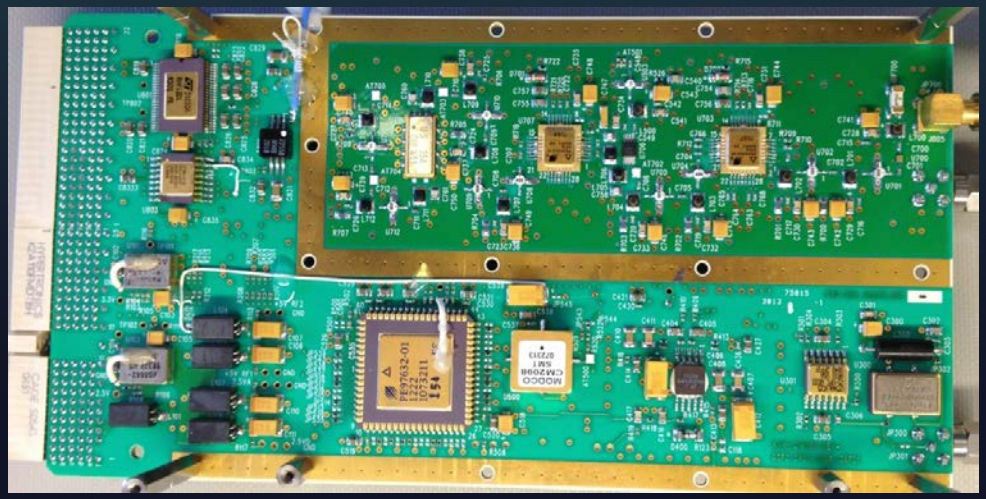
LIDAR Digitizer, Front-End, and Laser Card



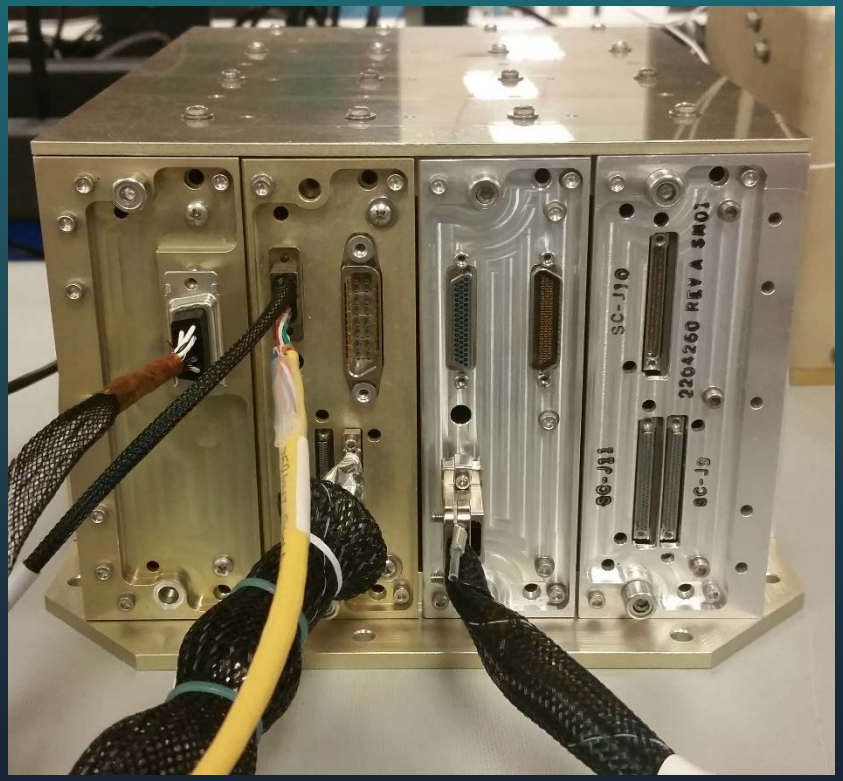




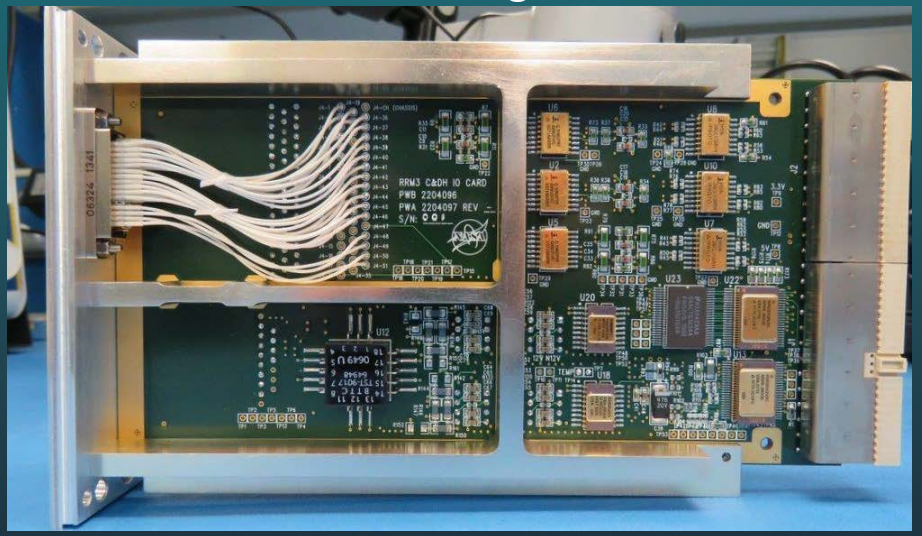
GPS RF Front-End Interface Card



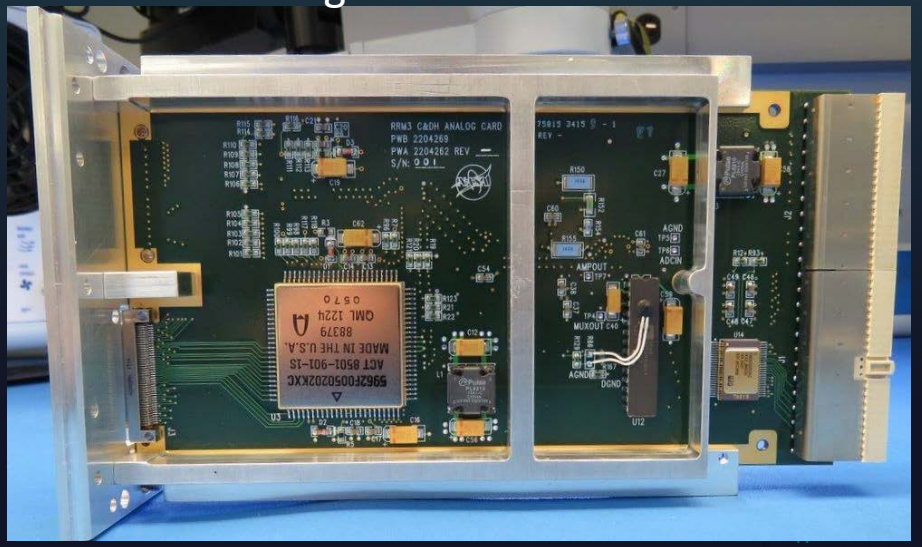
Robotic Refueling Mission 3 SpaceCube



1553/Ethernet/Digital Card



Analog Card

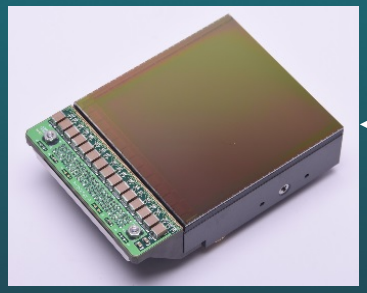


<u>High Level Requirements:</u>

- Interface with ISS and RRM3 instruments:
  - Cameras, thermal imager, motors
- Monitor/Control cryo-cooler and fuel transfer
- Stream video data
- Motor control of robotic tools
- Host Wireless Access Point

NEODaC Instrument Development

8x 3K x 3K detectors



21-ft

> 12 Gbps



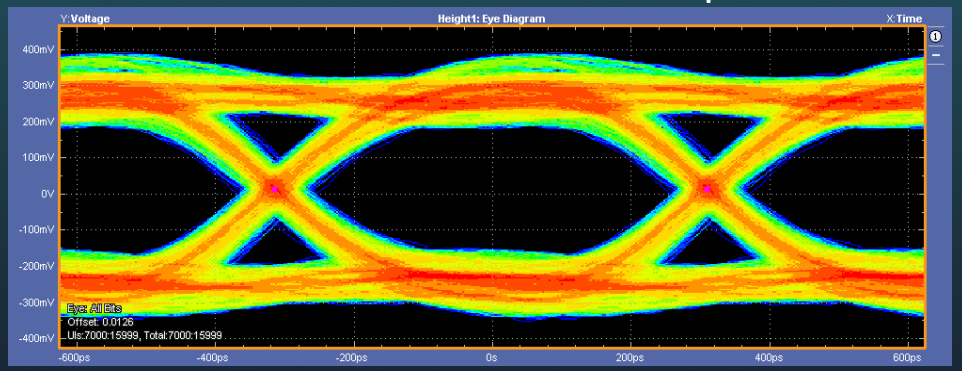
21-ft

8x 1.6Gbps ch.

"HOST"

- Near Earth Objects Detection and Characterization
  - Funded by NASA SMD/Planetary
- SerDes output drivers over 21-ft.
- SpaceCube FPGAs being used to interface with detectors, host on-board data processing applications and compression
- Successful multi-detector readout with SpaceCube completed during TVAC
- Flight system: 8 Processor Cards

Xilinx GTX Driver: 1.6Gbps



SerDes Link Test Results

Transmitter Swing (mV)	Transmitter % Pre-emphasis	Test Duration	Bit Error Count	BER (*)
500	0	6hr	32	9.2E-13
500	8	18hr	0	9.6E-15
800	0	4hr	4	1.7E-13
800	25	20hr	0	8.7E-15
1300	17	20hr	0	8.7E-15
1300	0	19hr	52	4.7E-13

- *Note: BER calculation assumes at least 1 error*
- *58-hours of error-free transmission*

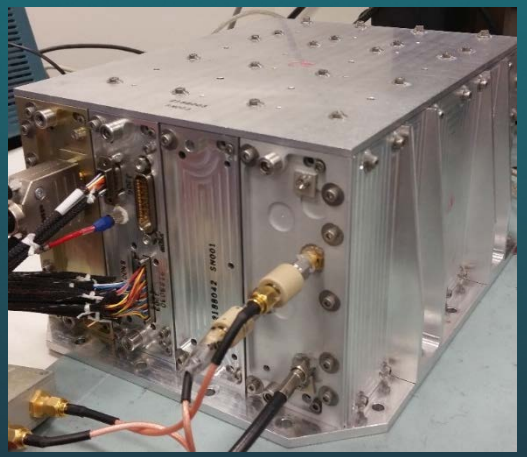
SpaceCube DTN Acceleration

1. FPGA IP Core to Accelerate components of the RFC 5050 Bundle Protocol (BP) Specification
2. Targets
   - SpaceCube 2.0 – Xilinx Virtex 5
   - SpaceCube 3.0 / Mustang – Microsemi RTG4
3. BP Transmission
   - Software Seeds Header Information
   - Hardware Auto Update Values and Encodes Header
   - Payload Data is DMA'd from Memory
   - Theoretical Transmission Rates
     - Virtex 5 w/ 125 Mhz Clock = 3.7 Gb/s
     - RTG4 w/ 50 MHz Clock = 1.5 Gb/s
4. BP Reception
   - Hardware decodes Header
   - Header and Payload Data are DMA'd to Memory

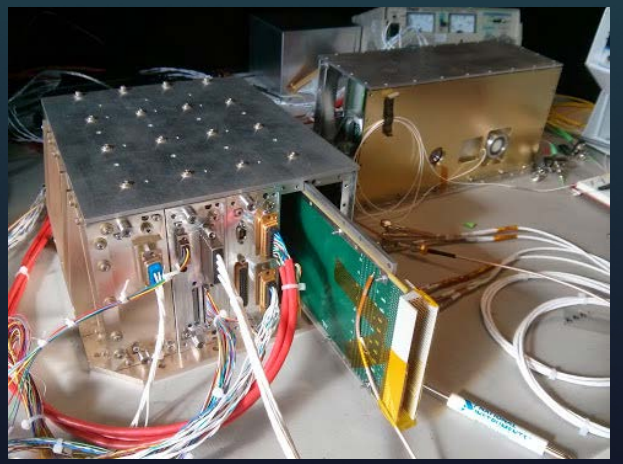
SpaceCube "Spin-offs" and Technology Infusion

9 Mission-Unique SpaceCube I/O Cards in various stages of integration and test

- SSCO Video Distribution Unit
- GRSSLi (Code 590)
- NavCube (Code 590)
- GEDI Digitizer design
- Complex PWB design using 1mm pitch CCGAs
  - TESS, GEDI, Mustang, OSIRIS-REx
- Proposal development
  - CycloPPS (Code 550 and Code 600)
  - DTN (Code 450)
  - DFB (Code 600)
  - Various others
- NICER/GEDI Ethernet Circuitry



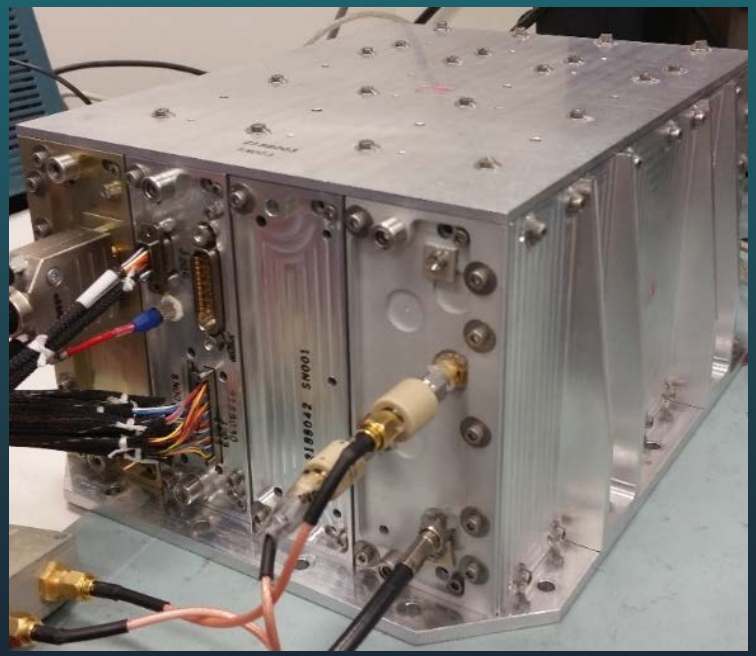
"NavCube"



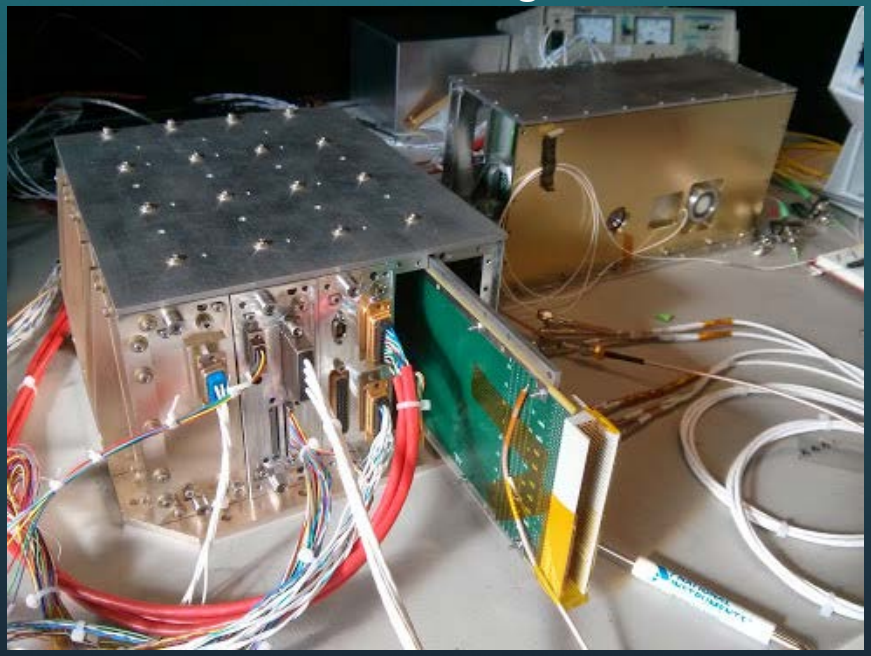
GRSSLi Lidar

Spinoff Technology Results

GPS Receiver – L1/L2C Tracking

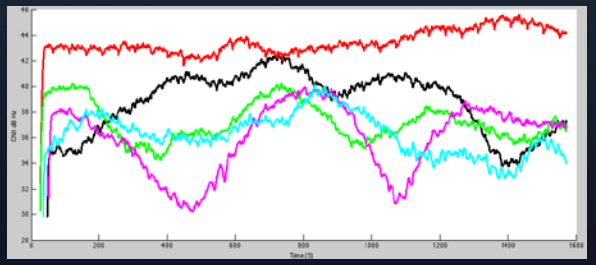


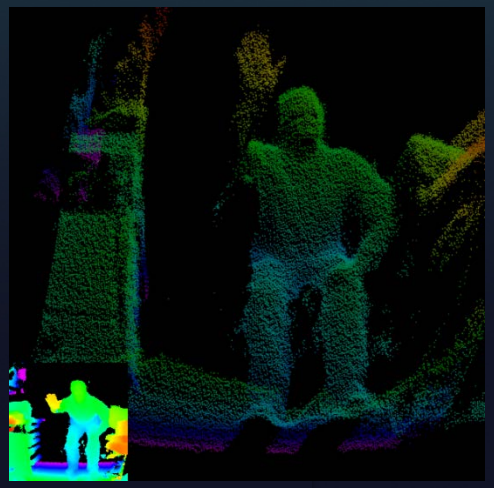
LIDAR Instrument – Configurable Resolution



"NavCube"

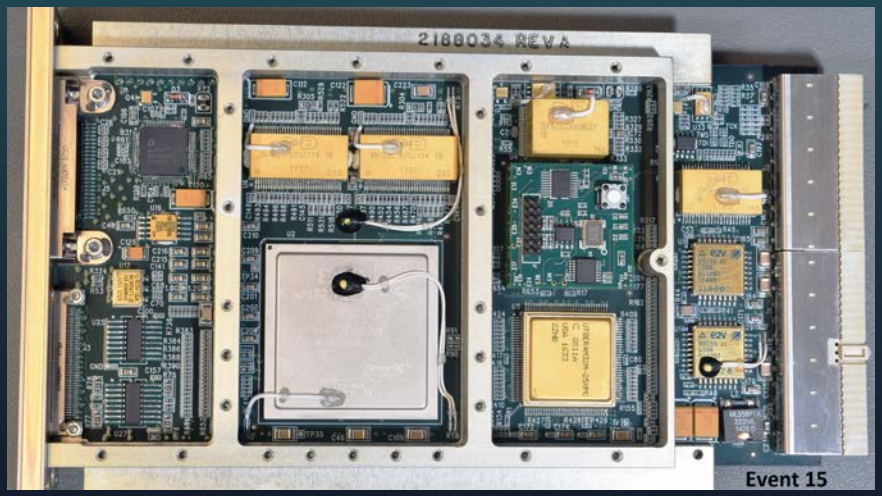
- Port of "World Record Breaking" Navigator technology to SpaceCube
- Full qualification, will fly on STP-H6
- 2016 Goddard Innovation of the Year
- 6 RTAXs → ½ of 1 Virtex 5





SpaceCube Commercialization

- SpaceCube 2.0 → Genesis Engineering Solutions Inc. “GEN6000”
- NSF CHREC Space Processor → Space Micro “Cubesat Space Processor”



GEN6000 Processor



Cubesat Space Processor

SpaceCube Reliability

Background Information

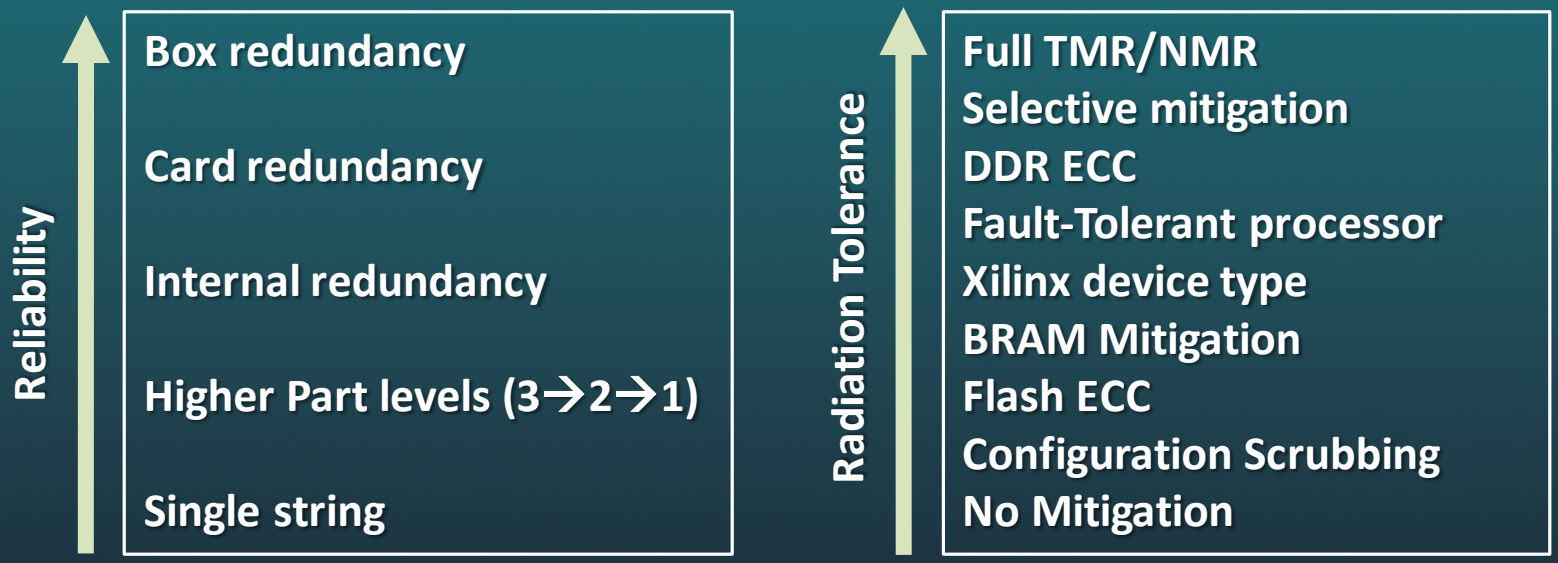
- Base SpaceCube unit consists of Power, Processor, and Backplane cards
- Single string SpaceCube > 99% reliability level per year (per Code 300)
- All parts can be screened to Level 1; implementing Level 2 on Restore-L
- 45+ device-years of on-orbit data shows that > 95% of all unmitigated SEUs are functionally benign
- Multiple levels of reliability and error mitigation steps can be added for mission-critical computing needs
  - Example: a 12 year MTBU embedded system is achievable for a polar orbit (~comparable to Rad750)
- Multiple mission-critical aerospace applications rely on Xilinx FPGAs
  - Examples: SLS main engine controller, commercial crew vehicle, SpaceX Dragon, Iridium constellation, Mars Lander, "other"
- The SpaceCube team has successfully tested and delivered 22 processor cards, 12 power cards, 12 backplanes (i.e. design confidence is high)

Reliability Analysis

Analysis	Status
Parts Stress and De-rating	Complete
Signal/Power Integrity	Complete
Reliability Block Diagram	Complete (specific to Restore-L use)
Worst Case Circuit Analysis	Assessment Complete
FMECA	Complete (specific to Restore-L use)
Radiation TID Analysis	Complete
Radiation SEE Rate Estimation	Complete for Polar, ISS, Mars
Back-to-Back CGA Solder Joint Fatigue	Complete

Test	Status
PWB Coupon Tests	Complete – All PASS IPC 6012B 3/A
Qual TVAC/Vibe per GEVS	Complete - PASS
RRM3 SpaceCube TVAC/Vibe/EMI	Complete - PASS
“Quick-Look” EMI/EMC	Complete - PASS
4x CGA Life Test Articles (-55/+100C)	Ongoing - > 5x MoS factor achieved

Reliability Spectrum (It's your choice)



The systems trades: Computing Performance vs. Radiation Performance (adding levels of radiation tolerance requires some level of resources)

<u>Mission Examples (low end to high end, in order of increasing cost)</u>:

- Tech Demo (Do no harm): ISS, Single string, "EDU" parts, Config scrubbing, Flash ECC, Defense-grade Xilinx using PowerPCs
- Class C: Level 2 parts, some redundancy, DDR ECC, FT processor for critical tasks, selective mitigation
- Class A/B critical function: Level 1 parts, Box redundancy, FT processor, memory EDAC, possibly full TMR

NASA Risk Assessment

Establishing Acceptable SEE Error Rates Using a Risk-based Engineering Analysis Approach

Assessment Process

- Radiation Environment
- Establish Device WCA
- Establish System WCA
- Establish Application WCA
- ID Functional Independence
- Selective FPGA Mitigation

NASA Risk Assessment

Likelihood	Safety Estimated likelihood of Safety event occurrence	Technical Estimated likelihood of not meeting performance requirements
5 Very High	$(P_{SE} > 10^{-1})$	$(P_T > 50\%)$
4 High	$(10^{-2} < P_{SE} \leq 10^{-1})$	$(25\% < P_T \leq 50\%)$
3 Moderate	$(10^{-3} < P_{SE} \leq 10^{-2})$	$(15\% < P_T \leq 25\%)$
2 Low	$(10^{-5} < P_{SE} \leq 10^{-3})$	$(2\% < P_T \leq 15\%)$
1 Very Low	$(10^{-6} < P_{SE} \leq 10^{-5})$	$(0.1\% < P_T \leq 2\%)$

<0.1% = not a credible risk

		100% Device Utilization WCA		Estimated Restore WCA Upset Rates		
Mode	Time (s)	Device WCA	PCC WCA	RPO PCC	RSW PCC	RPO + RSW
one orbit (96 minutes)	5760	0.484%	1.934%	1.074%	0.222%	1.296%
Rendezvous (30 min)	1800	0.151%	0.604%	0.336%	0.069%	0.405%
Capture (77 sec)	77	0.006%	0.026%	0.014%	0.003%	0.017%
Note: assumes BRAM Mitigation						
Note: Actual utilization for RPO and RSW PCCs as of 4/18/2016						
Note: assumes RPO & RSW PCCs must be error-free for full operation						

Single string with no TMR or other mitigation

Flight Tested Mitigation Techniques

- Self-scrubber internally TMR'd on every SpaceCube 1.0 flight mission/demo (STS-125, MISSE, STP-H4, STP-H5, STP-H6) … Total of ~37 device-years in orbit
- MISSE-7 Reed-Muller EDAC memory controller and dual processor configuration where each processor had a time window to report its answer to voting processor … MISSE-7 SpaceCube operated for 7.3 years
- ISE 2.0 Xilinx Virtex-5 FPGA 1 performed self-scrubbing using files stored in NAND Flash memory and configured/scrubbed the configuration memory of Xilinx FPGA 2 and Xilinx FPGA 3. Xilinx FPGA1 counted the number of detected and corrected configuration memory upsets for all 3 FPGAs using the internal CRC Readback feature of the Xilinx configuration controller. FPGA1's configuration file was stored in a rad-hard PROM which configured the FPGA on power up.
- ISEM rad-hard watchdog FPGA performed configuration/scrubbing of the Xilinx Virtex-5 FPGA. The rad-hard FPGA counted the number of detected and corrected configuration memory upsets for the Xilinx FPGA using the internal CRC Readback feature of the Xilinx configuration controller. Robust page-level and file-level redundancy and error detection were used to ensure the configuration files stored in the NAND Flash memory could be reconstructed despite radiation-induced upsets.
- RRM3 boot-up configuration files stored in radiation hardened PROM. Initial boot-up configuration is performed by a rad-hard FPGA. The rad-hard FPGA also monitors watchdog signals from the Xilinx FPGAs and will reconfigure them with the boot-up configuration files if the watchdogs aren't serviced. Multiple redundant flight configuration files are stored in the NAND Flash. Xilinx FPGA1 detects, counts, and corrects upsets on Xilinx FPGA2. Xilinx FPGA2 receives the FPGA1 configuration file from FPGA1 and stores it in local memory. FPGA2 detects, counts, and corrects upsets on FPGA1 so long as the configuration file in local memory remains valid.

*Note: In general, TMR and EDAC is platform agnostic. The mitigation techniques themselves have heritage, and that's what is important.

Mitigation Analysis Example

- In a worst-case GEO environment a Xilinx Virtex-5 PLL has a recoverable error Mean Time Between Upset (MTBU) of 82 years. The Xilinx PLL does not have an error condition that requires a reconfiguration or power cycle.
- The RTG4 PLL rad report for the same orbit (GEO solar-min behind 100mil Al) states a Recoverable error MTBU of 33 years and Error requiring a reset MTBU of 6,850 years
- "Both PLLs are rock solid. As a note, we currently have 15 PLLs in use on the Restore-L payload spread among 5 subsystems. Our Polar environment is about twice as bad as GEO given the proton densities."

FPGA	Recoverable Error MTBU	Error Requiring Reset MTBU
RTG4	33 years	6850 years
Xilinx V5	82 years	N/A

Source Data:
https://www.microsemi.com/document-portal/doc_download/137654-rtg4-pll-and-internal-oscillator-see-report
https://www.xilinx.com/member/space/V5QV-ArchFeatures-SEU-Summary-Report.pdf

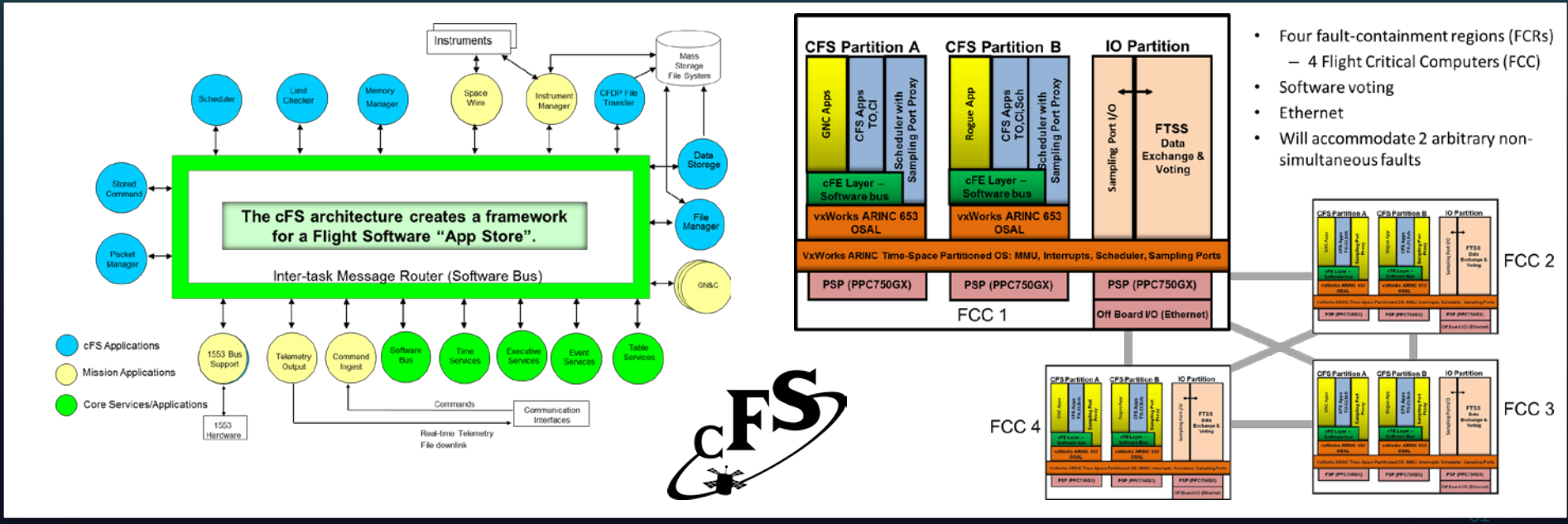
- The SpaceCube processor card can be populated with the space-grade Xilinx devices (QV/SIRF), and critical logic can be TMR'd if need be. A fault tolerant MicroBlaze processor coupled with the rad-hard SRAM yields a core processing system with a MTBU of 13 years, which is comparable to the RAD750.
- A hybrid approach where one Xilinx is rad-hard and the other is defense-grade gives the application access to dual PowePCs 440s capable of 1500 DMIPs each, in addition to the rad-hard FPGA resources

Software Techniques: Application of Time & Space Partitioning for Additional SpaceCube Fault Tolerance

- Combining a mix of rad-hard FPGAs with rad-tolerant FPGAs along with Time and Space partitioning provides additional fault tolerance with minimal impact on system performance
  - Time-Triggered Architecture (TTA)
    - Processing tasks are executed according to a pre-determined schedule
  - Time and Space Partitioning (TSP)
    - Processing tasks are executed according to a pre-determined schedule and isolated in address space such that a task cannot modify another tasks data or code
- Flexible SpaceCube architecture allows a two-sided card with a Space-grade Virtex-5QV FPGA on one side mated with an industrial grade Virtex-5 FPGA on the other
  - Virtex-5QV running MicroBlaze™ processor(s)
  - Virtex-5 with dual 440 Power PC processors
- Software application execution is synchronized to the critical data Input/Output schedule across all processors on a time triggered subnetwork
  - High performance processing is run redundantly and in parallel on 2 or more PPC processors
  - I/O voting and/or agreement algorithms are handled by Virtex-5QV MicroBlaze™ processor(s)
  - On miscompare, Rad-Hard MicroBlaze™ performs fault handling
    - MicroBlaze™ can retain state or checkpoint data for rapid recovery of system
    - MicroBlaze™ can perform safehold algorithms as needed

Software Demonstrations: Examples of Time & Space Partitioning in Fault Tolerant Systems

- Upcoming UVSC/NRL GEO flight experiment on SpaceCube
  - Redundant/parallel data processing synchronized to schedule with outputs voted on by independent processors
  - Hard-Real time performance, fault detection and handling
- Successful NASA/JSC demonstration of quad redundant architecture using NASA Core Flight System (cFS) software architecture (2 fault and byzantine tolerant)
  - Voted signed commands and state exchange over Time-Triggered Ethernet (TTE) subnetwork
  - All application processing synchronized to TTE schedule
  - Hard-Real time performance, fault detection and handling



On-going and Future Work

Restore-L Avionics



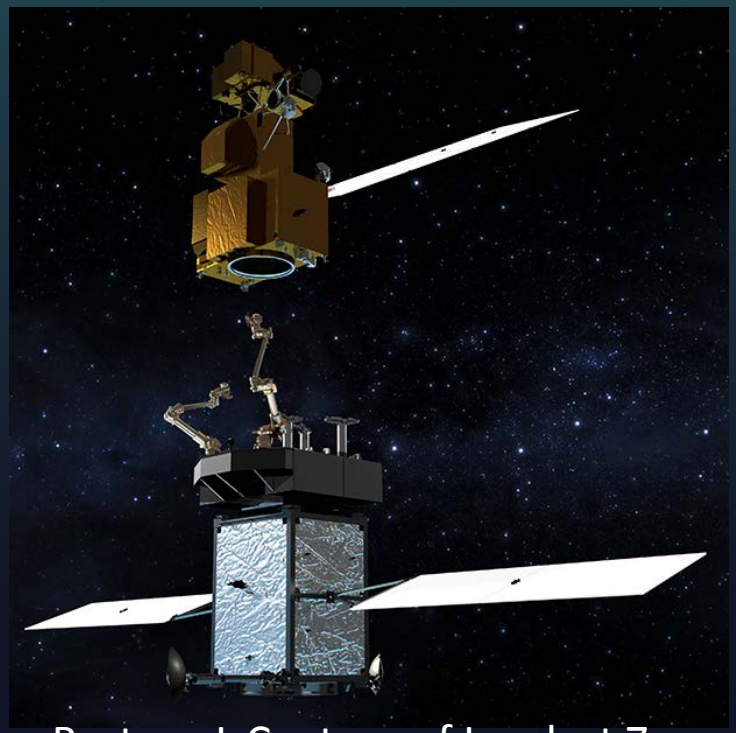
Restore-L Dual SpaceCube Payload Control Computers

High Level Requirements:

- Interface with Spacecraft and Payload Busses
- Interface with vision sensors
- Host Relative Proximity Operations application
- Host Robotic Manipulation Control application



Restore-L will fly 21 Xilinx Virtex-5 FPGAs

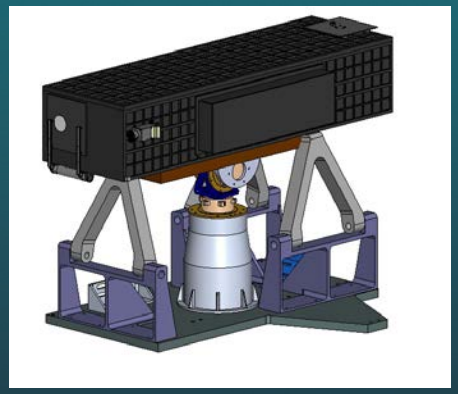


Restore-L Capture of Landsat 7

Restore-L Capture and Refuel Video



Ultraviolet Spectro-Coronagraph Pathfinder



The NRL UVSC Pathfinder combines an ultra-violet spectrograph with a novel, high-throughput coronagraph to search for the presence of suprathermal seed particles near the sun. These particles are believed to be necessary for the production of large solar energetic particle (SEP) events.

- Scheduled to fly in 2019 on STPSat6
- SpaceCube Mini serves as the UVSC instrument processor
- Hybrid high-performance fault-tolerant software architecture
- **First flight of SpaceCube technology in a GEO orbit**

The largest SEP events are thought to be produced when shocks created by fast-moving coronal mass ejections (CMEs) interact with a pre-existing population of seed particles. UVSC will detect the signature of these seed particles by measuring enhancements of the wings of the hydrogen Lyman alpha spectral line. The coronagraph section blocks the solar disk light to allow the corona to be imaged at 1.8 and 3 solar radii, which is the region where CME shocks are first formed.

SEP events disrupt Navy/DoD space operations with little or no warning by damaging critical spacecraft sub-systems. UVSC will demonstrate a **new capability that will extend the warning time for SEP events** and thereby allow time for mitigating the effects of these hazards.

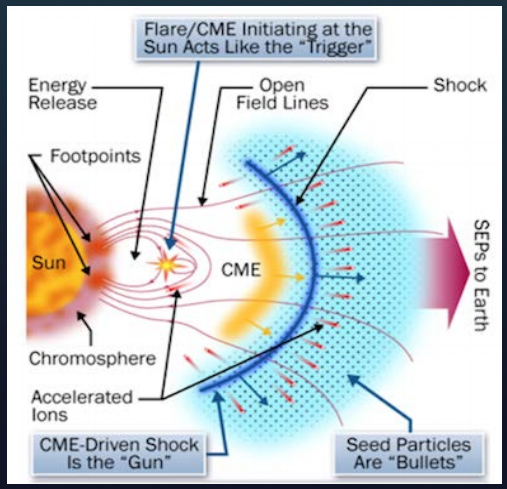
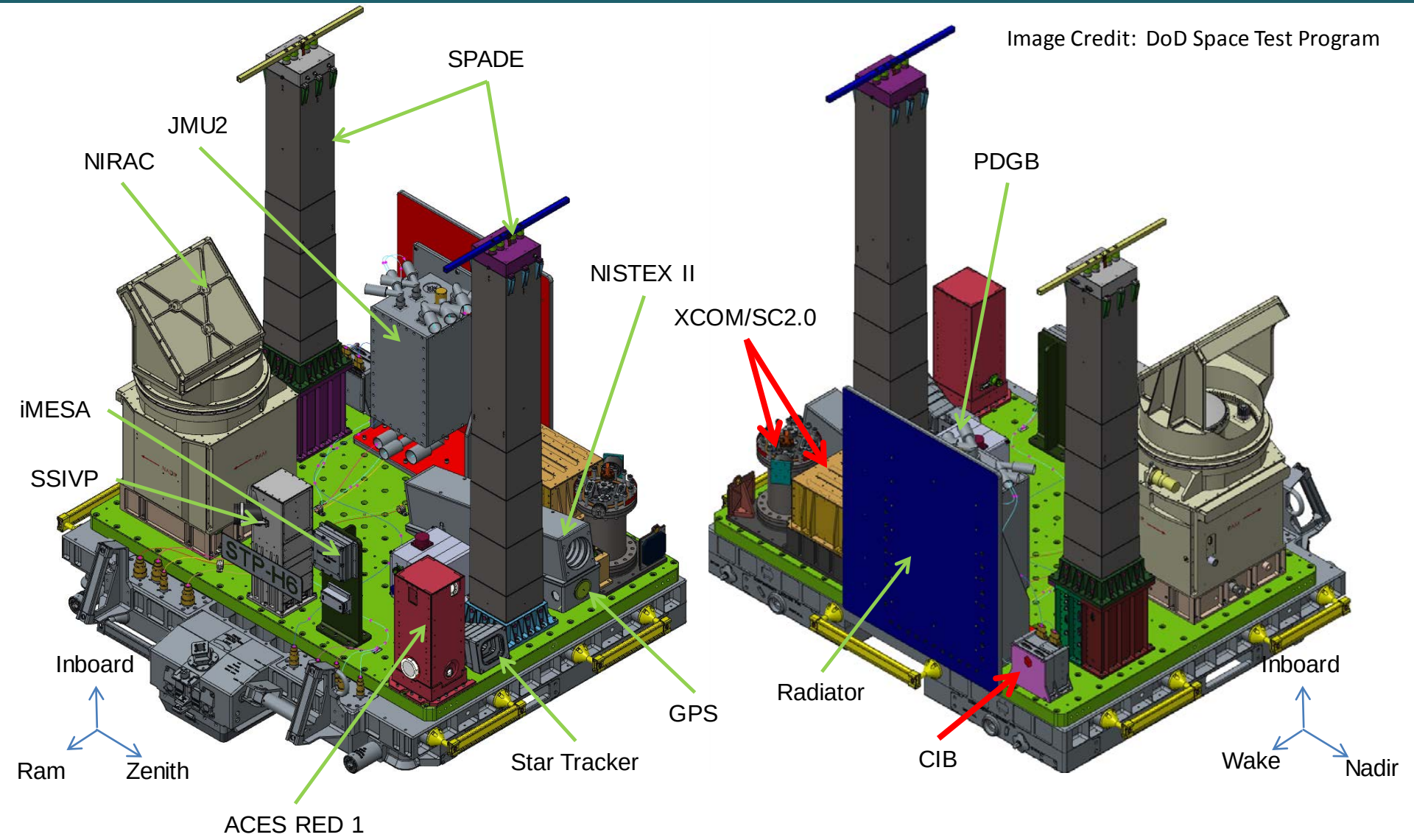
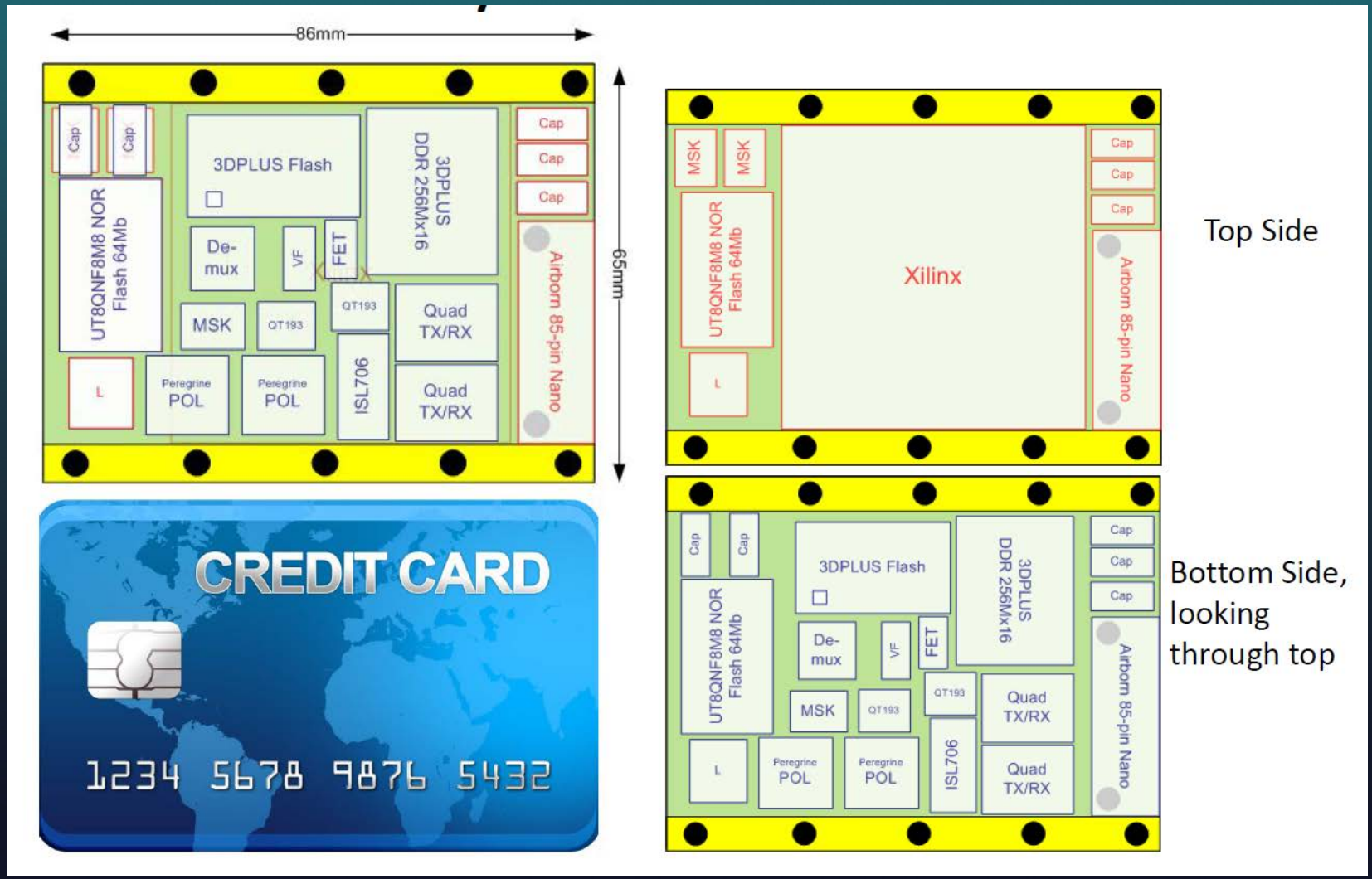


Image Credits: Naval Research Lab

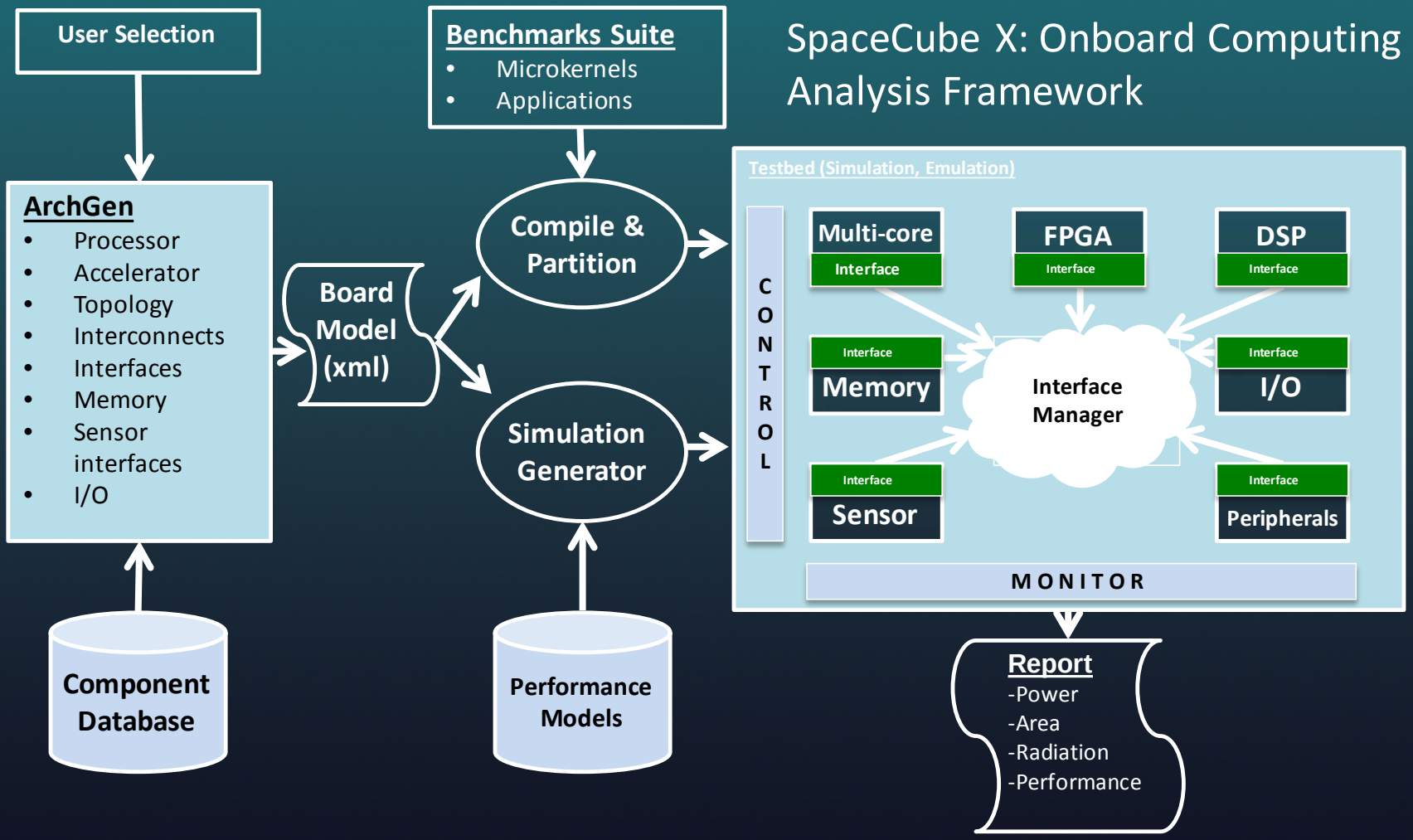
STP-H6 Experiment Pallet



SpaceCube 2.0 Micro

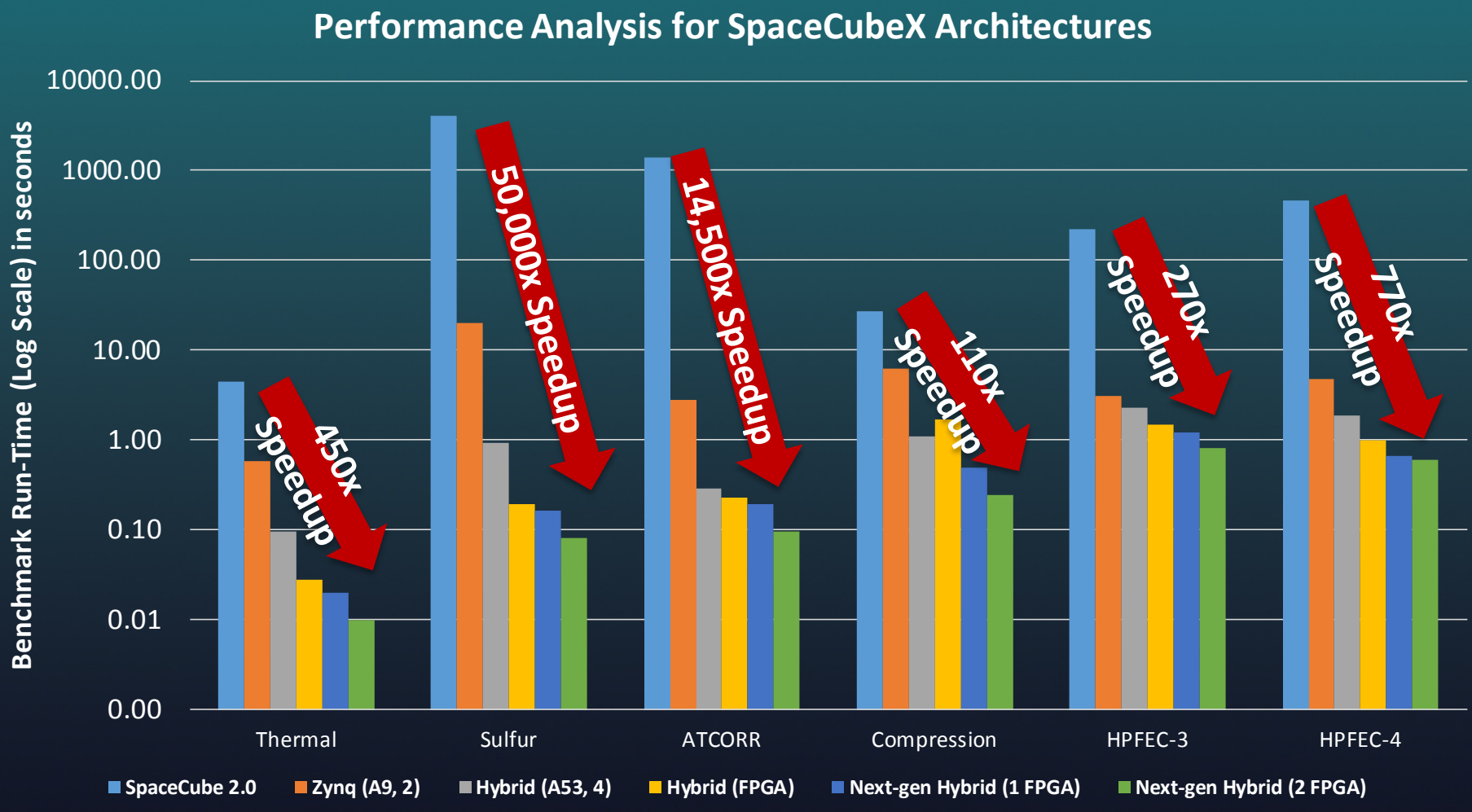


SpaceCubeX End-to-End Framework



End to end tools which enable rapid, accurate exploration of on-board computing architectures

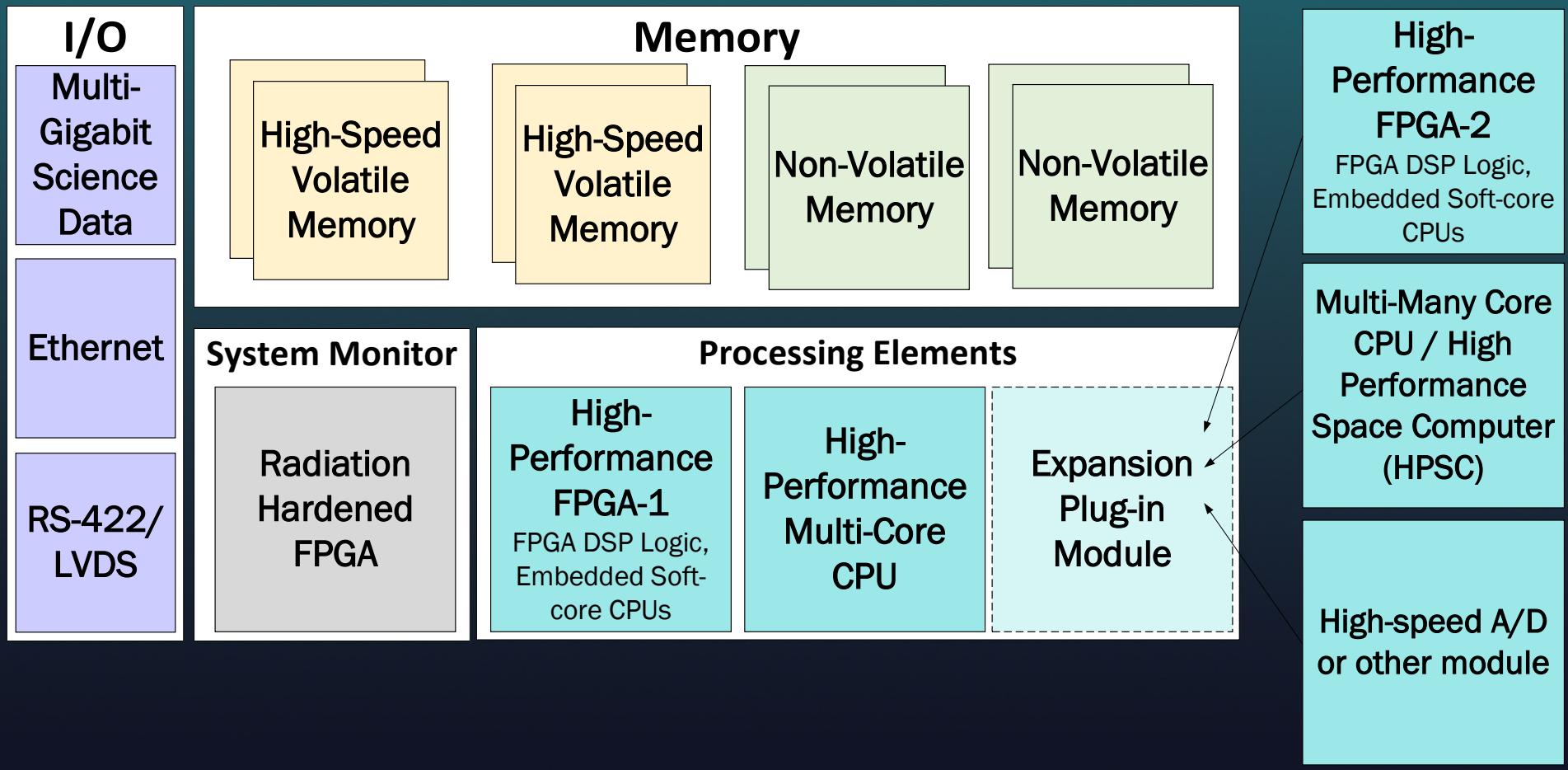
SpaceCubeX: Performance Comparison



Hybrid Multi-Core/FPGA Architectures provides orders of magnitude higher performance

***Simulation performance verified to be accurate within 1%-6% via emulation testing**

SpaceCube 3.0 Architecture



Conclusions

SpaceCube is a MISSION ENABLING technology

- Delivers 10x to 100x on-board computing power
- Cross-cutting (Earth/Space/Planetary/Exploration)
- Being reconfigurable equals BIG SAVINGS
- SpaceCube can be used in all mission applications
  … up to and including Class A
- Past research / missions have proven viability
- Ready for infusion into operational missions

The SpaceCube Team



Thank you! Questions?

tom.flatley@nasa.gov
spacecube.nasa.gov



Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)

Acronyms

A/D	Analog to Digital converter	IR	Infra Red
AGC	Automatic Gain Control	ISE 2.0	ISS SpaceCube Experiment 2.0
ATCORR	Atmospheric Correction	ISEM	ISS SpaceCube Experiment - Mini
CFE/CFS	Core Flight Executive / Core Flight Software	ISS	International Space Station
CHREC	NSF Center for High-performance Reconfigurable Computing	LEO	Low Earth Orbit
CIB	Communications Interface Box	LIDAR	Light Detection and Ranging
CPU	Central Processing Unit	MARDI	Mars Descent Imager
CRS	Cargo Re-Supply	MIPS	Million Instructions Per Second
CSP	CHREC Space Processor	MISSE	Materials on the International Space Station
DEM	Digital Elevation Map	MSL	Mars Science Laboratory
DoD	Department of Defense	NASA	National Aeronautics and Space Administration
DSP	Digital Signal Processor	NEODAC	Near Earth Object Detection And Characterization
EDL	Entry, Descent, Landing	NSF	National Science Foundation
EHD	Electro-Hydro Dynamic	ORS	Operationally Responsive Space
ELC	ISS Express Logistics Carrier	PCB	Printed Circuit Board
EM	Engineering Model	RNS	Relative Navigation System
EMD	Empirical Mode Decomposition	RRM	Robotic Refueling Mission
FPGA	Field Programmable Gate Array	SAR	Synthetic Aperature Radar
FPS	Fabry-Perot Spectrometer	SEP	Solar Energetic Particle
FPU	Floating Point Unit	SM4	HST Servicing Mission 4
GEO	Geosynchronous Orbit	SMART	Small Rocket/Spacecraft Technology
GigE	Gigabit Ethernet	SSPD	NASA GSFC Satellite Servicing Projects Division
GNFIR	Goddard Natural Feature Image Recognition	STMD	NASA Space Technology Mission Directorate
GOES	Geostationary Operational Environmental Satellites	STP	DoD Space Test Program
GSFC	NASA Goddard Space Flight Center	STS	Space Transportation System (Shuttle)
HHT	Hilbert-Huang Transform	TRN	Terrain Relative Navigation
HPFEC	High-Performance Fault-Tolerant Embedded Computing benchmarks	UVSC	Ultra Violet Spectral Chronograph
HPSC	High Performance Space Computer	WFF	NASA Wallops Flight Facility
HST	Hubble Space Telescope		