National Aeronautics and Space Administration

ISSI IS46DR16640B-25DBA25 DDR2 SDRAM Total Ionizing Dose Characterization Test Report

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1. Purpose

The purpose of this testing is to characterize the ISSI IS46DR16640B-25DBA25 parameter degradation for total dose response. This test's purpose is to evaluate and compare lot date codes for sensitivity. In the test, the device is exposed to both low dose and high dose rate (HDR) irradiations using gamma radiation. Device parameters such as leakage currents, quantity of upset bits or addresses, and overall chip and die health are investigated to determine which lot is more robust. These parameters directly affect the functionality of the memory within a system and may determine thresholds necessary to mitigate failure.

2. Test Samples

Two Lot Date Codes (LDC) for the ISSI IS46DR16640B-25DBA25 were provided for testing: 1504 and 1510. The datasheet was the March 2015[1] version. The SDRAM configuration is 64Mx16 (8Mx16x8 banks). More information can be found in Table 1 -

[1] http://www.issi.com/WW/pdf/43-46DR81280B-16640B.pdf

Table 3. A test vehicle for this test is defined as a populated small outline dual inline memory module (SODIMM) which contains eight (8) chip components. The chip components are the devices under test (SODIMM). The chip components were bonded to reworked Samsung SODIMMs which had the same pin-out for the BGA-84 packages. Further, the EEPROM on these SODIMM which contain the serial presence detect (SPD) data was not write protected, which allows test operator to change the module's memory organization which is read back upon initialization of the module prior to test.

Table 1: Part Identification Information

Quantity	Part Number	LDC	REAG#	Package	Vehicles
12	IS46DR16640B-25DBA25	1504	16-015	BGA-84	1.5
12	IS46DR16640B-25DBA25	1510	16-016	BGA-84	1.5

Table 2: SDRAM Address Table

Parameter	Addresses	Total
Row Addressing	A0-A12	13
Column Addressing	A0-A9	10
Bank Addressing	BA0-BA2	3
Pre-charge Addressing	A10	1

Table 3: Clock Cycle Timing

Parameter	-25D	Units
Speed Grade	DDR2-800D	
CL-tRCD-tRP	5-5-5	tCK
tCK(CL=3)	5	ns
tCK(CL=4)	3.75	ns
tCK(CL=5)	2.5	ns
tCK(CL=6)	2.5	ns
tCK(CL=7)	2.5	ns
Frequency (max)	400	MHz

3. General Test Procedure

Radiation testing was performed by exposing the parts to gamma radiation at a dose rate determinant on the maximum anticipated test duration. Each test vehicle either contained components from LDC 1504 or LDC 1510. The SODIMM with a 50% mix of LDC 1504 and 1510 (as noted by the ½ of a test vehicle in Table 1) was used as a control.

Prior to the first radiation dose, all twelve SODIMM were subjected to baseline characterization using the test vehicles.

1. Serial Presence Detect
2. Timing Configuration and Stress Test
3. Electrical Monitoring

The SODIMM was first placed in an SPD reader/writer circuit using a "SODIMM to DIMM riser adapter card". The SPD reader/writer was developed within the Radiation Effects Group at NASA GSFC to interrogate DDR, DDR2 and DDR3 devices assembled on DIMMs. The tool is based on an Arduino microcontroller and utilizes a DIMM riser card of the same DDR type to access the DIMM pins relevant to the EEPROM on the DIMM (VDD, VSS, SDA, SCL, A0, A1, and A2). The software retrieves and parses the SPD data from the EEPROM so that the test operator can confirm the DIMM's organization and change it if necessary. The DDR2 SPD parse is based on JEDEC Standard No. 21-C, Page 4.1.2.10-1, Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3). The SPD tool outputs to a serial console on a Windows computer.

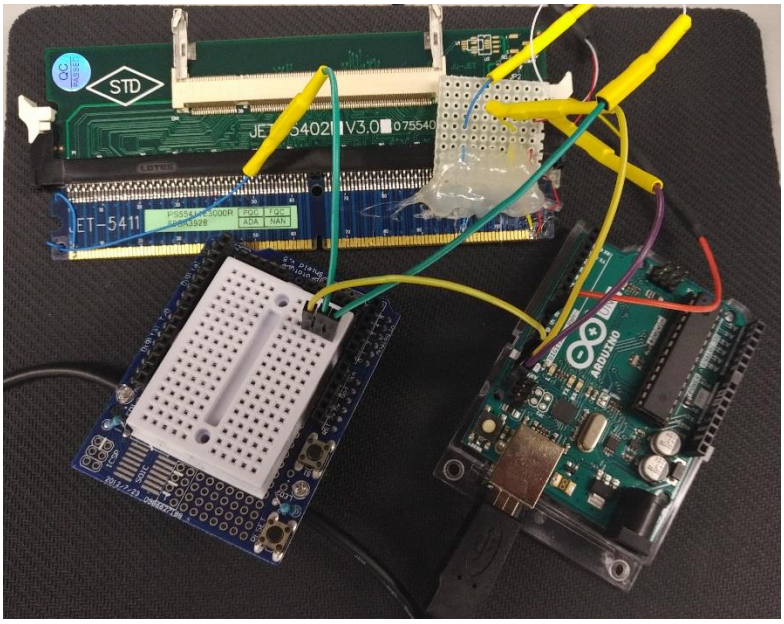

Figure 1: Serial Presence Detect (SPD) Tool

The SODIMM was then placed into a "SODIMM to DIMM riser adapter card" which permits access to the SODIMM using a PowerPC-based Development Reference Board from Freescale/NXP (Intrepid MPC8544DS). A custom DDR controller was developed from version 3 of Kozio's Verification and Test Operating System (VTOS) and customized for use within the Radiation Effects and Analysis Group. This software provides the low-level exercising of the SDRAM components which includes address, burst, noise, and stress testing. The platform software connects to the board via the Freescale CodeWarrior TAP (visible in the back of the image). Figure 2 shows the intrepid development board, the SODIMM adapter with current sense wiring (foreground) and the CodeWarrior tap (background). Figure 3 shows the same setup but with the power monitoring equipment connected.

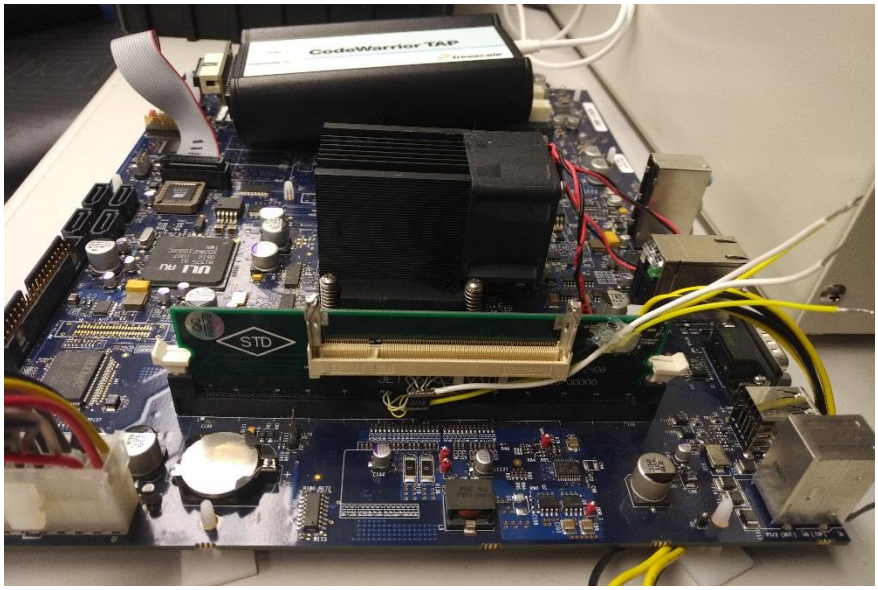

Figure 2: DDR2 Testing System

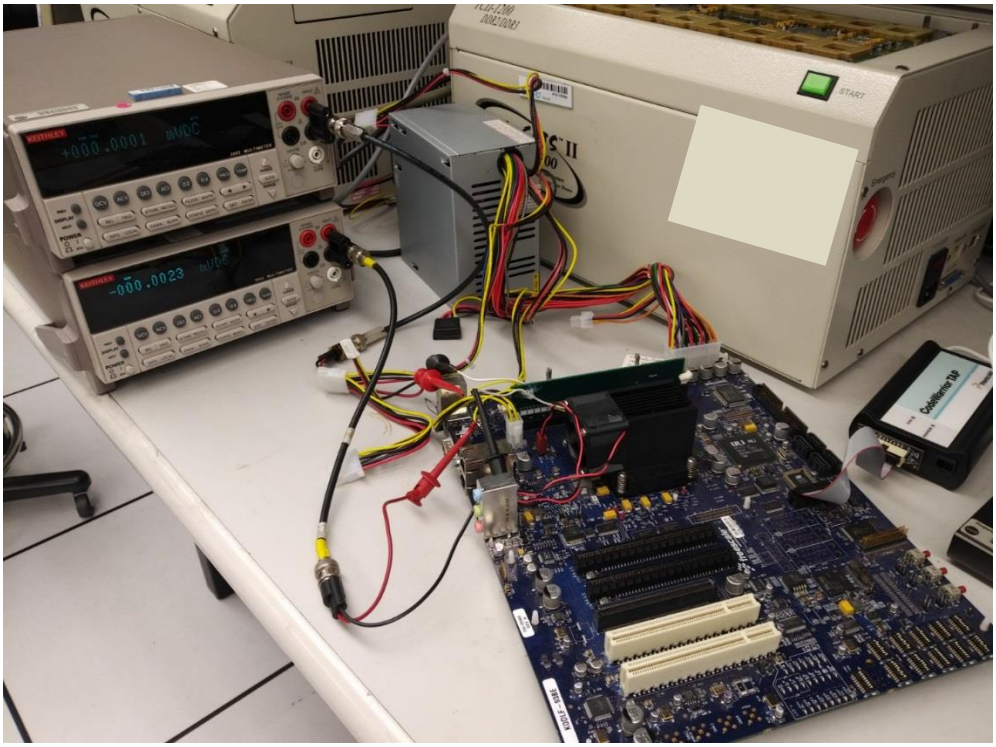

Figure 3: DDR2 Testing System with Power Monitoring Equipment

Electrical monitoring was performed using two Keithley digital multi-meters connected through two 0.01 ohm sense resistors connected to the "SODIMM to DIMM riser adapter card". In this configuration, the development board initializes the hardware, the custom DDR controller initializes the memory itself and the software configuration drives the test profile.

After baseline electrical measurements, the components were subjected to radiation. After each exposure level, the parts were tested again and returned to radiation within the time limits (within 2 hours) defined by MIL-STD-883, Method 1019. All parts were biased during the irradiation steps described in Table 4. Electrical and functional characterization was performed after each radiation dose step.

Table 4: Step-Stress Conditions

Test Levels (krad(Si))	Approximate Radiation Exposure Step Duration
0	-
1	48 seconds
2	48 seconds
5	2 minutes 24 seconds
10	4 minutes 8 seconds
20	8 minutes 16 seconds
40	16 minutes 32 seconds

4. Electrical Tests

Current measurement readings from two digital multi-meters while the devices are under electrical stress were combined and recorded. A sequential set of programmed patterns were utilized to assess the functionality of the SDRAM devices. These are shown within Table 5.

Table 5: List of Electrical Tests Performed

Test Pattern
32-bit Walking 0 Test
32-bit Walking 1 Test
DDR Address Test
DDR Simultaneously Switching Output Test
DDR Bus Noise Test
DDR Full Byte Test
DDR Full Word Test
cache read (32-bit) in MiB/s
cache write (32-bit) in MiB/s

5. Failure Criteria

The parameter limits are defined as those listed in the ISSI IS46DR16640B-25DBA25 datasheet. The current threshold was monitored so that a short, an open or intermittent behavior can be established. If functional failure was observed for any of the stress tests, those results were noted and compared relative to the dosing step, the individual device's previous dose step measurements and within the group of LDC for that device.

6. Source Requirements

The total dose sources is in a room air source gamma ray facility, which is compliant with MIL-STD-883, Method 1019. Dosimetry shall be NIST traceable.

7. Bias Conditions and Fixtures

The SODIMM were soldered to SODIMMs. The biased part configuration was consistent with the 1.8V±0.1V supply voltage from the datasheet.

8. Procedure and Setup

General test procedures are in accordance with MIL-STD-883, Method 1019 Condition D. Parts were serialized randomly. ESD procedures were followed during test and transfer of the devices between irradiation chamber and characterization. Exposures were performed at ambient laboratory temperature. Approximate cumulative test levels were provided by the values in Table 4. All results from the evaluation in Table 5 were recorded.

9. Results

Of the two LDC, there were not significant differences in Data-based Functional Verification over the course of the test to indicate a superior LDC. Consistent from baseline testing prior to irradiation, LDC 1510 had intermittent behavior on its 2nd column (with respect to the 32-bit data interpretation scheme of 0x12345678) when looking at a 32-bit data comparison. This behavior caused a failure during the Random Data Test as seen in Figure 4. This value tended to be one positive hexadecimal digit offset from the expected value. Without a technical deep-dive into the DRAM bit organization and physical construction of the SODIMM circuit board, it is not possible to determine root cause of the behavior.

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SDRAM: Constrained Random Test Suite
Changing memory noise test pattern to 0xb097eaf5
SDRAM: Full burst (32 bit) [00000000_00000000 - 00000000_3fffffff]
Bad value at address 0x00000000_00000000, expected 0x4f68150a, actual 0x1068150a
Bad value at address 0x00000000_00000008, expected 0x4f681502, actual 0x10681502
Bad value at address 0x00000000_00681510, expected 0x4effffa, actual 0x4fffffa
Bad value at address 0x00000000_00681518, expected 0x4effff2, actual 0x4fffff2
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Figure 4: Excerpt from Data-based Functional Verification on LDC 1510

	LDC 1510				LDC 1504			
Dose Step (krad)	Structural	Noise	Random	Performance	Structural	Noise	Random	Performance
0	0.204	6.698	10.196	0.708	0.186	6.718	19.728	0.699
1	0.212	6.698	16.815	0.723	0.210	6.692	19.736	0.678
2	0.215	6.679	16.796	0.686	0.206	6.678	19.735	0.712
5	0.203	6.688	16.794	0.750	0.201	6.669	19.731	0.702
10	0.211	6.679	15.858	0.651	0.216	6.688	19.724	0.649
20	0.216	6.677	10.210	0.647	0.219	6.689	19.727	0.672
40	0.235	6.678	9.234	0.722	0.195	6.709	19.730	0.697
	Data-based Functional Verification Test Duration (Seconds)				Data-based Functional Verification Test Duration (Seconds)			

Figure 5: Test Duration Comparison for Data-based Functional Verification

No significant changes were observed in current measurements over the course of the test for both lots. Of all operation modes, the IDLE current measured the least while the highest current was recorded during the SRUCTURAL CONSTRAINT mode. The initial (pre-rad) IDLE current was 10.8mA for LDC 1504 SODIMM and 13.2mA for LDC 1510 SODIMM and the initial SRUCTURAL CONSTRAINT current was 1.02A and 1.00A for LDC 1504 and LDC 1510, respectively. In comparison, the IDLE current was 10.9mA for LDC 1504 and 13.3mA for LDC 1510 after 40Krad irradiation. The current during the SRUCTURAL CONSTRAINT mode after the final irradiation was 1.01A for LDC 1504 and 998mA for LDC 1510. The table below shows the current readings for these two modes after each dose step.

Table 6: Current Measurement (A)

Mode	LDC	pre-rad	1Krad	2Krad	5Krad	10Krad	20Krad	40Krad
IDLE	1504	0.0108	0.0108	0.0108	0.0108	0.0108	0.0108	0.0109
	1510	0.0132	0.0133	0.0132	0.0132	0.0132	0.0133	0.0133
STRUCTUAL CONSTRAINT	1504	1.02	1.02	0.997	0.985	1.000	1.000	1.010
	1510	1.00	1.00	0.978	0.981	0.985	0.986	0.988

10. References

[1] ISSI IS46DR16640B-25DBA25. March 2015. http://www.issi.com/WW/pdf/43-46DR81280B-16640B.pdf