Building Reliable Printed Circuit Boards - the Lessons Learned

(Workshop F)

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August 7th, 2018

SAFETY and MISSION ASSURANCE DIRECTORATE Code 300

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Workshop Outline

Section 1: What is reliability and root cause?

Section 2: Overview of failure mechanisms

Section 3: Failure analysis techniques

- **Non-destructive analysis techniques**
- **Destructive analysis**
- **Materials characterization**

Section 4: Summary and closure

Discussions and case studies of actual failures and subsequent analysis.

What is Reliability?

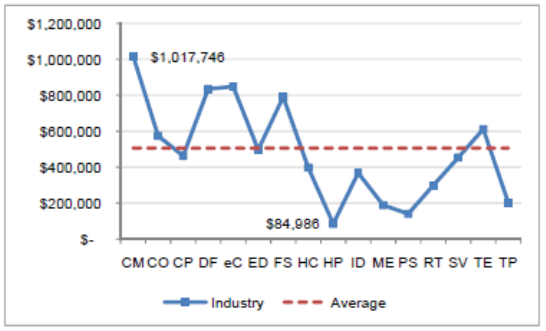
Reliability is the ability of a product to properly function, within specified performance limits, for a specified period of time, under the life cycle application conditions

- Within specified performance limits: A product must function within certain tolerances in order to be reliable.
- For a specified period of time: A product has a useful life during which it is expected to function within specifications.
- Under the life cycle application conditions: Reliability is dependent on the product's life cycle operational and environmental conditions.

When a Product Fails, There Are Costs . . .

- To the Manufacturer
  - Time-to-market can increase
  - Warranty costs can increase
  - Market share can decrease. Failures can stain the reputation of a company, and deter new customers.
  - Claims for damages caused by product failure can increase
- To the Customer
  - Personal injury
  - Loss of mission, service or capacity
  - Cost of repair or replacement
  - Indirect costs, such as increase in insurance, damage to reputation, loss of market share

Cost of a Single Unplanned Data Center Outage Across 16 Industries

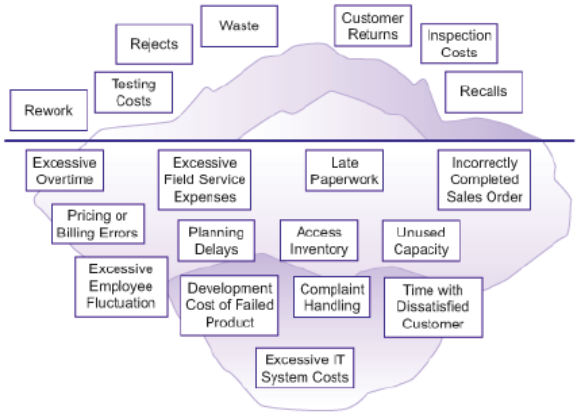


Industry	Code
Communication	CM
Co-location	CO
Consumer	CP
Defense	DF
eCommerce	eC
Education	ED
Financial	FS
Healthcare	HC
Hospitality	HP
Industrial	ID
Media	ME
Public sector	PS
Retail	RT
Services	SV
Technology	TE
Transportation	TP

The average cost of data center downtime across industries was approximately **$5,600 per minute.**

Ref: Ponemon Inst., "Calculating the Cost of Data Center Outages," Feb. 1, 2011.

Iceberg Model of Cost of Poor Quality



Ref: A. Buthmann, "Cost of Quality: Not Only Failure Costs," iSixSigma.

Failure Analysis

Failure Definitions*

Failure……	product no longer performs the intended function
Failure Mode……	change in performance by which a failure is observed (can vary in a system or sub-system context)
Failure Mechanism…..	physical, chemical, thermodynamic or other process that results in failure
Failure Site……	location of the failure
Fault/Defect……	weakness (e.g., crack or void) that can locally accelerate damage accumulation and failure
Load……	application/environmental condition (electrical, thermal, mechanical, chemical...) that can precipitate a failure mechanism
Stress……...	intensity of the applied load at a failure site

** - definitions are piece part, PCB or assembly level*

Classification of Failures

- It is helpful to distinguish between two key classes of failure mechanism:
  - *overstress*: use conditions exceed strength of materials; often sudden and catastrophic
  - *wearout*: accumulation of damage with extended usage or repeated stress
- It is also helpful to recognize early life failures:
  - *infant mortality*: failures occuring early in expected life; should be eliminated through process control, part selection and management, and quality improvement procedures

What Causes Products to Fail?

Generally, failures do not "just happen."

Failures may arise during any of the following stages of a product's life cycle:

- → Product design
- → Manufacturing
- → Assembly
- → Screening
- → Testing
- → Storage
- → Packaging
- → Transportation
- → Installation
- → Operation
- → Maintenance

The damage (failure mode) may not be detected until a later phase of the life cycle.

What is Root Cause Analysis?

Root Cause analysis has four major objectives:

- Verify that a failure occurred;
- Determine the symptom or the apparent way a part has failed (the mode);
- Determine the mechanism and root cause of the failure;
- Recommend corrective and preventative action.

While generally synonymous, "Failure analysis" is commonly understood to include all of this except determination of root cause.

What is a Root Cause?

The root cause is the <u>most basic causal</u> factor or factors that, if corrected or removed, will prevent the recurrence of the situation.*

The purpose of determining the root cause(s) is to fix the problem at its most basic source so it doesn't occur again, even in other products, as opposed to merely fixing a failure symptom. Identifying root causes is the key to preventing similar occurrences in the future.

Ref: ABS Group, Inc., *Root Cause Analysis Handbook, A Guide to Effective Incident Investigation*, ABS Group, Inc., Risk & Reliability Division, Rockville, MD, 1999.

Root Cause Analysis is Different from Troubleshooting

- Troubleshooting is generally employed to eliminate a symptom in a given product, or to identify a failed component in order to effect a repair.
- Root cause analysis is dedicated to finding the fundamental reason why the problem occurred in the first place, to prevent future failures.

From Symptoms to Root Causes

- **Symptoms** are manifestations of a problem; signs indicating that a failure exists.
  - Example: a symptom of printed circuit board failure could be the measurement of open circuits after fabrication.
- **An apparent cause (or immediately visible cause)** is the superficial reason for the failure.
  - Example: the apparent cause of open circuits could be that traces have discontinuities that result in open circuits.
- **Root Cause** is the most basic casual factor(s).
  - Example: the root cause could arise during the manufacturing process if the circuit boards are stacked improperly, resulting in scratches to circuit traces. Another possible root cause could be the presence of contaminants during the copper trace etching process, which resulted in discontinuities in the traces.

Root Cause Analysis

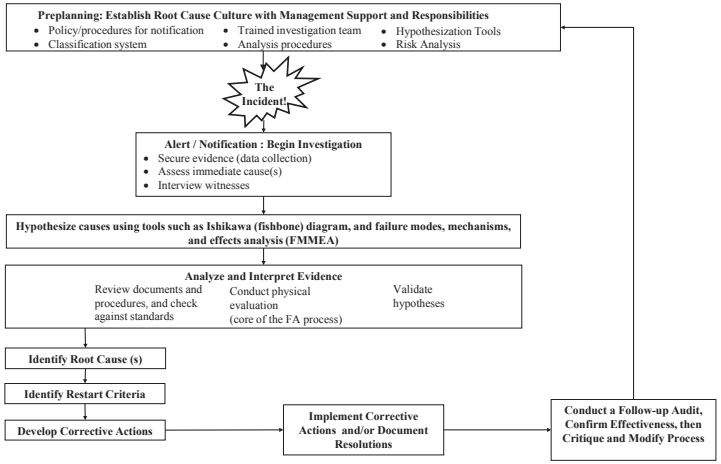
- Root cause analysis is a methodology designed to help:

  1) Describe WHAT happened during a particular occurrence,
  2) Determine HOW it happened, and
  3) Understand WHY it happened.

- Only when one is able to determine WHY an event or failure occurred, will one be able to determine corrective measures, and over time, the root causes identified can be used to target major opportunities for improvement.

- Uncovering ROOT CAUSE may require 7 iterations of "Why?"

Root Cause Analysis Process



Pre-planning

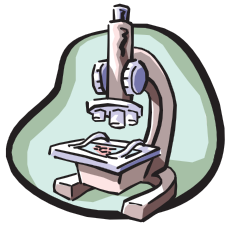
- The objective of preplanning is to establish a root cause culture with management support and responsibilities, through awareness and education, with **notification and investigation procedures and teams that can be activated as soon as an incident occurs**.
- Develop a **classification system of failures**, to aid the documentation of failures and their root-causes, and help identify suitable preventive methods against future incidents.

Pre-planning Activities

- Form a multi-disciplinary team of investigators
  - Complex failures often require *expertise in many disciplines*. For example, a failure may require investigating shipping, handling, assembly and usage processes and conditions.
- Define analysis strategies and procedures:
  - How to notify and report product equipment failure?
  - When to perform root cause analysis (e.g., for every failure? repeated failures? for what type of failures?)
  - What root cause hypothesization techniques (e.g., FMMEA, FTA) are most suited to identify specific failures?
- Provide training in the analysis techniques and their application, to personnel directly involved in root cause investigation.

Data Collection

- The objective of data collection is to **understand the events and the major causal factors** associated with the incident that led to the failure.
- The evidence gathered will be used to identify the critical aspects of failure, including the failure mode, site, and mechanism, time in the life-cycle where failure occurred, length of time required for the failure to initiate, and periodicity of the failure.
- The 5-Ps of data collection:
  - People
  - Physical evidence
  - Position (physical, time-event sequences, functional relationships)
  - Paper (procedures, manuals, logs, e-mails, memos)
  - Paradigms (view of situations and our response to them)
- Data gathering must be performed **as soon as possible after the event occurs** in order to prevent loss or alteration of data that could lead to root cause.
- A huge amount of information is not the goal of data collection. Unrelated data often cause confusion.



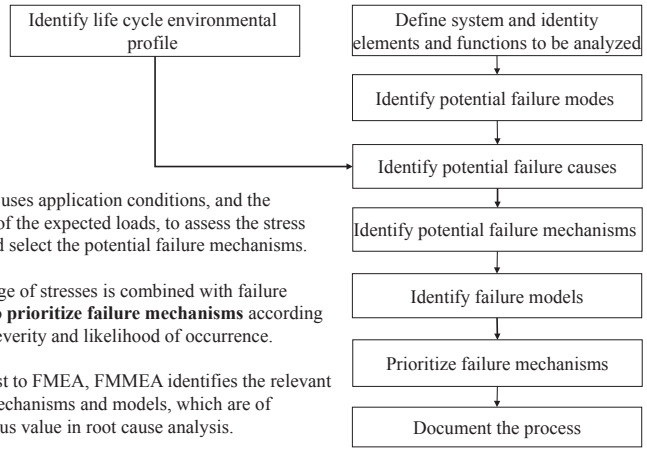
Hypothesizing Causes

Hypothesizing causes is the process of applying knowledge of risks associated with a product's design and life cycle to the data gathered about the failure event, in order to postulate a root cause.

- Tools for hypothesizing causes:
  - Failure modes, mechanisms, and effects analysis (FMMEA)
  - Fault tree analysis (FTA)
  - Cause and effect diagram – Ishikawa diagram (fishbone analysis)
  - Pareto analysis

Tools for Hypothesizing Root Causes

FMMEA Methodology

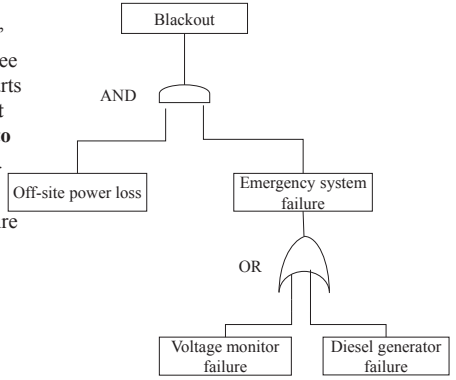


- FMMEA uses application conditions, and the duration of the expected loads, to assess the stress levels and select the potential failure mechanisms.
- Knowledge of stresses is combined with failure models to **prioritize failure mechanisms** according to their severity and likelihood of occurrence.
- In contrast to FMEA, FMMEA identifies the relevant failure mechanisms and models, which are of tremendous value in root cause analysis.

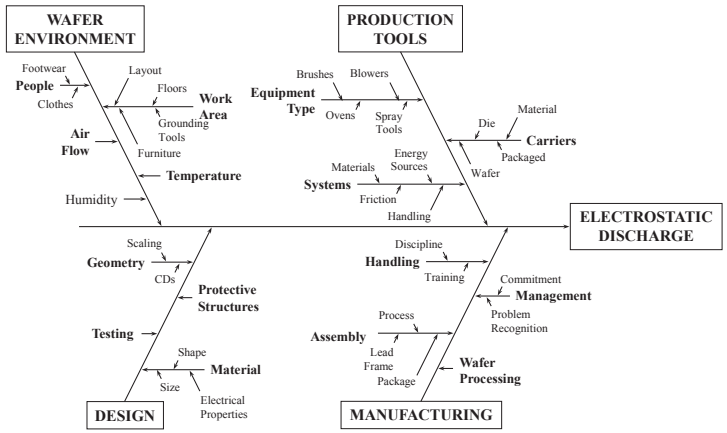
Ref: Mathew, S., et al. "A methodology for assessing the remaining life of electronic products." *International Journal of Performability Engineering* 2.4 (2006): 383-395.

Fault Tree Analysis

- In contrast with the "bottom up" assessment of FMMEA, fault-tree is a "top down" analysis that starts qualitatively to **determine what failure modes can contribute to an undesirable top level event**.
- It aims at developing the structure from which simple logical relationships can be used to express the probabilistic relationships among the various events that lead to the failure of the system.

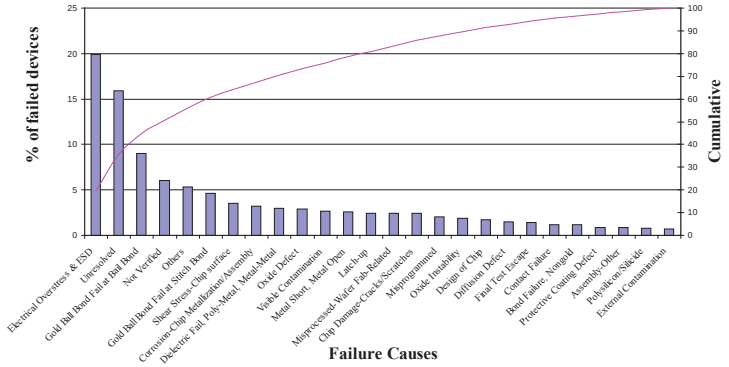


Cause and Effect Diagram



Ref: Pecht, M. G., R. Radojcic, and G. Rao, *Guidebook for Managing Silicon Chip Reliability*, CRC Press, Boca Raton, Florida, 1999.

Pareto Chart Example
- Failure Causes in Electronic Devices -



Ref: Pecht M. and V. Ramappan: "Review of Electronic System and Device Field Failure Returns," *IEEE Transactions on CHMT*, Vol. 15, No. 6, pp. 1160-1164, 1992.

Collecting Supporting Evidence

- Even if a root cause has been hypothesized, additional evidence is often required to assess (i.e., prove or invalidate) the hypotheses formulated.

- Evidence can be gathered by
  - conducting additional interviews,
  - reviewing documents and procedures against standards, and
  - undertaking sample physical evaluation.

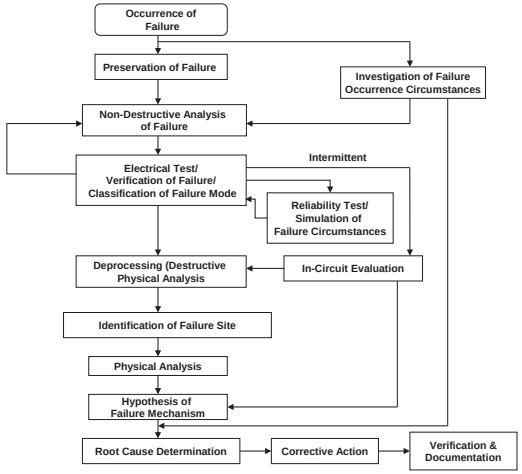
Analysis and Interpretation of Evidence

- Reviewing in-house procedures
  - (e.g., design, manufacturing process, procurement, storage, handling, quality control, maintenance, environmental policy, safety, communication or training procedures)
- against corresponding standards, regulations, or part- and equipment vendor documentation
  - (e.g., part data sheet and application notes, equipment operating and maintenance manuals)
- can help identify causes such as misapplication of equipment, and weakness in a design, process or procedure.
  - Example 1: misapplication of a component could arise from *its use outside the vendor specified operating conditions* (e.g., current, voltage, or temperature).
  - Example 2: equipment (e.g., assembly, rework or inspection equipment) misapplication can result from *uncontrolled modifications or changes* in the operating requirements of the machine.
  - Example 3: a defect may have been introduced due to *misinterpretation* of poorly written assembly instructions.

General Approach Used for Failure Analysis

- The overriding principle of failure analysis is to *start with the least destructive methods and progress to increasingly more destructive techniques*.
- The potential for a nominally non-destructive technique to cause irreversible changes should not be underestimated.
  - For example, the simple act of handling a sample, or measuring a resistance, can cause permanent changes that could complicate analysis further down the line.
- Each sample and failure incidence may require a unique sequence of steps for failure analysis. The process demands an *open mind*, *attention to detail*, and a *methodical approach*.

Example of Failure Analysis Process Flow



Non-Destructive Testing (NDT)

- Visual Inspection
- Optical Microscopy
- X-ray imaging
- X-ray Fluorescence Spectroscopy

- Acoustic microscopy
- Residual gas analysis
- Hermeticity Testing

External Inspection

- Visual inspection of external condition
  - differences from good samples
- Detailed inspection: appearance, composition, damage, contamination, migration, abnormalities
  - Low power microscope
  - High power microscope
  - Scanning electron microscope
  - Surface chemical analysis

Electrical Testing

- Electrical characteristics/performance
- DC test
- Parametrics (current-voltage characteristic)
- Simulated usage conditions
- Electrical probing

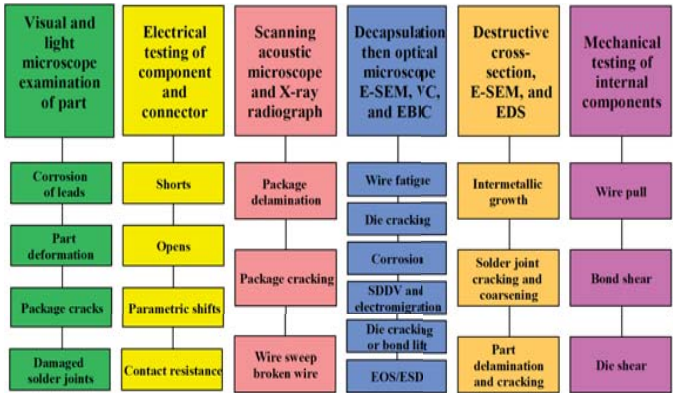
Deprocessing: Destructive Physical Analysis (DPA)

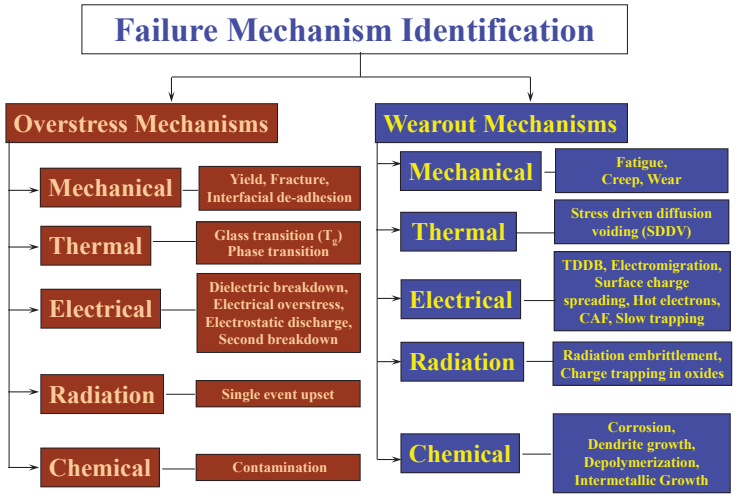
- Modification of specimen in order to reveal internal structures and analyze failure site. May involve:
  - Cross-sectioning and metallography
  - Decapsulation or delidding
  - Residual Gas Analysis for internal gases

Fault Isolation

- Electrical Probing
- Time Domain Reflectometry (TDR)
- Electron Beam Testing
  - electron beam induced current (EBIC),
  - voltage contrast (VC),
  - cathodoluminescence (CL)
- Emission Microscopy
- Scanning Probe Microscopy
- Thermal Analysis

Physical Analysis of Failure Site

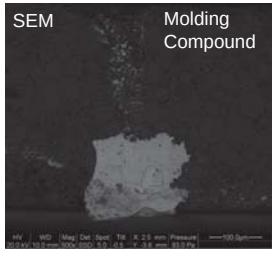


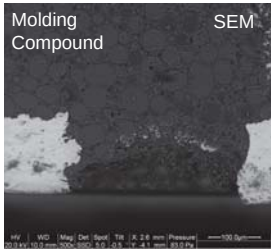


Root Cause Identification

- Testing may be needed to determine the effect of hypothesized factors on the failure.
- A design of experiment (DoE) approach is recommended to incorporate critical parameters and to minimize the number of tests.
- This experimentation can validate a hypothesized root cause.

Discussion 1 – µQFN (micro-leadframe QFN)





What is the failure mode, failure mechanism, root cause and corrective action?

Failure Mechanisms

Review: Failure Definitions

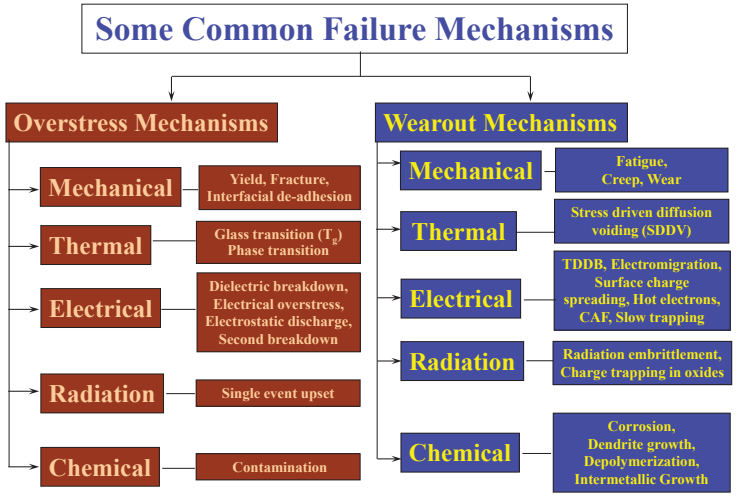
Failure	A product no longer performs the function for which it was intended
Failure Mode	The effect by which a failure is observed.
Failure Site	The location of the failure.
Failure Mechanism	**The physical, chemical, thermodynamic or other process that results in failure.**

In principle, it should be possible to develop a **failure model** for a specific failure mechanism, expressing the likelihood of failure (time-to-failure, probability of failure, strength, etc.) as a function of the stresses and characteristics of the material.

Review: Classification of Failures

Key classes of failure:

- ***overstress*:** use conditions exceed strength of materials; often sudden and catastrophic
- ***wearout*:** accumulation of damage with extended usage or repeated stress
- *infant mortality*: failures early in expected life; typically related to quality issues.



Examples of Failure Models

Failure Mechanism	Failure Sites	Relevant Stresses	Sample Model
Fatigue	Die attach, Wirebond/TAB, Solder leads, Bond pads, Traces, Vias/PTHs, Interfaces	Cyclic Deformations (Δ T, Δ H, Δ V)	Nonlinear Power Law (Coffin-Manson)
Corrosion	Metallizations	M, ΔV, T, chemical	Eyring (Howard)
Electromigration	Metallizations	T, J	Eyring (Black)
Conductive Anodic Filament Formation	Between Metallizations	M, ΔV	Power Law (Rudra)
Stress Driven Diffusion Voiding	Metal Traces	σ, T	Eyring (Okabayashi)
Time Dependent Dielectric Breakdown	Dielectric layers	V, T	Arrhenius (Fowler-Nordheim)

Δ:	Cyclic range	V:	Voltage
Λ:	gradient	M:	Moisture
T:	Temperature	J:	Current density
H:	Humidity	σ:	Stress

When a Product Fails, There Are Costs . . .

- To the Manufacturer
  - Time-to-market can increase
  - Warranty costs can increase
  - Market share can decrease. Failures can stain the reputation of a company, and deter new customers.
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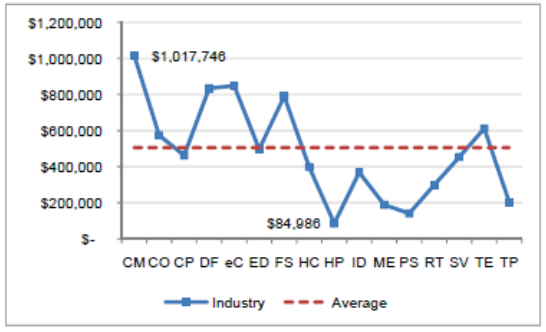
- To the Customer
  - Personal injury
  - Loss of mission, service or capacity
  - Cost of repair or replacement
  - Indirect costs, such as increase in insurance, damage to reputation, loss of market share

From 2002 - 2005, Field Failures of These Devices Amounted to over $10B in Losses

Manufacturer	IC function	Package type	Final product
Motorola	Frequency Synthesizer, etc	Unspecified	Automotive anti lock brake system (ABS)
Philips	Unspecified	80 pin QFP	Quantum, Hard disk drive
Cirrus Logic	HDD controller	208 pin QFP	Fujitsu, Hard disk drive
Infineon	SIPMOS Small-Signal-Transistor	4 pin SOT 223	Unspecified
Fairchild Semiconductor	Low Voltage Buffer Liner Driver	48 pin TSSOP	Seagate
	N-channel MOSFET	Various TSSOPs	HP
Maxim	Unspecified	48 pin TQFP	Sony
Intersil Corp	LSI's for WLAN	20 pin QFN	Unspecified
Conexant	Unspecified	ETQFP	Unspecified
LSA	Unspecified	128 pin TQFP	Unspecified

Cost of a Single Unplanned Data Center Outage Across 16 Industries



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Education	ED
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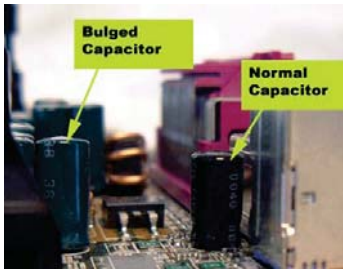
Electrolytic Capacitors : Field Failures

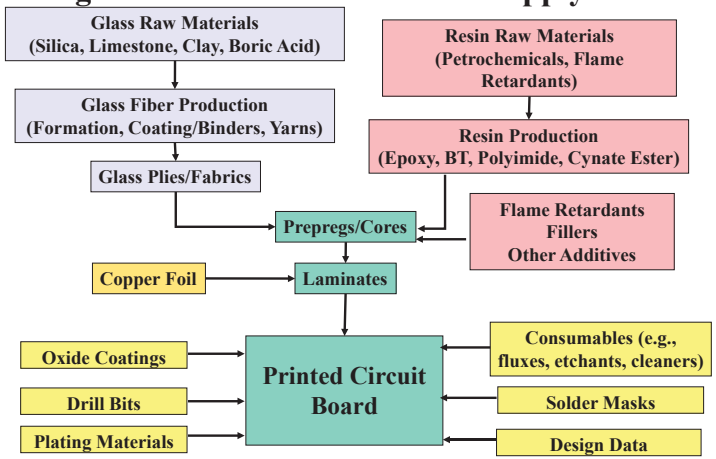
One computer company incurred $300 million financial charges to replace the motherboards having faulty capacitors



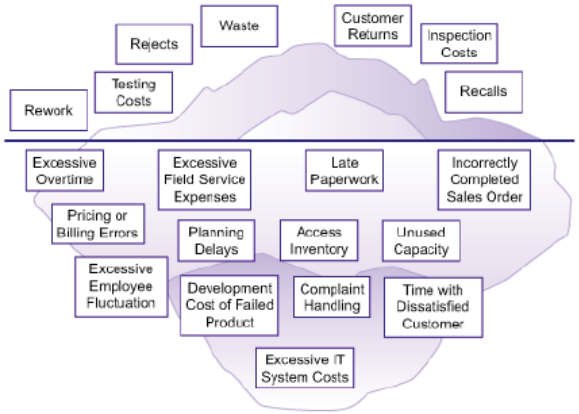
Reliability Requires that we Manage the Supply Chain

- Many companies do not adequately consider quality and reliability in the creation and management of efficient and cost effective supply chains
- Thus, many companies do not know what they are getting and what is changing

Organic Printed Circuit Board Supply Chain



Iceberg Model of Cost of Poor Quality



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Some Failure Related Definitions*

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Stress……..	intensity of the applied load at a failure site

** - definitions are piece part, PCB or assembly level*

PCB Failures – Moisture

- Printed circuit board (PCB) quality, reliability and functionality are highly influenced by moisture (both ambient and internal).
- PCBs witness moisture at various stages:
  - Lamination
  - Assembly
  - Rework
  - Transportation
  - Maintenance
  - Wet process
  - Screening
  - Storage
  - Operation
- Moisture can be initially present in the epoxy glass prepreg, absorbed during the fabrication of PCB or diffuse into PCB during storage
  - Presence effects the mechanical properties (Tg, CTE) and electrical performance.
- PCB handling and storage guidelines are required to prevent inadvertent damage and maintain reliability.

PCB Failures – Process

- The transition to lead-free soldering of printed circuit boards (PCBs) using solder alloys such as Sn/Ag/Cu has resulted in an increase in peak temperature exposures (by 30-40° C) and longer time above liquidus (by 15-30 seconds) during assembly compared with eutectic Sn/Pb solders.
- Rework and repair of assembled circuit boards also contributes to additional high temperature exposures.
- The high temperature exposures associated with lead-free soldering can alter the circuit board laminate material properties and can affect the performance and reliability of the PCB and entire electronic assembly.
- Knowledge of laminate material properties and their dependence on the material constituents, combined with their possible variations due to lead-free soldering exposures is an essential input in the selection of laminates for appropriate applications.

Board Level Failures

Plated Through Hole (PTH)/Via
1. Fatigue cracks in PTH/Via wall
2. Overstress cracks in PTH/Via wall
3. Land corner cracks
4. Openings in PTH/Via wall
5. PTH/Via wall-pad separation

Electrical
6. Electrical overstress (EOS)
7. Signal interruption (EMI)

Board
8. CFF (hollow fiber)
9. CFF (fiber/resin interface)
10. Electrochemical migration
11. Buckling (warp and twist)

Copper Metallization
12. Cracks in internal trace
13. Cracks in surface trace
14. Corrosion of surface trace

Assembly Level Failures

Solder Interconnect

- Poor Solderability/Wettability
  - Tombstoning; Can accelerate other solder failure mechanisms
- Overstress Interconnect Failures
  - Solder Fracture (accelerated by intermetallic formation)
- Wearout Interconnect Failures
  - Solder Fatigue, Solder Creep
- Solder Bridging
- Component Failure due to Handling

Common Failures in Today's PCB

- Initiated at plated through holes (PTHs)
- Initiated by handling (bow and twist)
- Pad cratering (stress)
- Conductive filament formation (CFF)
- Electrochemical migration (PCB cleanliness)

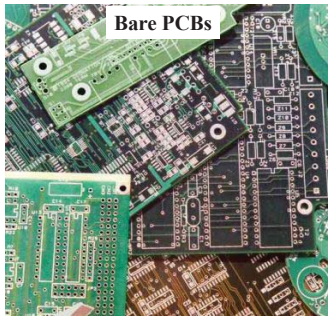
Section - I

Introduction to PCB Technology and PCB Fabrication Materials

Printed Circuit Board

Printed circuit boards are the baseline in electronic packaging – they are the interconnection medium upon which electronic components are formed into electronic systems.

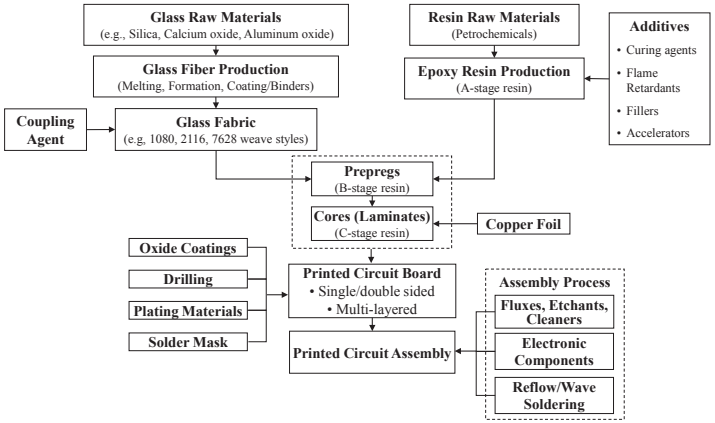
FR-4 PCB materials are glass reinforced PCBs.
- Epoxy resin reinforced with woven glass.
- "FR" stands for flame retardant.



PCB Classification

- PCBs are generally classified based on the following criteria:
  - Dielectric materials used – Epoxy, Bismaleimide Triazine, Cyanate Ester, Polyimide, Polytetraflouroethylene (PTFE), Phenolics, Polyester
  - Reinforcement materials – Glass fabric, Kevlar fabric, PTFE fabric, Paper, Polyethylene terephthalate (polyester), Silicon carbide
  - Circuit type – Digital, Analog, Mixed, RF, Microwave
  - Electronic components – Through-hole, Surface-mount, Mixed-technology
  - Board construction – Single-sided, Double-sided, Multilayer, Flex, Rigid-flex
  - Design complexity – Circuit density, and Low, moderate or high manufacturability
- There are differences in materials, processing steps or both depending on the PCB

Printed Circuit Board Assembly Fabrication



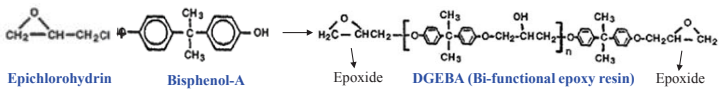
Constituents of FR-4 Laminates

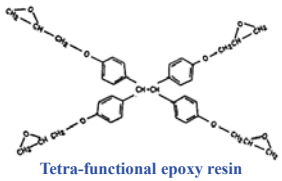
Constituent	Major function (s)	Example material (s)
Reinforcement	Provides mechanical strength and electrical properties	Woven glass (E-grade) fiber
Coupling agent	Bonds inorganic glass with organic resin and transfers stresses across the structure	Organosilanes
Resin	Acts as a binder and load transferring agent	Epoxy (DGEBA)
Curing agent	Enhances linear/cross polymerization in the resin	Dicyandiamide (DICY), Phenol novolac (phenolic)
Flame retardant	Reduces flammability of the laminate	Halogenated (TBBPA), Halogen-free (Phosphorous compounds)
Fillers	Reduces thermal expansion and cost of the laminate	Silica, Aluminum hydroxide
Accelerators	Increases reaction rate, reduces curing temperature, controls cross-link density	Imidazole, Organophosphine

Constituents of FR-4 Laminates

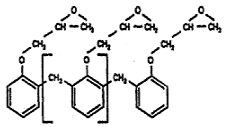
-Resin-

- Diglycidyl Ether of Bisphenol-A (DGEBA) is the epoxy resin used in FR-4 laminates
- DGEBA is derived from the reaction of Epichlorohydrin with Bisphenol-A





Tetra-functional epoxy resin



Multi-functional epoxy resin

- The epoxy groups react in subsequent resin polymerization and result in curing of the resin system

Curing Agents Comparison*

Dicy cured resin system	Phenolic cured resin system
• **Curing agent:** – dicyandiamide – low molecular weight organic compound • **Cured resin system:** – linear aliphatic molecule – These aliphatic bonds can be broken at elevated temperatures and hence dicy cured systems have lower thermal decomposition temperature – The presence of highly polar carbamidine-carbamide bond results in hygroscopic nature (less CAF resistant compared to phenolic systems) – Strong polar nitrogen atom can destabilize brominated epoxy resin at higher temperatures resulting in the increase in bromine content	• **Curing agent:** – phenolic (resin) – high molecular weight organic compound with greater resonating structures (relatively more stable than dicy) • **Cured resin system:** – Aromatic molecule – More stable aromatic bonds and hence higher thermal resistance when compared to dicy systems

* Peng, Y., Qi X., and C. Chrisafides, "The Influence of Curing Systems On Epoxide-based PCB Laminate Performance", Circuit world, Vol. 31, No. 4, pp. 14-20, 2005

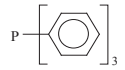
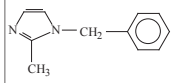
Coupling Agents

- Coupling agents bond inorganic glass fibers to organic epoxy resin
- They take care of high magnitude of shear forces that are established in bonding interface due to a significant difference in the CTE (10X) of glass fibers and epoxy resin, when subjected to high temperatures
- Ex: Organo silanes Y-$(CH_2)_n$-Si $(OX)_3$
  (Y-organo functional group; OX- silicon functional group)

Fillers

Common filler materials	Typical functions
Silica	Reduce cost
Hydrated alumina	Decrease coefficient of thermal expansion
Aluminum Silicate	Improve flammability
Ceramic Zircon	Reduce moisture absorption
Calcium Carbonate	Increase thermal conductivity
Aluminum Powder	Increase compressive yield strength
Mica	Improve arc resistance
Magnesium Silicate	Increase surface hardness
Zirconium Sulphate	Improve thermal shock resistance
	Reduce tensile strength
	Decrease flexural strength and modulus
	Reduce volume resistivity

Accelerators

Type	Characteristics	Chemical Structure
Organophosphine	• Storage stability • Low water absorption • Good acceleration • Good electrical property* • Good heat and humidity resistance	
Imidazole	• High heat resistance • High reactivity • Poor electrical property* • High water absorption • Good acceleration	
Lewis Base Salt	• Good electrical property* • Storage stability • Low water absorption	

* Electrical properties include dielectric constant, dissipation factor, volume resistivity, dielectric strength

Flame Retardants

- FR-4 PCBs, being plastics, are inherently flammable. Flame retardants are added into the resin system to enhance their self-extinguishing property.

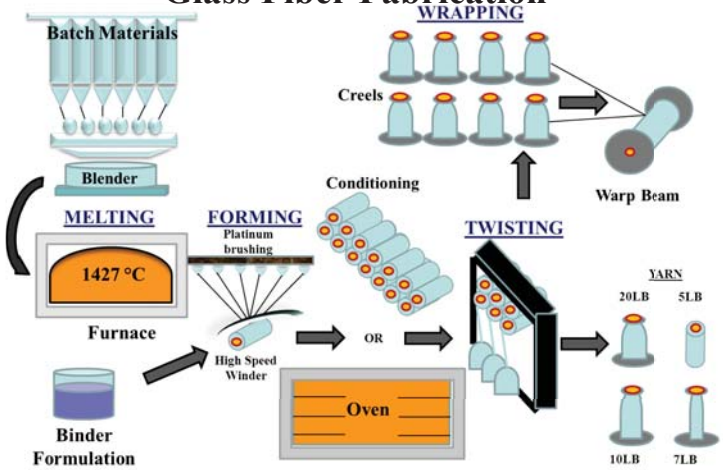
- Typical flame retardants used in PCBs
  - Halogenated flame retardants (Brominated and chlorinated)
  - Inorganic flame retardants [Aluminum trioxide, Magnesium hydroxide, Ammonium polyphosphate, Red phosphorus (elemental phosphorous-polymeric P_n)]
  - Organophosphorus flame retardants (Phosphate esters)
  - Nitrogen-based organic flame retardants

Reinforcement: E-Glass

Typical composition of E-glass:

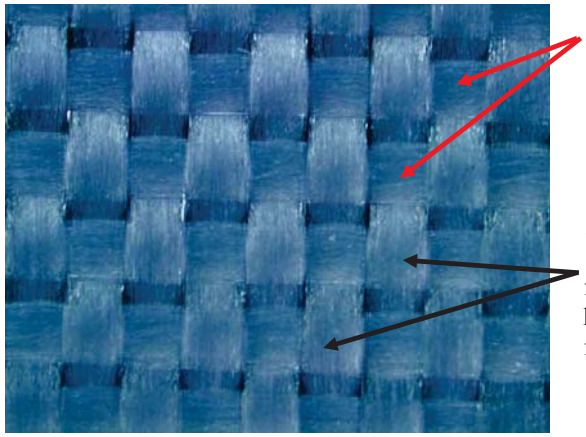
Component	% Composition
• Silicon dioxide (SiO_2)	52-56
• Calcium oxide (CaO_2)	16-25
• Aluminum oxide (Al_2O_3)	12-16
• Boron oxide (B_2O_3)	5-10
• Sodium oxide (Na_2O)+Potassium oxide (K_2O)	0-2
• Magnesium oxide (MgO)	0-5
• Iron oxide (Fe_2O_3)	0.05-0.4
• Titanium oxide (TiO_2)	0-0.8
• Fluorides	0-1

Glass Fiber Fabrication



Lu, Daniel, and C. P. Wong, eds. Materials for advanced packaging. New York: Springer, 2009.

Woven Fiberglass Fabric



The initial set of parallel fiber bundles is known as the warp, and lie in the machine direction

A second set of parallel fiber bundles known as the fill, is woven through the first set

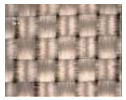
Glass Fabric Styles*

106 Style
Count: 56x56 (ends/in)
Thickness: 0.0015 (in)

1080 Style
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)

2113 Style
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)

2116 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)

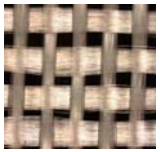


1652 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)

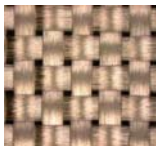
7628 Style
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)

* - Brist and Long, 2009

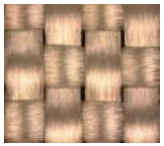
Glass Fabric Styles



1080 Style
Thickness: 63µm
Nominal glass dia.: 5µm

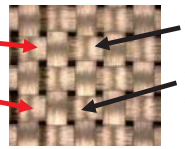


2116 Style
Thickness: 96µm
Nominal glass dia.: 7µm



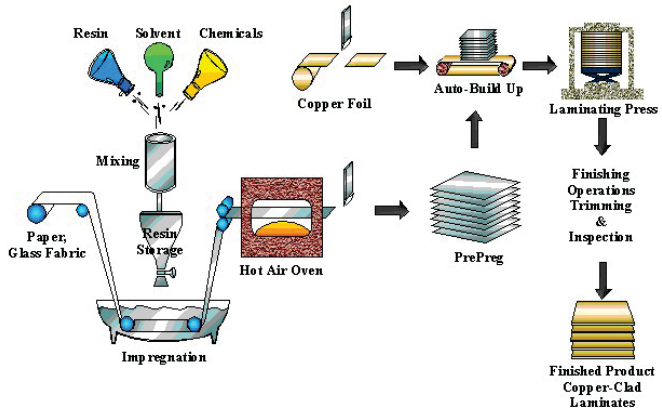
7628 Style
Thickness: 172µm
Nominal glass dia.: 9µm

Initial set of parallel fiber bundles is known as the warp, these lie in the machine direction.



A second set of parallel fiber bundles known as the fill, is woven through the warp bundles.

Laminate Fabrication



Types of PWBs

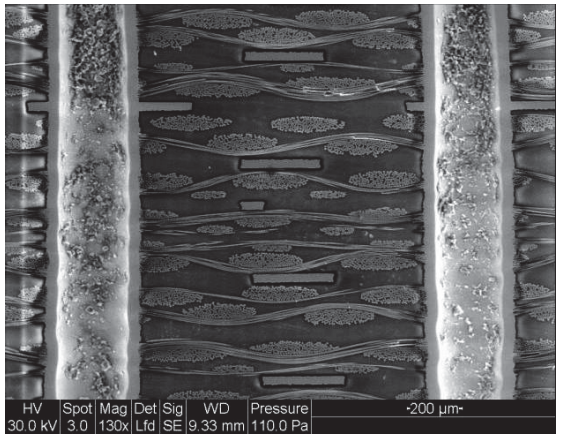
Complexity

- Single sided
- Double sided
- Layer count: Multilayer

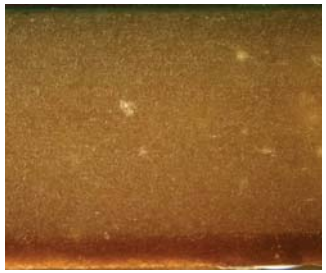
Materials

- Organic
  - FR-1, FR-2, CEM, FR-4, FR-5, BT, Polyimide, CE
- Ceramic
  - Alumina, Glass-Ceramic, Aluminum Nitride
- Silicon

E-SEM View of PCB Cross-section - Woven Fabric



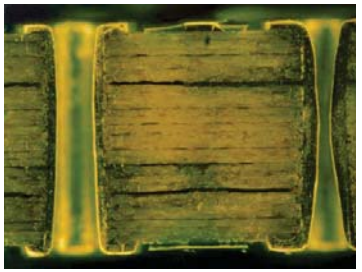
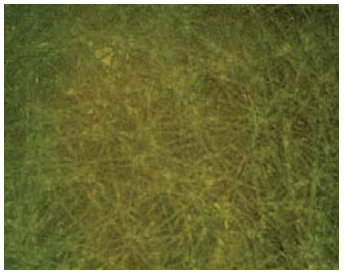
Paper Based Materials




FR1, FR2, FR3, and CEM-1 are examples of paper-based laminates.

- FR1 and FR2 use phenolic resin binder. These two differ in their glass transition temperatures (130° C for FR1 and 105° C for FR2).
- FR3 uses an epoxy resin binder. The basic layer is paper. It is not suitable for plated through holes.
- CEM-1 is a paper based laminate with one layer of woven glass fabric. It is not suitable for plated through holes.

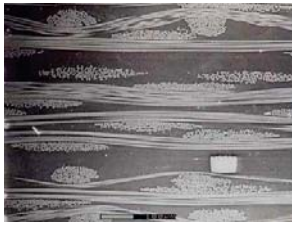
Non-woven Aramid Reinforcement

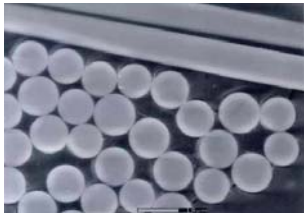



Side View Top View

Generally, non-woven laminates have compositions that are more homogeneous, can be made smoother, and have more isotropic properties than woven laminates. These properties are all important for fine pitch surface mount applications, where thermal mismatch and coplanarity are key to the ease of manufacture and component attachment (e.g., solder joints, direct attach or flip-chip) reliability.

Comparison of Woven & Non-woven Fabric





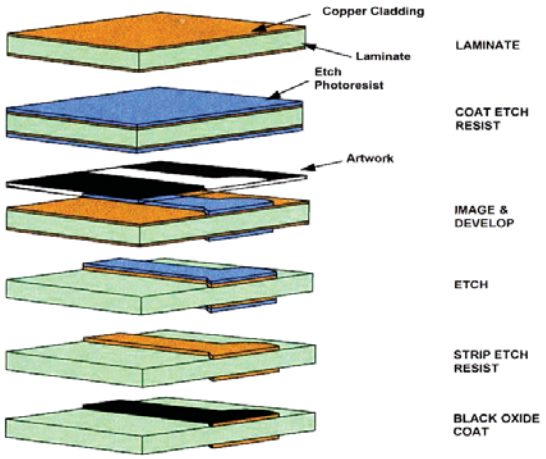

Copper Foil

- Thickness measured in oz./ft^2
  - 1 oz/ ft^2 => 1.35 mil, 2 oz/ ft^2 => 2.70 mil
- Electrodeposited copper
  - formed from plating polished steel drum; smooth and rough side; rough side makes for a good adhesive bond with laminate; grains elongated in direction perpendicular to sheet; not as ductile as rolled foil
- Rolled copper foil
  - progressive rolling and annealing; surface needs to be treated to form a good adhesive bond with laminate

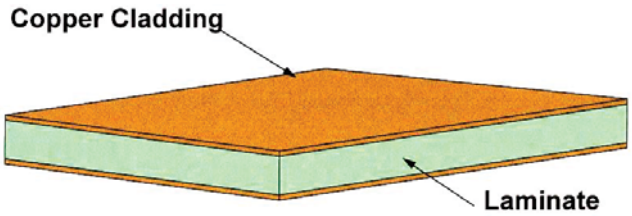
Factors in Selecting Circuit Board Materials

- Cost
- Electrical characteristics
  - Surface and volume resistivity and dielectric constant
- Mechanical properties
  - Flexural strength, modulus of elasticity, coefficient of thermal expansion (in plane and out of plane), glass transition temperature

Inner Layer Process Steps

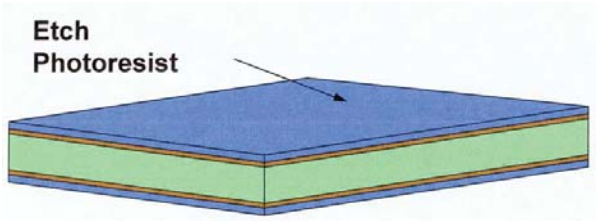


Laminate



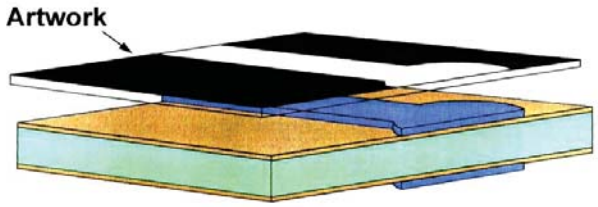
First, the proper laminate (core) is chosen. A core is made up of fully-cured epoxy resin ("C"-stage) sandwiched between two layers of copper cladding. The core must be the proper thickness, along with the required amount of copper cladding. The copper cladding will eventually become two inner layers, and the laminate will act as the dielectric spacing between these layers. The most common copper thickness for inner layers is one ounce of copper per square foot (typically 1.3 mils thick). Core thicknesses can run anywhere from 0.0015" to 0.070". The cores are either cut to size from larger sheets of material, or purchased to the specified panel size.

Coat Etch Resist



The core is chemically cleaned to remove any copper tarnish. It then passes through a cut sheet laminator where, through heat and pressure, a layer of dry film is placed on both sides of the core. This film will act as an etch resist later in the process, and will be removed after it has served its purpose.

Image and Develop

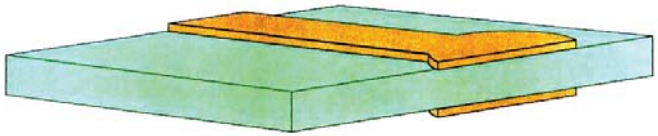


The resist-covered cores are placed into exposure frames where artwork is already in place. UV light is passed through silver halide artwork on both sides of the core simultaneously to expose the resist. This creates the circuit image in the dry film. The clear areas of the artwork through which light is allowed to shine on the film, are polymerized (hardened). Where light is blocked by artwork features, the film underneath stays soft. The soft, non-polymerized film is removed in the first section of the DES (Develop-Etch-Strip) line using a potassium carbonate solution, exposing only the unwanted copper for each layer.

Etch

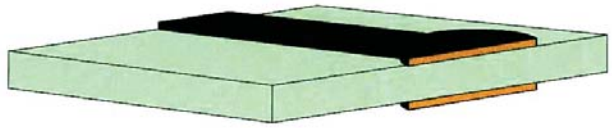
The core continues on through the DES line, passing through an ammoniacal etch, where the exposed, unwanted copper is attacked. The speed of the conveyor through etching is determined by the thickness of the copper being etched.

Strip Etch Resist



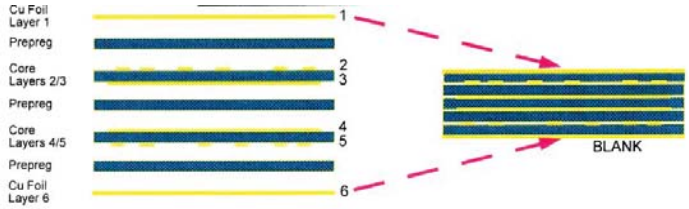
The dry film etch resist has completed its job. It is now removed in the final section of the DES line - the Stripper. Now a copper pattern for each layer can be seen. A Post-Etch Punch places a set of tooling slots in the core, by viewing targets placed precisely relative to the circuits and etched onto the core. These slots will be critical for proper registration of the cores used to construct the multilayer sandwich.

Black Oxide Coat



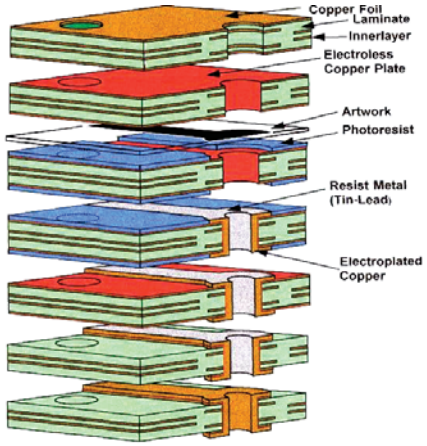
Prior to black oxide, the cores have undergone inspection using sophisticated AOI (Automated Optical Inspection) equipment. The inspected cores are then coated with an oxide in a programmed wet process line. The copper is changed to copper oxide, which has a crystal surface and will allow for better bonding when the multilayer is pressed together. The cores are then baked to remove any moisture.

KIT/ Laminate/ FAB



Once all the cores that go into the finished board are ready, they get released to kitting, where all the materials are put together to make a "blank". Copper foil will be placed on top and bottom, with the cores properly layered on the inside between sheets of prepreg ("B"-stage, fiberglass cloth impregnated with partially cured resin). This prepreg will act as the "glue" that holds the multilayer blank together, and will form the necessary dielectric between adjacent cores. All materials are placed over pins on registration plates to insure that the layers are perfectly lined up. Several boards laid up together separated by aluminum foil become a "book" with a top registration plate placed over the book. The books are placed in vacuum presses, where air is removed, and pressed together under heat and pressure. After pressing, pins are removed, "flash" is trimmed, and the blanks are separated, ready for drilling.

Outer Layer Process



DRILL & DEBURR

DESMEAR & COPPER DEPOSITION

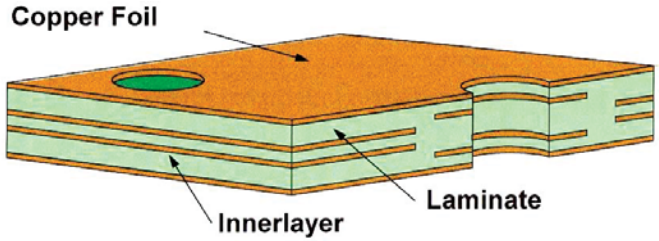
COAT , IMAGE & DEVELOP PHOTORESIST

COPPER & SOLDER PLATE STRIP PHOTORESIST

ETCH

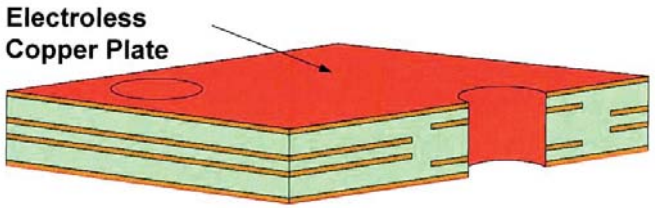
SOLDER STRIP

Drill and Deburr



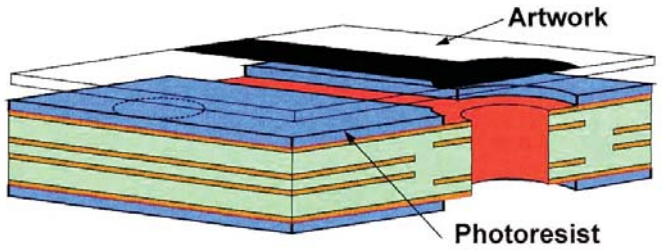
The blanks are pinned in stacks on tooling plates and drilled on multi-spindled drill machines. The computerized drill program determines where the holes are placed, and automatically changes drill sizes when each drill size has completed its path. Holes can be as small as .008" or as large as .250". X-ray and visual inspection are used to verify that the holes are fully drilled and properly aligned to the inner layer pads. Deburring equipment removes any burrs that may have formed.

Desmear and Copper Deposition



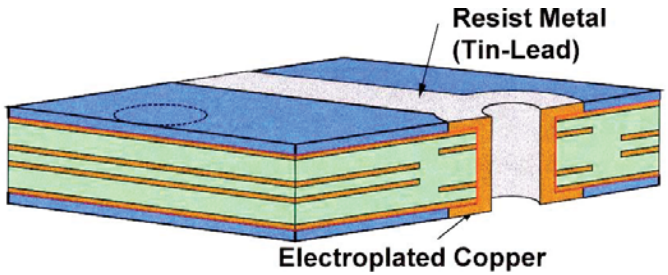
The holes undergo a process to remove any resin smear covering innerlayer connects and to slightly roughen the hole walls to allow for subsequent plating. The deposition process is an electroless plating process in which a very thin layer (80 to 100 millionths thick) of copper is deposited onto the surfaces of the hole wall (and incidentally on the copper foil surface). This will allow for subsequent electroplating of the holes.

Coat, Image and Develop Dry Film



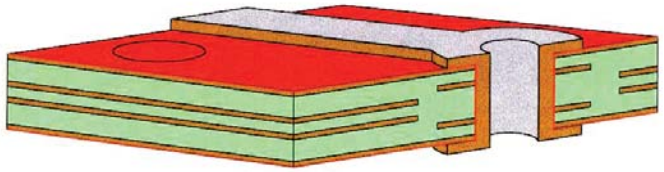
Dry film resist is applied to both sides of the panel under heat and pressure, similar to the cores in inner layers. The circuitry pattern of the artwork is aligned to the drilled holes and the panel is exposed to UV light from both sides. Where light is allowed to shine through, the film is polymerized. In the case of outer layers, a reverse artwork image is used, since the dry film is acting as a plating resist as opposed to the dry film being an etch resist in inner layer. The panels are developed, with the unexposed resist being washed away.

Copper and Solder Plate



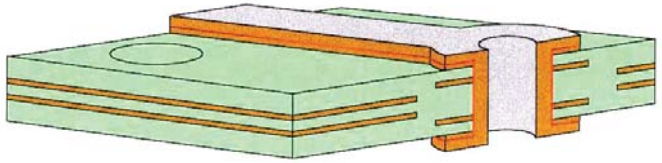
All copper exposed will be plated, with .001" nominal of copper in the hole barrels, followed by either tin or tin/lead, which will act as the etch resist further on. The panels are carried on racks by a hoist which is computer-controlled to repeat the same cycle time after time. The hoist places the racks of panels into the solution and rinse tanks for set time periods, so that the chemical solutions can deposit the metals to the traces, pads, and hole barrels electrolytically.

Strip Photoresist



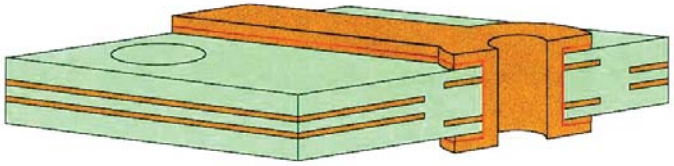
The dry film resist, which acted as a plating resist, is now stripped away with an alkaline solution in the Strip-Etch-Strip line. This exposed the unplated copper foil underneath on the surface. Any holes that were "tented" (covered) with dry film will have copper barrels from the electroless copper process.

Etch



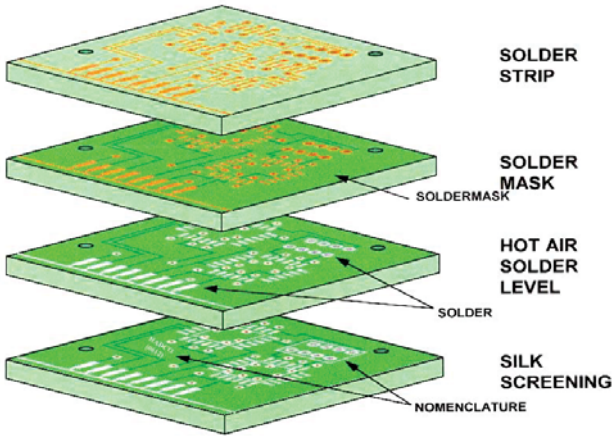
The copper foil is now etched away, using an ammoniacal solution. It is here where "a circuit is born," since the board is electrically functional at this point. There are still, however, several more steps.

Solder Strip

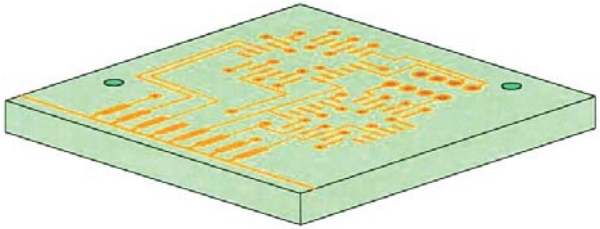


The tin or tin/lead that was protecting the traces, pads, and hole barrels from being etched is chemically stripped away at the end of the S/E/S line, leaving bare copper circuitry.

Outer Layer Process Steps

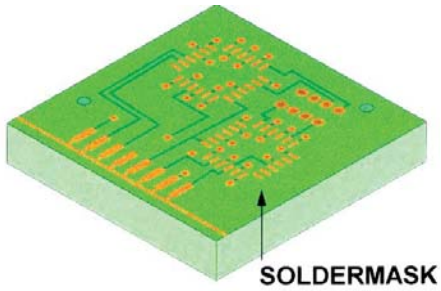


Solder Strip



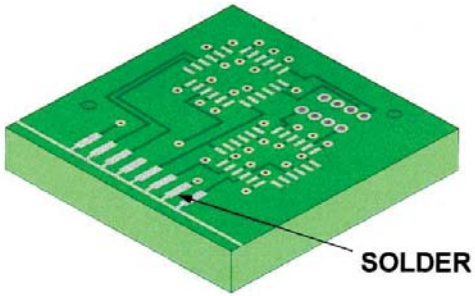
This details of this process, already discussed, involves the removal of the tin or tin/lead protecting the traces, pads, and hole barrels from being etched.

Soldermask



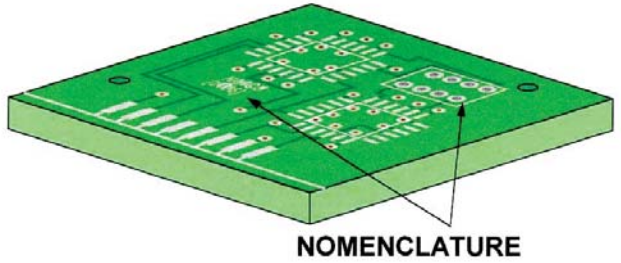
Soldermask is applied to protect and insulate the circuitry. The panels are cleaned, preheated, and coated with soldermask. Several stages of drying are performed to solidify the mask. The mask now acts much like the dry film in inner and outer layers. Artwork is exposed onto both sides of the panel, and the soft mask is removed where it is not wanted (pads). The panel is then baked for final curing.

Hot Air Solder Level



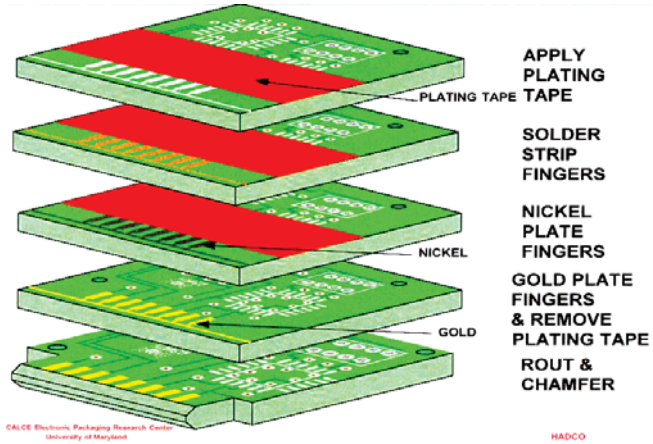
Hot Air Solder Level (HASL) involves the application of solder to selected board features, wherever copper was left exposed after soldermasking. The copper is cleaned and microetched in a preclean unit, preheated, and fluxed to promote solder wetting. The panel is horizontally immersed in the solder pot, and then excess solder is blown off with air knives. A cool down and cleaning stage follows.

Silk Screen

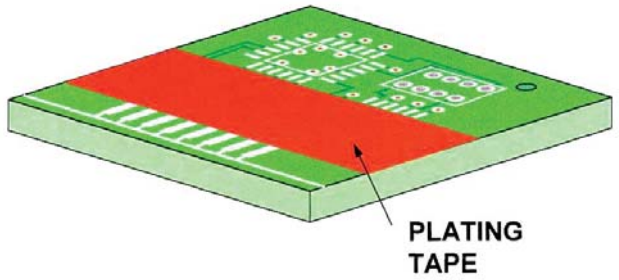


Information needed by the customer for assembly or troubleshooting is screen-printed onto the board. An epoxy ink is applied to the stenciled screen. Using a squeegee, the ink is forced through a screen fabric with a stencil image. The ink is then baked in order to cure the resin. Once baked, the ink is not easily removed.

Outer Layer Process Steps

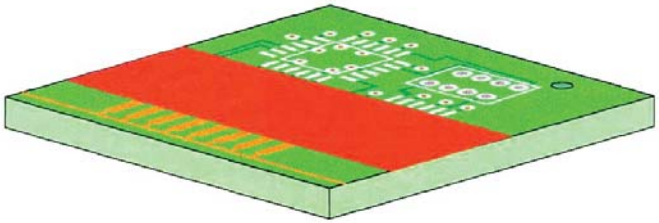


Apply Plating Tape



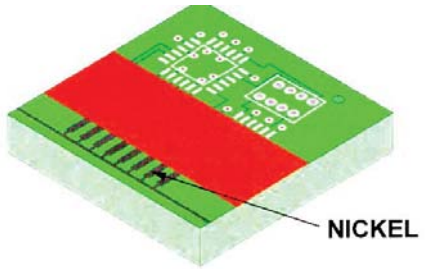
This nickel/gold plating process is used for edge connectors and critical contacts. A pressure tape is applied below the finger area in order to permit solder strip and nickel/gold plating in the finger area only.

Solder Strip Fingers



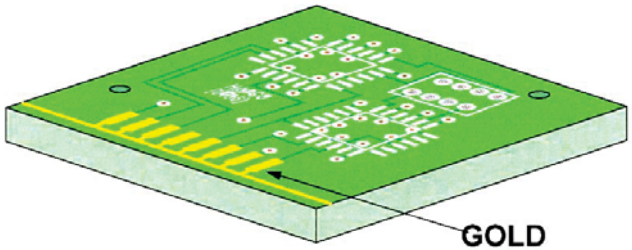
The boards travel within a conveyorized belt through shallow solution tanks. Solder, which had been leveled onto the connector fingers, is chemically stripped off.

Nickel Plate Fingers



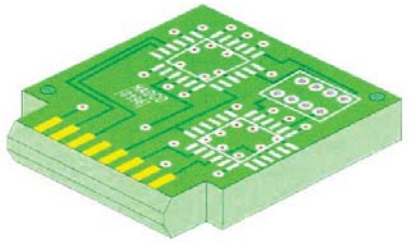
The nickel/gold plating process is electrolytic. As the board edges pass through plating solutions, brushes have made contact with blocks attached to a buss bar feeding to the fingers. This buss bar provides electrical continuity to the fingers and allows for plating. First, a layer of nickel about 100 - 150 microinches thick is plated onto the copper. This nickel increases wear-resistance. It also serves as a barrier to copper migration into the gold.

Gold Plating Fingers and Plating Tape Removal



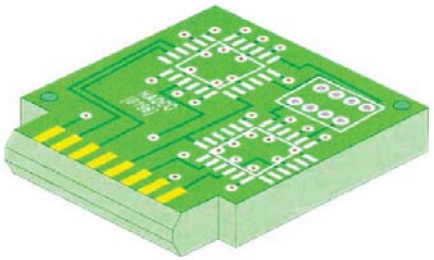
Gold, usually from 30 to 50 micro-inches thick, is plated directly over the nickel. Gold is used on the connector fingers because it is highly conductive and resists tarnishing. The plating tape is then pulled from the board, and the board is degummed.

Rout and Chamfer



Here the board is depanelized. The rout process is similar to the drill process, with the panels being stacked and pinned onto the tooling plates of a multiple spindle router. Utilizing a numerically controlled computer program, specialized carbide router bits are used to machine the edges, slots, and any required internal cutouts. The boards are removed and dimensionally verified to blueprint and shop traveler provided with the job. A bevel, or chamfer, is placed along the finger edge of the board, to remove the buss bar and allow for easier insertion of the card. Some boards with straight edges perpendicular to one another are scored, or V-grooved. The boards undergo a final clean of warm water and high-pressure rinse.

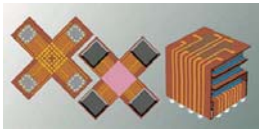
Electrical Testing, Final Inspection and Shipping



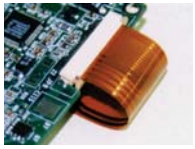
The boards undergo 100% electrical test on sophisticated simultaneous testers, to parameters set by the customer. This equipment runs from a downloaded program developed from net list or Gerber data. Final inspection looks for cosmetic flaws and performs dimensional checks. The shipping department then packages the boards for shipment to the customer.

Flex and Rigid-Flex Circuits

- Flex Circuits are thin, lightweight, bendable signal traces built on flexible dielectric substrates. Flex circuit technology enables 3D configurations, smaller, lighter and faster products, and can lower total applied cost.
- Characteristics
  - Meet dynamic flexing requirements: active and passive components can be added directly to the flex.
  - Impedance control
  - EMI control



Chip to chip connection



Board to board connection

Types of Flex Circuits*

- **Type 1:** One conductive layer, either bonded between two insulating layers or uncovered on one side. (Stiffeners, pins, connectors, components, are optional).
- **Type 2**: Double sided, two conductive layers, PTHs, with or without stiffeners.
- **Type 3:** Multi-layer flexible, three or more conductive layers, PTHs, with or without stiffeners.
- **Type 4**: Multi-layer rigid and flex, three or more conductive layers, PTHs.
- **Type 5:** Flex or rigid-flex, two or more conductive layers, no PTHs.

*** - IPC-6013C- Multi-layer rigid and flex, three or more conductive layers, PTHs, Nov 2003.**

Flex, Rigid-Flex Circuits - Materials

Base Material

- Polyester
- Polyimide
- Polyethylene napthalate (PEN)
- –Liquid crystal polymer
- –Flouropolymers

*** - Flexible Circuit Technology, Third Edition, J. Fjelstad, BR Publishing Inc, Sept 2006**

Flex, Rigid Flex - Base Materials

Substrate Material	Dielectric Constant	Dissipation Factor	Dielectric Strength (v/mil)	**Moisture Absorption**	Tensile Strength (kpsi)	Elongation
FEP	2	0.0002	5000	**< 0.01%**	2-3 kpsi	~ 300%
PTFE	2.5	0.0002	5000	**< 0.01%**	15- 25 kpsi	N/A
Polyester	3.2	0.005	7000	**< 0.08%**	25 kpsi	~ 120%
LCP	2.9	0.003	6000	**0.02 - 0.1%**	15-25 kpsi	~ 15%
PVC	4.7	0.093	500	**< 0.5%**	5 kpsi	~ 120-500%
Polyimide	3.5	0.003	7000	**1.3 – 3%**	25 kpsi	~ 60%
PEN	2.9	0.004	7500	**1%**	30-35 kpsi	~ 75%
Aramid Paper	2	0.007	380	**3%**	11 kpsi	~ 10%

Flex, Rigid-Flex Circuits - Materials

Bonding Adhesives

- Polyester
- Acrylic
- Epoxy
- –Polyimide
- –Butyl phenolic
- –Polythermides

Flex, Rigid Flex - Adhesive Materials

Adhesive Type	Peel Strength (post-solder) N/mm	Adhesive Flow mils/mil	**Moisture Absorption max %**	Surface Resistivity min M W	Dissipation Factor @1MHz	Dielectric Constant @1 MHz
PTFE	> 1 N/mm	125 mm max	**0.01**	1012	0.0007	2.2 nom
Polyester		250 mm max	**2**	104	0.02	4.0 max
Butyral-Phenolic	1.0 N/mm	125 mm max	**2**	104	0.025	3.0 max
Polyimide	1.0 N/mm	125 mm max	**3**	105	0.01	4.0 max
Epoxy	1.4 N/mm	125 mm max	**4**	104	0.06	4.0 max
Acrylic	1.6 N/mm	125 mm max	**6**	107	0.02	3.5 nom

Flex, Rigid-Flex Circuits - Materials

Conductors

- Copper foil or electrodeposited
- Annealed copper
- Electroplated copper
- Sputter deposited copper
- –Aluminum
- –Stainless steel
- –Beryllium copper
- –Polymer thick film

Board Level Failures (examples)

Plated Through Hole (PTH)/Via
1. Fatigue cracks in PTH/Via wall
2. Overstress cracks in PTH/Via wall
3. Land corner cracks
4. Openings in PTH/Via wall
5. PTH/Via wall-pad separation

Electrical
6. Electrical overstress (EOS)
7. Signal interruption (EMI)

Board
8. CAF (hollow fiber)
9. CAF (fiber/resin interface)
10. Electrochemical migration
11. Buckling (warp and twist)

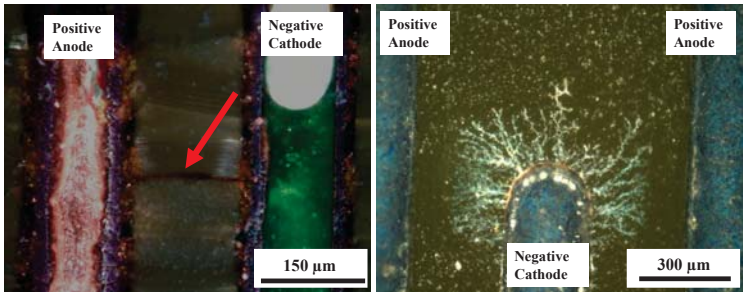
Copper Metallization
12. Cracks in internal trace
13. Cracks in surface trace
14. Corrosion of surface trace

Assembly Level Failures (examples)

Solder Interconnect

- Poor Solderability/Wettability
  - Tombstoning; Can accelerate other solder failure mechanisms
- Overstress Interconnect Failures
  - Solder Fracture (accelerated by intermetallic formation)
- Wearout Interconnect Failures
  - Solder Fatigue, Solder Creep
- Solder Bridging
- Component Failure due to Handling

ECM: Surface and Sub-surface Mechanisms



ECM	Conductive Anodic Filament (CAF)	Dendritic Growth
Growth Direction	Anode to cathode	Cathode to anode
Filament Composition	Metallic salt	Pure metal
Growth Position	Internal	Surface

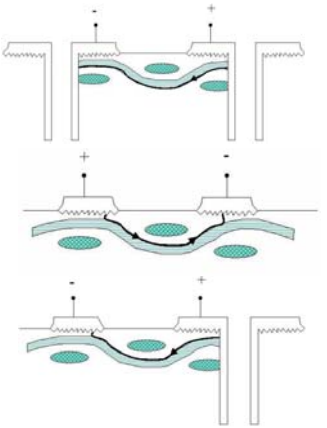
Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards." and Zhan, Sheng, Michael H. Azarian, and Michael Pecht. "Reliability of printed circuit boards processed using no-clean flux technology in temperature–humidity–bias conditions." Device and Materials Reliability, IEEE Transactions on 8.2 (2008): 426-434.

CAF Paths

A. Between two plated-through holes (PTHs)

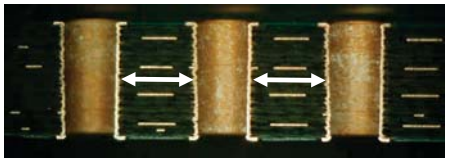
B. Between two traces

C. Between a trace and a plated-through hole (PTH)

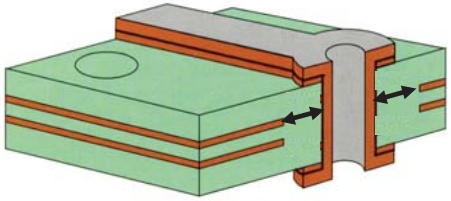


Ref: Rogers, Keith, et al. "Conductive filament formation failure in a printed circuit board." Circuit World 25.3 (1999): 6-8.

Factors Affecting CAF: PCB Internal Conductor Spacings



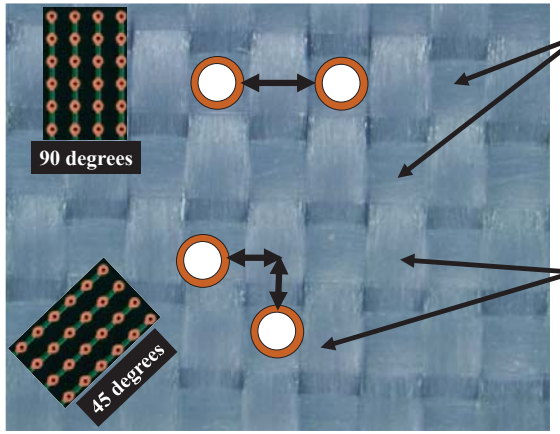
PTH-to-PTH spacings



PTH to plane spacings

Ref: Rogers, Keith, et al. "Conductive filament formation failure in a printed circuit board." Circuit World 25.3 (1999): 6-8.

Factors Affecting CAF: Board Orientation Respective to Fabric Weave

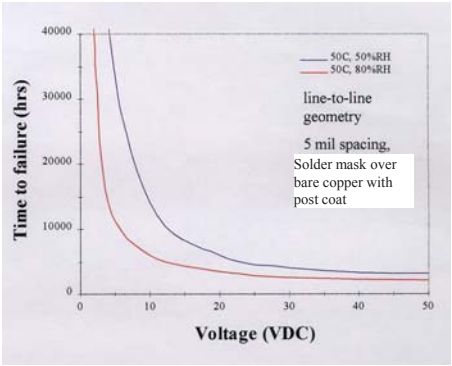


The initial set of parallel fiber bundles, known as the warp, lie in the machine direction

A second set of parallel fiber bundles, known as the fill or weft, is woven through the first set

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

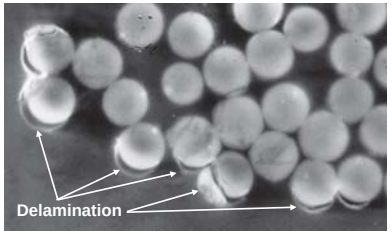
Effect of Voltage and Humidity on Time to Failure



Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Fiber/Resin Interface Delamination

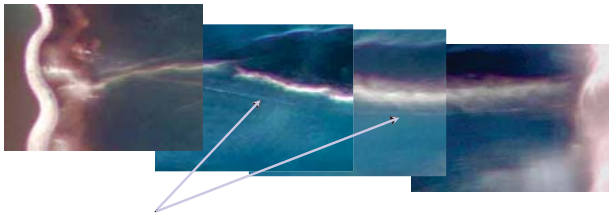
Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (ratio of 1 to 12).



Delamination can be prevented/resisted by selecting resin with lower CTE's and optimizing the glass surface finish. Studies have shown that the bond between fiber and resin is strongly dependent upon the fiber finish.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Hollow Fibers

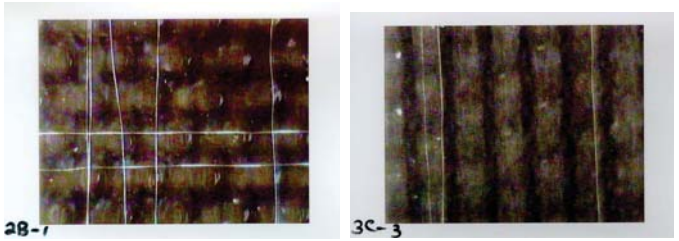


Hollow fibers are vacuous glass filaments in E-glass laminates that can provide paths for CAF.

With the appearance of hollow fibers inside the laminates, CAF can happen as a one step process. In this case, the number of hollow fibers inside the laminates is most critical to reliability.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Images of Hollow Fibers

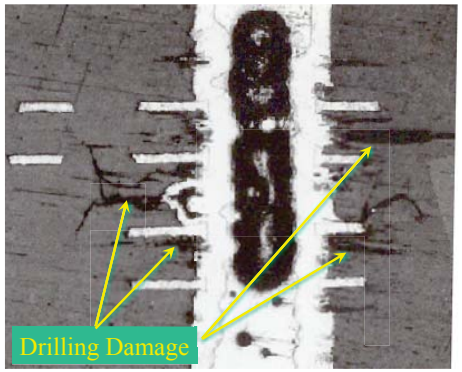


Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Drilling

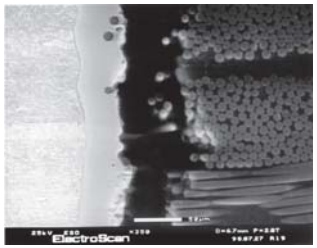
Drilling damage can accelerate CAF through

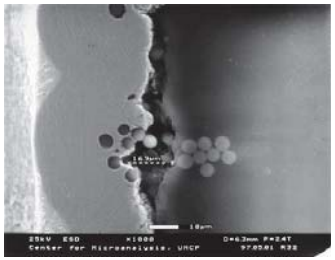
- Fiber/resin delamination,
- Creation of paths for moisture to accumulate
- Wicking due to cracking of the board material



Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

PTH-Resin Separation



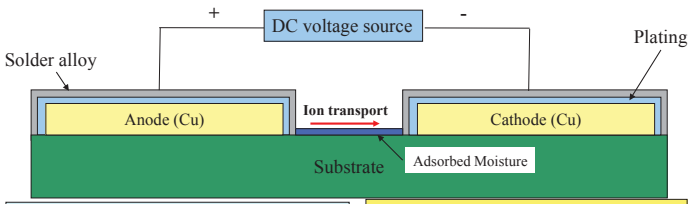


In both of these SEM pictures, a separation can be seen at the copper plating to fiber epoxy resin board interface. These gaps provide an accessible path for moisture to accumulate and CAF to initiate. These voids can be adjacent to inner-layer copper foil or to the PTH barrel and normally result from contraction of the epoxy (resin recession) due to the heat of thermal stress.

Ref: Rogers, Keith Leslie. "An analytical and experimental investigation of filament formation in glass/epoxy composites." (2005).

Background on Dendritic Growth

Dendritic Growth is a form of electrochemical migration (ECM) involving the growth of conductive filaments on or in a printed circuit board (PCB) under the influence of a DC voltage bias. [IPC-TR-476A]

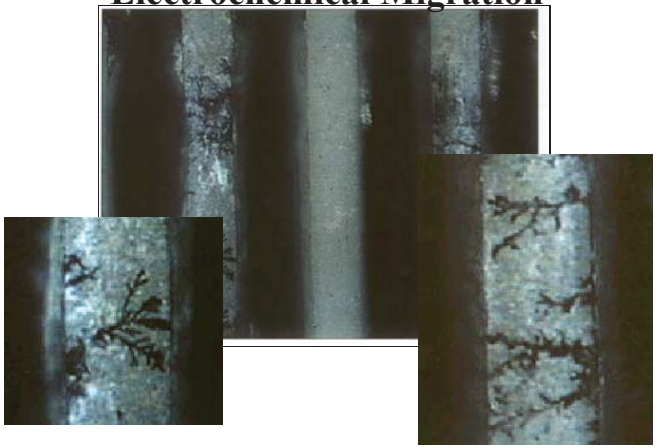


Necessary Conditions for ECM
- Electrical carriers (ions).
- A medium, usually water, to dissolve the ionic materials and sustain them in their mobile ionic state.
- Electrical potential between the electrodes to establish an ionic current in the liquid medium.

Stages of ECM
- Path formation
- Electrodissolution
- Ion transport
- Electrodeposition
- Filament growth

He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." *IPC printed circuit Expo, APEX & Designer summit proceedings.*

Electrochemical Migration



Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

Contaminants

- Halide residues, such as chlorides and bromides, are the most common accelerators of dendritic growth.
- Chlorides are more detrimental, but easier to clean
- Bromides can resist cleaning; often require DI water with saponifier
- In general, an increased risk of ECM will tend to occur once the levels of chloride exceed 10µg/in^2 or bromide exceeds 15µg/in^2
- Rapid failure can occur when contaminant levels exceed 50µg/in^2

Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

What Are the Sources of Contaminants?

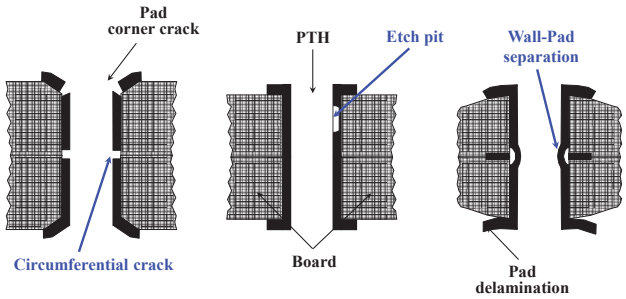
- Board Manufacturing
  - Flame-proofing agents
  - Copper plating deposits
  - Etchants
  - Cleaners
  - Fluxes (for HASL coatings)
  - Poorly polymerized solder masks
  - "Fingerprints"
- Assembly
  - Fluxes
  - Solder paste residues
  - "Fingerprints"
- Environmental
  - Liquid (i.e., salt spray)
  - Gaseous (i.e., Cl_2)

Ref: He, Xiaofei, M. Azarian, and M. Pecht. "Effects of solder mask on electrochemical migration of tin-lead and lead-free boards." IPC printed circuit Expo, APEX & Designer summit proceedings and Ambat, Rajan, et al. "Solder flux residues and electrochemical migration failures of electronic devices." Eurocorr proceedings, Nice 10.1.3321953 (2009).

Plated Through Hole (PTH) Failures

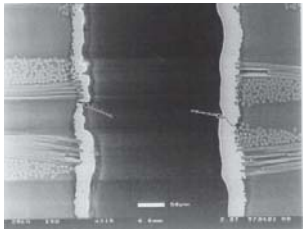
- Circumferential cracking
  - Single event overstress
  - Cyclic fatigue
- Openings (voids, etch pits)
  - Accelerate circumferential cracking
- Wall-Pad Separation
  - Also known as “breakout of internal lands” or “plated-barrel separation”

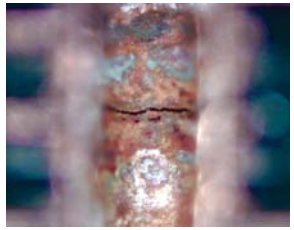
PTH Failures (cont.)



Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Circumferential Cracking – Single Event Overstress





Since the difference in the coefficient of thermal expansion (CTE) of the copper plating and the resin system in the PWBs is at least a factor of 13, stress exerted on the plated copper in the plated-through holes in the z-axis can cause cracking.

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Single Event Overstress (cont.)

- Failure Mode
  - Complete electrical open
- Failure History
  - Primarily occurs during assembly; may not be detected until after operation
- Root-Causes
  - Excessive temperatures during assembly
  - Resin Tg below specification
  - Insufficient curing of resin
  - Outgassing of absorbed moisture
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Insufficient mechanical properties of deposited copper
  - Plating voids
  - Etch pits
  - Insufficient PTH wall thickness

Design Considerations to Avoid Fatigue Damage in PTHs

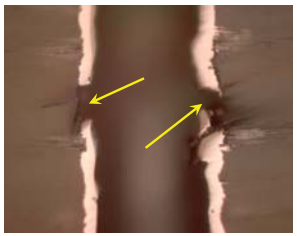
- PTH Spacing
  - Decreasing spacing improves mechanical reliability
- Aspect Ratio
  - Decreasing board thickness more effective than increasing hole diameter
- Plating Thickness
  - Increasing leads to increasing in fatigue strength
- Nonfunctional Internal Pads
  - Minimal effect. Results in localized stress relief; most effective when results in elimination of resin-rich areas

Ref: Kapur, Kailash C., and Michael Pecht. Reliability engineering. John Wiley & Sons, 2014.

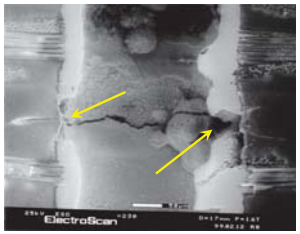
Root-Cause Analysis of Circumferential Fatigue Cracking

- Failure Mode
  - Intermittent to complete electrical open
- Failure History
  - Requires an environment with temperature cycling; often occurs after extended use in the field ("child" or "teenage" mortality)
- Root-Causes
  - Resin CTE below specification
  - Plating folds
  - PTH wall recession
  - Resin-rich pockets adjacent to PTH
  - Customer use exceeds expected environment
  - Insufficient mechanical properties of deposited copper
  - Presence of overstress crack
  - Plating voids
  - Etch pits ("mouse bites")
  - Insufficient PTH wall thickness

Openings in PTH Walls



Optical micrograph of cross section of PTH with etch damage

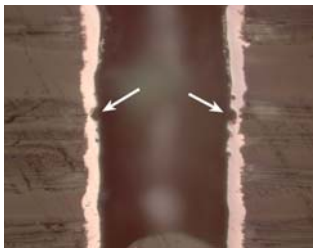


Electron micrograph of same PTH shown on left

Overetching can cause electrical opens or induce overstress circumferential cracking

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Evidence of Overetching



Optical micrograph of cross section of PTH with etch damage (bright field)

Optical micrograph of cross section of PTH with etch damage (dark field)

Evidence of overetching can include reduced plating thickness and discoloration of PTH barrel walls

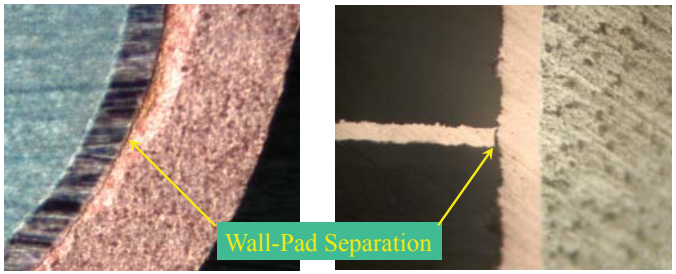
Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

Opening in PTH/Via

- Failure Mode
  - Complete electrical open
- Failure History
  - Often occurs during assembly; may not be detected until after operation
- Root-Causes
  - Openings in PTH's/Vias are etch pits or plating voids and often occur because the following manufacturing processes are not optimized:
    - Drilling
    - Desmear/Etchback
    - Electroless copper plating or direct metallization
    - Electrolytic copper plating
    - Tin resist deposition
    - Etching
  - Openings can also occur due to poor design (i.e., single-sided tenting of vias, resulting in entrapment of etchant chemicals)

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

PTH/Via Wall-Pad Separation



Optical micrograph of cross section perpendicular to the PTH axis

Optical micrograph of cross section parallel to the PTH axis

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

PTH/Via Wall-Pad Separation

- Failure Mode
  - Intermittent or complete electrical open
- Failure History
  - Will primarily only occur during assembly
- Root-Causes
  - Insufficient Curing of Resin.
  - Outgassing of absorbed moisture
  - Excessive temperatures during assembly
  - Resin CTE or Resin Tg below specification
  - Number of nonfunctional lands (only useful for failures during assembly)
  - Drilling process resulting in poor hole quality
  - Insufficient desmearing process.
  - Substandard processes or materials in electroless copper plating

Ref: Bhandarkar, S. M., et al. "Influence of selected design variables on thermo-mechanical stress distributions in plated-through-hole structures." Journal of Electronic Packaging 114.1 (1992): 8-13.

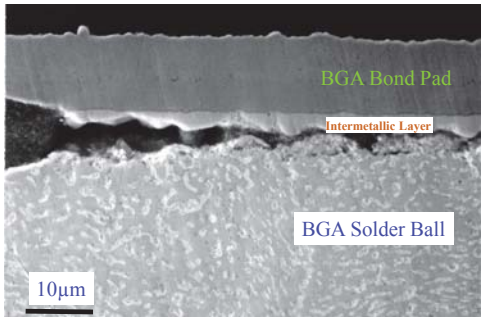
Failure Mechanisms due to Handling

- Affects leadless components
  - Ball grid arrays (BGAs), Flip Chip on Board
- Affects brittle components
- Insidious
  - Failures due to handling tend to difficult to screen and intermittent in nature
  - Often occur after testing

When Do Handling Failures Occur?

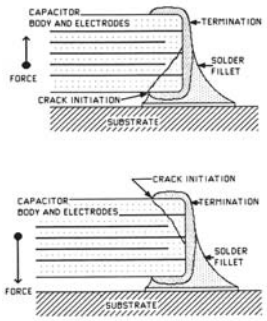
- Assembly
  - Transfer of product between lines; during rework
- Heatsink Attachment
  - Use of screws
- Connector Insertion
  - Large press-fit connectors; daughter boards into mother boards
- Electrical Testing
  - Bed-of-Nails testing can bend local areas
- Packaging
- Transportation
- Customer Site
  - Slot insertion

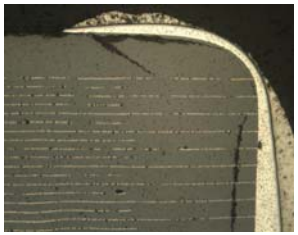
Evidence of Damage Due to Handling -- BGAs



Ref: SEM Lab.

Evidence of Damage – Ceramic Capacitors





Keimasi, Mohammadreza, Michael H. Azarian, and Michael G. Pecht. "Flex Cracking of Multilayer Ceramic Capacitors Assembled With Pb-Free and Tin–Lead Solders." Device and Materials Reliability, IEEE Transactions on 8.1 (2008): 182-192.

Intermittent Failures

- An intermittent failure is the loss of some function in a product for a limited period of time and subsequent recovery of the function.
- If the failure is intermittent, the product's performance before, during, or after an intermittent failure event may not be easily predicted, nor is it necessarily repeatable.
- However, an intermittent failure is often recurrent.

Ref: Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674.

No Fault Found

- No-Fault-Found (NFF): Failure (fault) occurred or was reported to have occurred during product's use. The product was tested to confirm the failure, but the testing showed "no faults" in the product.
- Trouble-Not-Identified (TNI): A failure occurred or was reported to have occurred in service or in manufacturing of a product. But testing could not identify the failure mode.
- Can-Not-Duplicate (CND): Failures that occurred during manufacture or field operation of a product cut could not be verified or assigned.
- No-Problem-Found (NPF): A problem occurred or was reported to have occurred in the field or during manufacture, but the problem was not found during testing.
- Retest-OK: A failure occurred or was reported to have occurred in a product. On retesting the product at the factory, test results indicated that there was no problem.

Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674.

The Impact of Intermittents

- Can not determine root cause and thus the reason for the failure (NFF)
- Reliability modeling analysis can be faulty
- Potential safety hazards
- Decreased equipment availability
- Long diagnostic time and lost labor time
- Complicated maintenance decisions
- Customer apprehension, inconvenience and loss of customer confidence
- Loss of company reputation
- Increased warranty costs
- Extra shipping costs

Common Examples of Intermittents

Some common examples of intermittent failures:

- Medical: asthma attacks, allergy attacks, angina, toothaches (especially if food- or temperature- dependent)
- Automotive: squealing sound or failure to charge battery due to loose fan belt
- Utility: brown-outs
- Cell phone or computer: multiple letter entries for a single keystroke, which may be due to bad contact or sticky keys on keypad
- Household: water ingress through leaky roof, especially if leak is wind-driven; running toilet, due to problems with mechanism or plunger seal

General Categories of NFFs

- Typical physics-based issues at the part level.
- Circuit sensitivities
- Test sensitivities
- System sensitivities
- Usage sensitivities
- Infrastructure sensitivities
- User abuse
- Psychic influences

NFF Circuit Sensitivities

- Material degradations
- Noise increases as aluminum capacitors degrade
- Electrically noisy neighbor
- ESD margins decreasing
- Timing errors
- Setup errors
- Cross-talk
- Leakage currents
- Power supply sequence sensitivities
- End-of-life on relays, optics, calibration, etc.
- Software errors

NFF Test Sensitivities

Testing has five possible outcomes:

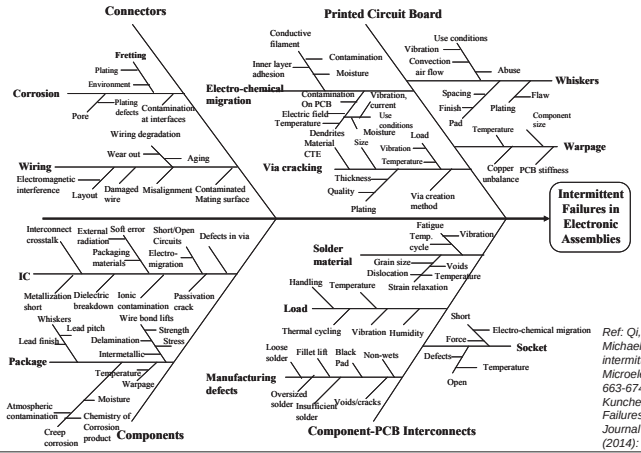
- Test can say it is good when it is good.
- Test can say it is bad when it is bad.
- Test can say it is good when it is bad.
- Test can say it is bad when it is good.
- Test can be inconsistent.

User Abuse

- Users can abuse the system and influence the NFF results.
- A user who sends two boards back for every field failure is automatically contributing to the NFF rate.
- A user who buys inventory from eBay and then sends it to the original manufacturer for retest is guilty of abuse.
- Disgruntled unions and employees cannot be disregarded.

Intermittent Failures in Electronic Assemblies

Cause-and-Effect Diagram



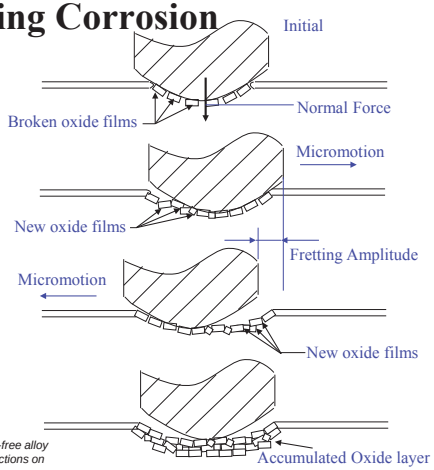
Ref: Qi, Haiyu, Sanka Ganesan, and Michael Pecht. "No-fault-found and intermittent failures in electronic products." Microelectronics Reliability 48.5 (2008): 663-674 and Bakhshi, Roozbeh, Surya Kunche, and Michael Pecht. "Intermittent Failures in Hardware and Software." Journal of Electronic Packaging 136.1 (2014): 011014.

Characteristics of Intermittent Failures

- May indicate that a failure has occurred. Intermittent failure may be due to some extreme variation in field or use conditions.
- May indicate the imminent occurrence of failure.
- May not leave a failure signature making it difficult to isolate the site.

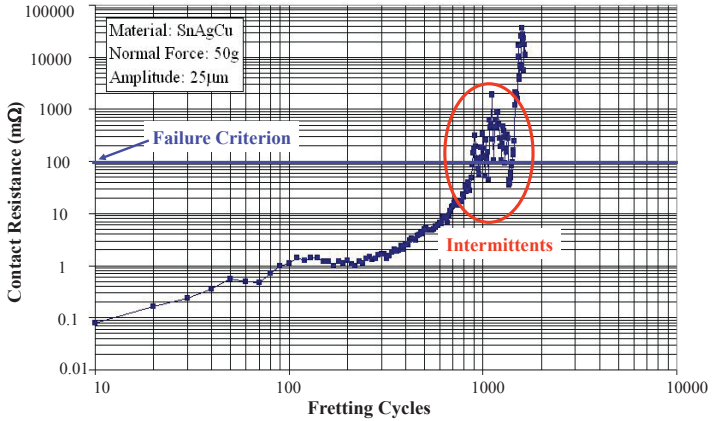
Example: Intermittent Failures Due to Fretting Corrosion

- Tin alloys are soft metals on which a thin but hard oxide layer is rapidly formed.
- Being supported by a soft substrate, this layer is easily broken and its fragments can be pressed into the underlying matrix of soft, ductile tin-lead alloy.
- The sliding movements between contact surfaces break the oxide film on the surface and expose the fresh metal to oxidation and corrosion.
- The accumulation of oxides at the contacting interface due to repetitive sliding movements causes contact resistance to increase, leading to contact open.
- Tin based lead-free solders are expected to show similar fretting corrosion susceptibility as tin-lead solder coatings.



Ref: Wu, Ji, and Michael G. Pecht. "Contact resistance and fretting corrosion of lead-free alloy coated electrical contacts." Components and Packaging Technologies, IEEE Transactions on 29.2 (2006): 402-410.

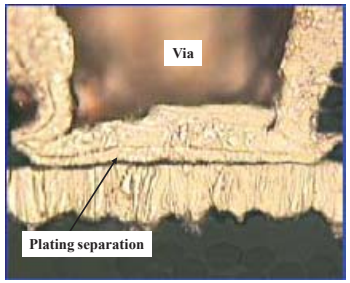
Electrical Contact Resistance vs. Fretting Cycles



Ref: Wu, Ji, and Michael G. Pecht. "Contact resistance and fretting corrosion of lead-free alloy coated electrical contacts." Components and Packaging Technologies, IEEE Transactions on 29.2 (2006): 402-410 and Antler, Morton, and M. H. Drozdowicz. "Fretting corrosion of gold-plated connector contacts." Wear 74.1 (1981): 27-50.

Example: Intermittent Failure Due to Improper Micro-via Plating in PCB

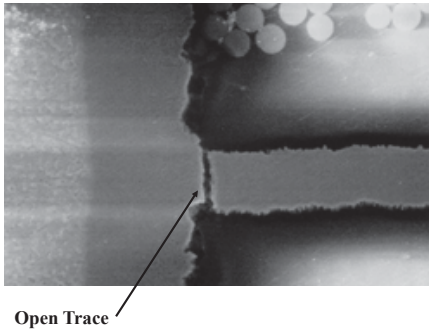
A computer graphics OEM was experiencing intermittent failures on printed circuit boards with chip scale packages (CSPs) and ceramic ball grid array packages (CBGAs). High magnification metallurgical microscope imaging of micro-etched cross sections of micro-vias in the printed circuit board showed a separation of the via plating from the capture pad [Nektek Inc. Service Report, 2004]. The plating separation was found to be the cause of intermittent failure.



Plating separation at base of micro via [Nektek Inc. Service Report, 2004]

Example: Intermittent Failure Due to Open Trace in PCB

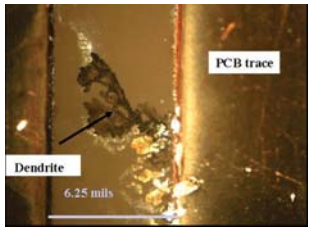
Open trace can also cause intermittent failures in PCB under environmental loading conditions. Under thermal cycling or vibration loading, the open trace may reconnect with intermittent electrical continuity observations.



Ref: A Study in Printed Circuit Board (PCB) Failure Analysis, Part 2, Insight Analytical Labs, Inc

Example: Intermittent Failures Due to Electro-chemical Migration (Surface Dendrites)

- Electrochemical migration (ECM) can cause shorts due to the growth of conductive metal filaments in a printed wiring board (PWB).
- Surface dendrites can form between the adjacent traces in the PWB under an applied voltage when surface contaminants and moisture are present.
- It is often difficult to identify the failure site because the fragile dendrite structure will burn upon shorting, often leaving no trace of its presence.

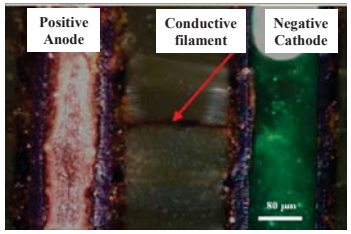


Dendritic growth during an ECM test

Ref: Zhan, Sheng, Michael H. Azarian, and Michael Pecht. "Reliability of printed circuit boards processed using no-clean flux technology in temperature–humidity–bias conditions." Device and Materials Reliability, IEEE Transactions on 8.2 (2008): 426-434.

Example: Intermittent Failures Due to Electro-chemical Migration (Conductive Anodic Filament Formation)

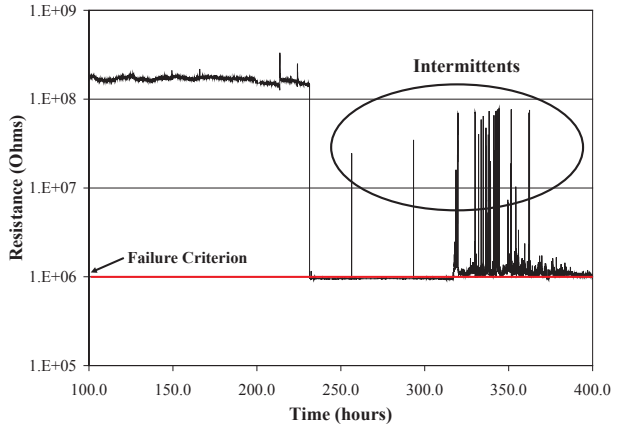
- Conductive filament is formed internal to the board structure.
- In CAF, the filament is composed of a metallic salt, not neutral metal atoms as in dendritic growth.
- One of distinct signatures of CAF failures is intermittent short circuiting. The conductive filament bridging the two shorted conductors can blow out due to the high current in the filament, but can form again if the underlying causes remain in place.



A conductive filament bridging two plated through holes in a PWB

Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards."

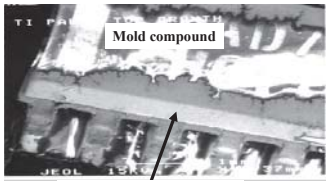
Electrical Resistance vs. Time Due to CAF



Ref: Sood, Bhanu, Michael Osterman, and Michael Pecht. "An Examination of Glass-fiber and Epoxy Interface Degradation in Printed Circuit Boards."

Example: Intermittent Failures Due to Creep Corrosion

- Definition
  - Creep corrosion is a mass transport process in which solid corrosion products migrate over a surface.
- Failure mode
  - On IC packages, creep corrosion can eventually result in electrical short or signal deterioration due to the bridging of corrosion products between isolated leads.
  - Depending on the nature of the environment, the insulation resistance can vary and cause intermittents.

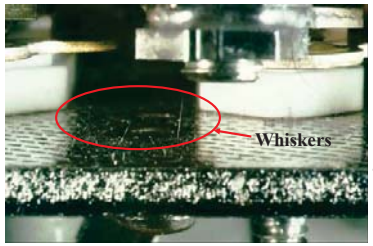


Creep corrosion

Ref: *Zhao, Ping, and Michael Pecht. "Field failure due to creep corrosion on components with palladium pre-plated leadframes." Microelectronics Reliability 43.5 (2003): 775-783.*

Example: Intermittent Failures Due to Tin Whiskers


Failed relay due to tin vapor arcing

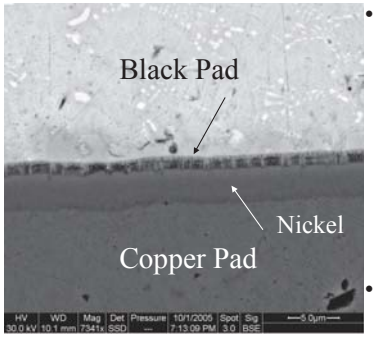


Whiskers on the armature of a relay

- Whiskers are elongated single crystals of Sn which grow spontaneously out of the surface. Internal stresses within the plated deposit drives growth
- Tin (and other conductive) whiskers or parts of whiskers may break loose and bridge isolated conductors, resulting in an intermittent short circuit. These field failures are difficult to duplicate or are intermittent because at high enough current the conductive whisker can melt, thus removing the failure condition. Alternatively, disassembly or handling may dislodge a failure-producing whisker.
- Failure analysis concluded that tin whiskers initiated the current surge to the ground. Once a whisker bridged a terminal stud to the armature, plasma arcing could occur with enough voltage and current to damage the relay.

Photos : Northrop Grumman and Ref: Davy, Gordon. "Relay Failure Caused by Tin Whiskers." (2002).

Example: Intermittent Failures Due to Black Pad



- The 'Black Pad' phenomenon in Electroless Nickel over Immersion Gold (ENIG) board finish manifests itself as gray to black appearance of the solder pad coupled with either poor solderability or solder connection, which may cause intermittent electrical 'opens.'
- Bulwith et al. [2002] identified numerous Ball Grid Array (BGA) package intermittent electrical open failures to be black pad related.

Zeng, Kejun, et al. "Root cause of black pad failure of solder joints with electroless nickel/immersion gold plating." Thermal and Thermomechanical Phenomena in Electronics Systems, 2006. ITHERM'06. The Tenth Intersociety Conference on. IEEE, 2006.

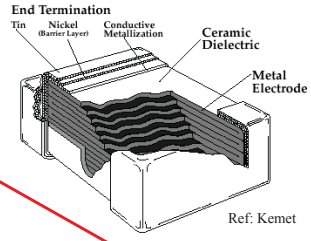
CASE STUDY*

Failure Analysis of Multilayer Ceramic Capacitor (MLCC) with Low Insulation Resistance

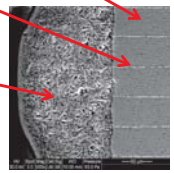
* - Adapted from: Brock, Garry Robert. "The Effects of Environmental Stresses on the Reliability of Flexible and Standard Termination Multilayer Ceramic Capacitors." PhD diss., 2009.

MLCC Construction

- Ceramic Dielectric
  - Typically comprised of compounds made with titanium oxides
    - $BaTiO_3$ ("X7R") for this study
- Electrodes
  - Base metal consisting of nickel (BME)
    - Precious metal consisting of silver/ palladium (PME)
- End Termination
  - Standard termination consists of silver or copper coated with nickel and tin
    - Flexible termination consists of a silver-filled polymer coated with nickel and tin

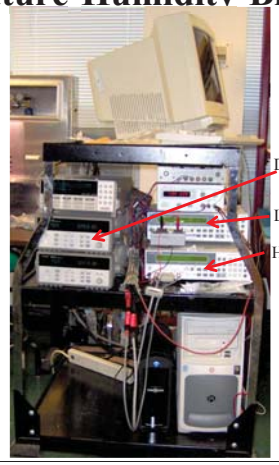


Ref: Kemet

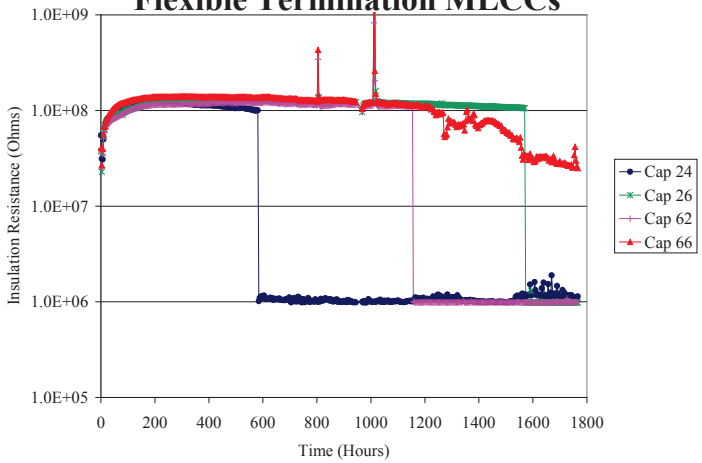


Loading Conditions: Temperature-Humidity-Bias

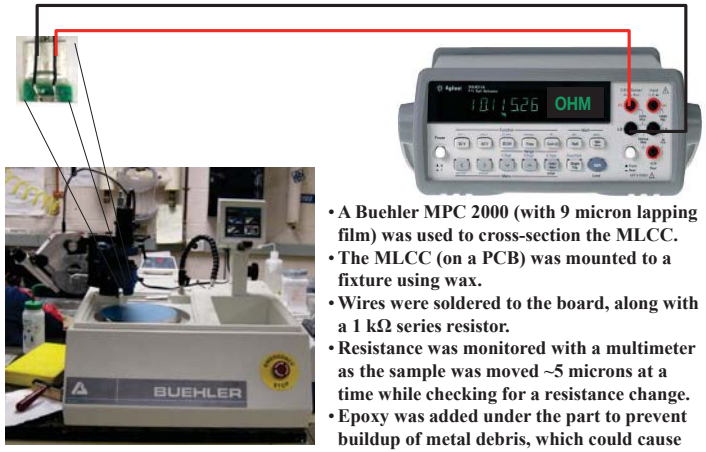
- A Temperature-Humidity-Bias (THB) test was performed for 1766 hours at 85° C and 85% RH, at the rated voltage of 50V.
- Capacitance, Dissipation Factor (DF) and Insulation Resistance (IR) were monitored during the test.
- A 1 MΩ resistor was placed in series with each of the MLCCs.
- The MLCCs were size 1812 and soldered to an FR-4 printed circuit board using eutectic tin-lead solder.



IR Test Data for Failed Flexible Termination MLCCs

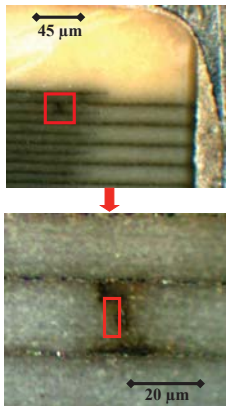


THB Failure Analysis Methodology for Biased MLCCs

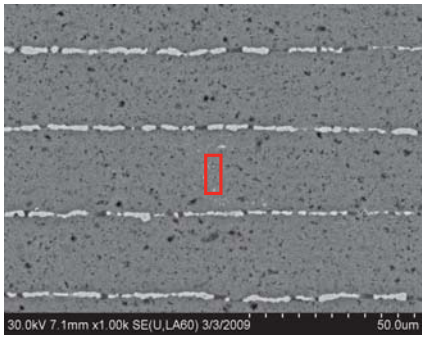


- **A Buehler MPC 2000 (with 9 micron lapping film) was used to cross-section the MLCC.**
- **The MLCC (on a PCB) was mounted to a fixture using wax.**
- **Wires were soldered to the board, along with a 1 kΩ series resistor.**
- **Resistance was monitored with a multimeter as the sample was moved ~5 microns at a time while checking for a resistance change.**
- **Epoxy was added under the part to prevent buildup of metal debris, which could cause an inaccurate resistance value.**

Metal Migration Between Electrodes

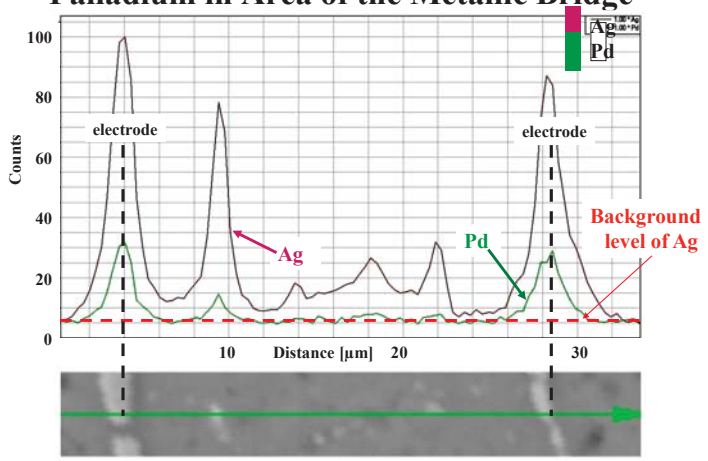


Optical Micrographs of Cross-section

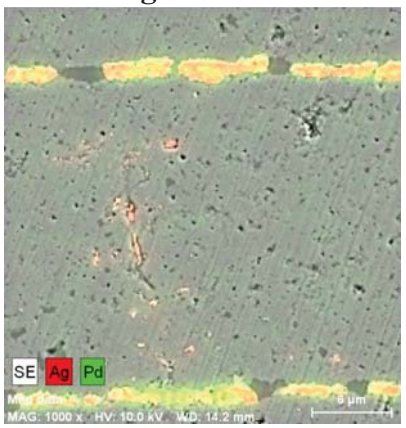


SEM Image of Cross-section

EDS Line Scan Showing Silver and Palladium in Area of the Metallic Bridge



EDS Map Showing Silver Migration and Voiding in Ceramic



Failure Mechanism

- Metal migration was found in several of the failed MLCCs.
- Voids in the ceramic, without silver or palladium, were also found close to the conduction path.
- The failure mechanism was electrochemical co-migration of silver and palladium, aided by porosity in the dielectric.

Non-Destructive Techniques

- Electrical Testing
- Scanning Acoustic Microscopy (SAM)
- X-ray Inspection
- X-ray Fluorescence (XRF)
- Optical Inspection

Electrical Testing of Components and Printed Circuit Boards

Electronic Testing Equipment

- Digital meters
  - Multimeters
  - Specialized parametric meters, such as LCRs, high resistance meters, etc.
- Oscilloscopes, Spectrum Analyzers
- Curve tracer/Parameter Analyzers
- Time Domain Reflectometers
- Automated Test Equipment (ATE)

Digital Multimeters

- Typically provide:
  - Voltage (DC, AC rms)
  - Resistance (2 wire)
  - Current
- Other common options:
  - Resistance (4 wire)
  - Frequency or count
  - Diode voltage
  - Capacitance
  - Temperature
  - Datalogging

Agilent 34401A

LCR Meters and Impedance Analyzers

- Variable AC voltage and frequency.
- Used to characterize
  - Capacitors
  - Inductors
  - Transformers
  - Filters
  - Dielectric materials (e.g., PCB substrates)

Agilent 4263B

High Resistance Meters

- Typically measure:
  - Leakage current
  - Insulation resistance
- Common applications:
  - Insulation resistance of dielectrics (capacitors, substrates)
  - Surface insulation resistance of PCBs

Agilent 4339B

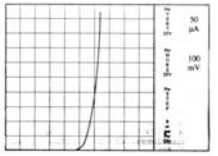
Oscilloscopes and Spectrum Analyzers

- Digital scopes allow:
  - –Waveform storage
  - –Capture of transients
  - –Waveform measurements
  - –Math (e.g., FFT)
  - –Complex triggering
- Spectrum analyzers are used for frequency domain measurements.

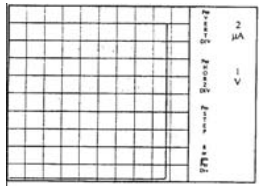
Agilent 54601

Curve Tracer or Parameter Analyzer

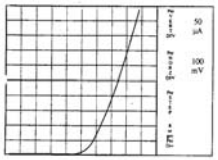
- Low frequency display of voltage versus current



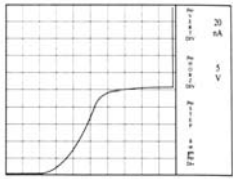
Normal I-V curve



Normal I-V curve



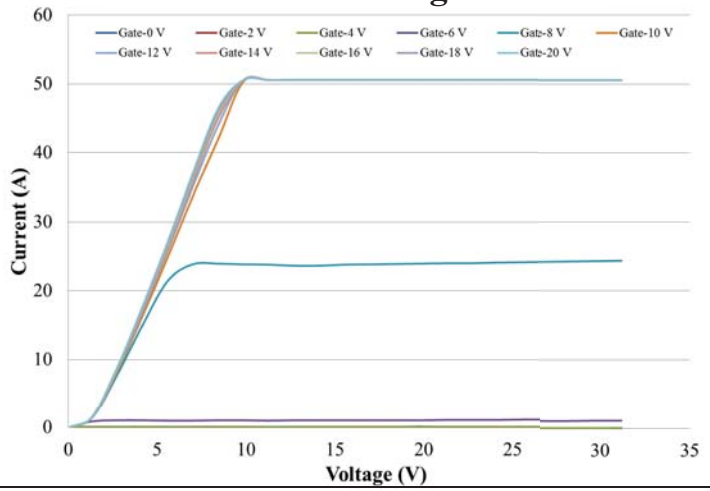
Abnormal I-V curve (due to the presence of a series resistance)



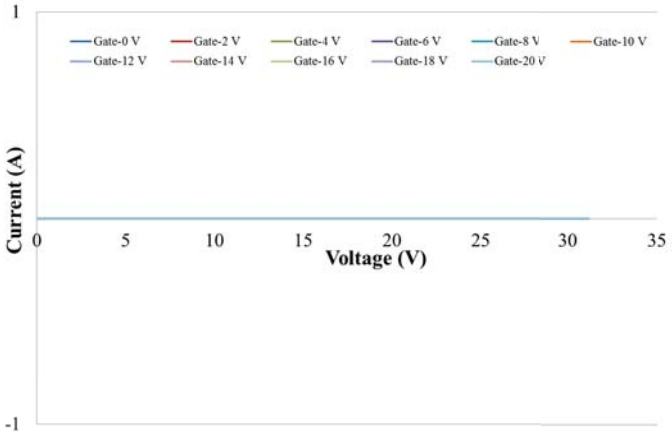
Abnormal I-V curve – Ionic Contamination (Reverse Bias)

Current-Voltage Characteristics of Failed and Non-failed Insulated-gate Bipolar Transistor (IGBT)

Behavior of Known good IGBT



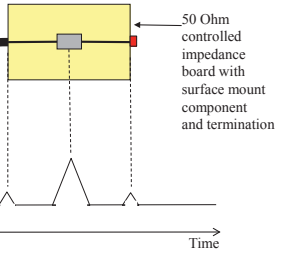
Behavior of Failed IGBT (Failed OPEN)



Time Domain Reflectometry (TDR)

- TDR reflection coefficient (Γ) is the ratio of the incident and reflected voltage due to impedance discontinuities in the circuit.
- In the time domain, any discontinuities due to impedance mismatches within the circuit are seen as discrete peaks.
- TDR reflection coefficient is a measure of RF impedance, and can be measured using a short pulse or high frequency sinusoidal signal (requires transformation).

Agilent E8364A Vector network analyzer (VNA)



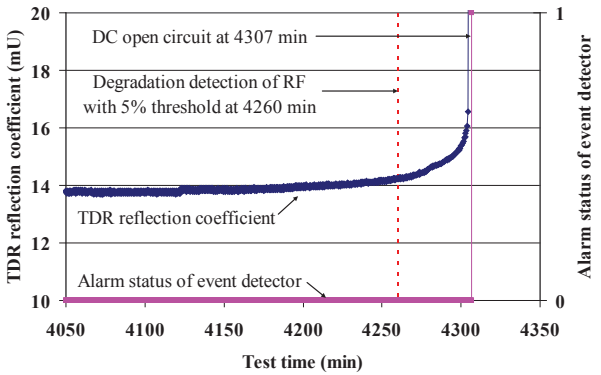
$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

- $-1 \le \Gamma \le 1$; Γ is dimensionless
- $\Gamma=1$ when $Z_L=\infty$; $\Gamma=-1$ when $Z_L=0$
  - Z_L: the impedance of device under test
  - Z_0: characteristic impedance of the circuit (50 Ohm)

Ref: Kwon, Daeil, Michael H. Azarian, and Michael Pecht. "Early detection of interconnect degradation by continuous monitoring of RF impedance." Device and Materials Reliability, IEEE Transactions on 9.2 (2009): 296-304.

TDR Sensitivity to Solder Joint Cracking

A 5% increase of the initial value occurred at 4260 minutes, which was 47 minutes earlier than the time to failure based on an event detector.



Ref: Kwon, Daeil, Michael H. Azarian, and Michael Pecht. "Early detection of interconnect degradation by continuous monitoring of RF impedance." Device and Materials Reliability, IEEE Transactions on 9.2 (2009): 296-304.

Automated PCB Test Equipment

- Dedicated Wired Grid – test probes wired to the grid. High cost.
- Universal Grid ("Bed of Nails") –Low cost, reusable. Spring loaded or rigid test probes in mechanical contact to the grid.
- Flying Probe or Fixtureless System with moveable single or double probes. Expensive. Empirical techniques applied on capacitance /impedance data to determine a good board. Good for micro products. Issues with pad damage.

Scanning Acoustic Microscopy

Common Applications

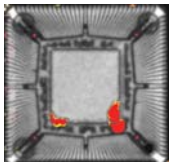
Defects specific to IC packages include:

- Delamination at wirebonds, substrate metallization, dielectric layers, element attaches, and lid seals.
- Die-attach field-failure mechanisms induced by improper die mounting and de-adhesion.
- Delamination of the molding compound from the leadframe, die, or paddle
- Molding compound cracks
- Die tilt
- Voids and pinholes in the molding compound and die attach

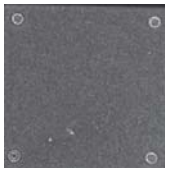
Other applications:

- Flip Chips
- Bonded Wafers
- Printed Circuit Boards
- Capacitors
- Ceramics
- Metallic
- Power Devices/Hybrids
- Medical Devices
- Material Characterization

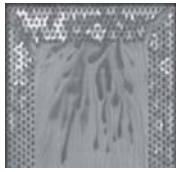
Common Applications



Die Top Delamination

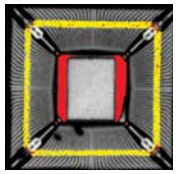


Mold compound voids

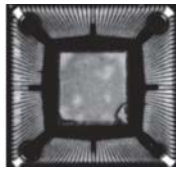


Flip Chip Underfill Voids

Die Tilt, B-Scan



Die Pad delamination

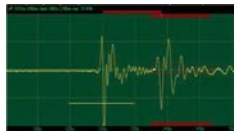


Die Attach Voids

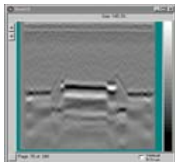
Ref: Moore, T. M. "Identification of package defects in plastic-packaged surface-mount ICs by scanning acoustic microscopy." ISTFA 89 (1989): 61-67 and Briggs, Andrew, ed. Advances in acoustic microscopy. Vol. 1. Springer Science & Business Media, 2013.

Scanning Acoustic Modes

A-Scan: Raw ultrasonic data. It is the received RF signal from a single point (in x,y).



B-Scan: Line of A-scans. (Vertical cross-section)



C-Scan: Data from a specified depth over the entire scan area. (Horizontal cross-section).

Limitations of the Techniques

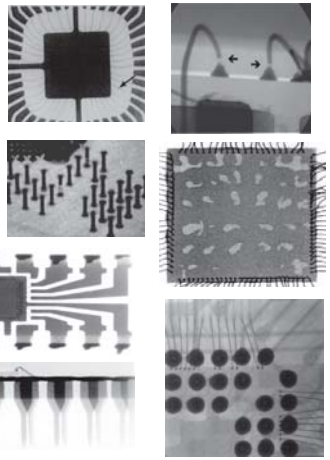
- Materials and interfaces of interest have to be flat (i.e., not useful on solder balls or joints unless at a flat interconnection sites.
- Materials have to be relatively homogeneous (not practical for PWB internal examination, hence not applicable for BGAs on PWB substrates, but allowable for BGAs on ceramic).
- Metals tend to interfere with the acoustic signal (i.e., unable to examine underneath of metal layers such as a copper die paddle or an aluminum heat sink. The copper metallization on PWBs is another hindrance for their internal examination).
- Operator needs to be highly skilled to correctly acquire and interpret data.
- Since resolution and penetration depth are inversely related, a trade off must be made.

X-ray Radiography

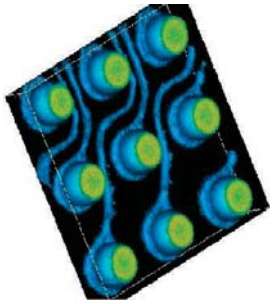
Applications and Examples

Typical applications include:

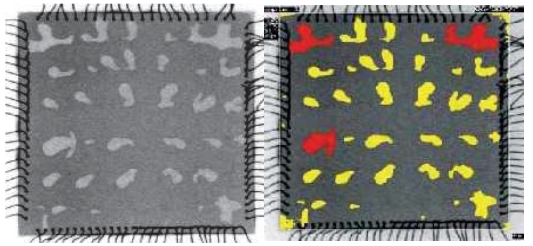
- Internal structures of electronic devices
- Connection techniques (Flip Chip, µBGA, BGA, MCM, COB)
- Inner layers of PCBs
- Popcorning *in situ* visualization



Applications: CT Visualization and Software



The computed tomography (CT) technique enables 3-dimensional inspection of planar components as seen in this BGA assembly.



Use of voiding calculation software enables the estimation of voided area observed in die attach. Given a nominal size area, voids can be color coded for easier visualization of areas larger than or smaller than these dimensions. The yellow represent normally sized voids, whereas, the red ones are larger.

Limitations of X-ray Techniques

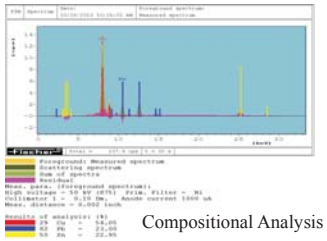
- Although considered a non-destructive test, X-ray radiation may change the electrical properties of sensitive microelectronic packages such as EPROMS, and hence should not be used until after electrical characterization has been performed on these devices.
- For samples on or below thick metal layers such as large heat sinks as seen in power devices, X-ray imaging is more difficult and requires high voltages and currents.
- Magnification using contact X-ray equipment can only be done externally by a magnified view of the 1:1 photo, or from an enlarged image of the negative. Hence, resolution will decrease as the image is enlarged.
- The operator may have to experiment with voltage settings and exposure times, depending on the type of sample and film used, to obtain proper contrast and brightness in the photos.

Discussion 2 – PTH Fill on Electrolytic Cap

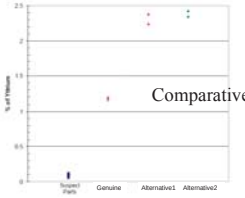
X-Ray Fluorescence (XRF)

Types of Analysis

- Spectrum analysis to determine the elements and the composition of an unknown sample.
- Material analysis for bulk samples (one layer sample)
- Thickness analysis to determine the thickness and the composition of different layers.
- Pure element and alloy standards (such as Ni, Cu, Ag, Sn, Au, Pb and SnAgCu or SnPb alloys) can be used to calibrate the spectrometer.

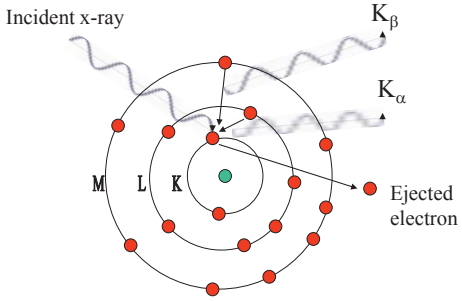


Compositional Analysis



Comparative Analysis

Background on X-Ray Fluorescence



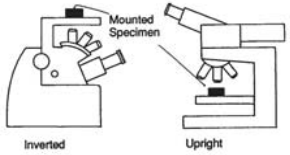
- Incident x-ray is incident on sample
- Core electron is ejected
- Electron from outer shell falls down to fill up the vacancy
- X-ray photon is emitted (energy equal to the difference between the two levels involved in the transition), which is characteristic of the element and the electronic transition

Conclusion

- XRF is a powerful tool to analyze composition and coating thickness on a variety of electronic products
- A non-destructive tool, does not require sample preparation, provides quick analysis results
- Users should be aware of the issues related to the automated analysis software

Visual Inspection

External Visual Inspection



Low power stereo macroscope (up to 65x)

- Overview
- Package level
- PCB level

Typical stereo macroscope

Higher power light optical microscopes

- Inverted
- Upright

Light Optical Microscopes

Resolution

Limit of Resolution $= \lambda / (2 \times N.A.)$

- λ , light wave length (eg 0.55 µm for green light)
- Numerical Aperture (N.A.), objective lens

For example,

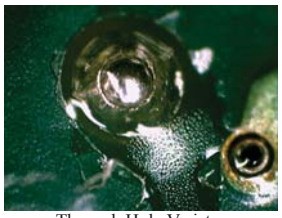
Combination of a 20x objective lens (N.A. = 0.40) with a 10x eyepiece

$$0.55\mu m / (2 \times 0.40) = 0.69\mu m$$

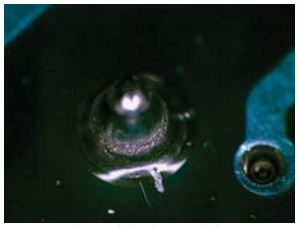
Analytical Techniques

- Environmental Scanning Electron Microscopy (ESEM)
- Energy Dispersive Spectroscopy (EDS)
- Thermo-mechanical Analysis
- Microtesting (Wire Pull, Ball Bond and Solder Ball Shear, Cold Bump Pull)
- Decapsulation / Delidding
- Dye Penetrant Inspection (Dye and Pry)

Discussion 3 – PTH



Through Hole Varistor



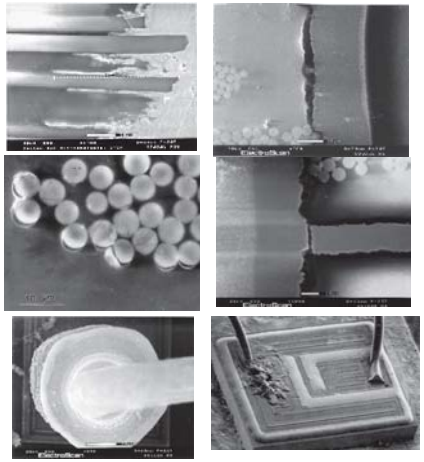
Through hole Cracking

What is the mode, mechanism and root cause (s) ?

Environmental Scanning Electron Microscopy

Applications and Examples

- Excessive wicking of copper in PTHs of a PWB
- Separation at the interface between the copper plating and the fiber epoxy resin board interface
- Fiber/resin interface delamination
- Corrosion and intermetallic growth at the bondpad under the gold ball bond
- Stress-driven diffusive voiding and hillock formation of Al metallization lines
- Metallization corrosion
- Wirebond fracture
- Passivation cracking
- Delamination at the die/die paddle interface
- Dendritic growth
- Electrostatic discharge/electrical overstress
- Wire fatigue
- Solder fatigue



Applications

- By eliminating the need for a conductive coating, ESEM allows imaging of delicate structures and permits subsequent energy-dispersive X-ray spectroscopy (EDS) compositional analysis.
- The ESEM can image wet, dirty, and oily samples. The contaminants do not damage the system or degrade the image quality.
- The ESEM can acquire electron images from samples as hot as 1500ºC because the detector is insensitive to heat.
- ESEM can provide materials and microstructural information such as grain size distribution, surface roughness and porosity, particle size, materials homogeneity, and intermetallic distribution.
- ESEM can be used in failure analyses to examine the location of contamination and mechanical damage, provide evidence of electrostatic discharge, and detect microcracks.

Limitations

- Large samples have to be sectioned to enable viewing in a SEM or an E-SEM, due to the limited size of the sample chamber.
- Only black and white images are obtained. Images can be enhanced with artificial color. Thus, different elements in the same area, having close atomic numbers may not be readily distinguished as in optical viewing.
- Samples viewed at high magnifications for extended periods of time can be damaged by the electron beam (e.g., fiber/resin delamination can be initiated this way).
- Areas having elements with large atomic number differences are not easily viewed simultaneously; increasing the contrast to view the low atomic number element effectively makes the high atomic number element appear white, while decreasing the contrast allows a clear view of the high atomic number element, the image of the low atomic number element is drastically compromised.
- Variations in the controllable pressure and gun voltage can allow samples to appear differently. Lower pressure and voltage give for more surface detail; the same surface can look smoother by just increasing the pressure. Therefore, sample comparisons before and after experiments, especially cleaning treatments should always be examined under the same conditions.
- Image quality is determined by scan rate; the slower the scan rate, the higher the quality. However, at lower scan rates, the image takes a longer time to be fully acquired and displayed. Therefore, sample movement appears visually as jerky motions. A trade off must be made between image quality and visual mobility.

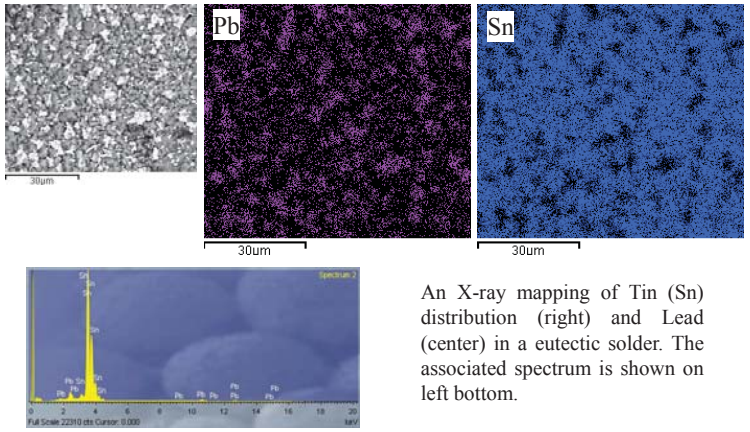
X-ray Spectroscopy

Applications

X-ray analysis can be used to detect:

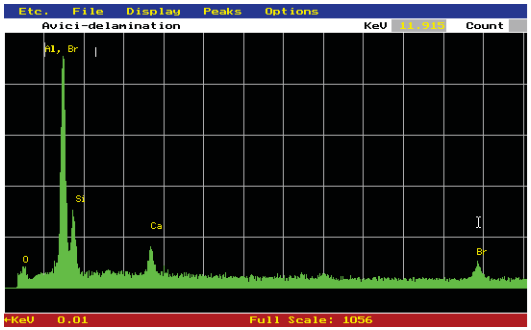
- Surface contamination (chlorine, sulfur)
- Presence of native oxides
- Corrosion
- Concentrations of phosphorus, boron, and arsenic
- Compositional analysis (i.e., Sn to Pb ratio)
- Conductive filament formation
- Intermetallic growth
- Elemental distribution using mapping techniques

X-ray Mapping



An X-ray mapping of Tin (Sn) distribution (right) and Lead (center) in a eutectic solder. The associated spectrum is shown on left bottom.

Acquired Spectrum Using EDS



The bromine and aluminum peaks overlap, at 1.481 and 1.487 KeV respectively. It is not clear, using EDS, whether or not aluminum is in this sample. Bromine is present, as evidenced by its second identified peak at 11.91 KeV. The elemental KeV values can be found on most periodic tables.

Limitations of EDS

- Resolution is limited, therefore it is possible to have uncertainties for overlapping peaks (i.e., tungsten overlap with silicon and lead overlap with sulfur)
- Cannot detect trace elements
- Limited quantitative analysis
- No detection of elements with atomic number < 6
- If a Beryllium window is used, cannot detect light elements such as carbon, nitrogen and oxygen with atomic number < 9
- Specimen must be positioned in such a manner that an unobstructed path exists from the analysis site to the detector.

Thermal Analysis Techniques

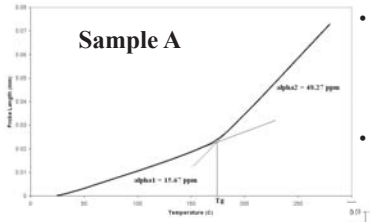
- DSC – Differential Scanning Calorimetry
  - Measures changes in heat capacity
  - Detects transitions
  - Measures Tg, Tm, % crystallinity
- TGA – Thermogravimetric Analysis
  - Measures changes in weight
  - Reports % weight as a function of time and temperature
  - Helps determine composition
- TMA – Thermomechanical Analysis
  - Measures changes in postion
  - Detects linear size changes
  - Calculates deflection, CTE, and transition temperature
- DMA – Dynamic Mechanical Analysis
  - Measures changes in stiffness
  - Measure deformation under oscillatory load
  - Determines moduli, damping, and transition temperature



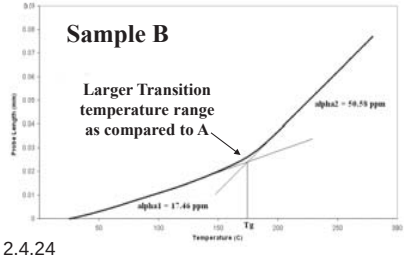

Thermal Techniques - Use

- All techniques are destructive to the sample
  - Sample will be heated above transitions
  - Will have to be cut to fit in instrument
- All techniques use small samples
  - 10 mg or so for DSC and TGA
  - Samples from 5 to 40 mm long for TMA and DMA

TMA (Samples A and B)*



- Coefficient of thermal expansion before glass transition temperature (alpha 1) and after glass transition temperature (alpha 2) is determined.
- Glass transition temperature (Tg) is also determined.



- Constant stylus force applied on the sample: 2 mN.
- Typical scan setup:
- Hold 1 minute at 25 C.
- Heating from 25° C to 280° C at 20° C/minute.

* - Sample preparation and test refer to IPC TM-650 2.4.24

Wire Pull, Ball Bond and Solder Ball Shear Testing

Microtesting Applications

The wirebond pull test is the most widely used method for assessing the quality and degradation of wirebonds and providing assurance that semiconductor devices will not fail in the field due to weak bonds.

The ball bond and solder ball shear tests provide methods for determining interfacial adhesion strength and effects of environmental conditioning or parameter changes, on the shear strength of the ball attachments. Variations in strength from ball to ball on a sample and from batch to batch are also monitored using these methods.

Although a die shear test is not commonly used, deterioration of or flaws in the die attach material can be assessed by this type of shear test.

Devices include:

- Plastic and hermetic packages,
- Multi-chip modules,
- Ball grid arrays, and PWB's used for BGA assembly

Equipment Overview

Applications include:

- Ball shear, aluminum wedge shear, and low force die shear using up to 5Kg force.
- Die shear testing up to 50Kg force
- Wire-pull testing up to 10Kg force.

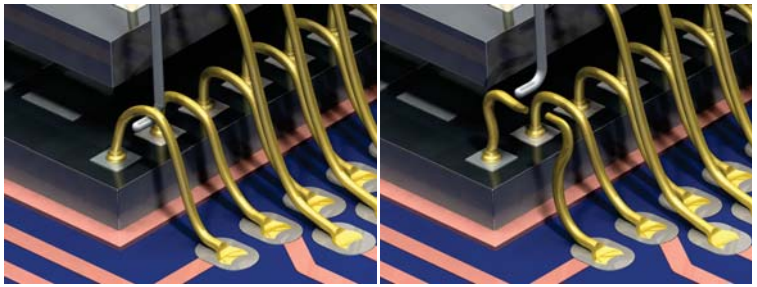
Dage 4000

Ref: nordson.com

Wire Pull, Ball Bond and Solder Ball Shear Testing

- Wirebonds interconnect chips, substrates, and output pins.
- Pull test and the ball bond shear test are simple mechanical tests to access the integrity of wirebonds, thereby ensuring reliable operation of electronic components.
- Wirebonds come in various forms, depending on the technique used to create them, and require different means of assessing their integrity.
- Electrical and mechanical attachment from component to substrate can be accomplished through pins, leads or solder ball ball attachments.
- Solder ball shear test allows one to access the effect of parameter changes such as pad plating type, pad geometry, cleaning methods, solder type, and ball size on the strength of the interfacial adhesion.

Principles of Operation (Wire Pull)



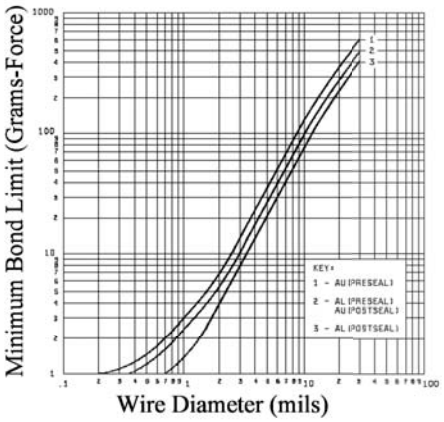
The procedure for obtaining optimal pull test results is as follows:

- Calibrate the equipment.
- Carefully place the hook in the center of the loop.
- Pull straight up, and record the value.

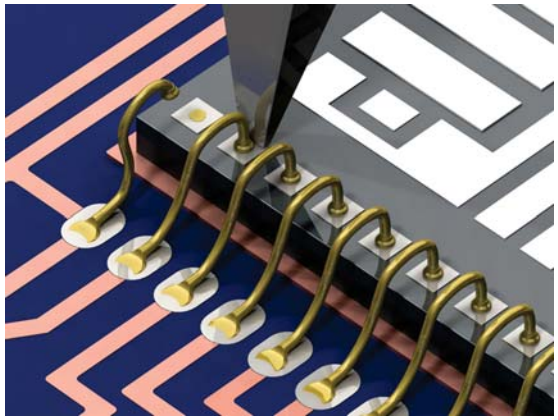
Ref: https://bondlab-qa.web.cern.ch/bondlab-qa/pull_tester.html

Wire Pull limits According to Wire Type and Diameter

(MIL-STD-883E)

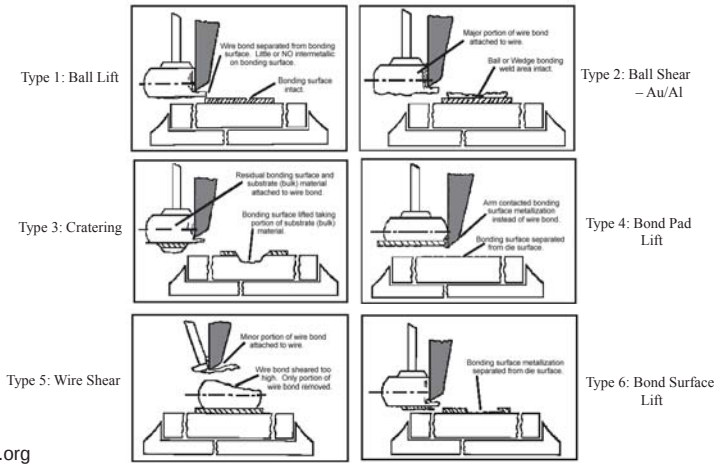


Ball Bond Shear



Ref: https://bondlab-qa.web.cern.ch/bondlab-qa/pull_tester.html

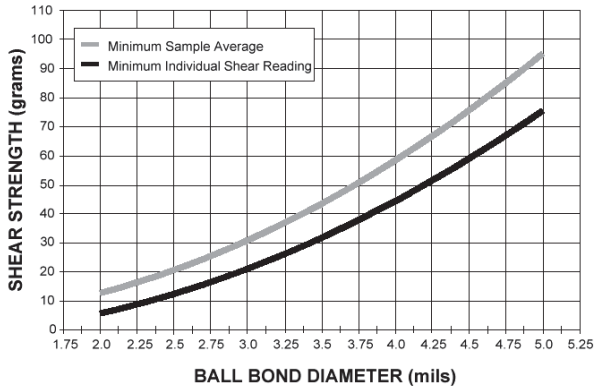
Ball Bond Shear Modes



Ref: jedec.org

Minimum Shear Values

(JEDEC Standard 22-B116)

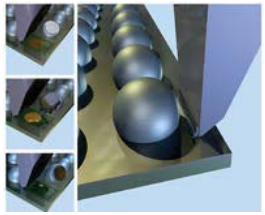


Ball Shear and Cold Bump Pull Tests

- Ball shear test and cold bump pull test are destructive tests conducted to determine solder ball attachment strength of Ball Grid Array (BGA) packages.
- Both ball shear test and cold bump pull test are quality evaluation test of BGA components.
- A substantial amount of literature has focused on the ball shear test on BGA components. Not much literature addressed on cold bump pull tests.

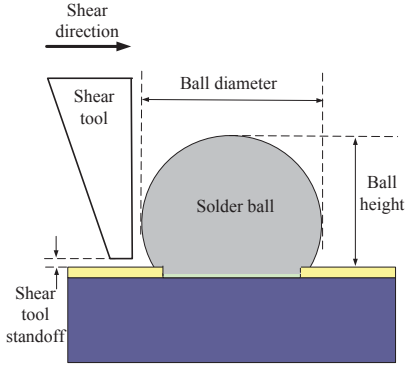
Ball Shear Test

- Ball shear test is a destructive test conducted to determine the ability of Ball Grid Array (BGA) solder balls to withstand mechanical shear forces. This test represents possible applied force during device manufacturing, handling, test, shipment and end-use condition.
- The industry standard used to conduct this test is: JEDEC JESD22-B117A (October, 2006)
- IPC-9701 also mentions the solder shear test.



Ref: solder Ball Shear, JESD22-B117A

Ball Shear Tool to Solder Ball Alignment

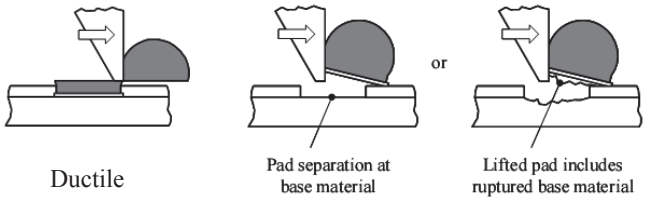


Shear tool standoff is the distance between the device planar surface and the shear tool tip. In JESD22-B117A, the shear tool standoff should be no greater than 25% (10% preferred) of the solder ball height. In IPC-9701, the shear tool standoff should be at least 50 µm.

Ref: solder Ball Shear, JESD22-B117A

Failure Modes of Ball Shear Test

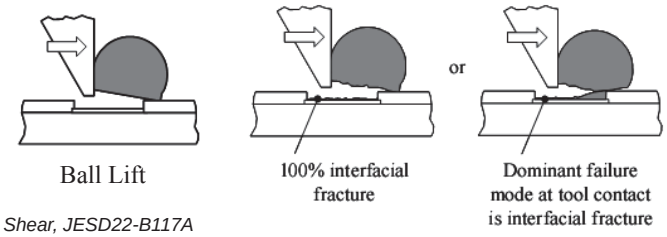
- Ductile – Solder ball fracture at or above the surface of the solder mask within the bulk solder material.
- Pad Lift – Solder pad lifts with solder ball; lifted pad may include ruptured based material.



Ref: solder Ball Shear, JESD22-B117A

Failure Modes of Ball Shear Test (Cont.)

- Ball Lift – Solder ball lifts from pad; pad is not completely covered by solder/intermetallic and the top surface of the pad plating is exposed.
- Interfacial Break – The break is at the solder/intermetallic interface or intermetallic/base metal interface. The interfacial fracture may extend across the entire pad or be the dominant failure mode at the tool contact region.



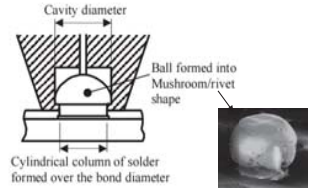
Ref: solder Ball Shear, JESD22-B117A

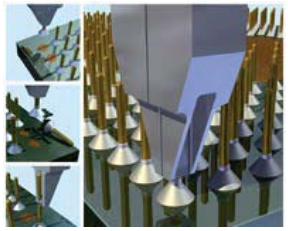
Cold Bump Pull Test Setup

- Cold bump pull (CBP) test is an alternative to the traditional ball shear testing method for characterizing the attachment strength of solder interconnection.
- CBP testing helps in evaluation of interface of all types of bumps. JEITA EIAJ ET-7407 outlines the method for cold ball pull testing.

Test setup

- Equipment: DAGE 4000, load cell: CBP/TP 5Kg
- Jaw close time: 1.8 sec
- Pull speeds: 500µm/sec and 5000µm/sec

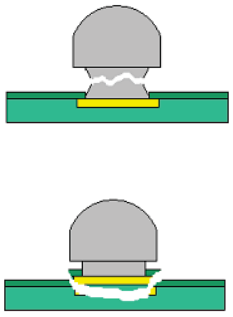




Ref: nordson.com and EIAJ ED-4702A

Failure Modes

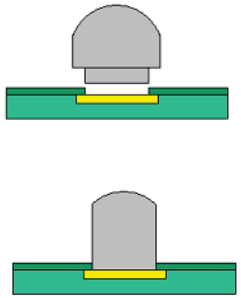
- Ball failure
  - Solder ball facture in the bulk solder materials.
- Pad failure
  - The pad peels off of the substrate or fractures in the substrate materials.
  - Possible pad design problem may lead to this failure.



Ref: nordson.com and EIAJ ED-4702A

Failure Modes (Cont.)

- Bond failure
  - Failure occurs when the separation is at the interface of the solder and the pad.
  - Possible process or material problems may lead to this failure.
- Ball extruded
  - Failure occurs when the ball deforms into a cylinder shape due to the jaws pulling away excess solder without producing a bulk solder failure.
  - Setup of the pull test has a problem or the solder material is very soft.



Ref: nordson.com and EIAJ ED-4702A

Limitations of the Techniques

As applied to degradation analysis, both the wire-pull test and the ball bond shear test are destructive, since the package has to be decapsulated or delidded and the wire/ball bonds broken.

Only in cases of catastrophic failure, such as low-temperature impurity-driven intermetallic growth, will the destructive wirebond pull test yield information other than the relative breaking strength of the wire at the weakened neck area. Thus, it has to be supplanted by the ball bond shear test.

The presence of intermetallics provides a site for fatigue crack initiation. However, since the intermetallics are much stronger than both the gold and aluminum, the ball bond shear strength need not be lowered when they are present, and could be missed by a ball shear test. In such cases, where electrical resistances could increase along with ball bond shear strength in the early stages of intermetallic growth, other evaluation techniques are necessary.

Ref: nordson.com and EIAJ ED-4702A

Limitations of the Techniques

Varying parameters such as shearing tool velocity, height, planarity of surface, wire pull test speed or angle could all affect resulting data; for relative comparisons, all parameters should be kept constant.

Only by using a microscope attachment and visually monitoring every test from start to end, will reliable results be obtained. When the shear test is initiated, the shear tool automatically moves up to a preset height and then shearing is initiated. If the tool scrapes on debris or an uneven surface while shearing the ball, the resulting shear strength may be too high.

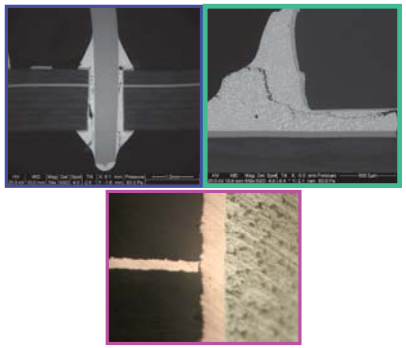
Metallographic Sample Preparation*

*- Adapted from Buehler Limited/ITW

What Is Micro-sectioning of Printed Circuit Board?

Technique used to evaluate printed wiring board quality by exposing a cross-section at a selected plane such as

- **Plated through-holes**
- Plating thickness
- Via
- **Soldered connections**
- Delamination in PCB
- **Inner layer connections**



Primary Purpose of Micro-sectioning

- To monitor the processes rather than to perform final inspection because it makes no sense to add value to a product that is already rejectable!
- Therefore, the objective is to detect any deviations from normal in the manufacturing processes as early as possible to avoid adding value to a defective product. Corrections to the process should then be made as soon as possible.

Goal of Specimen Preparation

Reveal the true microstructure of all materials

- Induce no defects during specimen preparation
- Obtain reproducible results
- Use the least number of steps in the shortest time possible
- Achieve a cost effective operation

Goal of Specimen Preparation for Failure

Failure to obtain these goals can affect the microstructure as follows:

- Details in soft ductile phases may be hidden by smeared materials
- Hard constituents such as silicon may be fractured
- Fine precipitates may be removed, leaving pits that could be misinterpreted as porosity
- Critical edges may be rounded causing a loss of visual information
- Hard constituents in highly dissimilar materials could experience relief making an accurate analysis difficult

Preparation Steps

'Each step is equally important"

- Documentation
- Sectioning
- Mounting
- Grinding and Polishing
- Visual Examination
- Etching
- Analysis

Documentation

- Process data: vendor, material, batch #, part #, sampling
- Description of specimen orientation, location, cut area, Macro image
- Type of analysis and defect, area of interest
- Record mounting, polishing, etching parameters
- Record microstructure data: inclusions, porosity, grain size, etc.

Sectioning

- Equipment
- Blade, wheel (SiC, alumina, diamond)
- Load
- Blade RPM
- Feed rate
- Coolant
- Delicate materials may require encapsulation or chuck padding for holding

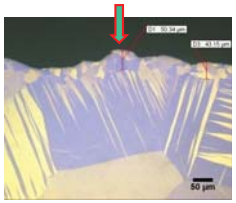
Methods

Method	Comments
Shearing	Severe torsion damage to an undetermined distance adjacent to the cutting edges
Hollow punch (Saved hole)	Convenient, and rapid but limited to boards 0.08" thick or less
Routing	Rapid and versatile with moderate damage but noisy and hard to control.
Band saw	Rapid, convenient moderate damage and easy to control when a 24-32 pitch blade is used at 3500-4500 ft./min.
Low speed saw	Least damage of any method allowing cuts to be made even into the edge of the plated through-hole barrel. However, it is too slow for high volume micro-sectioning.
Precision table saw	Least destructive method of removing specimens from component mounted boards for soldered connection analysis

Sectioning damage

Method	Type of damage	Possible depth
Shearing	**Deep mechanical damage**	**5 mm**
Band / hack saw lubricated not cooled	**Moderate thermal and mechanical damage**	**2.5 mm**
Dry abrasive cutting	**Moderate to severe thermal damage**	**1.5 mm**
Wet abrasive cut-off saw	**Minimal thermal and mechanical damage**	**250 µm**
Diamond / precision saw	**Minimal thermal and mechanical damage**	**50 µm**

Sectioning Damage - Zinc

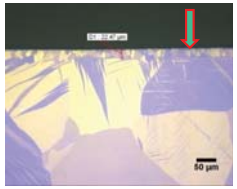


Band saw recrystallization depth ~50 microns

Note the jagged edge and heavy mechanical twinning will prolong grinding time

Abrasive wheel recrystallization depth ~ 30 micron

Some mechanical twinning



Precision blade recrystallization depth ~20 microns

Minimum area of twinning

Mounting Principles

- Sample encapsulated in epoxy, acrylic or other compound
- Sample edges protected during polishing process
- Delicate samples protected from breakage
- Smooth mount edges increase life of polishing surfaces
- Allows automation and ability to prepare multiple samples simultaneously
- Uniform pressure on mount maximizes surface flatness
- Safety

Mounting Method Selection

Castable (cold) mounting
- Resin/hardener selection
- Vacuum
- Additives for edges, conductivity

Compression (hot) mounting
- Compound selection
- Pressure
- Heat

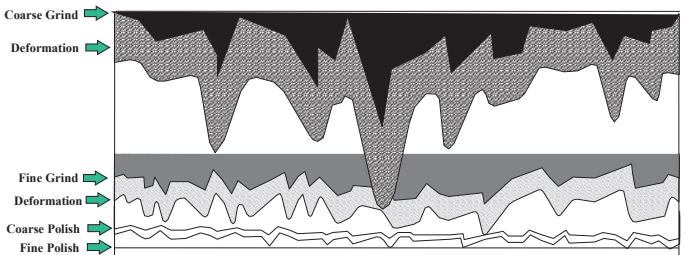
Specimen characteristics to consider:
- Softening/melting temperature
- Sample thickness, ability to withstand pressure
- Brittleness, friability
- Porosity
- Hardness & abrasion resistance relative to mounting compound
- Importance of edge retention

Potting Compounds

Resin of Choice?…EPOXY!

- **Low shrinkage and moderate hardness are important for microelectronics.**
  - **Less surface relief**
  - **Better edge protection**
- **Uncured epoxy typically has low viscosity for filling small cavities.**
- **Epoxy can be cast while under vacuum. This enhances its cavity filling ability.**

Damage



Incremental Removal of Damage

Each abrasive step leaves deformation. As abrasive size is reduced, less deformation is left behind.

Grinding Steps

- The initial grinding surface depends on the condition of the cut surface – more damaged surfaces require coarser first-step grinding
- For excessive damage, re-sectioning with an abrasive or precision saw is recommended
- A single grinding step is adequate for most materials sectioned with an abrasive or precision saw
- Softer materials require multiple grinding steps and smaller abrasive size increments
- Remove damage with progressively smaller abrasive particle sizes
- With decreasing particle size:
  1. Depth of damage decreases
  2. Removal rate decreases
  3. Finer scratch patterns emerge

Polishing Principles

- Further refinement of ground surface using resilient cloth surfaces charged with abrasive particles
- Depending on material characteristics, cloth selected may be woven, pressed or napped
- Commonly used abrasives are diamond and alumina
- The polishing process consists of one to three steps that:
  1. Remove damage from the last grinding step
  2. Produce progressively finer scratches & lesser depth of damage
  3. Maintain edges and flatness
  4. Keep artifacts to an absolute minimum

Time

- Each step must remove the surface scratches and sub-surface deformation from the previous step
- Increase time to increase material removal
- Smaller increments in abrasive size require shorter times at each step
- Increases in surface area may require longer times
- Too long times on certain cloths can produce edge rounding and relief

Additional Considerations

- Bevel mount edges to increase cloth life
- Clean specimens and holder between steps to prevent cross contamination of abrasives
- Ultrasonic cleaning may be required for cracked or porous specimens
- Dry thoroughly with an alcohol spray and a warm air flow to eliminate staining artifacts
- Remove polishing debris by rinsing cloth surface after use to increase cloth life

Final Polishing Principles

- Removes remaining scratches, artifacts and smear
- Produces a lustrous, damage-free surface
- Maintains edge retention
- Prevents relief in multiphase materials

Etching Principles

- Etching is a process of controlled corrosion
- Selective dissolution of components at different rates reveals the microstructure
- Completion of etching is determined better by close observation than timing
- Etching is best performed on a freshly polished surface before a passive layer can form
- A dry surface produces a clearer etched structure than a wet one
- An under-etched surface may be re-etched but an over-etched surface requires re-polishing

Etching Techniques

- Immersion – sample immersed directly into etchant solution
  - Most commonly used method
  - Requires gentle agitation to remove reaction products
- Swab – polished surface swabbed with cotton ball soaked with etchant
  - Preferred method for materials in which staining is a problem
- Electrolytic – chemical action supplemented with electric current
  - Attack controlled by chemical selection, time, amps

PWB Etchants (For Copper)

- Equal parts 3% H_2O_2 and ammonium hydroxide, swab for 3 to 10 seconds, use fresh etchant to reveal grain boundaries of plating and cladding copper material.

- 5 g $Fe(NO_3)_3$, 25 mL HCl, 70 mL water, immerse 10 – 30 seconds, reveals grain boundaries very well.

Decapsulation of Plastic Packages

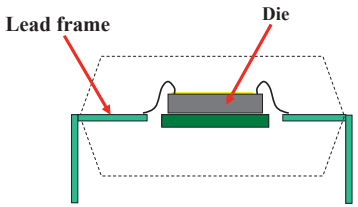
Decapsulation is the removal of the encapsulant from a plastic encapsulated microcircuit (PEM) to expose the die and the interconnects for failure examination with the aid of other techniques, such as optical microscopy, electron microscopy, energy dispersive X-ray spectroscopy, and ball-bond and die shear and wire pull testing.

Decapsulation can be accomplished by any of three methods:

1. Mechanical Decapsulation
2. Chemical Decapsulation
   - Manually
   - Automated
3. Plasma Etching

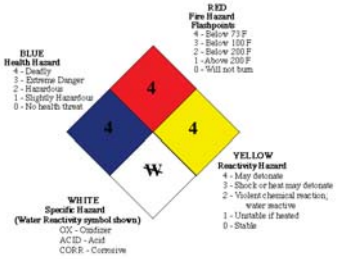
Mechanical Decapsulation

Mechanical decapsulation is achieved by sanding the back of the package to reveal the back of the leadframe, heating the package on a hot plate to approximately 200°C to soften the molding compound, and then prying the paddle and die from the package with a scalpel. This type of decapsulation is preferred when there is concern about exposing the die surface to chemicals. For situations requiring ball-bond shear or wire-pull tests, mechanical decapsulation is not an option, as the process will displace bonds and break wires.



Important – Laboratory Safety

- **Chemical**
  - Clean up Spills
  - Label
  - MSDS
  - Safe Disposal
- **Personal protection equipment**
  - Safety glasses / goggles
  - Gloves
  - Apron
- **Facility**
  - Hood
  - Eyewash
  - Shower



Chemical Decapsulation (Manual)

Manual Decapsulation Procedure

1. Using a drill press and the milling tool bit (about half of the width of the plastic package), drill a cylindrical hole from the top center of the plastic package. The depth of the hole should be about one-third of the package thickness. (It is not advisable to use a regular drill bit in place of a milling tool because the resulting conical hole is undesirable.)
2. Place the drilled package on a scrap metal plate and heat it on a hot plate to about 80°C.
3. While the package is being heated, prepare a squeeze bottle of acetone and a small amount (~5 ml) of red fuming nitric acid in a small glass beaker.
4. Using a Pasteur pipette, drop 1 to 2 drops of red fuming nitric acid in the hole of the heated package. Rinse away the dissolved plastic with acetone in a waste glass beaker after the fumes die away. Repeat until the microcircuit is exposed.

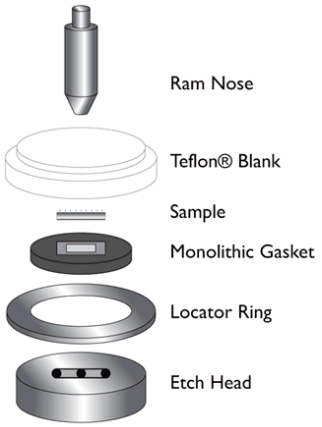
Automatic Chemical Decapsulation*

- Does every part use the same "recipe“?
  - No. While groups of parts may have similar recipes, you will have to adjust recipe to meet the requirements of your sample.
- Decapsulation times can vary depending on the thickness of encapsulant, package size (length and width), and ease of encapsulant removal.
  - General rule: the thicker the part (i.e. the more plastic), the longer the etch time.
  - Some samples, such as BGAs manufactured in the late 1990s/early 2000s, will require a high temperature sulfuric acid as the etchant.
- Other etch parameters may also be affected by the characteristics of the device to be etched. Example include:
  - Whether the sample has been "burned in“
  - Samples with heatsinks
- Nitric acid is the recommended acid to start with on all parts; however, use sulfuric acid as well.

Ref: nisene.com

Example of a "stack-up"

A Typical Monolithic Gasket Stack-up



Ref: nisene.com

Chemical Decapsulation – Die Size

- Die size can be determined two ways:

X-ray part to determine die size

- Set the sample on the X-ray stage and capture the image using image-capturing software.
- Print the captured image at a 1:1 ratio and make measurement of the die within the package.
- Select the appropriate gasket based on the dimensions.

Start with small decapsulation hole in your gasket and work out if too small

- Select a gasket with a small aperture that is obviously smaller than the die.
- Etch the sample until you start to see the surface of the die.
- Continue to etch outward toward the edge of the die until all sides are exposed (if desired for your application).
- Select new gasket based on the size of the die. This can be done by visual approximation ("eyeballing"), but exact measurements may be taken at this step if desired.

- X-ray provides a quicker method of determining die size, since this information is available immediately; however, not all facilities have x-ray on site.

Ref: nisene.com

Limitations

- Chemical decap only works for plastic-encapsulated parts (and other similar epoxies).
- Mechanical decap is used for ceramic parts.
- Some parts contain passivation layers over the die. In some cases, the decapsulation process ceases here and further chemical removal techniques may need to be employed.
- Heatsinks must be removed prior to decap. Decapsulation does not etch (most) metals.
- Samples with copper wiring require more trial and error before finding a proper set of etch parameters, but tend to be very uncommon in the counterfeit distribution world.

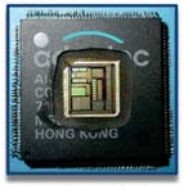
Post-Decap Inspection Criteria

- Overview optical image of the decapsulated device.
- Higher magnification image (min 500X) showing only the die. Attributes to document:
  - Manufacturer markings
  - Name
  - Logo
  - Unique image
  - Die part numbers
  - Die mask ID numbers
  - Year of design
  - Number of metal layers
  - Pin 1 bond pad outline
  - Bond wire material
  - Bond wire diameter
  - Bond types
    - Thermal sonic
    - Crescent with or without safety bonds
    - Ultrasonic bonds
    - Compound bonds

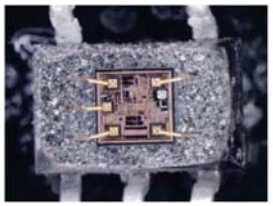
Ref: nisene.com

Decapsulated Part Inspection

1x Magnification:
Before Decapsulation



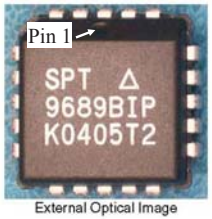
1x Magnification:
After Decapsulation*



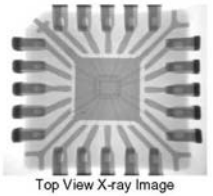
Showing logo identification*

Optical images of a decapsulated part

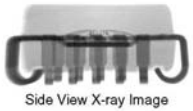
Fairchild 20L PLCC Dual Ultra-fast Voltage Comparator



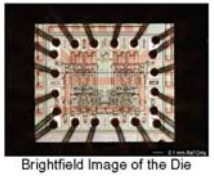
External Optical Image



Top View X-ray Image



Side View X-ray Image



Brightfield Image of the Die

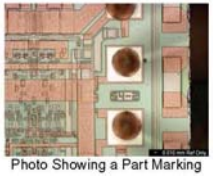


Photo Showing a Part Marking

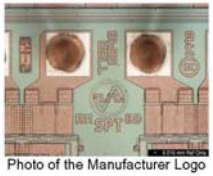
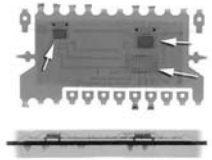


Photo of the Manufacturer Logo

Ref: nisene.com

MACOM 24P SOW (Small Outline Wide) Multichip Digital Attenuator

External Optical Image



Top and Side View X-ray Images Showing the Locations of Three Dice (arrows)

Photo of the Decapsulated Device With All Three Dice Exposed

Ref: nisene.com

Plasma Etching

- Radio frequency (RF) energy source is used to ionize gas in a reaction chamber.
- Ionized gas attacks the plastic and the integrated circuit's layer materials.
- Plasma treatment has proven valuable because of its selectivity, gentleness, cleanliness, and safety.
- However, the time involved in opening an entire package with plasma time is too long for routine use and limits its application to the more critical failure analysis studies.
- Plasma etching is typically used as an alternative method only for final removal of residual encapsulant material in devices where residue still persists after chemical decapsulation.

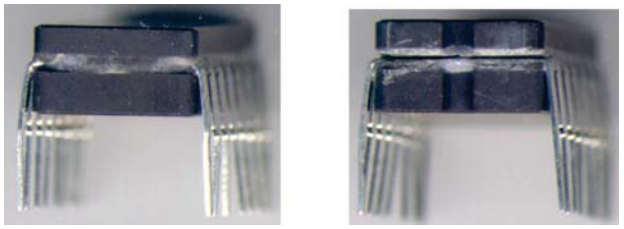
Delidding of Ceramic/Metal Lid Packages

Delidding a cavity-type hermetic package is more straightforward than removing plastic encapsulants; there are no parameters or acid types to select.

To delid a ceramic package with a ceramic lid, the following procedure can be used:

1. Grip the base of the package in a vise or clamp.
2. Carefully score around the glass seal between lid and base with a scalpel or similar sharp instrument.
3. Insert a small flathead screw driver in a corner of the scored area between the lid and base, and gently twist until the cover pops off. For samples not completely scored all around the perimeter, breakage - as opposed to popping off the complete lid - may occur.

Ceramic Package Scoring Prior to Delidding

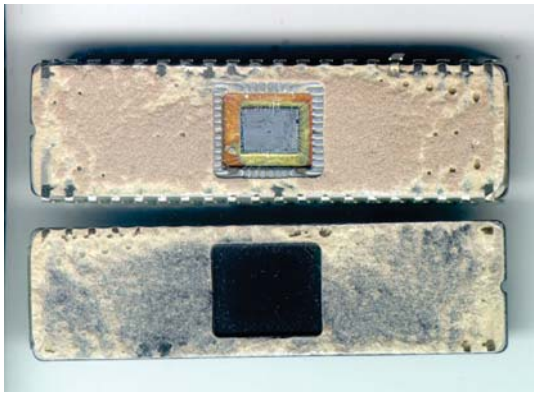


A **B**

A ceramic package can be seen before (A) and after scoring the glass seal around the perimeter between the lid and the base (B) in preparation for delidding.

Ref: engr.uconn.edu

Ceramic Package Delidded



Picture of a delidded hermetic ceramic package. Notice that there are some voids in the top right side of the ceramic base.

Ref: engr.uconn.edu

Applications (Chemical Decapsulation)

1. Exposes the die circuitry, and interconnections for inspection using optical and electron microscopy
2. Allows for mechanical wire pull, ball shear and die shear testing
3. Since the decapsulation procedure, if correctly done, is not destructive to the operation of the device, it can permit thermal profiling of the die surface in operation (i.e., identification of hot spots - usually the first areas of failure),assuming that the devices are stored in an inert environment

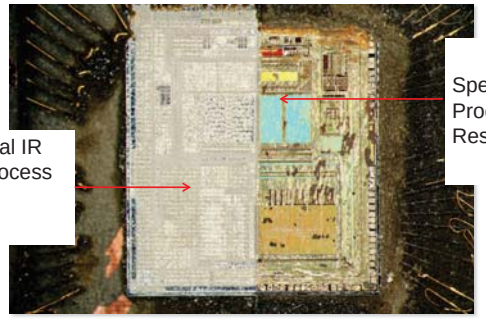
Limitations (Chemical Decapsulation)

1. Can only expose die circuitry and interconnections in plastic packages and where the die circuitry is facing the exterior of the package (i.e., not applicable to ceramic, metal cased or flip chip packages)
2. Is difficult to expose the complete die in chip scale packages since the etched cavity is cone shaped, and not much surface distance from die package exterior
3. Over etching can cause the die attach material to be removed and deposited on the die surface, or around bond pads, appearing as dentritic growth
4. Areas in plastic packages that are burnt, charred, or ESD damaged, are highly resistive to the chemical etching
5. Damage to die circuitry can occur in non-passivated devices
6. May remove evidence of bond pad corrosion

Laser Ablation

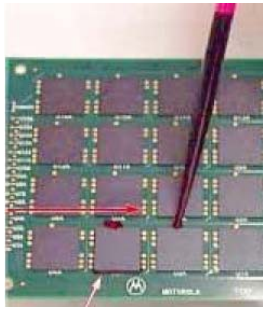
- Laser ablation is used to remove the majority of the plastic mold compound.
- Current laser technology is limited to removal of plastic only so as to not damage the die surface.
- Samples are laser ablated to just above the die surface, without making contact at any point with the die surface.
  - Once finished the sample is completed using an automated or manual chemical decap processes.

Laser Decap - Old vs. Newer Technology



Dye Penetrant (Dye and Pry)

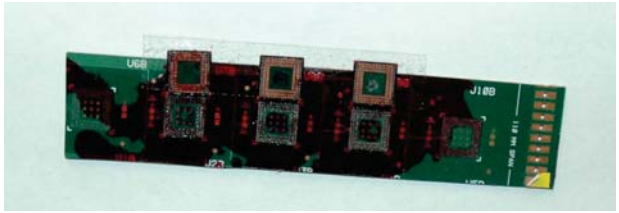
- Identify failed components (electrical measurement)
- Boards are immersed in stripping agent (Miller-Stephenson MS-111) for 25 min at room temperature to remove the solder mask. IPA can be used for a final rinse. Dry in air.
- Dye is applied to the board (DYKEM steel red layout fluid) with a pipette. Important: Flip the board, so that the dye flows into the cracks
- Place boards in vacuum for 5 minutes so that the dye penetrates into fine cracks that otherwise would be blocked by trapped air pockets. A strong vacuum pressure is not important for this process (Typical 220 mm Hg)
- Place the board on a hot plate for 30min 80° C to dry the dye (as prescribed by DYKEM).



Picture: "Solder joint failure analysis" **Dye penetrate technique**
BY TERRY BURNETTE and THOMAS KOSCHMIEDER

Dye and Pry Steps

- Flex the board with a pair of pliers until the components peel away.
- Remove the components with tweezers and fix with double sided tape on the board, because it is important to see the component side and the substrate side to identify the failure site.

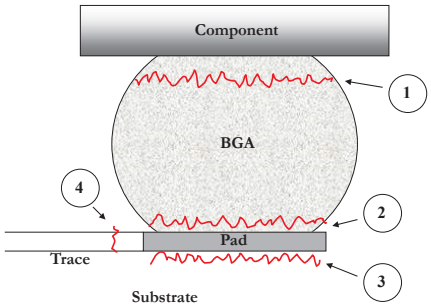


Picture: "Solder joint failure analysis" **Dye penetrate technique**
BY TERRY BURNETTE and THOMAS KOSCHMIEDER

Potential Nonconformities

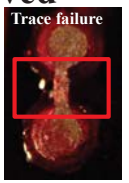
(For BGAs)

1. Solder Fail (component side)
2. Solder Fail (substrate side)
3. Pad Lift
4. Trace Fail



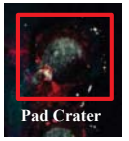
Dye and Pry: Failure Sites Observed

(a) Failure on board side



(b) Trace failure

(b) Failure on component side



(d) Pad crater

Miscellaneous Failure Analysis Techniques

Focused Ion Beam Etching

FIB Introduction

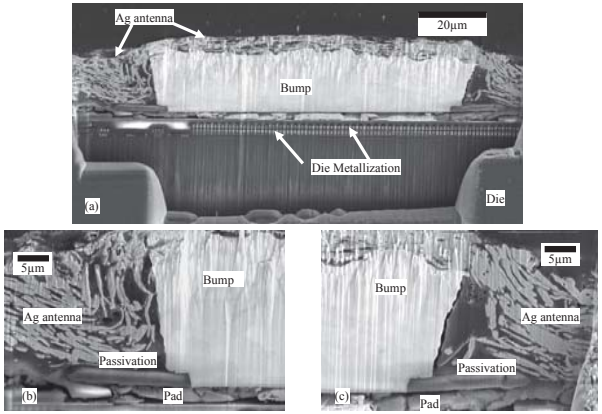
- Focused ion beam (FIB) processing involves directing a focused beam of gallium ions onto a sample.
- FIB etching serves as a supplement to lapping and cleaving methods for failure. The beam of ions bombarding the sample's surface dislodges atoms to produce knife-like cuts.

FIB Cross-section of Bumps

SEM image of a die-bump interface after FIB etching. Overview of the interface in

(a) shows the bump, die and silver antenna,

(b) and (c) show close up of the bump at two sides.



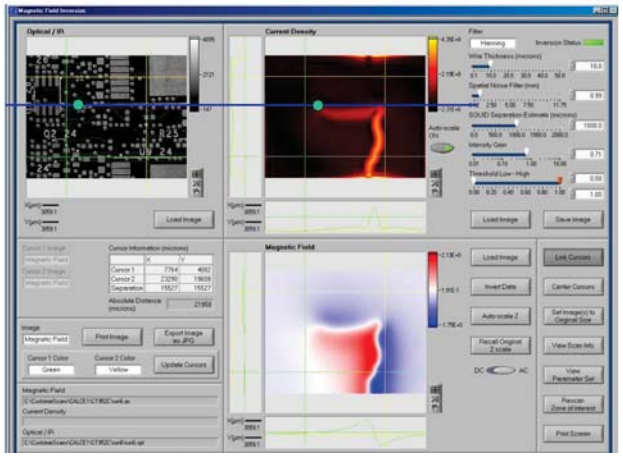
Ref: Sood, Bhanu, et al. "Failure site isolation on passive RFID tags." Physical and Failure Analysis of Integrated Circuits, 2008. IPFA 2008. 15th International Symposium on the. IEEE, 2008.

Focused Ion Beam Limitations

- Equipment is relatively expensive
- Large scale cross-sectional analysis is impractical since the milling process takes such a long time
- Operator needs to be highly trained
- Samples could be damaged or contaminated with gallium
- Different materials are etched at different rates, therefore uniform cross-sectioning using ion milling is not always possible

Superconducting Quantum Interference Device (SQUID) Microscopy

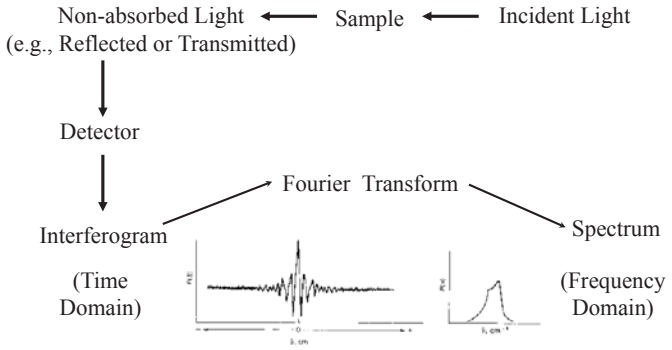
Magnetic Imaging Used to Locate Failures



Ref: Sood, Bhanu, and Michael Pecht. "Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants." Journal of Materials Science: Materials in Electronics 22.10 (2011): 1602-1615.

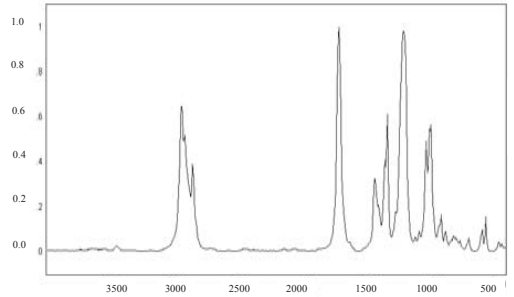
Spectroscopy, including Fourier Transform Infrared Spectroscopy (FTIR)

Fourier Transform Infrared Spectroscopy – Spectrum Production



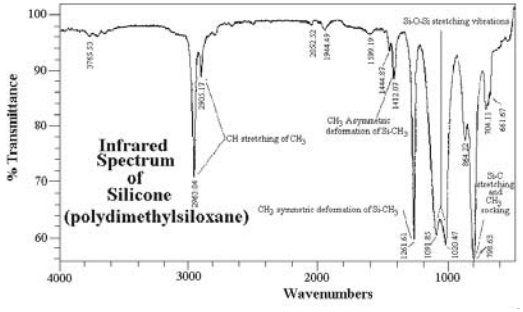
Properties of an Infrared Spectrum

- An infrared spectrum contains absorption peaks corresponding to the frequencies of vibration of the atoms of the molecules making up the sample.



Infrared Spectrum of Acetic Acid Butyl Ester

Fourier Transform Infrared Spectroscopy – Spectrum Interpretation



Correlation with charts of characteristic absorption frequencies ⟶ Identification of material

Ref: ChemAnalytical LLC: FT-IR Spectra

Engineering Applications of FTIR

- Materials identification and evaluation
  - Identification of unknown inorganic and organic materials by comparison to standards and by molecular structure determination
  - Determination of the locations of known and unknown materials
  - Determination of material homogeneity
- Failure analysis
  - Identification of contaminants
  - Identification of corrosion products
  - Identification of adhesive composition change
- Quality control screening
  - Comparison of samples to known good and known bad samples
  - Comparison of materials from different lots or vendors
  - Evaluation of cleaning procedure effectiveness
  - Identification of contaminants

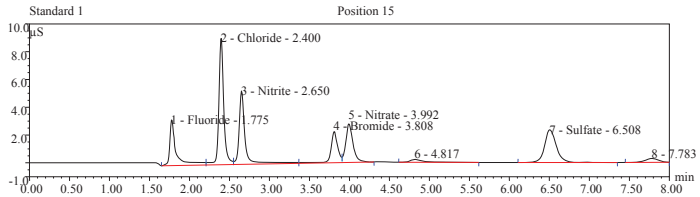
Chromatography

Ion-exchange Chromatography

- Ion exchange chromatography exploits ionic interactions and competition to realize analyte separation.
- It can be further classified into
  - cation exchange chromatography (CEC): separates positively charged ions; and
  - anion exchange chromatography (AEC): separates negatively charged ions.
- The output of an IC test is a graph of conductivity versus time.
- Calibration is with standards of known composition (elution time) and concentration (peak area).

Example of IC Results on a Mixture of Anions

- The eluent was 0.01 mol/L NaOH.
- The column used was an Dionex AS11.



- Based on the retention time, the type of ions can be determined with comparison to standard ions.
- Based on the area under the peaks, the concentration of the ions can be determined.

Ref: Dionex AS11 Carbon Eluent Anion-Exchange Column

Applications of Ion Chromatography in Electronics Reliability

1. Tests on assembled or bare printed wiring boards (PWBs) to relate cleanliness to electrochemical migration.

2. Determination of amount and type of extractable ions present in encapsulation materials to relate amount and type of ionic content to corrosion failure.

3. Electroplating chemistry analysis to relate breakdown products to plating adhesion failure.

Ref: IPC-TM-650 Test Method No. 2.3.28

PCB Supplier Evaluation Study

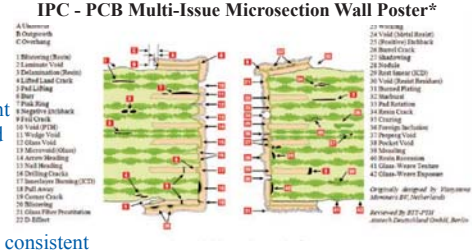
Study Objective

- Evaluate a subset of GSFC PCB suppliers (direct or indirect) and corresponding PCB coupon microsection testing data.
- Develop a methodology for data generation and collection to provide trend analysis
  - Identifies/predicts violation of a process limit criteria (in case of an egregious NC).
- Provide analysis for severity categories of the nonconformance.
- Provide recommendations to the suppliers (i.e. supplier quality engineering, continuous process monitoring, quality metrics definition).

Microsectioning

- Suppliers perform microsectioning and inspect per specifications.
- Secondary GSFC independent microsection analysis yielded 20-30% inspection rejects, caused by:
  - Screening escapes:
    - Test sample quality not consistent
    - Supplier microsection process, inadequate coupons
  - Requirement interpretations
  - Requirements flow-down issues
    - Alternative specifications (MIL, ECSS)
    - Buying heritage and off-the-shelf designs

IPC - PCB Multi-Issue Microsection Wall Poster*



* - https://blog.ipc.org/2010/11/22/pcb-multi-issue-microsection-wall-poster/

Requirements, Nonconformance, Data Generation and Collection

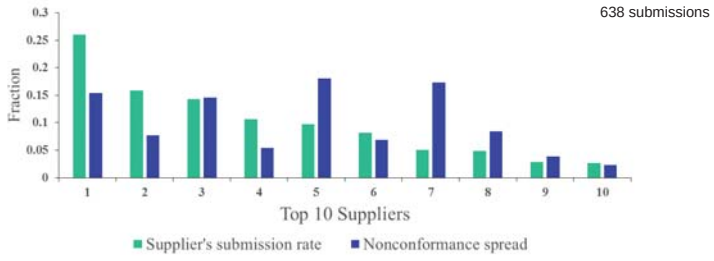
- Present study evaluates only the microsections performed by GSFC.
  - PCB coupon microsection evaluation in accordance to IPC Standard (IPC-6018B Class 3, IPC-6012C Class 3/A).
  - Coupon evaluation reports were generated, identified non-conformances.
- All PCB coupon testing results from all GSFC suppliers were recorded for the past 3 years (from 2015 – present)
  - Data include nonconformance and conformances in accordance with IPC Standards.
  - Total number of data points are approximately 882 jobs.
  - Each job has number of nonconformance with different severity.

Study Methodology

- Since 2015, received and analyzed 882 PCB coupon submissions from PCB suppliers.
- Top ten suppliers sent 638 submissions.
- Total nonconformance observed: 260

- For each supplier, analyzed nonconformance (s)
  - Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
  - Classifying and analyzing top 5 severity categories.

Data Analysis –Submission and Nonconformance for Supplier



$$\textit{Supplier submission rate} = \frac{\textit{total submission by individual supplier}}{\textit{total submission by all suppliers}}$$

$$\textit{Nonconformance spread} = \frac{\textit{total nonconformance by individual supplier}}{\textit{total nonconformance by all suppliers}}$$

Classification and Analysis - Top 5 Nonconformances

Twenty one distinct conformances observed among the ten suppliers

NC	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greather than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminate cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess of 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil	IPC 6012B Class 3/A
T	Dielectric thickness less than 3.0 mil min	IPC 6012B Class 3/A
U	Laminate void greater than 3.0 mil	IPC 6012B Class 3/A

Common Nonconformances from suppliers

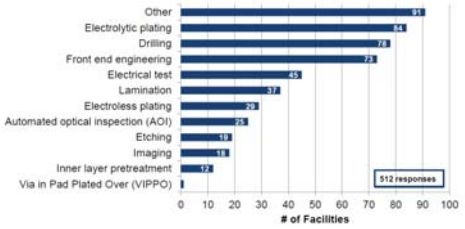
PCB Suppliers →

1	2	3	4	5	6	7	8	9	10
A	F	E	K	A	N	E	E	A	E
B	G	D	F	F	O	P	A	F	F
C	H	B	L	D	F	C	D	S	T
D	A	I	J	J	E	D	F	D	U
E	D	J	A	M	P	Q	R	P	R

Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to implement techniques which may eliminate theses nonconformances from at least 7 suppliers.

(A) Inner layer separations/inclusions
(D) Separation/inclusions between plating layers
(E) Copper wicking in excess of 2.0 mil
(F) Internal annular ring less than 2.0 mil
(J) ENIG is less than the minimum requirements

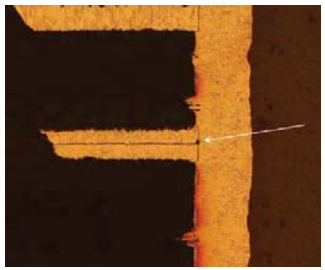


** - "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.*

Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in

Risk: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)



1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

Inner Layer Separations or Inclusions

Contributors

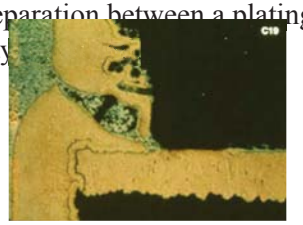
- Improper lamination press or cure cycles whether it be pressure, time, temperature.
- Others include inadequate coverage of inner layer oxide, moisture not completely removed in pre-lamination bake cycle.
- Bad batch of prepreg and or laminate.
- Post electroless copper cleaning

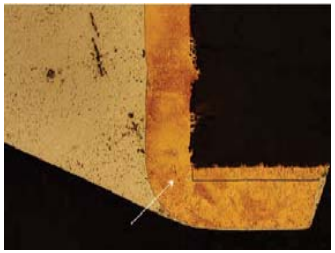
Resolution

- Consistency in drilling processes.
- Reduce the resin content in the stack up.
- Good desmear, with adequate texture.
- Provide adequate copper border for support and resin venting

Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating lay





Risk: intermittent electrical open or complete opens due to mechanical or thermal stresses.

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

Separation or Inclusions Between Plating Layers

Contributors

- Incomplete wrap plating
- Overly-aggressive cleaning process
- Insufficient cleaning

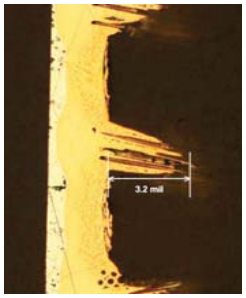
Resolution

- Adjust plating parameters
- Optimize cleaning processes

Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.

Risk: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.



1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Copper Wicking in Excess of 2.0 mil

Contributors

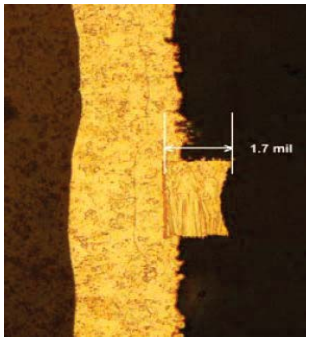
- Dull drill bits or broken drill bits that causes a crack in the laminate.
- Incompatible laminate material
- Insufficient glass etch.
- Poor glass to organic adhesion.

Resolution

- Optimize desmear parameters
- Improve drilling operation (feed and speed).
- Ensure sufficient resin wet-out of glass fibers (siloxane treatment).

Internal Annular Ring Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.



Risk: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.

1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards", Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Internal Annular Ring Less Than 2.0 mil

Contributors

- Drilled-hole pattern not matching the lands on the internal layers (Misregistration).
- Lamination process.
- Prelamination treatments that involve scrubbing or bending may stretch the thin laminate, which will then shrink after it is etched and baked dry.
- Application of specification or drawing notes.

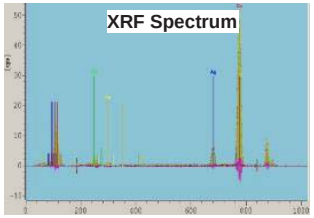
Resolution

- Better material selection of laminate, improved cleanliness, and reduction in the amount of volatiles.
- Confirm whether or not it is operator error.
- Update drawing notes to bring the notes in line with current industry maturity levels.

ENIG (Au or Ni) Less than the Minimum

Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (I
m

Risk: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.



1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

ENIG Less than Minimum

Contributors

- Improper cleaning of surfaces.
- Improper or inadequate rinsing.
- Bath parameters not being followed (pH and chemical).
- Bath temperature too low.
- Copper surface not clean of oil or inhibiting film.

Resolution

- Re-clean copper using chemical cleaners or mechanical
- scrubbing Institute micro-etch step to improve cleaning
- Improve rinsing(Check flow, agitation and water quality)
- Raise temperature per supplier specifications
- Readjust to supplier operational parameters

Summary of Supplier Study

- The test data is analyzed using statistical method to provide trend analysis for all suppliers.
  - Root cause(s) and key contributors are identified.
  - Mitigation plan is included for the root cause of nonconformance.

- Provide recommendations to the supplier's process, identification and prediction of nonconforming process limit criterion, and to improve test standards.
- New technologies (example: smaller annular rings, via-in-pads, thinner laminates or newer plating) are implemented on the basis of supplier maturity and reported NCs.

Summary

Restart Criteria

- Failures with severe consequences (e.g., safety) may require processes (e.g., manufacturing, distribution) to be interrupted after discovery of the failure.

- Depending upon the identified root cause, processes interrupted may be re-started if **corrective action** (s) can be implemented that will prevent the recurrence of the failure, or sufficiently minimize its impact.

Corrective Actions

- Many of the failures having a direct impact on production require **immediate corrective actions** that will minimize downtime.
- Although many immediate actions may correct symptoms,
  - temporary solutions may not be financially justifiable over the "long haul"; and
  - there is a large risk that a temporary solution may not solve the problem.

Verification

Verification of the corrective action includes:

- verifying the approval and implementation of the corrective action;
- verifying a reduction in the incidence of failures;
- verifying the absence of new failures associated with the failure sites, modes, and mechanisms identified during the failure analysis.

Root Cause Analysis Report

The report should include the following information:

1. Incident summary
2. History and conditions at the time of failure
3. Incident description
4. Cause evaluated and rationale
5. Immediate corrective actions
6. Causes and long-term corrective actions
7. Lesson learned
8. References and attachments
9. Investigating team description
10. Review and approval team description
11. Distribution list

Failures of a Failure Analysis Program

- Shutting down the malfunctioning equipment
- Refusing to recognize that a failure can or does exist
- Assuming an apparent cause to be the root cause
- Determining the failure cause by assumption
- Collecting insufficient information and ending an analysis before it is complete
- Discarding failed parts
- No documentation

Further Suggested Reading

- Journal of Failure Analysis and Prevention, ASM International.
- Electronic Device Failure Analysis (EDFA) Journal, ASM International.
- Engineering Failure Analysis, Elsevier.
- Electronic Failure Analysis Handbook, Perry L. Martin, McGraw-Hill Professional.
- Microelectronics Failure Analysis Desk Reference (Book + CD set) [Hardcover], EDFAS Desk Reference Committee.

Questions?

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