

# Application of PoF Based Virtual Qualification Methods for Reliability Assessment of Mission Critical PCBs

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**Presented to: Symbiosis Institute of Technology**

# Outline

- Motivation
- Introduction to Physics of Failure (PoF)
- Steps in PoF based reliability and risk assessment
  - Focus on PCB Supply Chain
- PoF Application Case study
- Closure

# Motivation

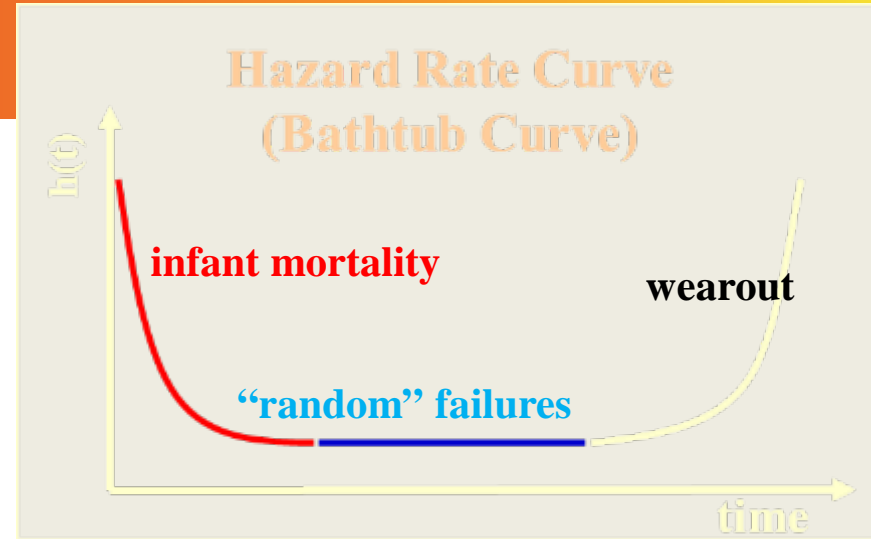
- The playing field in the design and development of systems *continues to evolve*.



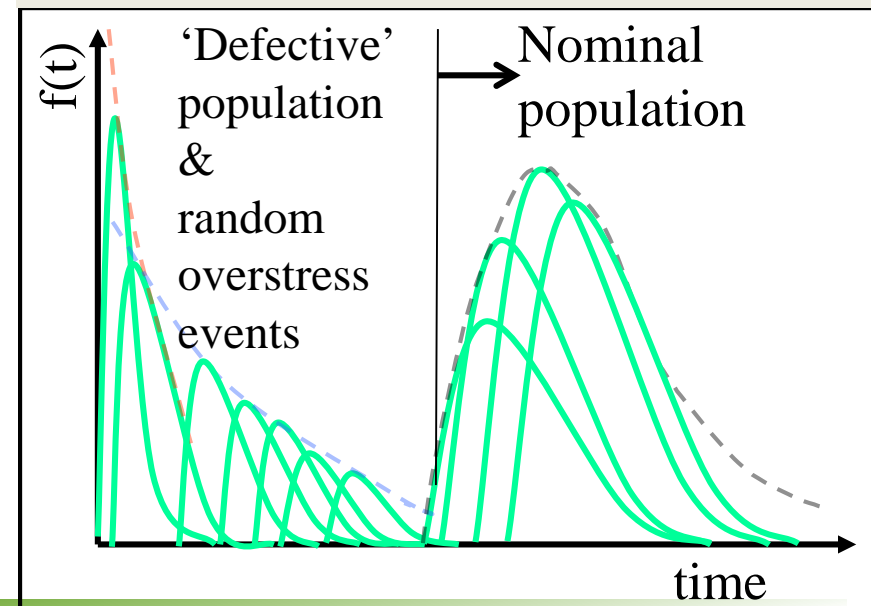
- Mission Assurance remains document centric.
  - Endeavors should be focused to move to a model centric and design based decision environment in a structured manner.
- Or *risk*:
  - Loss of effective oversight
  - Loss of relevant insight
  - Cost Drag

# PoF Perspective of Reliability

Reliability statisticians are interested in tracking system level failure data during the service life for logistical purposes, and in determining how the hazard rate curve looks.



- PoF reliability engineers are interested in understanding and controlling the individual failures that cause the curve.
- PoF engineers do so through systematic and detailed assessment of
  - influence of hardware configuration and life-cycle stresses...
  - on root-cause failure mechanisms...
  - in the materials at potential failure sites.

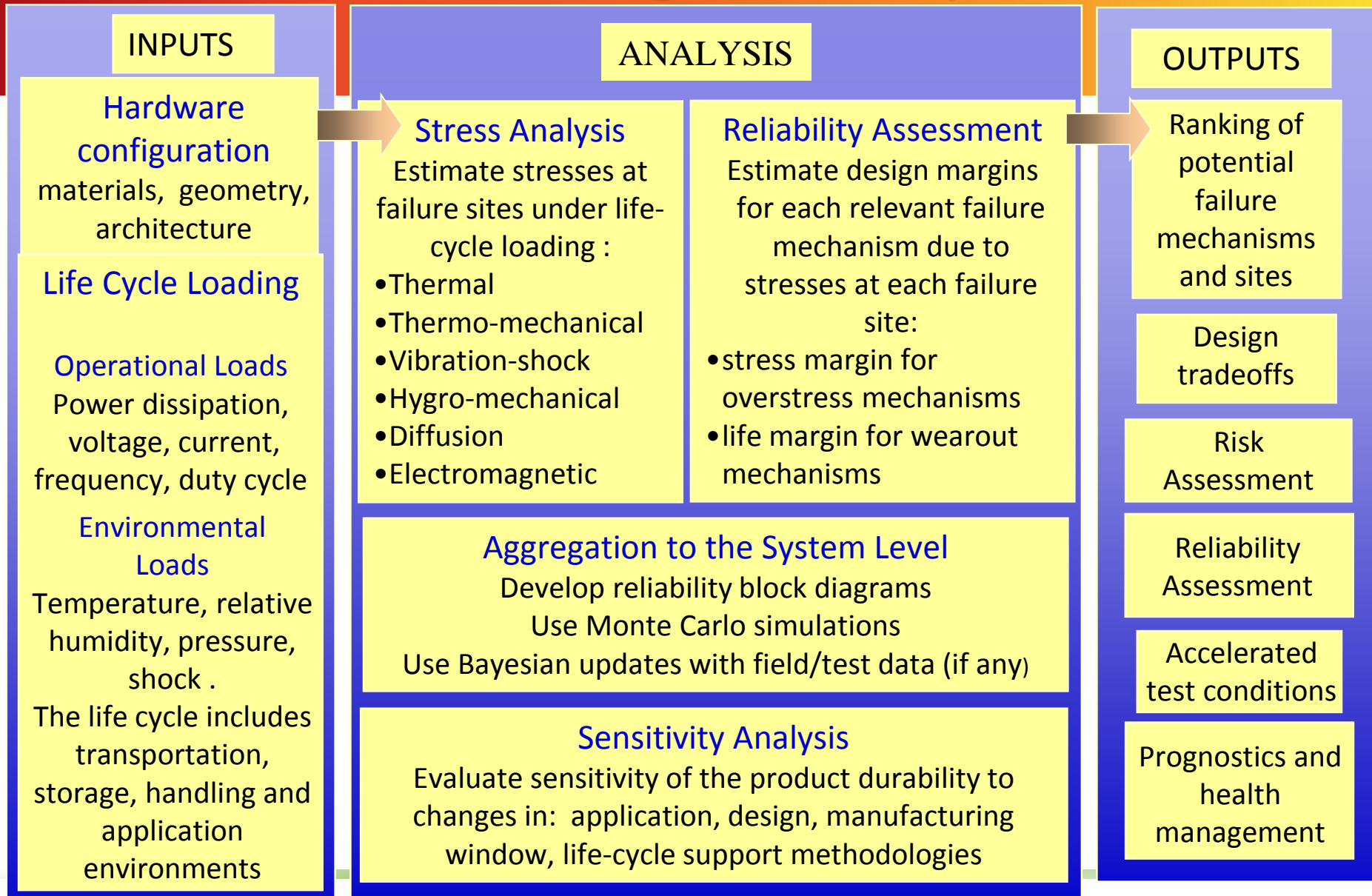


# PoF Fundamentals: Terminology\*

<i>Failure</i> .....	product no longer performs the intended function
<i>Failure Mode</i> .....	change in performance by which a failure is observed (can vary in a system or sub-system context)
<i>Failure Mechanism</i> .....	physical, chemical, thermodynamic or other process that results in failure
<i>Failure Site</i> .....	location of the failure
<i>Fault/Defect</i> .....	weakness (e.g., crack or void) that can locally accelerate damage accumulation and failure
<i>Load</i> .....	application/environmental condition (electrical, thermal, mechanical, chemical...) that can precipitate a failure mechanism
<i>Stress</i> .....	intensity of the applied load at a failure site

\* - definitions are piece part, PCB or assembly level

# PoF Process for Assessing Reliability

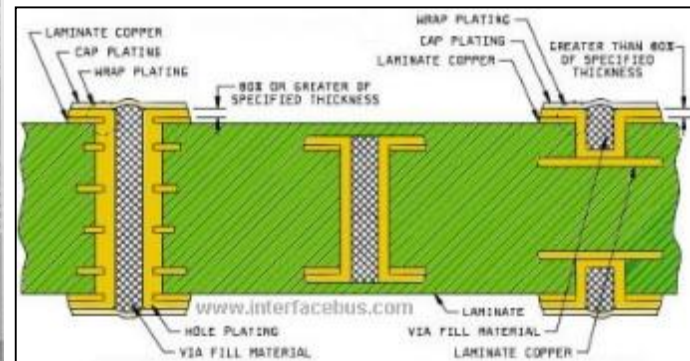
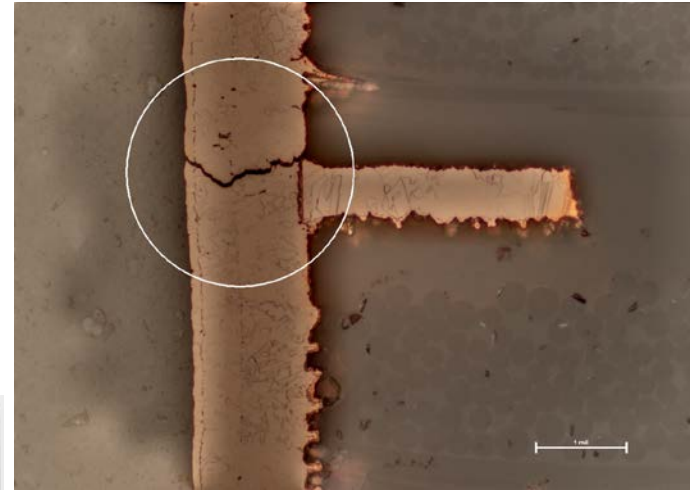
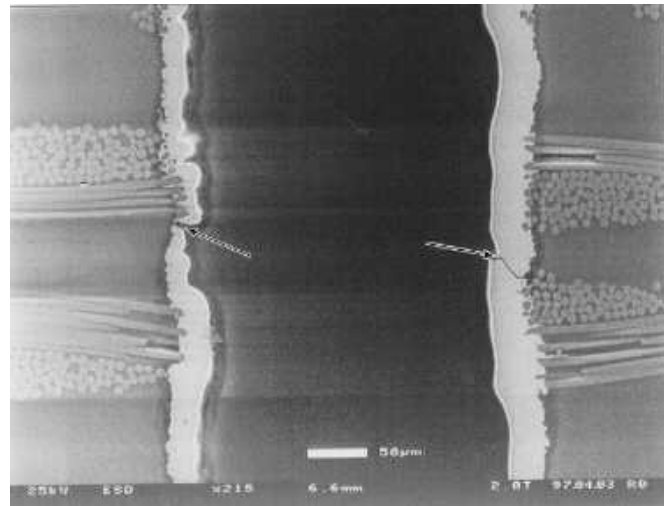
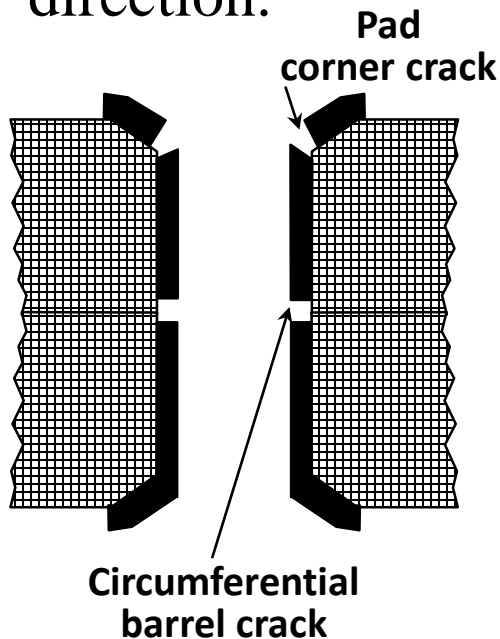


# PTH Low-Cycle Fatigue in PWBs

PWB-CTE in thickness (z) direction: ~50-90ppm/°C

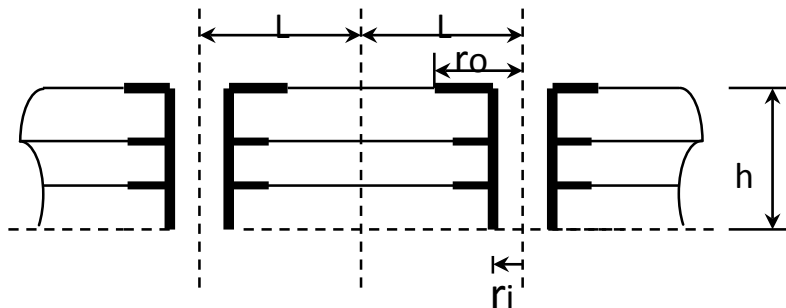
Cu-CTE in plating: ~20 ppm/°C

Thermal excursions cause thermal expansion mismatch in the thickness direction.



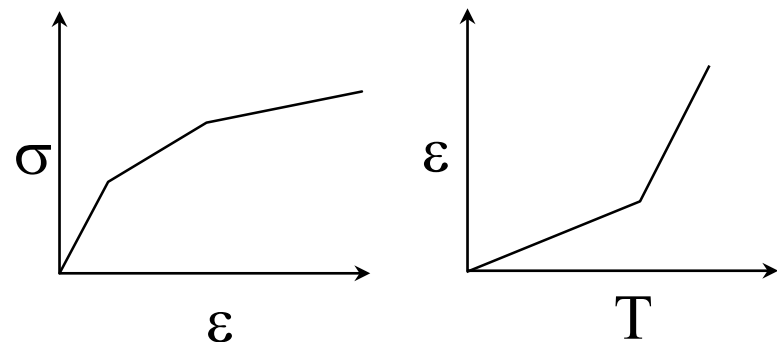
# PTH Parameters

## Geometric Factors

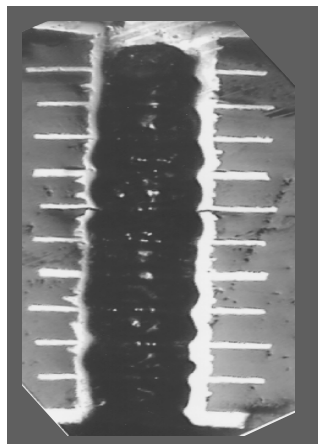


- Plating thickness
- Aspect ratio
- PTH spacing
- Non-functional pads
- Pad radius

## Material Properties



- Board material
- Plating material
- Filler material

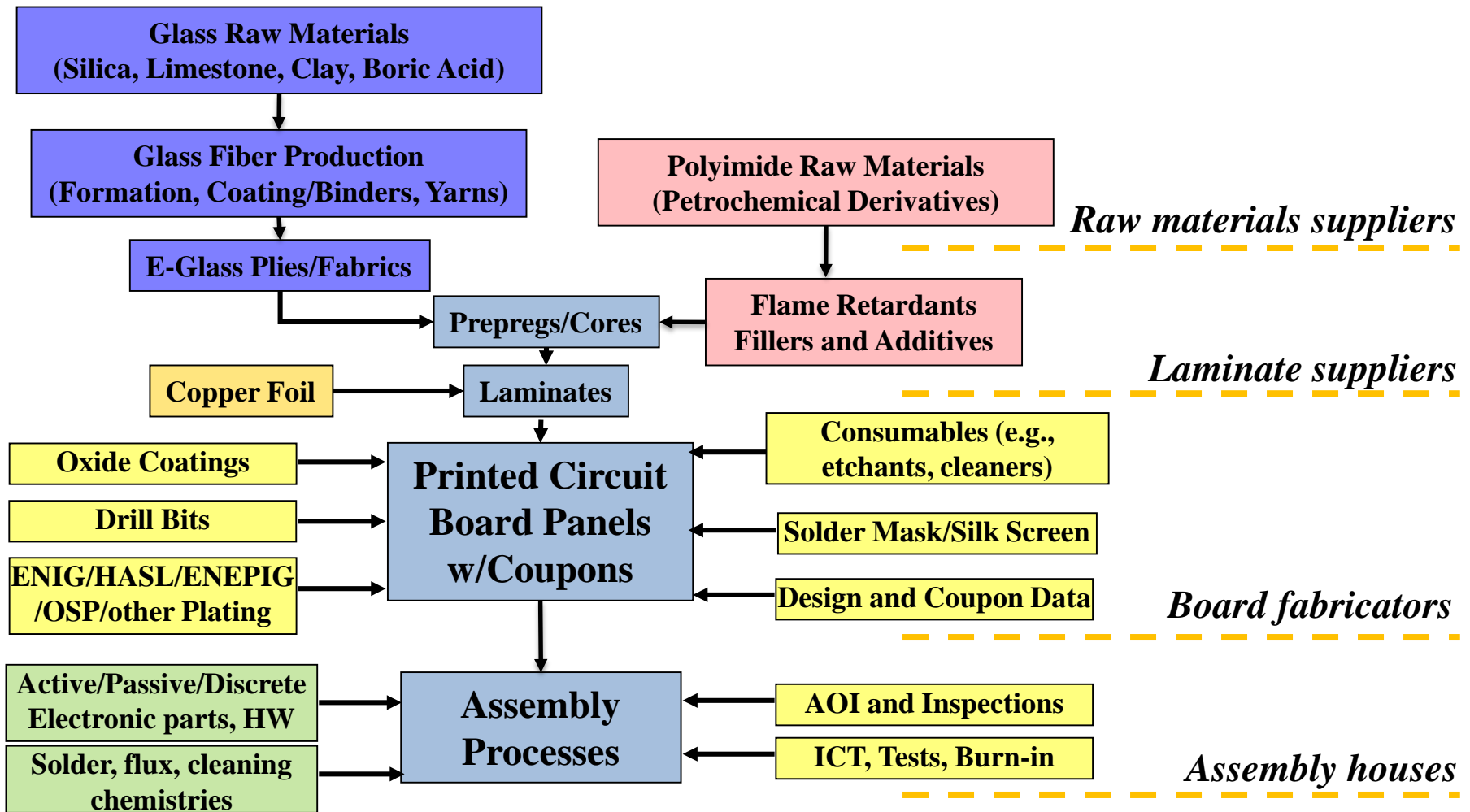


## Manufacturing Parameters

- Plating thickness uniformity
- Drill hole roughness
- Etchback
- Adhesion to PWB
- Eccentricity (misregistration)
- Resin/solder fillers

Feature	Variant	Effect on PTH Stress	Reason
Location of the Plated Through Hole	Spacing between PTHs	More closely spaced PTHs associated with a reduction in stresses	Out of plane constraints reduced and more readily shared between adjacent PTHs.
Plated Through Hole Barrels	Stress variation with respect to midplane	Stress increases closer to mid plane; maximum barrel stress at mid plane.	Results of thermally induced stress analysis.
Innerplanes	FR-4 boards	<ul style="list-style-type: none"> <li>Local stress reduction at innerplane</li> <li>No overall reduction in barrel stress (vs no innerplanes)</li> </ul>	CTEs between FR-4 and Cu are reasonably matched in plane.
Innerplanes	Polyimide boards	<ul style="list-style-type: none"> <li>Local stress concentration at innerplane (could exceed midplane stress depending on location w.r.t. midplane)</li> <li>Overall reduction (10%) in barrel stress outside concentrations (vs no innerplanes)</li> </ul>	In plane CTE between Cu and Polyimide have a larger delta than FR-4 and Cu
Aspect Ratio	Multilayered Board Thickness/Hole Diameter	High aspect ratio associated with high stresses.	0.030" boards are most robust according to IPC TR-579; 0.090" boards are less robust all other dimensions being equal.
Plating	Thickness	2 mils variation (1-3 mils thickness) can change stress levels by 25%	More metal, less stress
Solder Filling PTHs	Solder Filled	Reduction in overall barrel stress 3%-9%	More metal (solder); small effect due to properties of solder

# Polyimide PCBA Supply Chain\*



\* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).

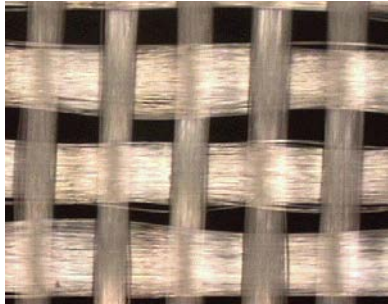
# Major Constituents of Laminates\*

Constituent	Major function (s)	Example material (s)
<b>Reinforcement</b>	Provides mechanical strength and electrical properties	Woven glass (E-grade) fiber
<b>Coupling agent</b>	Bonds inorganic glass with organic resin and transfers stresses across the structure	Organosilanes
<b>Matrix</b>	Acts as a binder and load transferring agent	Polyimide
<b>Curing agent</b>	Enhances linear/cross polymerization in the resin	Dicyandiamide (DICY), Phenol novolac (phenolic)
<b>Flame retardant</b>	Reduces flammability of the laminate	Halogenated (TBBPA), Halogen-free (Phosphorous compounds)
<b>Fillers</b>	Reduces dissipation (high frequency), thermal expansion and cost of the laminate	Silica, Aluminum hydroxide
<b>Accelerators</b>	Increases reaction rate, reduces curing temperature, controls cross-link density	Imidazole, Organophosphine

\* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." *Wiley Encyclopedia of Composites* (2011).

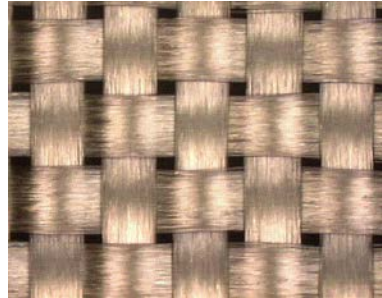
# Example: Glass Fabric Treatment\*

Glass Weave Style



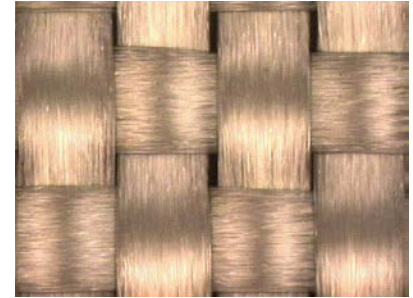
1080 Style

Glass Weave Style

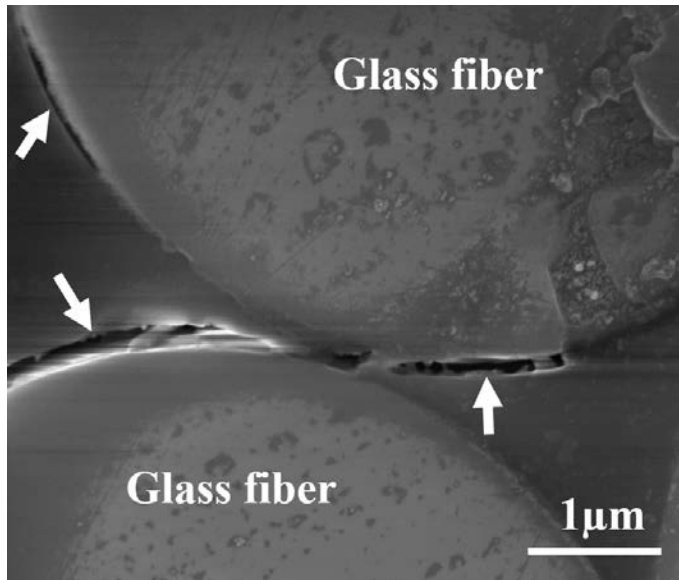


2116 Style

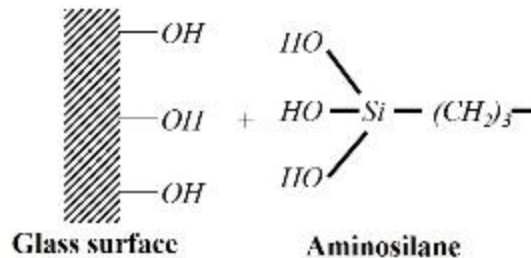
Glass Weave Style



7628 Style



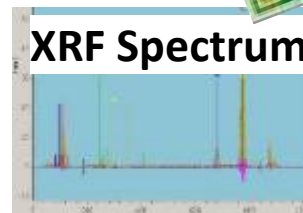
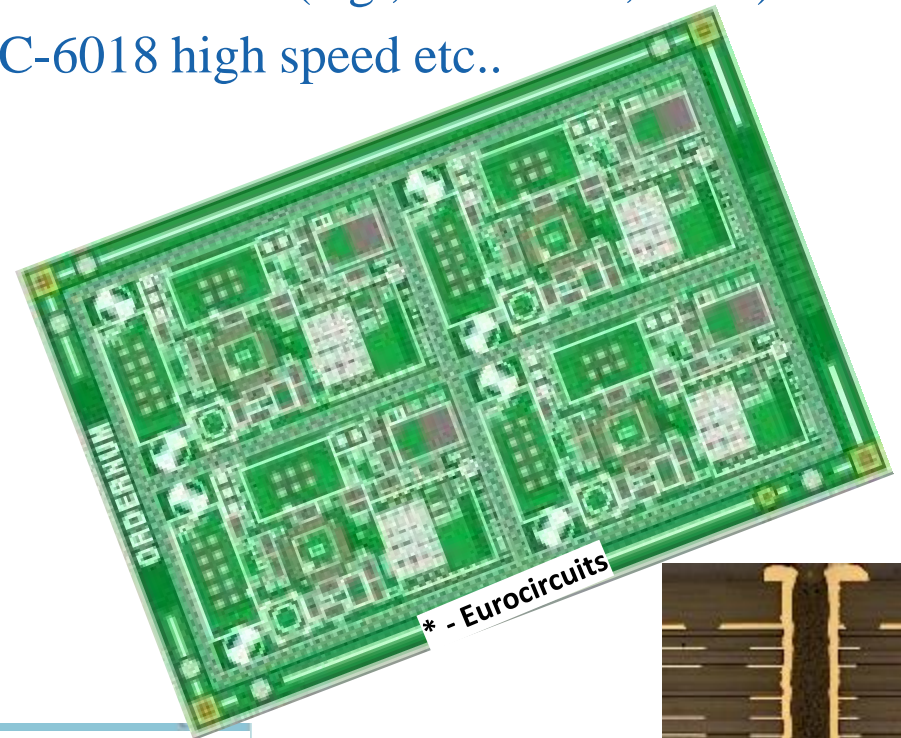
Fiber/resin interphase delamination occurs due to poor glass treatment.



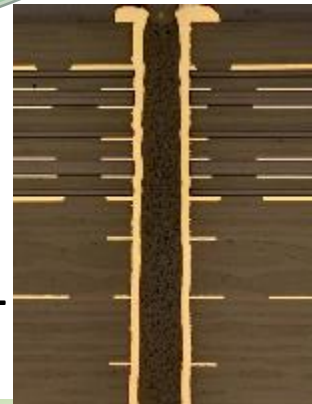
\* - Sood, Bhanu, and Michael Pecht. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." *Microelectronics Reliability* (2017).

# PCB Quality

- In a vast majority of cases, NASA uses IPC standards (e.g., IPC-6012, 6013)
  - IPC-6012 for rigid, IPC-6013 flex, IPC-6018 high speed etc..
- Inspection include:
  - Microsection evaluation (coupons)
  - Surface finish evaluation (coupons)
- Test include:
  - External visual examination
  - Electrical continuity and isolation
  - Solderability (not 100% cases)
  - Cleanliness
- In some cases MIL, ESA or “in-house” standards are applied.



**PTH in Cross-section**



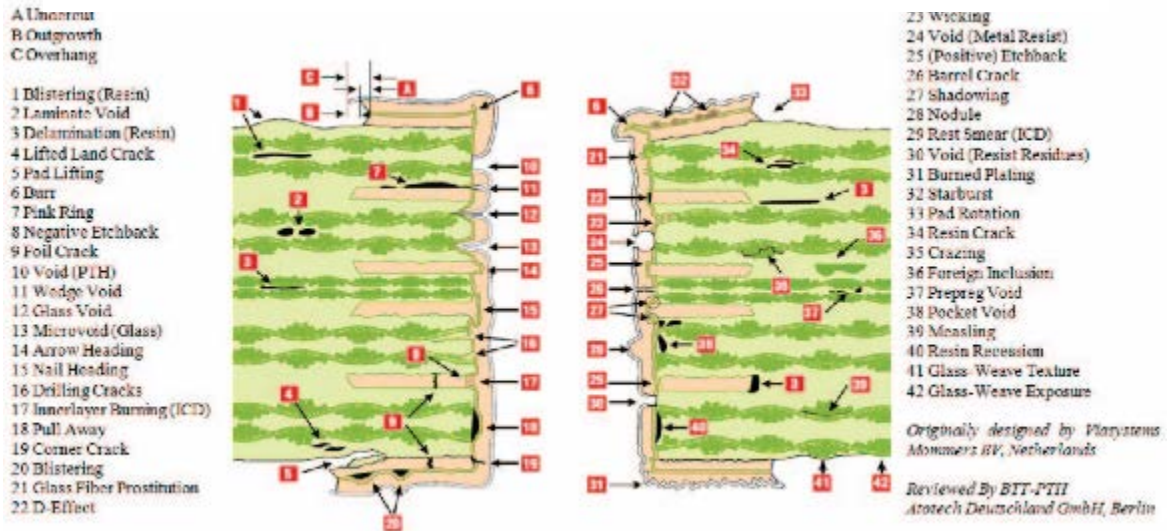
# Significance of Board Requirements

- The requirements and coupons are a “front door”.
- Examples:
  - Internal Annular Ring:
    - Egregious violations indicate there may have been a serious problem in development of the board (layup or lamination).
    - Other NCs don’t indicate any risk at all (example: application of IPC-6012 Rev B. v/s IPC-6012 Rev. D)
  - Negative etchback v/s positive etchback:
    - Modern cleaning processes and flight experience result in equal reliability with both etchback conditions or no etchback.
  - Wicking of copper:
    - Requirements are conservative based on broad statistics.
    - A basic analysis of the board layout can indicate directly if there is risk or not, regardless of requirements violations.

# Microsectioning

- Suppliers perform microsectioning and inspect per specifications.
- Secondary GSFC independent microsection analysis yielded 20-30% inspection rejects, caused by:
  - Screening escapes:
    - Test sample quality not consistent
    - Supplier microsection process, inadequate coupons
  - Requirement interpretations
  - Requirements flow-down issues
    - Alternative specifications (MIL, ECSS)
    - Buying heritage and off-the-shelf designs

## IPC - PCB Multi-Issue Microsection Wall Poster\*



\* - <https://blog.ipc.org/2010/11/22/pcb-multi-issue-microsection-wall-poster/>

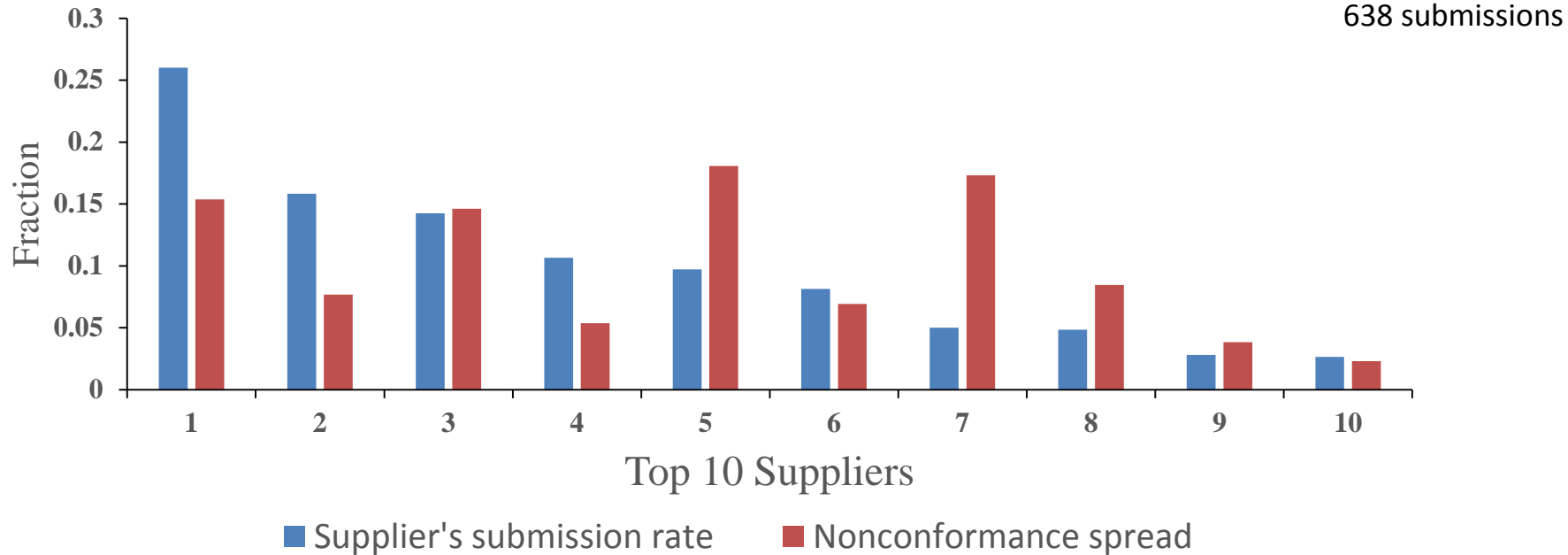
# Requirements, Nonconformance, Data Generation and Collection

- Present study evaluates only the microsections performed by GSFC.
  - PCB coupon microsection evaluation in accordance to IPC Standard (IPC-6018B Class 3, IPC-6012C Class 3/A).
  - Coupon evaluation reports were generated, identified non-conformances.
- All PCB coupon testing results from all GSFC suppliers were recorded for the past 3 years (from 2015 – present)
  - Data include nonconformance and conformances in accordance with IPC Standards.
  - Total number of data points are approximately 882 jobs.
  - Each job has number of nonconformance with different severity.

# Study Methodology

- Since 2015, received and analyzed 882 PCB coupon submissions from PCB suppliers.
- Top ten suppliers sent 638 submissions.
- Total nonconformance observed: 260
  
- For each supplier, analyzed nonconformance (s)
  - Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
  - Classifying and analyzing top 5 severity categories.

# Data Analysis –Submission and Nonconformance for Supplier



$$\text{Supplier submission rate} = \frac{\text{total submission by individual supplier}}{\text{total submission by all suppliers}}$$

$$\text{Nonconformance spread} = \frac{\text{total nonconformance by individual supplier}}{\text{total nonconformance by all suppliers}}$$

# Classification and Analysis - Top 5 Nonconformances

Twenty one distinct conformances observed among the ten suppliers

NC	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greather than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminate cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess of 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil	IPC 6012B Class 3/A
T	Dielectric thickness less than 3.0 mil min	IPC 6012B Class 3/A
U	Laminate void greater than 3.0 mil	IPC 6012B Class 3/A

Common Nonconformances from suppliers

← PCB Suppliers →									
1	2	3	4	5	6	7	8	9	10
A	F	E	K	A	N	E	E	A	E
B	G	D	F	F	O	P	A	F	F
C	H	B	L	D	F	C	D	S	T
D	A	I	J	J	E	D	F	D	U
E	D	J	A	M	P	Q	R	P	R

# Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to implement techniques which may eliminate these nonconformances from at least 7 suppliers.

**(A) Inner layer separations/inclusions**

**(D) Separation/inclusions between plating layers**

**(E) Copper wicking in excess of 2.0 mil**

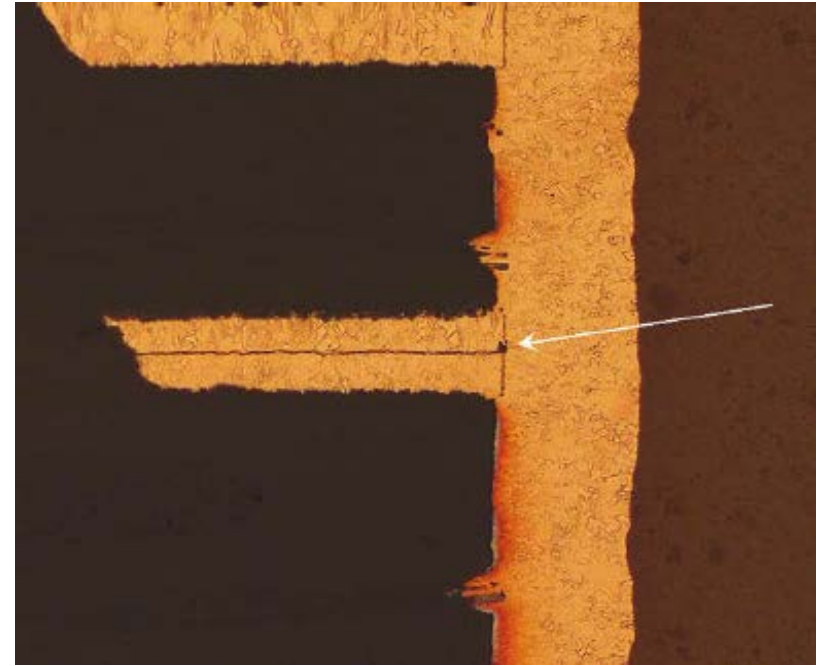
**(F) Internal annular ring less than 2.0 mil**

**(J) ENIG is less than the minimum requirements**

# Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in an area where it is not expected.

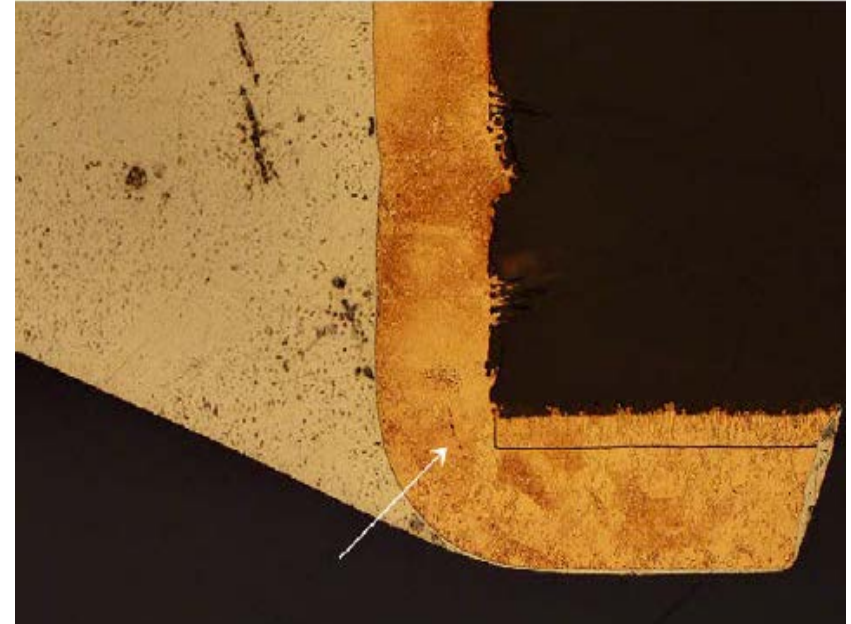
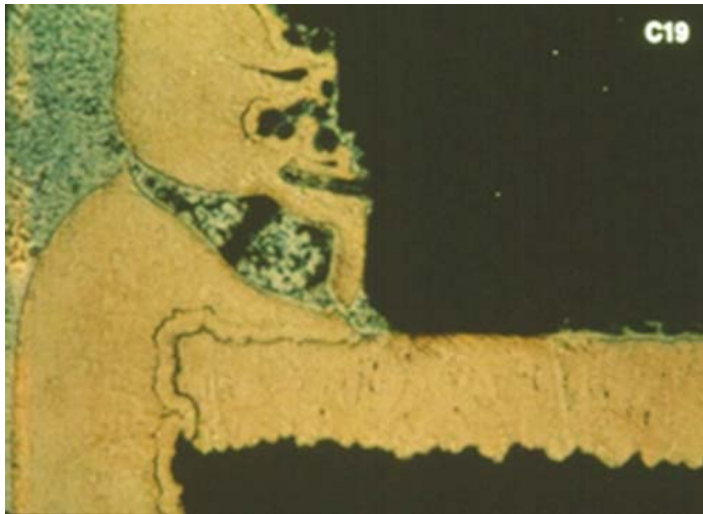
**Risk: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)**



1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

# Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating layer and foil.



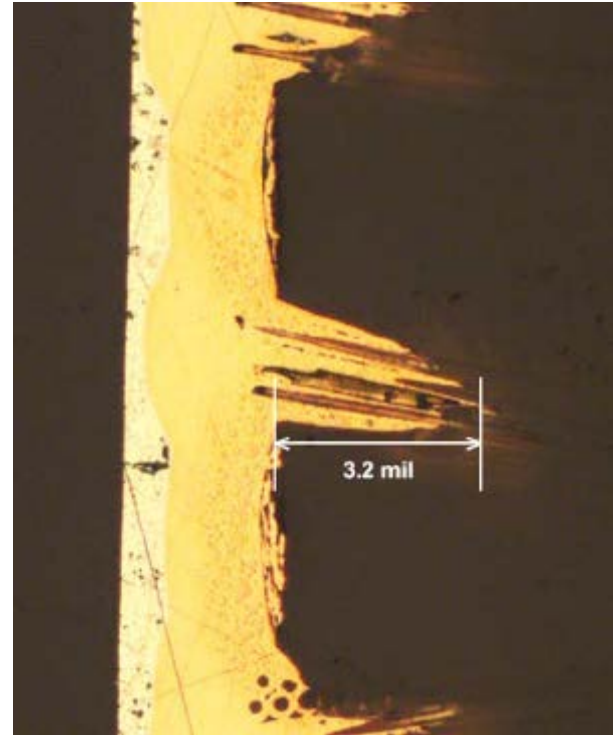
**Risk: intermittent electrical open or complete opens due to mechanical or thermal stresses.**

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

# Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.

**Risk: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.**

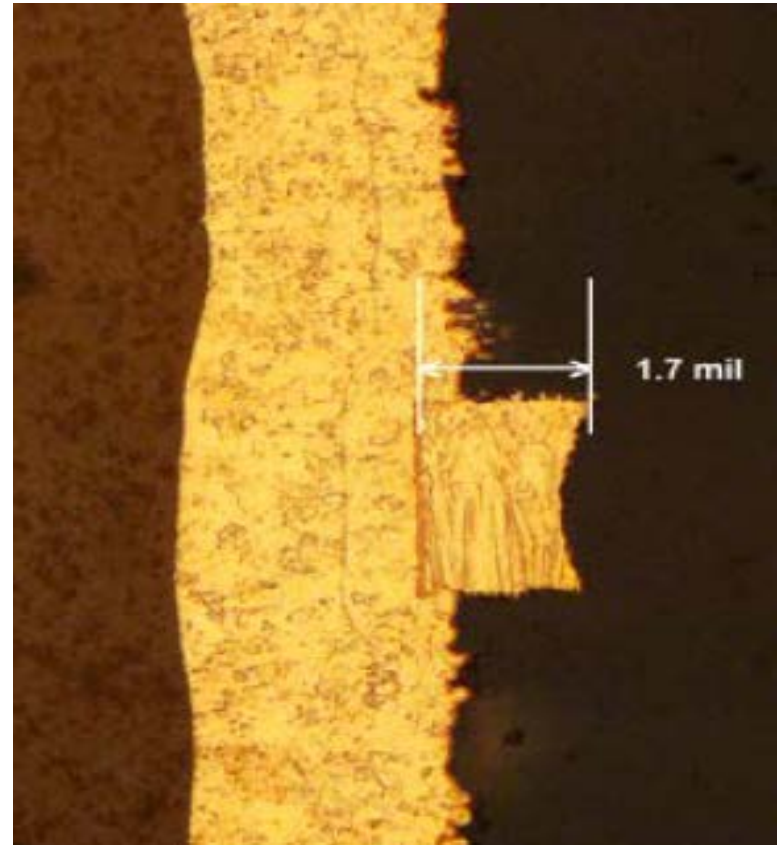


1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

# Internal Annular Ring Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.

**Risk: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.**

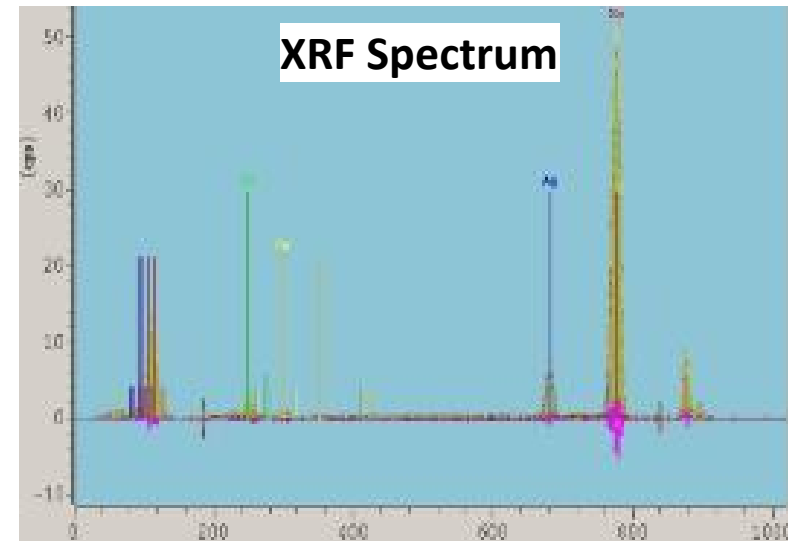


1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards", Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

# ENIG (Au or Ni) Less than the Minimum

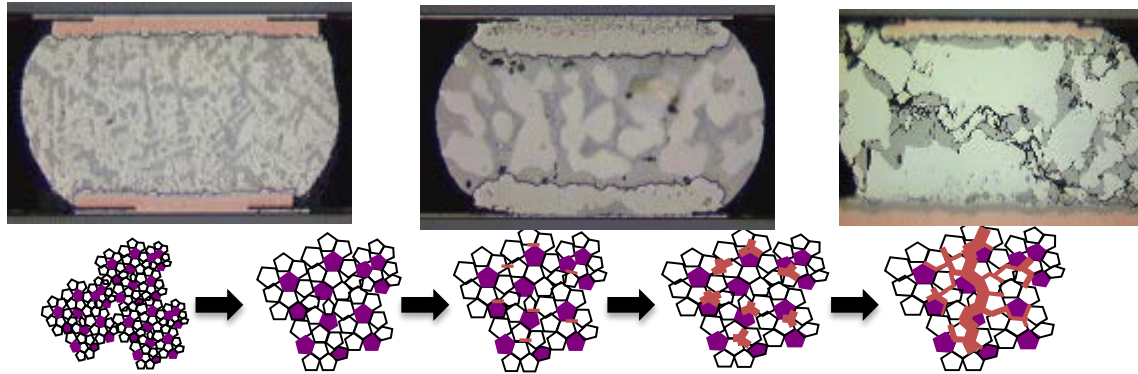
Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (118 micro-inches for Ni and 2 micro-inches for Au).

**Risk: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.**



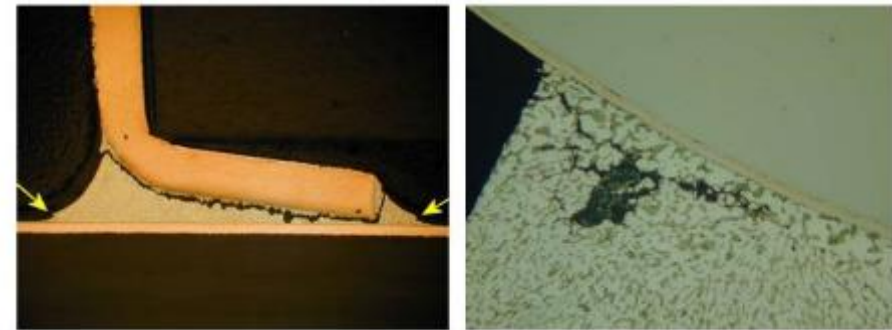
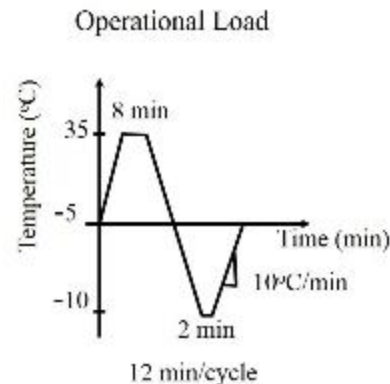
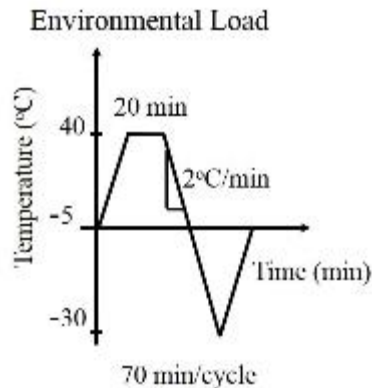
1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

# Cumulative Damage to Solder Joints Under Cyclic Thermo-mechanical Stresses [1, 2]



Damage mechanisms consist of grain coarsening, intergranular and transgranular microcracking, void nucleation, and void coalescence.

**Damage accumulation** →



1. Dasgupta, A., C. Oyan, D. Barker and M. Pecht, "Solder Creep-Fatigue Analysis by an Energy-Partitioning Approach," ASME Transactions on Electronic Packaging, Vol. 144, pp. 152-160, 1992.
2. Frear, D., Dennis Grivas, and J. W. Morris. "A microstructural study of the thermal fatigue failures of 60Sn-40Pb solder joints." Journal of Electronic Materials 17.2 (1988): 171-180.
3. Roger Devaney, "Failure Analysis of Solder Joints and Circuit Boards".

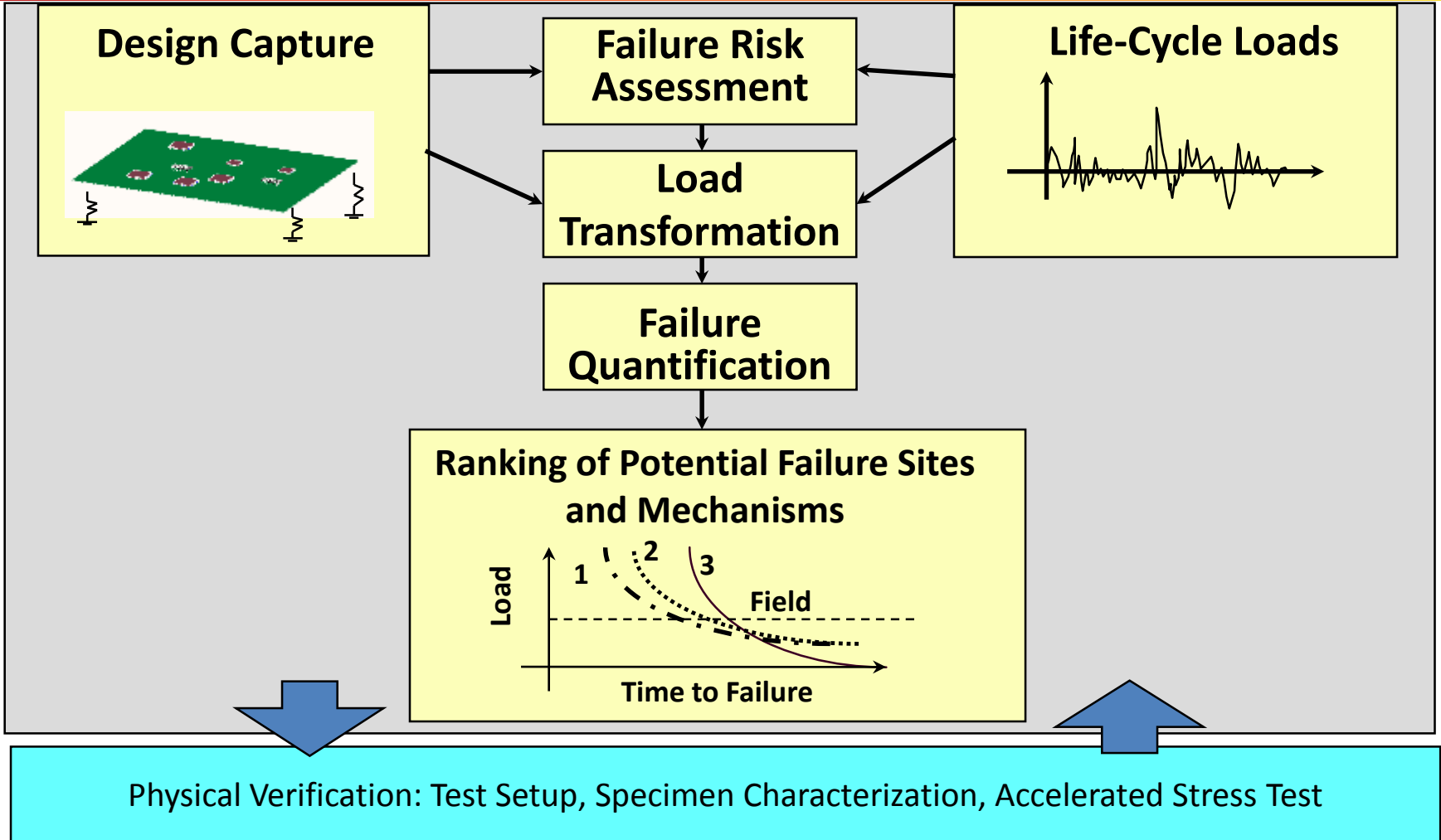
# Case Study: PoF Based Virtual Reliability Assessment of GSFC PCB Hardware

- Develop a risk assessment approach that details a ranked list of
  - failure mechanism and sites
  - time to failure distribution under anticipated environmental and operational loading conditions.
  - mitigation recommendationsfor the on-board processor printed circuit board assembly used in NASA Goddard SmallSat hardware architecture.
- Inputs to the risk assessment are obtained using University of Maryland's model-based lifecycle analysis software suite.

# Virtual Qualification: A Method to Apply PoF in Electronic Design

- Virtual qualification (VQ) is a simulation-based methodology (based on PoF principles) that assesses whether a part or system can meet defined life cycle requirements based on its materials, geometry, and operating characteristics.
- Outputs of the VQ effort are time to failure distribution under anticipated environmental and operational loading conditions. Risk assessment and recommendations are drawn from these outputs.
- VQ tool focuses on the dominant wearout mechanisms in electronic products
  - Solder joints
  - Plated through-hole (PTH)

# Steps in Virtual Qualification\*

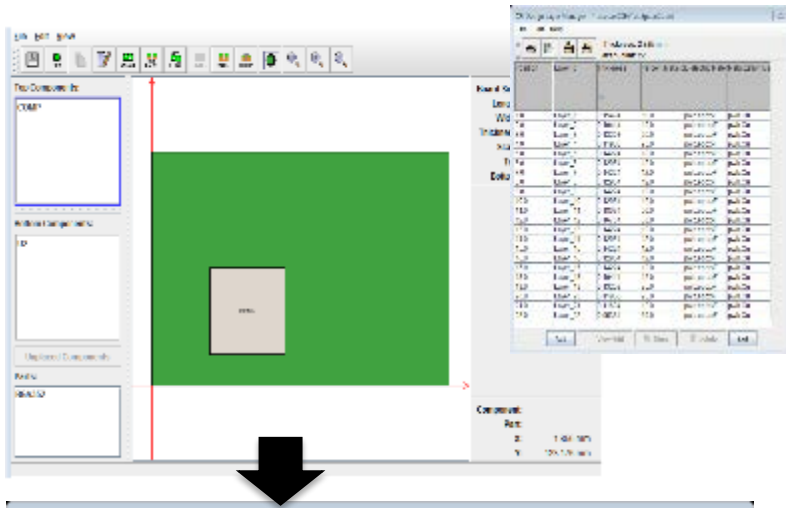


\* - User documentation – Univ. of Maryland Software Suite

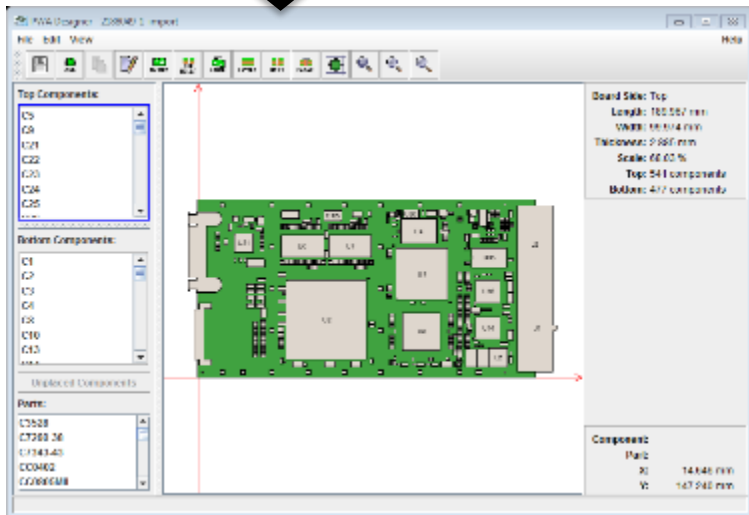
# Steps Involved in SmallSat VQ

- ✓ Obtain available card specific drawings, CAD models and bill(s) of material
- ✓ Import available CAD models (ODB++) to the software
- ✓ Complete the model population specific to the board under study
  - Populate component data fields that reflecting physical (mass, materials) and electrical (power dissipation, Theta Jc, etc.)
  - Populate board layer properties
  - Populate via properties
  - Populate via locations
- ✓ Specify thermal boundary conditions in the model
- ✓ Specify mechanical boundary conditions in the model
- ✓ Specify lifecycle phases in the UMD Software VQ model
- ✓ Specify required inputs from GEVS in the model
- ✓ Run the specified analyses and obtain critical features
  - Random vibration and thermal vac temperature cycles
- ✓ Recommend risk mitigation activities with respect to board design

# Creating the Model from the Data Sources

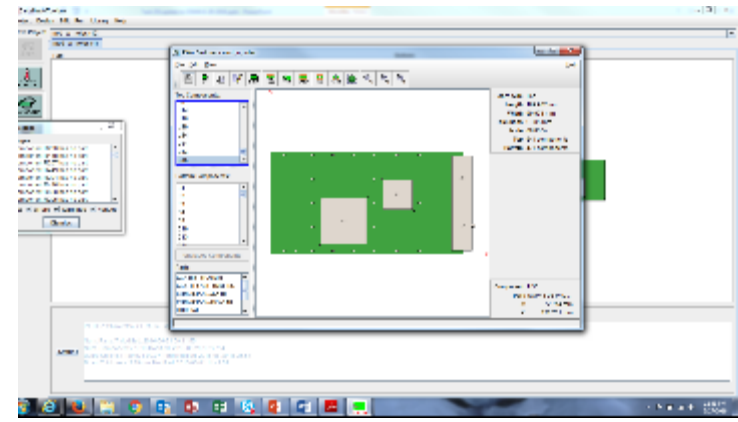


Model manually built from the PDF drawings and the parts list. All features drawn manually. Board layers specified in this version and were made available to the model below.



Similar, more complex CAD model downloaded from .tgz (ODB++) file:

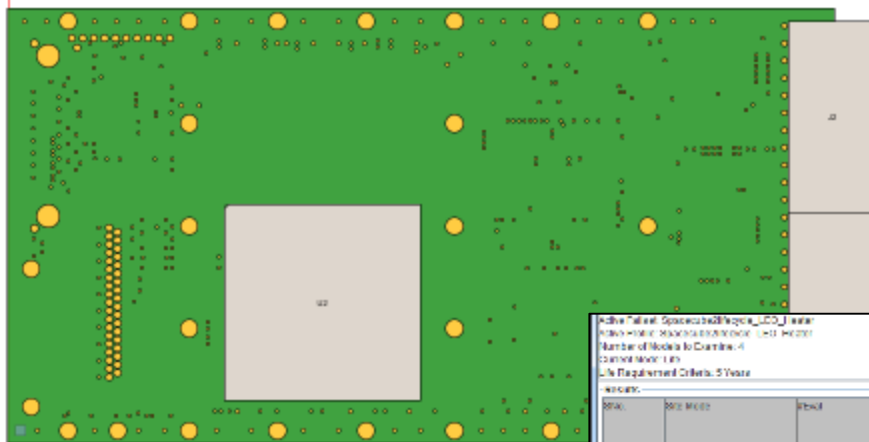
- All component and board dimensions.
- Does not import via locations or board layer information.
- Does not populate component information unless recognized by the library.



Unused components were depopulated from the model to reflect the actual board design of interest.

# Model Updates

- Imported plated through hole vias (enabled with a software update)
- Refined material definitions for the PCB and assembled parts
  - Polyimide material properties
  - Updated CTE value and distribution for chip carrier material
- Created 3 life cycle cases for use and on-orbit conditions and running Monte Carlo simulations (1% failure at 5 years at LEO)



Active Failure: SpacedOut2Inpck\_LCO\_J\_wake  
 Active Time: 3600000000000000 (1st 14000)  
 Number of Models to Evaluate: 4  
 Current Model: 1/4  
 Life Requirement Criteria: 5 Years  
 Location:

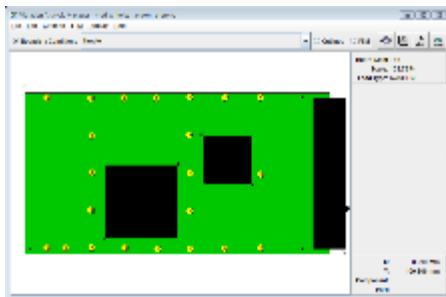
FAIL	FAIL MODE	INDEX	WEEKS TO FAILURE	DANGEROUSNESS	STATUS
1	U2-Base-down	2	1ST_TT_CGA	344.82 days (D:0:T:25)	Fail
2	U2-Base-down	2	1ST_TT_CGA	2497.71 days (D:7:T:25)	Fail
3	J2-Base-down	2	1ST_TT_T1	2 45 years (D:0:0:0)	Fail
4	J2-Base-down	2	1ST_TT_T1	8 85 years (D:0:0:0)	Fail
5	J2-Base-down	2	1ST_TT_T1	13 25 years (D:0:0:0)	Fail
6	J2-Base-down	2	1ST_TT_T1	17 65 years (D:0:0:0)	Fail
7	J2-Base-down	2	1ST_TT_T1	22 05 years (D:0:0:0)	Fail
8	J2-Base-down	2	1ST_TT_T1	26 45 years (D:0:0:0)	Fail
9	J2-Base-down	2	1ST_TT_T1	30 85 years (D:0:0:0)	Fail

**First Order Thermal Fatigue Model For Column Grid Array**

Part ID:	U2
Component Name:	U2_Thermal_Cock_Up
Component Number:	4
Order ID Number:	4520
Location Name:	7293418
Location Type:	Model:035
<b>Value Reliability (DER) Percent Failure</b>	
MC Sample Size:	2000
MC Trials:	1000000000
MC Simulated Lives:	20495045200
MC Mean:	2154162844
MC Min:	200000000000
<b>Problem Information</b>	
Package Factor:	1.00000
Package Length:	45.00000 mm
Package Width:	45.00000 mm
Interconnect Spacing:	41.00000 mm
Interconnect Spacing:	41.00000 mm
Joint Height:	0.00000 mm
Package CTE:	5.888888888E-06
Board CTE:	1.620000000E-05
<b>Stress Condition</b>	
Max Package Temperature:	53.95628 °C
Max Board Temperature:	53.91762 °C
Min Package Temperature:	23.91000 °C
Min Board Temperature:	24.00000 °C
Max Diff Temp:	45.26667 °C
Power Input:	20.00000 mW

# Random Vibration and Board Response

Import the  
“built” board  
into the  
Vibration  
Analysis  
module



GEVS\* PSD defines the  
random vibration inputs  
required

Table 2-2.3  
Generalized Random Vibration Test Levels  
Components (G's)  
22.7kg (50lbs) or less

Frequency (Hz)	Qualification	Acceptance
20	0.02G	0.01G
20-50	+6 dB/oct	+6 dB/oct
50-100	0.16G	0.08G
100-2000	-6 dB/oct	-6 dB/oct
2000	0.05G	0.01G
Overall	14.1 Gms	10.9 Gms

The acceleration spectral density level may be reduced for components weighing more than 22.7kg (50 lb) according to:

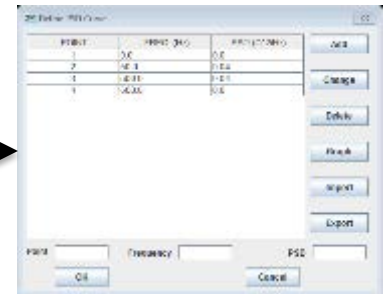
Weight (kg)	Weight (lb)	
10 kg (22.7)	22.7 (50)	
45 kg (100)	100 (220)	
450-800 Hz	0.16G(2.7Hz) 0.16(35Hz)	for postflight
450-800 Hz	0.05G(2.7Hz) 0.05(35Hz)	for acceptance

Where W = component weight

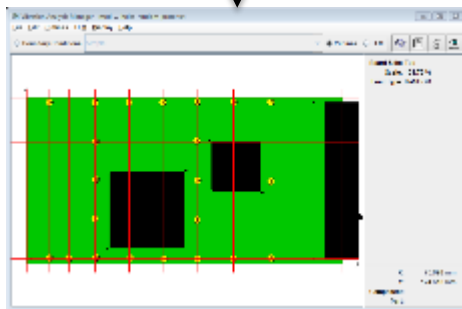
The slopes shall be maintained at + and - 6dB/oct for components weighing up to 50-kg (110-lb). Above that weight, the slopes shall be equated to maintain an ASD level of 0.01 G's/Hz at 20 and 2000 Hz.

For components weighing over 182-kg (400-lb), the test specification will be maintained at the level for 182-kg (400 pounds).

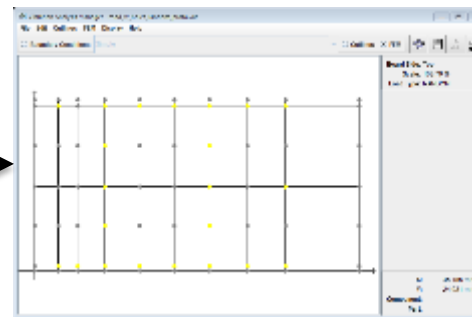
...to VQ Tool  
PSD



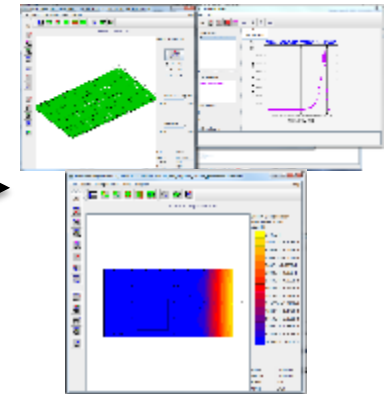
Affix  
Boundary  
Conditions  
and Mesh to  
imported  
PWB model



Generate  
FEM



Run the  
model

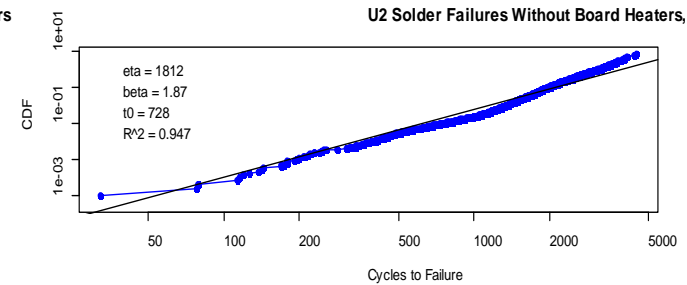
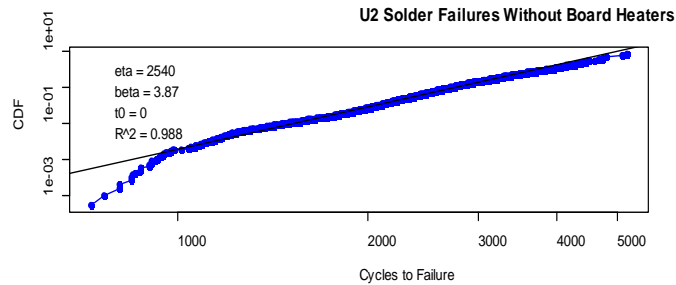


\* - GSFC-STD-7000 – General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects

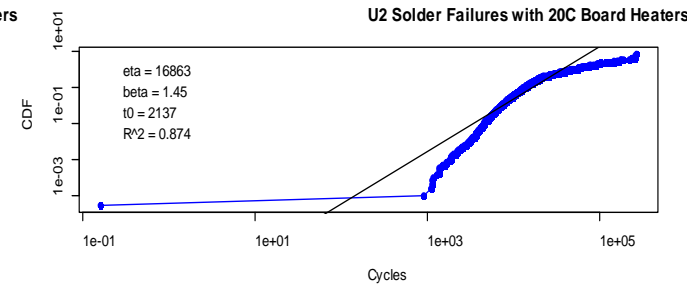
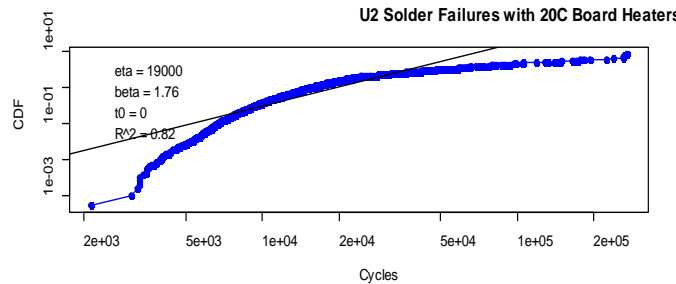
# Failure Data for Different Life Cases (Weibull)

Location Parameter ( $t_0 = \text{MC minimum}$ ) Does not Improve Fit in all Cases

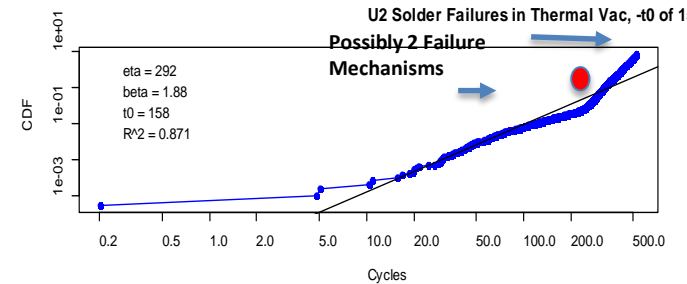
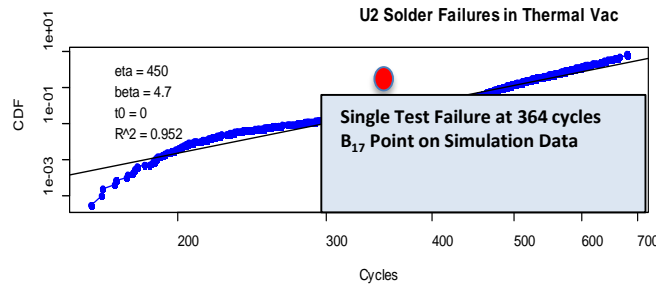
Case 1	
High (box)	50C
Low	-30C
U2 Power	5.9W
Ramp	22 min
Dwell	22 min



Case 2	
High	50C
Low	15C
U2 Power	5.9W
Ramp	22 min
Dwell	22 min



Case 3	
High	100C
Low	-55C
U2 Power	0.0W
Ramp	3C/ min
Dwell	30 min



# SmallSat PCB Assembly Analysis

- Replicated thermal cycling life test performed by the project
  - Single thermal vacuum test failure (364 cycles) falls within simulated CDF curve.
- Comparing cycles-to-failure result with predictive cycles in the University of Maryland VQ tool.
- Selected parameters – board thickness, dielectric material, column attach area – to conduct sensitivity analysis.
- Outputs are used for recommending design changes to improve PCBA reliability.

## Sample results, variable board material

	Isola P95 (manufacturer datasheet)	Epoxy Fiberglass (from Library)	Arlon 85NT (manufacturer datasheet)
Dielectric elastic modulus [MPa]	26834	17200	22063
Dielectric CTE (X/Y) [ppm/°C]	13	17.6	9
Dielectric CTE (Z) [ppm/°C]	55	70	93
Board elastic modulus [Pa]	6.757650e+004	6.871997e+004	6.996647e+004
Board CTE (X/Y) [ppm/°C]	1.473067e-005	1.730220e-005	1.287345e-005
Cycles to Failure, FPGA (mean)	1641	649	4433
Cycles to Failure, PTH (mean)	9624	3576	1091

**Possible Trade Space: SMT solder fatigue life improvement at the expense of PTH life.**

# GSFC PCBA HW Analysis - Summary

- Model results provide a reasonable prediction with respect to this configuration given only one recorded test and failure.
- If the single failure point is an indication of model validity, then design changes are needed to attain the minimum reliability goals for LEO conditions.
  - Solder joint fatigue of CGA components (U2 and U3) is the top driver at 245 days at LEO.
- Controlling (minimizing) temperature extremes on orbit provides the most benefit to reliability of the solder joints in current configuration.
  - Effect of thermal control to minimize temperature swings is significant (7.5X better characteristic lives in this case).
- PWB Material changes (board or metallization layers) to better match CGA to PWB CTEs will be critical to attaining desired reliability along with effective thermal control.
  - Sensitivities and trades for different board materials and failures can be performed in the VQ tool (see previous chart data).

# Adoption of Physics of Failure...Next Steps...

- Adoption of physics of failure allows teams to understand the product degradation processes, account for degradation in the design and manage it better.
  - Multifaceted PoF tools and methods are applied in the development process.
- Ongoing work at NASA Goddard SMA focuses on VQ of EEE parts.
- Skill development for PoF at NASA Goddard SMA is facilitated by collaboration with academic institutions.

# Acknowledgements

The research was a collaborative effort between

- NASA R & M Program
- NASA Goddard
  - ❑ Components & Hardware Systems Branch
  - ❑ Science Data Processing Branch
  - ❑ Risk and Reliability Branch (SMA)
- NASA PCB Working Group
- NASA Workmanship Standard Program

