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Development of a robust, efficient process to produce scalable, superconducting kilopixel Far-IR Detector Arrays

Johannes Staguhn[a,b], Samuel H. Moseley[b], Ari Brown[b], Gene Hilton[c], Kent Irwin[d], Stephen Maher[b], Karwan Rostem[a,b], Elmer Sharp[b], and Edward Wollack[b]

[a]Johns Hopkins University, Code 665, Building 24, Greenbelt, MD 20771, USA
[b]NASA Goddard Space Flight Center, Greenbelt, MD 20771, USA
[c]National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80305, USA
[d]Stanford University, Mail Code:4060, Stanford, California 94305

ABSTRACT

The far-IR band is uniquely suited to study the physical conditions in the interstellar medium from nearby sources out to the highest redshifts. FIR imaging and spectroscopy instrumentation using incoherent superconducting bolometers represents a high sensitivity technology for many future suborbital and space missions, including the Origins Space Telescope. Robust, high sensitivity detector arrays with several 10^4 pixels, large focal plane filling factors, and low cosmic ray cross sections that operate over the entire far-IR regime are required for such missions. These arrays could consist of smaller sub-arrays, in case they are tileable. The TES based Backshort Under Grid array architecture which our group has fielded in a number of FIR cameras, is a good candidate to meet these requirements: BUGs are tileable, and with the integration of the SQUID multiplexer scaleable beyond wafer sizes; they provide high filling factors, low cosmic cross section and have been demonstrated successfully in far-infrared astronomical instrumentation. However, the production of BUGs with integrated readout multiplexers has many time and resource consuming process steps. In order to meet the requirement of robustness and efficiency on the production of future arrays, we have developed a new method to provide the superconducting connection of BUG detectors to the readout multiplexers or general readout boards behind the detectors. This approach should allow us to reach the goal to produce reliable, very large detector arrays for future FIR missions.

Keywords: cryogenic detectors, far-infrared, detector arrays, superconductivity

1. INTRODUCTION

Robust, high sensitivity kilopixel format arrays with large focal plane filling factors and low cosmic ray cross sections that operate over the entire far-IR regime are required for future NASA missions, such as the Far-Infrared Surveyor (now called the Origins Space Telescope, OST). Our kilopixel Backshort Under Grid (BUG) detectors [1] are designed to meet all those requirements: By bump-bonding two-dimensional detector arrays to SQUID based readout multiplexers, these arrays are tileable, and with the integration of the multiplexer scalable beyond wafer sizes; they provide high filling factors ($> 90\%$ at 1mm pixel pitch), and are designed to have low Cosmic ray cross sections. Individual BUG detectors have been demonstrated in the HAWC+ camera on SOFIA [2] to provide background-limited performance for suborbital far-IR applications. Furthermore, membrane-suspended TES detectors with low noise (NEP$\sim 10^{-19} W/\sqrt{Hz}$) and $< 1\ ms$ time constants which are compatible with our BUG detector design, have already been demonstrated [3]. These individual pixels already meet the requirements for space based, background limited FIR continuum cameras, such as the FIP camera being studied by our group for the Far-Infrared Surveyor (OST). One technical approach to increase those sensitivities are phononic structures that will enable phononic-isolated TES detectors with NEP reaching into the NEP$\sim$ a few $10^{-20} W/\sqrt{Hz}$, which will be sufficient for background limited medium resolution ($R \sim 3,000$) space-based spectroscopy.

Further author information: (Send correspondence to Johannes Staguhn)
E-mail: johannes.staguhn@nasa.gov, Telephone: +1 301 814 7840

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2. GOAL: STREAMLINING AND SIMPLIFICATION OF PROCESS TO PRODUCE LARGE FAR-INFRARED ARRAYS

We have obtained funding to streamline the fabrication processes required to produce background limited large far-infrared arrays with large pixel numbers $n \sim$ several 10^4 . We will achieve this goal by combining mature detector and readout technologies from our previous work, to fabricate a robust, close packed high sensitivity bolometer array with reliable high-quantum efficiency absorbers that operates over the entire FIR range and can be efficiently and reliably produced . The simplified process will integrate detector arrays through superconducting bonds to a cold readout multiplexer or a fanout board. It is very versatile in its applications, since it will allow the mating of TES detectors to time domain, frequency domain, microwave and code division multiplexers which will not necessarily have the same cell sizes. The main objectives will be achieved by meeting the following goals: a) Develop a novel BUG architecture in which the superconducting through via process is separated from the detector production, improving production speed and reducing risk; b) Refine our AlMn process for quickly and reliably fabricating TES with highly predictable and uniform transition temperatures (less than 5% variation) across the entire wafer; and c) Refine a standard process for reliably fabricating impedance- matched and robust absorbers for the entire FIR wavelength range, which are not susceptible to room temperature aging. The anticipated end product will be the production of background-limited kilopixel array suitable for the FIR spectrometer Super-HIRMES .

3. THE BACKSHORT UNDER GRID (BUG) DETECTOR

We have developed an integrated 2-dimensional large format, high efficiency low noise bolometer array operating in the far-infrared to submillimeter wavelength regimes. [1]. Three of those arrays have been successfully integrated into the SOFIA 2nd generation instrument HAWC+ and provide background limited performance. BUGs will follow to be integrated into GISMO-2 [4] and PIPER [5]. While the BUG architecture has been very successful, it has proven to be very time consuming to build these arrays. This, combined with the fact that the many fabrication steps and required fabrication accuracies, has lead us to a refined design which we will lay out in the following.

4. THROUGH WAFER VIA

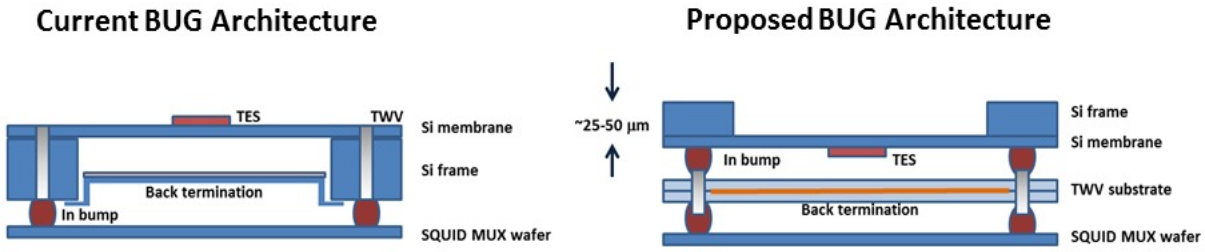

Figure 1. Cross-section view schematics of the current and proposed Backshort Under Grid detector architecture. In the current embodiment, the through wafer vias are integrated in the array wafer, while they are in a separated wafer in the proposed architecture.

A main goal of the proposal is to simplify the process of routing of the detector readout and bias signals perpendicular to the plane of the detector pixels. For this we need through wafer vias. The currently existing through wafer via process for Backshort Under Grid detectors involves placing the vias directly on the detector device wafers, which is technically extremely challenging. This is primarily because the vias need to be filled with a polymer that is planar with the silicon membranes to within a micron so that subsequent micron-scale lithography is not compromised. In order to circumvent this challenge, we have moved the vias to a separate substrate (see Figure 1), which relaxes the tolerances on the lithography and greatly simplifies the detector

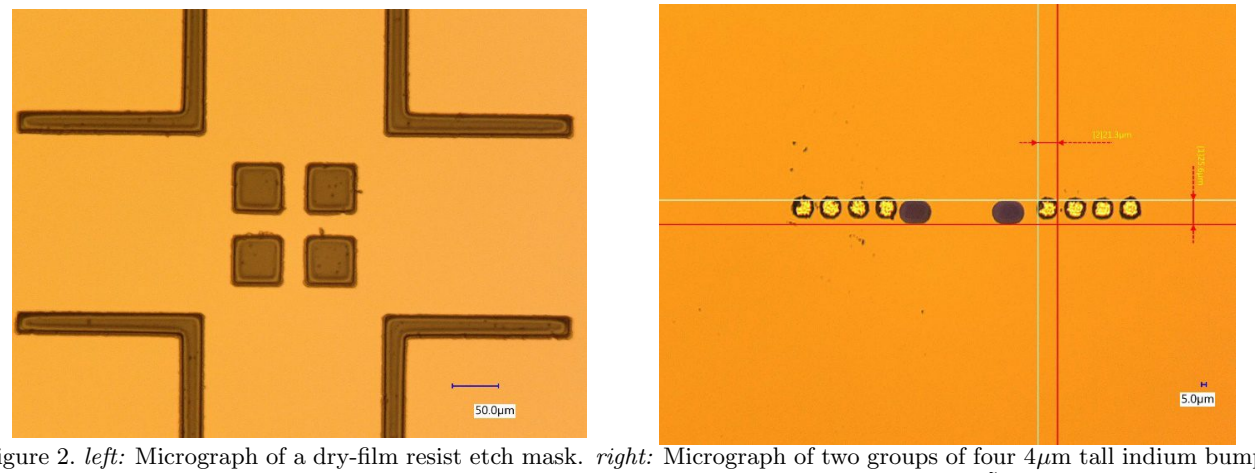

Figure 2. *left:* Micrograph of a dry-film resist etch mask. *right:* Micrograph of two groups of four 4μm tall indium bumps next to two through wafer vias. The silicon wafer in which the vias were micromachined was $\tilde{0}$.4 mm thick.

fabrication process. Furthermore, in order to increase the through wafer via fabrication throughput, we have not filled the vias.

The primary technical challenge associated with this new approach involves patterning superconducting traces and indium bumps on the through wafer via substrate. We have addressed this challenge by developing two novel patterning processes. The first process, which is used to etch metallic traces on a via-containing substrate, involves using a two-layer etch mask. The first layer consists of an anti-reflection coating and the second consists of a dry film resist, which is laminated on the wafer. The dry film resist is photolithographically patterned and the anti-reflection coating is reactive ion etched. In contrast with a conventional, spin-on resist, a dry film resist can effectively cover the vias. The second process, which is used to lift-off the indium bumps on a via-containing substrate, involves using a two-layer lift-off mask. The first layer consists of positive photoresist and the second consists of a dry film resist, and the lift-off mask is patterned in a similar manner as the etch mask described above. Demonstration of these patterning process are shown in the Figure 2 (left): the smallest features seen in the image are 20 microns wide, which can be reliably patterned using the first process. If we conservatively allow for a 20 micron buffer region around the patterned features, in this case superconducting TiN leads, our novel process will permit the fabrication of bolometric detector arrays, with a backshort under grid architecture, with a filling fraction $\sim 94\%$.

Figure 2 (right) shows the smallest indium bumps, 20 microns, which can reliably be lifted off a substrate containing through wafer vias. As it is in the case of all patterned features fabricated on the through wafer via substrate, the size of the bumps will limit the optical filling fraction of the focal plane bolometric detector arrays. Placement of the bumps can be as close as five microns away from the vias, which illustrates the versatility of this process.

5. HYBRIDIZING DETECTOR ARRAYS TO MULTIPLEXERS

GSFC has established a critical capability of indium bump bonding with broad applications for kilopixel detector integration. This process allows for a high filling factor and enables us to optimize three components, (bolometer array, grid with through vias and SQUID multiplexers) separately. Through numerous bump bond interface samples, which consistently demonstrated critical currents exceeding 2 mA and thus far exceed the requirements of any of the aforemen-tioned FIR applications, we have been able to demonstrate the reliability of our bump bond process.

Furthermore, we have hybridized 32x40 BUG arrays to NIST multiplexers and were able to successfully integrate them in the HAWC+ instrument. Figure 3 shows a photograph of one of the two focal plane arrays for SOFIAs FIR polarimeter HAWC+. The pixel yield of this hybridized array is $> 80\%$, while the measured detector noise is at the thermodynamic limit [2]. HAWC+ commissioned these detectors in April, 2016.

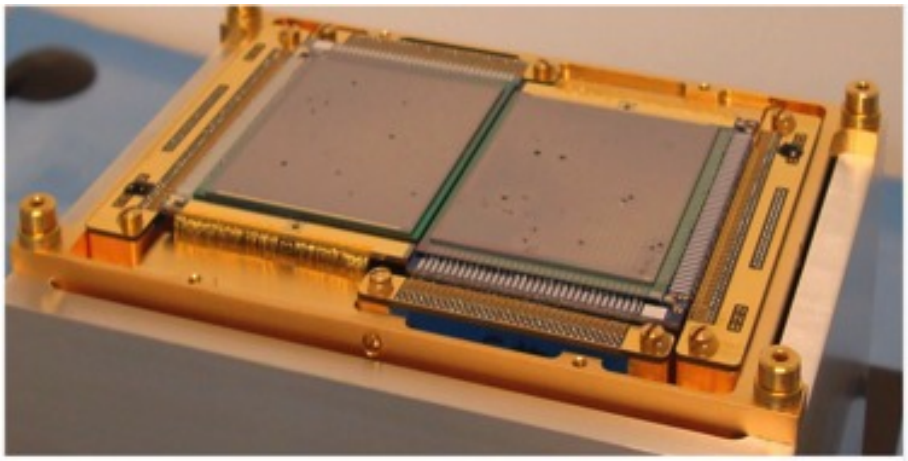

Figure 3. Photograph of one of the two focal plane arrays for SOFIAs FIR polarimeter HAWC+

6. READOUT BOARD

While our initial plan was to directly mate the detector to a 2-D multiplexer (Fig. 1), we have decided to also explore more flexible options. This scheme will allow for more flexibility and possibly less complexity in the design of the readout multiplexers. The mating fanout board (we call the "wiring chip") which replaces the SQUID multiplexer has the same metal layers as the boards used to produce the interface chips used for time domain readout boards: 2 Nb, 2 insulators, and one resistive layer. One feature of the board is that it has a polyimide layer in the center over which the Nb wiring is deposited (Fig. 4). The part of the wiring chip under the polyimide can be removed via a deep edge process, allowing the folding of part of the board out of the plane of the detector. This method will enable close to gapless tiling of detector arrays.

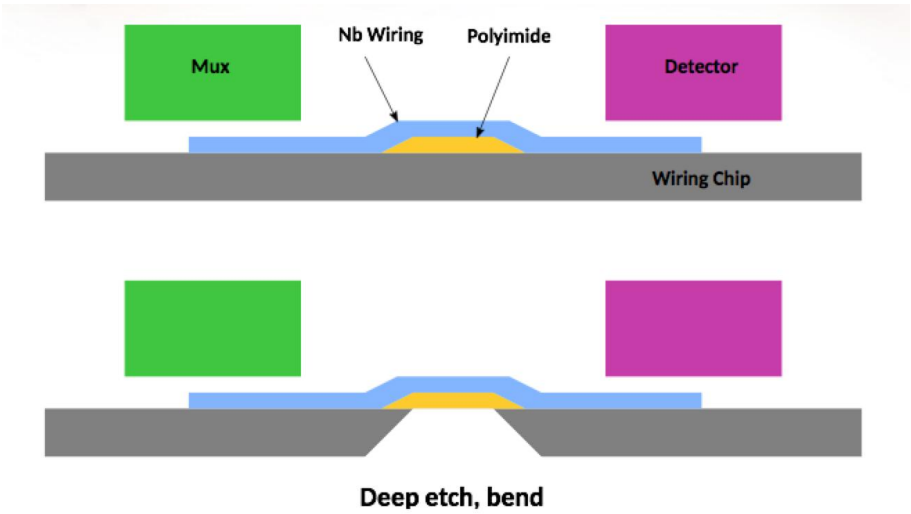

Figure 4. Schematic demonstrating how the "wiring chip" allows the folding of part of the board out of the plane of the detector, without breaking the Nb wires.

7. SINGLE LAYER TUNABLE TES DETECTORS

Our Co-Investigators at NIST have pioneered the use of AlMn as a single-layer tunable TES material [6] that mitigates many of the difficulties of proximity bi-layers. In this material system a weakly doped 2000 ppm

Mn aluminum film is used as the TES. The Tc is controlled (in the range of 100-400 mK) by adjusting the doping, film thickness and by a post-deposition thermal annealing step. AlMn has considerably higher resistivity than convention TES material (Au/Mo, Cu/Mo, Al/Ti). In order to meet the needed TES normal resistance ($\sim$ 10 $m\Omega/square$) suitable for use with time domain multiplexing (TDM) readout schemes, we successfully tuned the thickness of the substrate, and achieved both desired Tc and lower normal resistance, while these thicker films exhibit the same uniformity and stability as thinner films [7]. For the production of the TES we take advantage of this progress and use AlM single layer for our demonstration array.

8. FAR-INFRARED ABSORBERS

While we have not converged yet on an absorber material, our plan is to patterning the material to achieve the required impedance, leaving us with a wide range of materials such as molybdenum-silicite.

9. CONCLUSION

We have developed a new architecture and approach to enable the efficient production of large, TES based detector arrays for FIR astronomy. In this scheme we can directly bump-bond a detector array to a 2-D SQUID multiplexer. Alternatively we can use a dedicated "wiring chip" to route the signal to a the cryogenic multiplexers with different cell sizes than the detector pixels. These fwiring chips can be folded so that the final integrated detector will be nearly gapless tileable. This technology is expected to enable future large arrays with $\sim 10^4$ pixels, which is required for future FIR space missions such as OST.

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