One Time Programmable Antifuse Memory Based on Bulk Junctionless Transistor

Jin-Woo Han, Dong-Il Moon, and M. Meyyappan

Abstract— **One time programmable (OTP) antifuse base memory is demonstrated based on a bulk junctionless gate-all-around (GAA) nanowire transistor technology. The presented memory consists of a single transistor (1T) footprint without any process modification. The source/drain (S/D) and gate respectively become bit line and word line where the antifuse is formed by oxide breakdown across the gate and the channel. The channel is connected directly to the bit line due to junctionless S/D and inherently isolated from the neighboring cell by the GAA channel. Therefore, an array of 1T antifuse OTP can be a candidate for the sub-5nm technology node.**

Index Terms— **OTP memory, embedded non-volatile memory (NVM), antifuse, junctionless transistor, logic compatible NVM**

I. INTRODUCTION

ONE time programmable (OTP) non-volatile memory has long been used in security key, analog calibration, identification tag and SoC configuration [1]. The OTP market is expected to grow continuously due to the anticipated demand from internet of things and shortening the time to market cycle [2]. The types of OTP include embedded floating gate or charge trapped memory, electrical fuse (eFuse) and antifuse [3], where the antifuse is the most widely used due to its small cell size, logic process compatibility, high security level and high temperature tolerance. The antifuse is programmed by the gate oxide breakdown to create a conductive path across the gate and the channel/diffusion. **Fig. 1** illustrates variations of bit cell structures. In 2T cell, an access transistor is connected in series to a memory cell wherein the antifuse is formed between the n^+ gate and n^+ diffusion as shown in **Fig. 1(a)** [4]. In this structure, tail bits are often problematic because the breakdown is occasionally formed near the p-well region. The 1.5T bit cell is a two terminal device that looks like a MOS capacitor. This device adapts a split-channel using thin oxide for logic and thick oxide for I/O transistors in a standard logic process, which leads to the breakdown favorably happening near the oxide corner as shown in **Fig. 1(b)** [5]. Therefore, the state distribution becomes tightened. The 2T and 1.5T cell occupy a larger area than the 1T cell, which becomes a drawback as the storage capacity demand is increased. In order to boost the area efficiency, a vertical cross point memory (VCM) structure or 1T bit cell was suggested, which looks similar to the conventional transistor structure as shown in **Figs. 1(c) and 1(d)** [6]. The VCM is also a two-terminal device where the breakdown is formed across the P^+ gate as word line (WL) and the n-well as bit line (BL), yielding rectifying conduction characteristics. In order for the n-well to be the BL, however, non-standard deep trench isolation (DTI) process needs to be added to isolate neighboring BLs as well as a higher dose of n-well is needed to reduce the BL resistance.

At the latest technology node, the antifuse memory has been demonstrated on FinFET technology [7]. As technology node further advances to its end, a gate-all-around (GAA) nanowire device is thought to be an ultimate technology [8]. In principle, the operation mechanisms of 2T and 1.5T bit cells can be applied in the GAA. However, the 1T bit cell seems not implementable because the body contact cannot be made due to its inherent floating body.

In this paper, we experimentally demonstrate that a junctionless type GAA is inherently practical for 1T OTP without any process change. As shown in **Figs. 1(e) and 1(f)**, the 1T GAA OTP is almost identical to a standard GAA transistor, except that the source/drain (S/D) are tied to be BL. Due to the junctionless nature, the channel is directly connected to the BL. Furthermore, the BL is naturally isolated from adjacent BLs. Therefore, the breakdown across the gate and the body forms a rectifying junction regardless of the breakdown location because the doping type for the S/D and the body are identical.
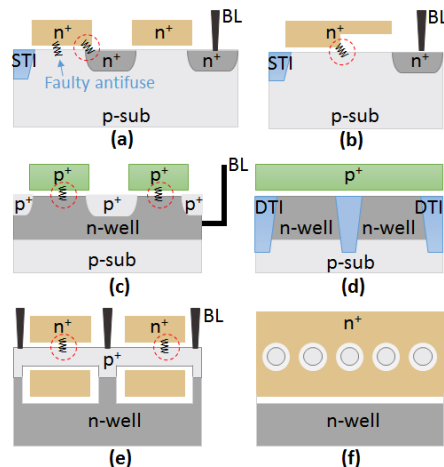
Fig. 1 Schematic illustration of a conventional one time programmable (OTP)

memories based on conventional (a) 2T cell, (b) 1.5T split-gate cell, (c) 1T cell along BL and (d) WL direction, and (e) proposed junctionless gate-all-around 1T cell along BL and (f) WL direction.

II. RESULTS AND DISCUSSION

Fig. 2 shows the fabricated device and the drain current versus gate voltage (I_d-V_g) curve to demonstrate its normal transistor behavior. The fabrication process follows the conventional GAA technology previously demonstrated in [9]. **Fig. 3(a)** shows the operation conditions for OTP. **Fig. 3(b)** shows the programming and program inhibiting characteristics for selected and unselected cell, respectively. The breakdown occurs around WL=4.4 V and BL=0V at selected cell whereas BL=2.5V suppresses the electric field to inhibit the programming to the unselected cell. The read characteristics in **Fig. 3(c)** show that the read currents are approximately 1 μA and 1 pA in the programmed and unprogrammed cells, respectively. In order for a successful two-terminal cross point array, the reverse current path made by neighboring cells needs to be eliminated. When the read bias is WL=0V and BL=1V, the other unselected WLs are disabled by applying WL=1V. In this case, the unselected bit lines are reverse biased. In this regard, **Fig. 3(d)** compares the forward read current and the reverse disturb current. The discrepancy demonstrates that the antifuse shows rectifying characteristics.
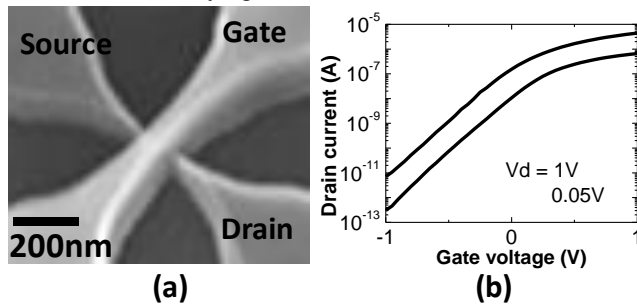

Fig. 2 (a) Bird's eyeview SEM image of the fabricated device and (b) I_d-V_g characteristics to demonstrate its normal device behavior.

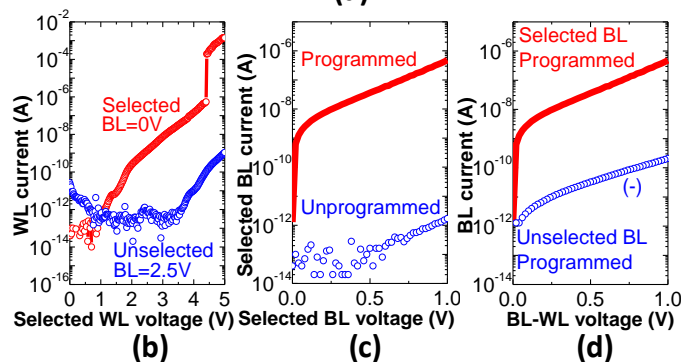|		WL	BL	Feature
Program	Selected	5.0 V	0.0 V	High oxide field
	Unselected	0 V	2.5 V or floating	Low oxide field
Read	Selected	0.0 V	1.0 V	Forward bias
	Unselected	1.0 V	0.0 V or floating	Reverse bias

(a)

(b)　**(c)**　**(d)**

Fig. 3 (a) summary of program and read conditions, (b) measurement result of DC oxide breakdown characteristics of the programming cell and program

disturb cell. The antifuse condition path is made by a high electric field across the WL and BL, whereas the program disturb in unselected cell is inhibited by lowering the electric field. (c) diode characteristics across the WL and BL at selected cell. (d). Comparison of the forward read current and the reverse disturb current.

The reverse biased leakage in p-n junction is supposed to be substantial due to band-to-band tunneling when the doping concentrations on both sides exceed 10^{19} /cm³. The measured reverse biased leakage current of the present OTP structure is well suppressed even when the gate and the channel doping concentrations are 10^{20} /cm³ and 10^{19} /cm³. An energy band simulation is carried out in order to verify the suppression mechanism of the band-to-band tunneling. **Fig. 4(a)** shows the device schematic used in the simulation. The breakdown oxide is emulated using n⁺ silicon bridging the gate and the channel near a gate corner, which is the worst-case breakdown point. The energy band diagram in **Fig. 4(b)** is extracted along the cut line crossing the antifuse shown in **Fig. 4(a)**. The gate field effects on the channel potential are investigated using two different dielectric constants. A hypothetical gate dielectric with a dielectric constant of 10^{-7}, *i.e.* nearly zero, is considered in order to neglect any gate field effect to the channel. In this case, the energy band is formed solely by the doping conditions. At a reverse bias of -1V, the valance band of the p-type channel becomes higher than the conduction band of the n-type gate, which can cause the band-to-band leakage. In reality, the silicon dioxide around the gate with a dielectric constant of 3.9 induces the gate field across the gate oxide and fringing gate field via the spacer region. Therefore, the channel potential near the antifuse is depleted due to the gate field and nanowire nature. As a result, the reverse biased tunneling energy band width becomes wider, resulting in suppression of the band-to-band tunneling. The potential contours in **Fig. 4(c)** support further the gate field induction of the effectively depleted channel. **Fig. 4(d)** shows the reverse saturation current for various dielectric candidates. As the dielectric constant is increased, the leakage current decreases by five orders of magnitude. However, when the dielectric constant is increased beyond 10, the leakage current becomes worse due to the gate field induced band-to-band tunneling.

The various reliability factors are investigated next. **Fig. 5(a)** shows read characteristics at elevated temperature. The read window degradation is negligible at 85 °C. The write disturb reliability is assessed by repeated pulse with 60 μsec at WL=0V and BL=2.5V. **Fig. 5(b)** shows that the unprogrammed cell read current after write disturb is increased up to one order of magnitude compared to the fresh state. This is attributed to the stress induced leakage current. Nevertheless, it is assured that the operation condition guarantees the write disturb for 10^3 write cycles. The antifuse retention at an elevated temperature of 200 °C is measured with the post-stressed cell. **Fig. 5(c)** shows that the sensing window still remains at more than four orders of magnitude. At early retention duration, the read currents for both the programmed and unprogrammed are reduced. The reduction is attributed to the fact that the conduction along the soft-breakdown path at the programmed cell is recovered by low temperature long term annealing effect. Likewise, the stress induced leakage at the unprogrammed cell is found to be restored. The ratio between the forward current and reverse leakage current is approximately 10^3, which would determine the maximum array size.

Fig. 4 (a) Schematic of the junctionless OTP device used in the simulation, (b) T-CAD simulation of reverse biased energy band diagram along the cutline in (a) for different dielectric constants, (c) potential contour for increasing reverse bias voltage, and (d) T-CAD simulation of reverse biased leakage current normalized by that for zero dielectric constant.
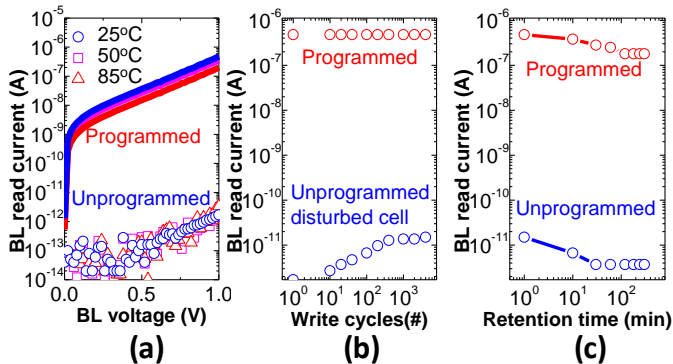
Fig. 5 (a) read current for various temperatures, (b) Read current after cumulative half-select write disturb and (c) Retention time characteristic at 200 ºC after hold.

III. CONCLUSIONS

In this work, junctionless gate-all-around nanowire transistor is used to demonstrate one-time-programmable nonvolatile memory application without any process modification. The OTP function is implemented with a single-transistor form factor. The rectifying current-voltage behavior is shown when the antifuse is formed. The read current at the selected cell is the forward biased p-n diode current. The reverse leakage current becomes the read disturb current at the unselected cell where the suppression mechanism of the reverse biased leakage current is attributed to the gate field and fringing field induced channel depletion. The demonstration here suggests that the junctionless device structure based OTP may be a candidate for sub-5nm

technology node.

REFERENCES

[1] Y. Ma and E. Kan, "One-Time Programmable Memories in Logic Processes," in *Non-logic Devices in Logic Processes*, 1st ed., Springer, Cham, 2017, pp 185-198.

[2] R. S.-J. Shen, M.-Y. Wu, H.-M. Chen, and C. C.-H. Lu, "A high-density logic CMOS process compatible non-volatile memory for sub-28 nm technologies," in *VLSI Symp. Tech. Dig.*, Jun. 2014, pp. 1–2. (10.1109/VLSIT.2014.6894353)

[3] E. Ebrard, B. Allard, P. Candelier and P. Waltz, "Review of fuse and antifuse solutions for advanced standard CMOS technologies," *Microelectronics Journal*, vol. 40, no. 12, pp. 1755-1765, Dec. 2009. (DOI: 10.1016/j.mejo.2009.09.007)

[4] W. Y. Hsiao, P.C Peng, T.S Chang, Y.D Chih, W.C Tsai, M.F Chang, T.F Chien, Y.C King and C.J Lin, "A New High-Density Twin-Gate Isolation One-Time Programmable Memory Cell in Pure 28-nm CMOS Logic Process," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 121–127, Jan. 2015. (DOI: 10.1109/TED.2014.2371617)

[5] G. W. Holloway, O. Ivanov, R. Gavrilov, A. G. Bluschke, B. K. Hold, and J. Baugh, "Electrical Breakdown in Thin Si Oxide Modeled by a Quantum Point Contact Network," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3005–2016, Aug. 2016. (DOI: 10.1109/TED.2016.2577611)

[6] H.S. Luan, "One-time programmable memory and method for making the same," U.S. Patent US9887201B2, Feb. 6, 2018.

[7] P.C Peng, Y.Z Chen, W.Y Hsiao, K.H Chen, C.P Lin, B.Z Tien, T.S Chang, C.J Lin and Y.C King, "High-Density FinFET One-Time Programmable Memory Cell With Intra-Fin-Cell-Isolation Technology," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1037–1039, Oct. 2015. (DOI: 10.1109/LED.2015.2472300)

[8] H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S. C. Jeon, G. S. Lee, J. S. Oh, Y. C. Park, W. H. Bae, H. M. Lee, J. M. Yang, J. J. Yoo, S. I. Kim, and Y.-K. Choi, "Sub-5 nm all-around gate FinFET for ultimate scaling," in *VLSI Symp. Tech. Dig.*, Jun. 2006, pp. 70–71. (DOI: 10.1109/VLSIT.2006.1705215)

[9] D.I Moon, S.J Choi, J.P Duarte and Y.K Choi "Investigation of Silicon Nanowire Gate-All-Around Junctionless Transistors Built on a Bulk Substrate", *IEEE Transactions on Electron Devices*, vol. 60, no. 4, pp. 1355-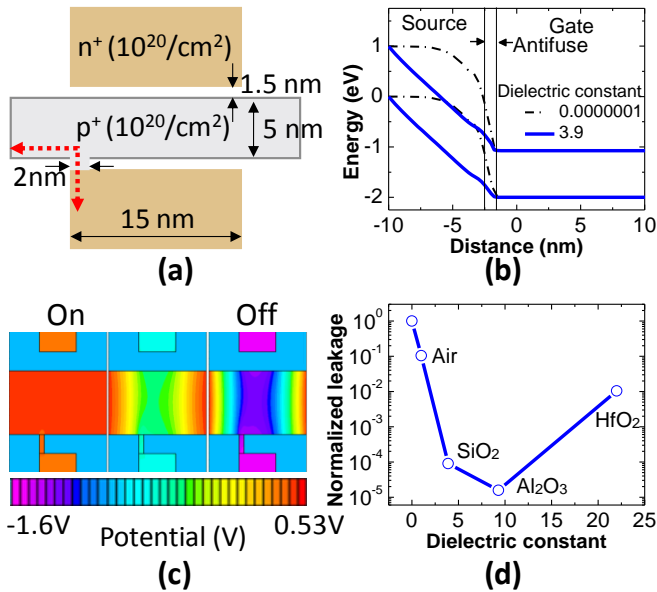1360, Apr. 2013. (DOI: 10.1109/TED.2013.2247763)