Graphical Primer of NASA Glenn SiC JFET Integrated Circuit (IC) Version 12 Layout

How to layout 500 °C durable integrated circuit cells for fabrication by NASA Glenn





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NASA Glenn SiC JFET IC Version 12 7 Drawn Layers Needed to Define Circuit Mask Layout

Key Background Info: See https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf slides 20-32 for a series of cross-sections illustrating the use of these 7 layers to build SiC JFETs, resistors, and integrated circuits [1].

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All circuits (transistors and resistors)	p layer	drawing		2	0			
	n layer	drawing		4	0			
	Metal1	drawing		10	0			
implemented/defined	Via1	drawing		11	0			
in those 7 drawn layers	Metal2	drawing		12	0			
in these 7 drawn layers.	Via2	drawing		13	0	ノ		
	💽 Via3	drawing		15	0			
Other layers in grey are	Metal3	drawing		18	0			
for chip bond pads that	I p layer	drawing		41	0			
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information that follows in the rest of this layout primer. NASA Glenn IC12 Layout Primer April 2019

The NASA SiC JFET IC fabrication process mask order [1]:
1. "p layer" defines JFET p+ gate mesa.
2. "n layer" defines JFET and resistor n mesa channel.
3. "Deep N Well" defines n+ contact implant.
4. "Via1" defines where Metal1 contacts the SiC devices.
5. "Metal1" defines 1 st layer interconnect pattern.
6. "Via2" defines Metal1 to Metal2 connections.
7. "Metal2" defines 2 nd layer interconnect pattern.

So long as layout geometries and layers described in this document are followed, NASA Glenn can import a GDS file of your design into its master IC mask design for fabrication[2].

[2] Under mutually agreed Space Act Agreement.

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Illustration of p+ Gate Mesa (p layer) and N-Channel Mesa (n layer) Layout (Dimensions in μm)



Additional Mesa Layout Rules

- 1. No n n layer or p layer mesa feature may exceed 200 µm in length or width dimension.
- 2. No p layer gate fingers longer than 50µm in length (excluding the contact/via region length).
- 3. <u>All JFET p layer gate finger contact/via regions must be "flag" geometry as shown above.</u>
- 4. Gate lengths longer than $3\mu m$ are permitted.
- 5. All n layer n-channel resistors must be isolated and straight-line as shown above, "<u>U" or "serpentine" shapes are NOT allowed.</u>
 - "Flag" geometry resistor end contacts (analogous to gate finger contacts) are permitted (as shown Slide 9).
 - Resistor widths wider than 2µm are permitted (as shown Slide 9).



NASA Glenn SiC JFET IC Version 12 Illustration of N+ Source/Drain Implant (Deep N Well) Layout (Dimensions in μm)

Additional N+ Source/Drain Implant (Deep N Well) Layout Rules

1. No source/drain implant dimension may exceed 48µm.

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Illustration of Via1 Layout: ALL Via1 FEATURES MUST BE 3µm x 3µm, separated by at least 3µm!!!



Via1 features must reside at least $3\mu m$ from n-mesa edge.

"M" factor describes how many Via1 contacts are made to JFET source or drain.

M x $6\mu m$ approximates the total effective gate width (W_G) of the JFET.

M should not be larger than 6, due to 50µm gate finger length restriction stated on slide 3 (bullet 2).

NASA Glenn SiC JFET IC Version 12 Illustration of Metal1 Layout (Dimensions in μm)



Metal1 Layout:

- 1. Surround all Via1 features by 3µm of Metal1.
- 2. 6µm minimum Metal1 to Metal1 Isolation spacing.
- 3. 6µm minimum Metal1 feature width.
- 4. Do not route Metal1 traces that traverse separated n layer mesa features that are supposed to be electrically isolated from each other.
 - Such features have potential to create undesired parasitic inversion channel MOSFET.
- 5. Parasitic resistance of Metal1 is roughly 5 ohms per square.

NASA Glenn SiC JFET IC Version 12 Illustration of Via2 Layout (Dimensions in μm)



Via2 Layout:

- 1. Surround all Via2 features by 2.25µm of Metal1
- 2. All Via2 features are 4.5µm x 4.5µm.
- 3. All Via2 features must reside at least 2.25µm from any underlying n layer or p layer mesa or Via1 edges.
 - In other words, all Via2 features must reside on flat topography with 2.25µm alignment tolerance.
 - Via2 feature can reside on top of flat regions above n layer or p layer mesas (areas without Via1 features).

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Metal2 Layout:

- 1. Surround all Via2 features by 5.25µm of Metal2
- 2. 6µm minimum Metal2 to Metal2 Isolation spacing.
- 3. 6µm minimum Metal2 feature width, but 12µm or larger Metal2 linewidth is preferred.
- 4. OK to traverse adjacent underlying n layer mesa features with Metal2 trace (as shown above)
- 5. Parasitic resistance of Metal2 is roughly 5 ohms per square.

NASA Glenn SiC JFET IC Version 12 Illustration of NASA Glenn Resistor Layouts (Dimensions in μ m)



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n layer					4	0	
n layer	drawing				4	0	
n layer	label				4	1	11
Active Contact					8		
Poly Contact					9		
Metal1					10	0	
Metal1	drawing				10	0	
Metal1	label				10	1	
Metal1	pin				10	5	
Metal1	fill				10	10	
Metal1	slot				10	7	
BE Metal1	blockage				10	30	
Via1					11	0	
Via1	drawing				11	0	
Metal2				므	12	0	
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NASA Glenn SiC JFET IC Version 12 "Base" NOT Logic Gate (<u>Layout Illustration is Rotated 90 degrees,</u> Dimensions in μm)



NASA Glenn standardized logic gate power bus (thickness and separation) of VDD, VSS, and GND are shown. - Use of labeled electrical connection ports (e.g., "VDD", "IN", etc. shown above) is not required.

- Labeled electrical connection ports reside on Metal1:pin and Metal2:pin separate layers (Data Type 5).

- Ports can assist with documentation and verification of layouts vs. circuit schematics.

← Corresponding schematic circuit diagram of NASA Glenn "Base" NOT gate, including corresponding ports.

NASA Glenn SiC JFET IC Version 12 Example AND Logic Gate (constructed using NAND + NOT base cells)

Circuit Schematic Diagram



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Corresponding Layout Cell

In NASA Glenn Layouts:

Metal1 traces predominantly run in vertical direction. Metal2 traces predominantly run in horizonal direction.

NASA Glenn SiC JFET IC Version 12 Illustration of NASA Glenn Multi-Finger JFET Layout

Layer Palette	†×	ICv12Design	📴 ICv12Design : Design Navigator 👖 cello 🔃 CatalogJFETsICv12 🗙						
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Notable Features of Mult-Finger JFET Layout:

- 1. Via 2 resides on top of (and is 2.25μm surrounded by) <u>flat Metal1</u> and region <u>flat n layer mesa</u> <u>without Via1</u>.
 - Deep N Well source/drain implant produces no surface topography, so it is allowed to extend underneath Via2.
 - No Via1 feature exists underneath or with 2.25µm of Via2 feature.
- 2. Electrical connection to Multi-Finger JFET Drain (D) must be made in Metal2.
- 3. Electrical connection of the multiple adjacent p layer gate fingers must be made in Metal1.
 - Do NOT use p layer (mesa) to connect multiple adjacent gate fingers, as this violates desired "flag geometry" (Slide 3, Bullet 3).

NASA Glenn SiC JFET IC Version 12 Device Orientation



Use only vertical and horizontal 90° device and via orientations.

DO NOT use devices and vias oriented at non-90° angles.

NASA Glenn SiC JFET IC Version 12 Diagonal Routing of Metal1 and Metal2 Traces (Dimensions in μ m)



Vertical and horizontal 90° routing of Metal1 and Metal2 is preferred.

Diagonal Metal1 and Metal2 traces are permitted only where all three below conditions are met:

- Diagonal portion of metal trace resides in field area where topography is flat.
- Diagonal portion of metal trace is at least 12µm away from topographic feature.
- Metal trace is at least 12µm wide.

NASA Glenn SiC JFET IC Version 12 Illustration of NASA Glenn Metal1 to Metal2 Capacitor Layout



Capacitor Layout

"Unit cell" (CBase40fF) consists of 48µm x 48µm square of Metal2 residing on top of 48µm x 48µm square of Metal 1

- Capacitance of a unit cell is 40 fF.

Repeat (adjacently connect) 48µm x 48µm square unit cells to build larger capacitors of desired shape.

- Larger capacitor can be any overall shape so long as it is comprised of adjacently connected unit cells.
- Capacitor peripheries must be surrounded by a 6um extension "ring" of Metal1.

NASA Glenn SiC JFET IC Version 12 Chip Size and Bond Pad Configuration

NASA Glenn will place the GDS layout file you send of your circuit layout into its standard IC Version 12 chip frame cell.

Your integrated circuit cell (including power bus traces) must fit within less than a square 4 mm x 4 mm area.

The NASA standard chip frame provides for an even distribution of 64 high-temperature durable bond pads.

- Bond pads are evenly distributed around the chip frame cell periphery, NO bond pads permitted in chip middle.
- Bond pads are designed to be compatible with either gold wire bonding or flip chip.
- Each high-temperature bond pad has a parasitic electrical series resistance of roughly 100 ohms.
 - Because of this series resistance, larger-current (power bus) connections should use multiple bond pads.
- Route your top-level cell signals and power to the cell periphery, NASA will route from there to chip bond pads.
 - Metal1 is preferred for larger-current (power bus) connections to bond pads.

NASA will carve (add) stress-management hole patterns into selected larger Metal1 and Metal2 traces and capacitors.

- Stress-management patterns will only be added to flat metal areas larger than 50 μm by 50 μm in your layout.

Key Online Technical References

Yearlong 500 °C Operational Demonstration of Up-Scaled 4H-SiC JFET Integrated Circuits (2018): Article: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf</u> Presentation: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190001885.pdf</u>

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits (2016): Article: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf</u> Presentation: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf</u>

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits (2016): Article: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf</u> Presentation: <u>https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf</u>

Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C (2016): Article: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf</u>

Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors (2018): Article: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf</u> Poster Presentation: <u>https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf</u>

SiC Resistor Modeling for IC Version 12