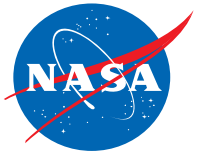

Technical Primer on Design and SPICE Modeling of Circuits for NASA Glenn SiC JFET IC Version 12 Prototype Wafer Run
Part 2: SiC Resistor Behavior and SPICE Modeling

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May 2019

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Outline

Goal: Enable anyone to SPICE-model and design 500 °C durable integrated circuits for their intended application.

IC Technology Overview:
- SiC n-channel JFETs
- SiC n-channel Resistors

Part 1: SiC JFET Behavior and SPICE Modeling

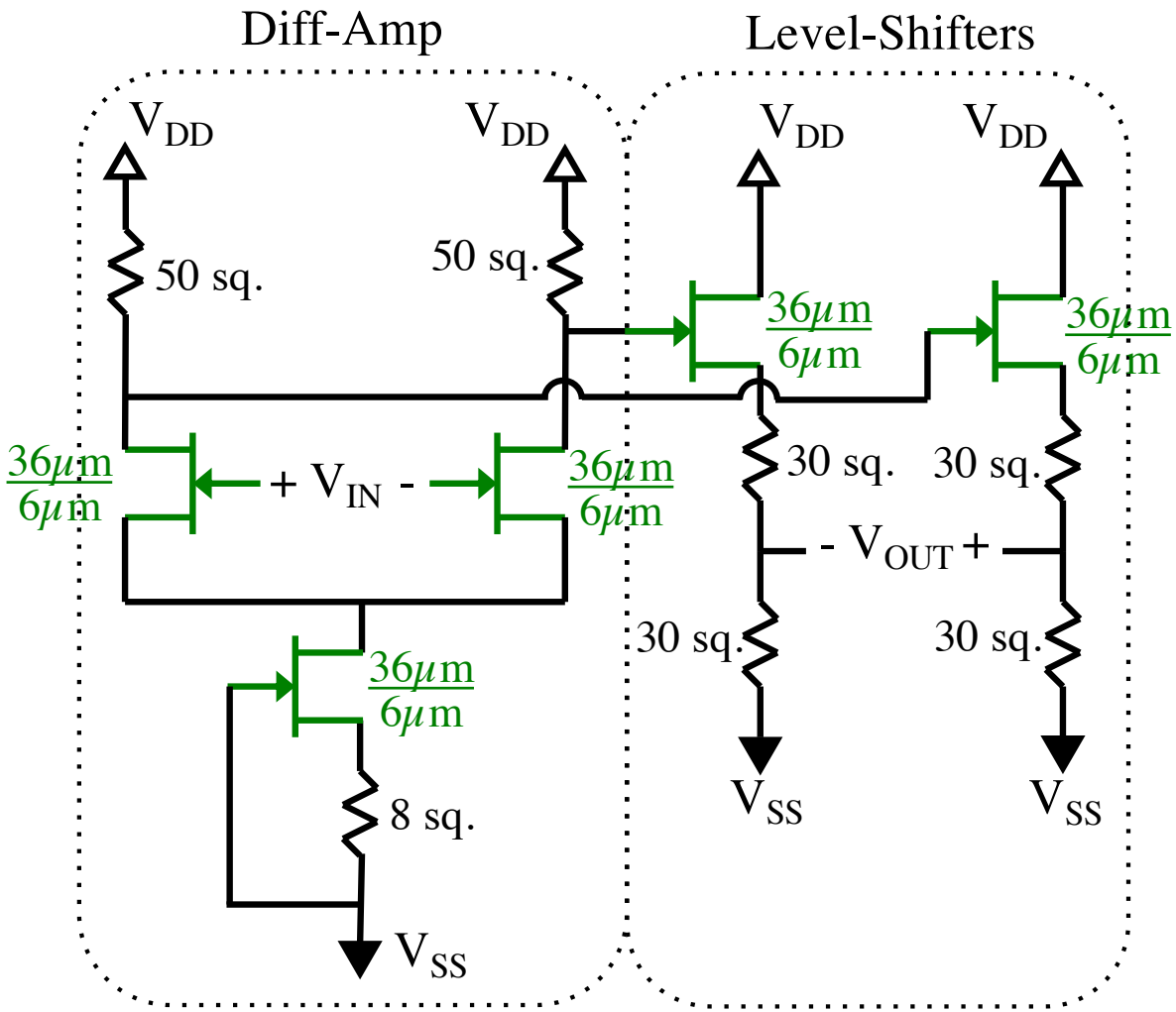
Part 2: SiC Resistor Behavior and SPICE Modeling

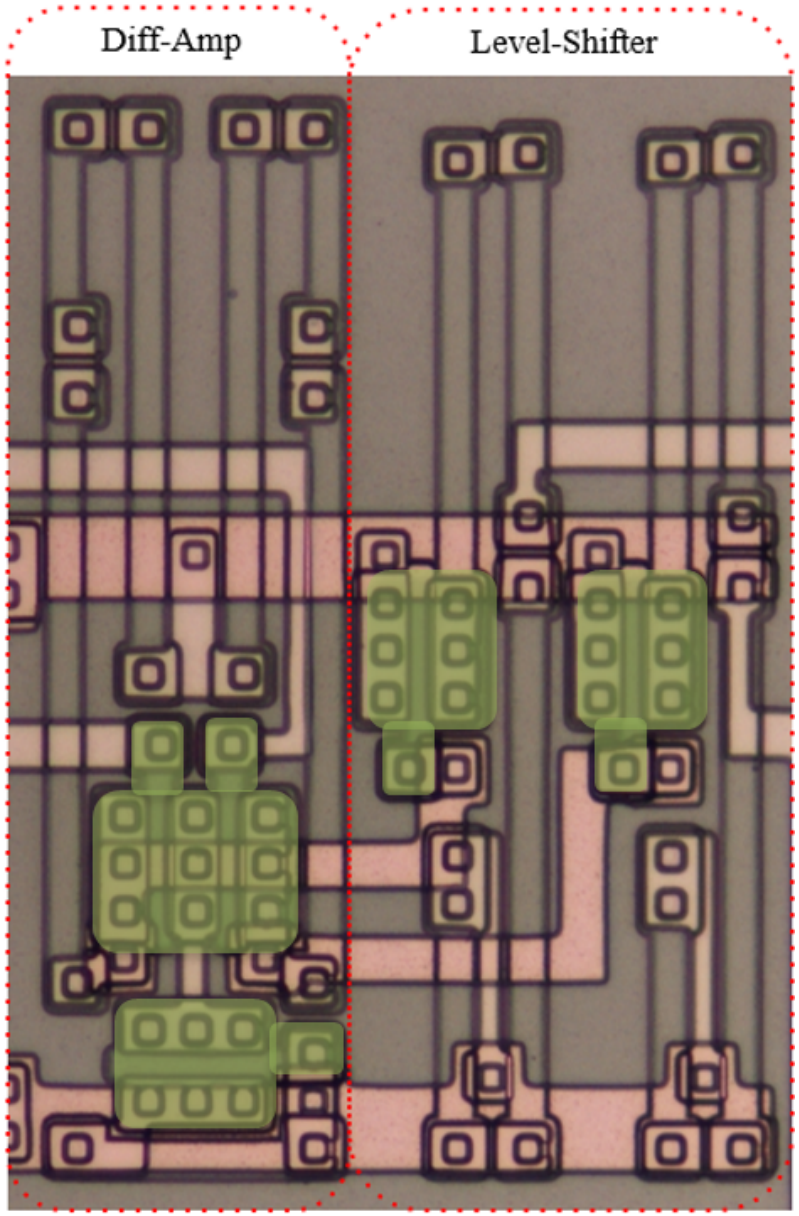
NOTE: Background information in web links provided in these presentations are key to needed technology understanding.

Circuit Approach

See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf

All integrated circuits in this project are comprised of interconnected 4H-SiC n-JFET's and 4H-SiC n-resistors.



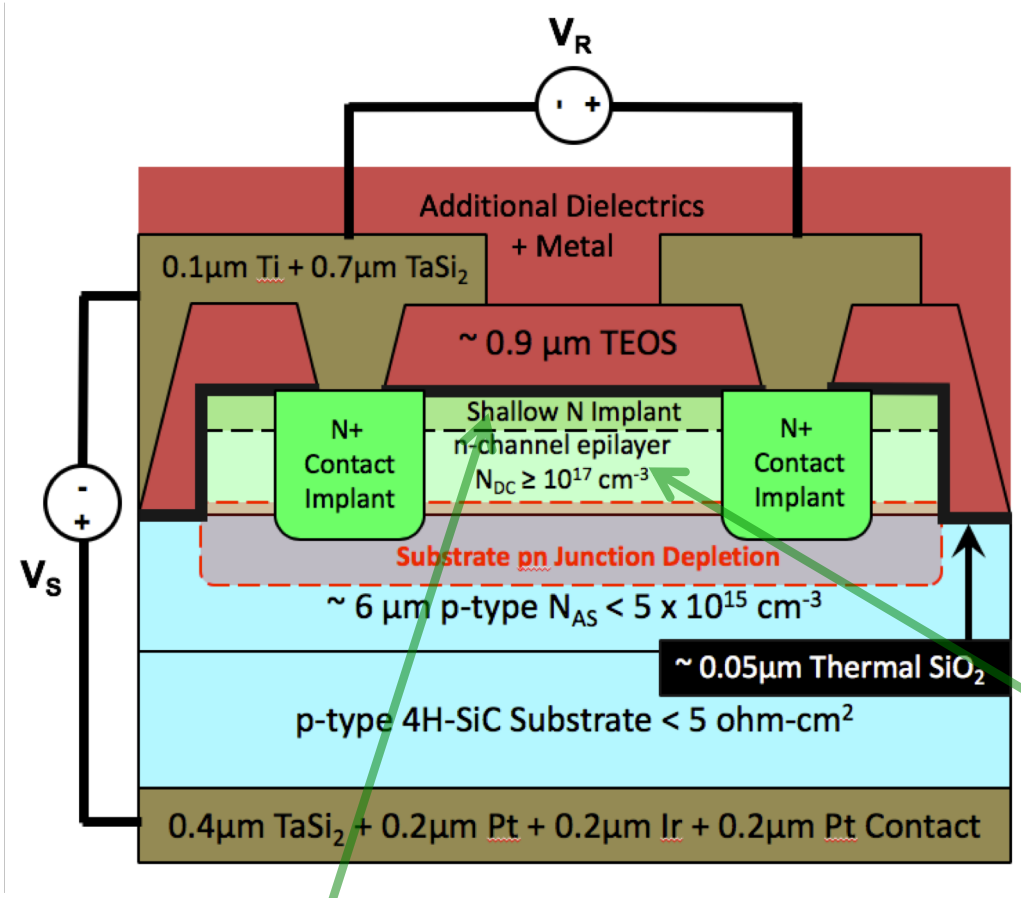


SiC Resistor Behavior

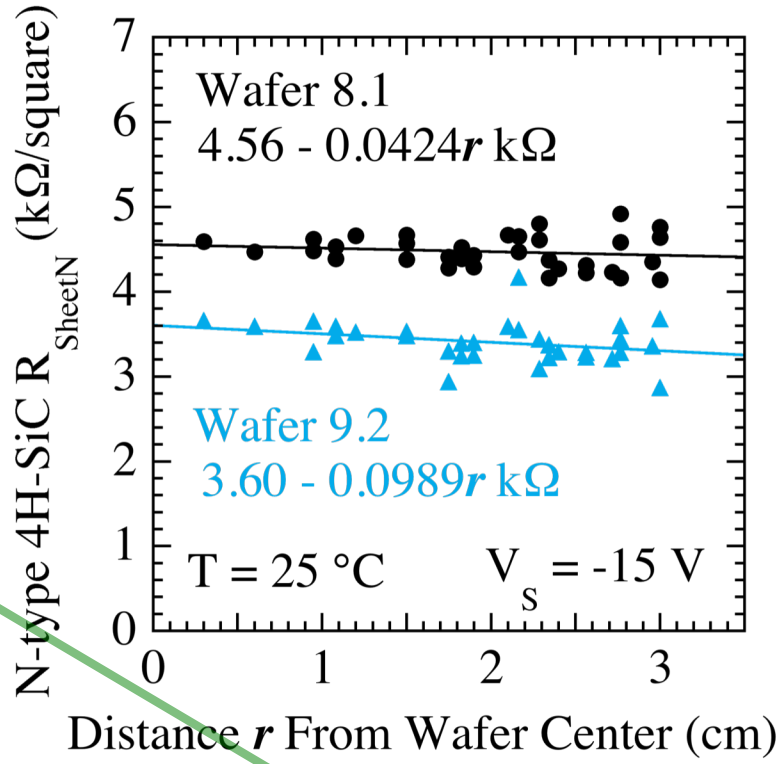
The following 3 slides summarize the resistor structure and substantial temperature and substrate body-bias dependence of resistor electrical properties observed in past NASA Glenn IC wafer runs.

These substantial temperature and substrate body-bias dependencies must be understood and taken into account when conducting design and SPICE modeling of circuits to be implemented in the NASA Glenn SiC JFET IC Version 12 wafer run.

Resistor Dependence on Wafer Position



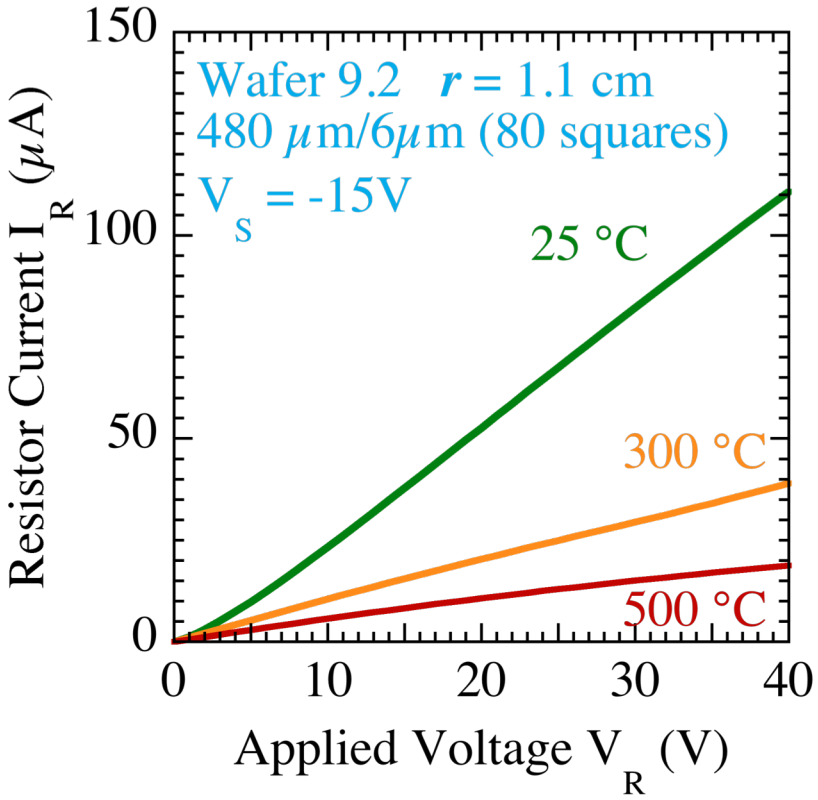
n-SiC Sheet Resistance (R_{SheetN}) from Transmission Line Method (TLM) data

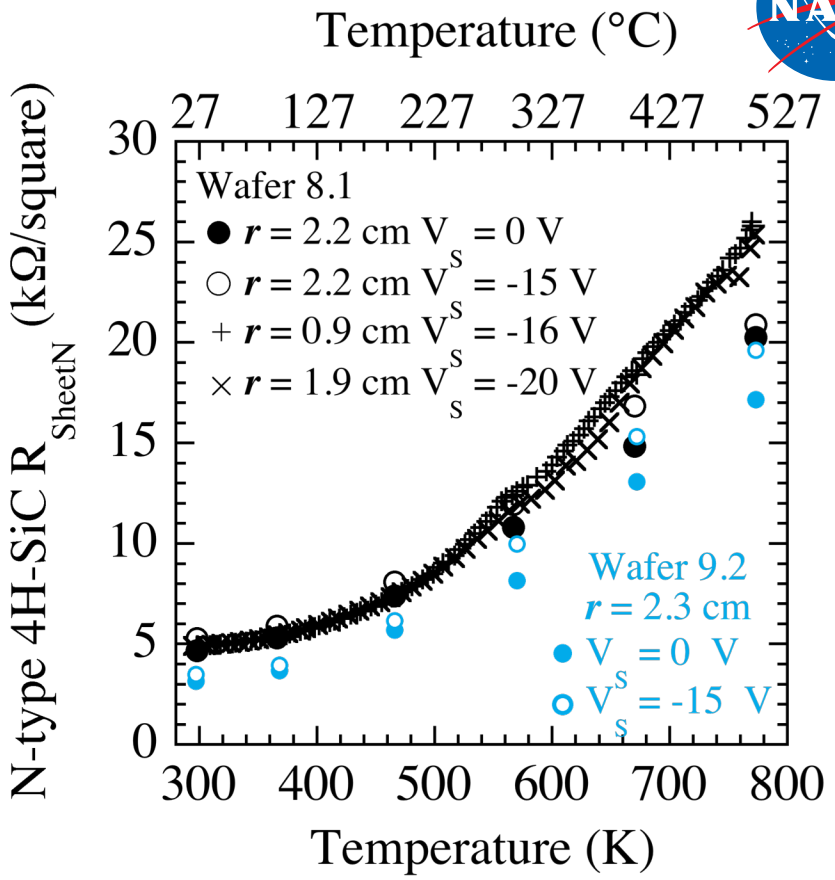


SiC *n-channel resistors* exhibit *negligible* wafer position dependence.

- The shallow N implant is uniform and provides more conductance than n-channel epilayer.

Resistor Dependence on Temperature





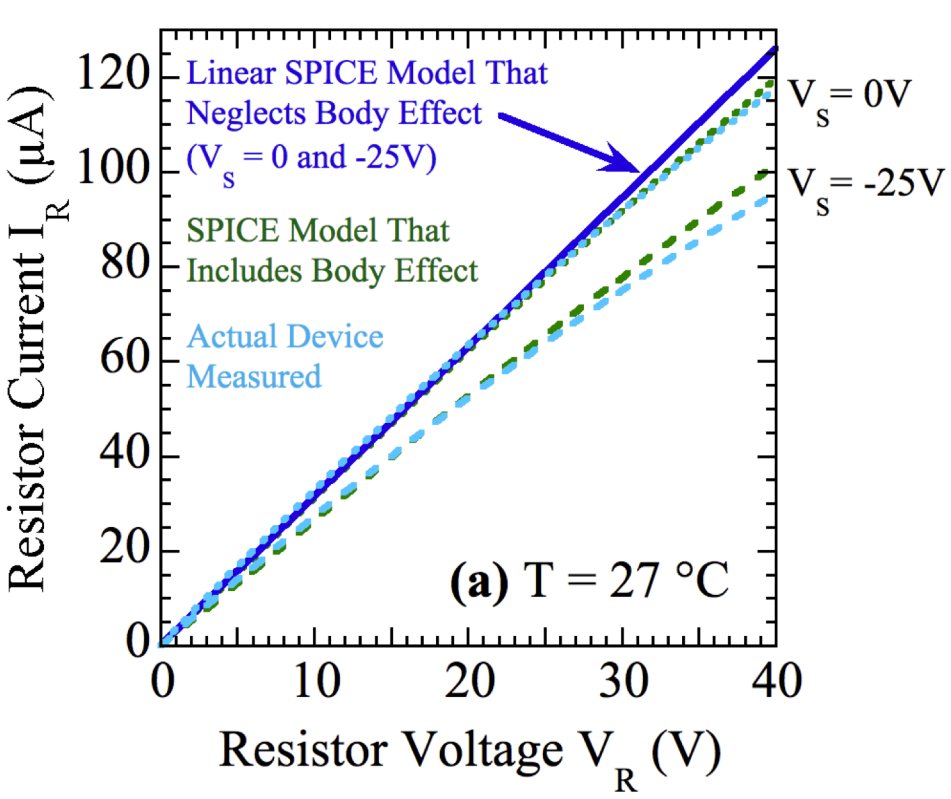
R_{Sheet} (and R) values increases about 5-fold as T increases from 25 °C to 500 °C.

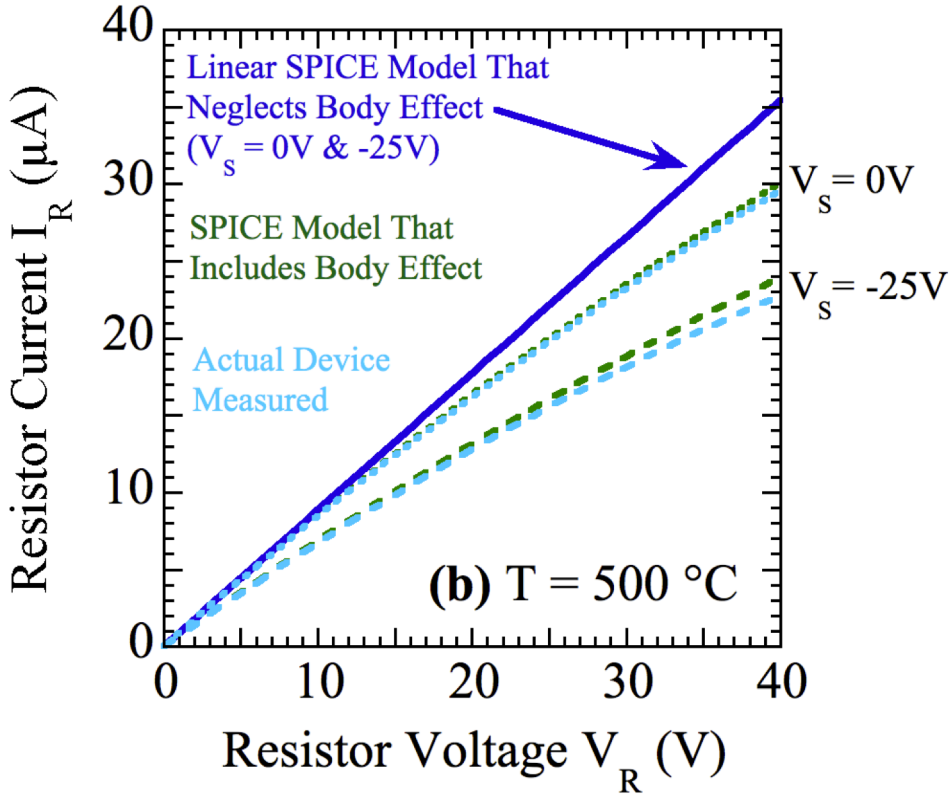
- Consistent to first-order with prior n-type 4H-SiC conductivity vs. T studies.

Resistor Dependence on Substrate Body Bias Effect

Substrate body bias effect on SiC IC resistor electrical characteristics is significant.

- Below plots show how body effect affects resistor current-voltage properties.
- SPICE model that accounts for (i.e., includes) body bias effect is recommended.





See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf
and https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf

SiC Resistor SPICE Modeling

NASA Glenn SiC Resistor SPICE Modeling Approach

Many different SPICE versions and enhancements are available, but most share "baseline" features and device models from original SPICE version (developed at UC Berkeley).

However, baseline version SPICE resistor model **DOES NOT include body bias effect** that significantly impacts electrical behavior of NASA-implemented IC devices.

Baseline SPICE NMOS LEVEL 1 model (n-channel MOSFET, that includes body effect via SPICE parameter GAMMA) is therefore employed to model SiC resistors to first-order accuracy PROVIDED:

- Forward bias IS AVOIDED for substrate pn junctions.
- Wafer substrate bias voltage is connected to gate and bulk terminals of all modeled devices in order to properly model body bias effect.
- "Situationally correct" SPICE resistor models & parameters are employed.

Handle resistor temperature and body bias dependence by selecting the corresponding resistor SPICE model from the table on the next slide.

- DO NOT change the SPICE TEMP parameter from its default value (of 27 °C).
- NASA Glenn uses ".include" SPICE statement to load the corresponding SPICE model file from the "ICv12Models" folder.

See: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf
and https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf

Estimated SPICE Models for NASA Glenn IC Version 12 Resistors

Below models are ESTIMATED, NOT exact.

- See data scatter slides 5 & 6.
- Version12 IC technology is not yet experimentally implemented or characterized.

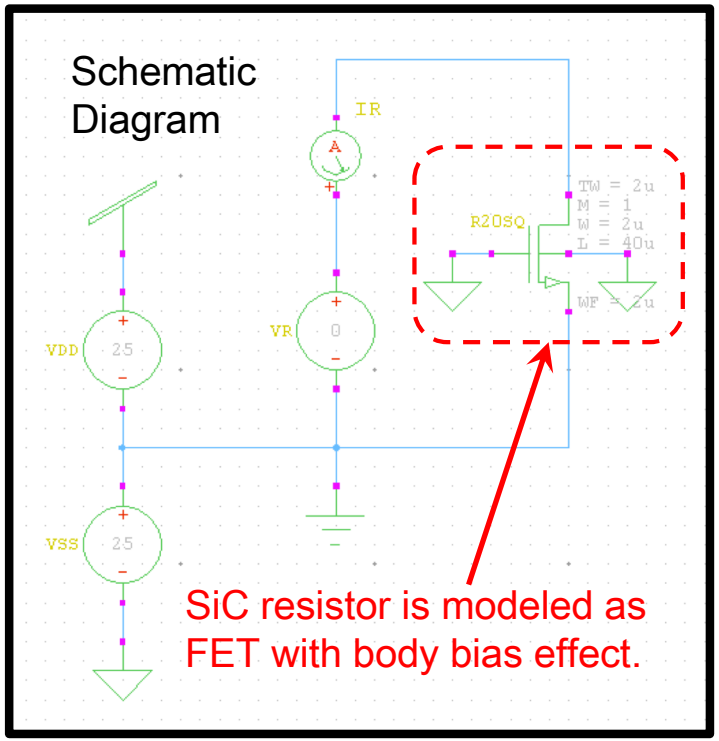
Minimum resistor width dimension is 2 µm. Maximum resistor length dimension is 200 µm.

T	SPICE Model for IC Resistors Including Substrate Body Bias Effect
25 °C	.MODEL RBodyBiasModel NMOS LEVEL=1 VTO=-151.256 KP=1.819E-6 CJ=6.856E-5 PB=2.870 PHI=1.435 RSH=0.000E+0 GAMMA=1E-12 RS=5073 RD=5073 JS=1.00E-25
460 °C	.MODEL RBodyBiasModel NMOS LEVEL=1 VTO=-136.774 KP=5.647E-7 CJ=8.065E-5 PB=2.074 PHI=1.037 RSH=0.000E+0 GAMMA=1.00E-12 RS=1753 RD=1753 JS=1.00E-25
500 °C	.MODEL RBodyBiasModel NMOS LEVEL=1 VTO=-135.480 KP=5.183E-7 CJ=8.220E-5 PB=1.997 PHI=0.998 RSH=0.000E+0 GAMMA=1.00E-12 RS=1634 RD=1634 JS=1.00E-25

Example SPICE instance text line for 20-square resistor (layout depicted below, dimensions in µm):

MR20SQ PLUSnode VSSnode MINUSnode VSSnode RBodyBiasModel L=40u W=2u AS=81p AD=81p

Example SPICE Simulation of SiC IC Resistor I-V Characteristics



Simulation example for a 20-Square L=40µm x W=2um SiC resistor at T=460 °C.

SPICE Input Deck Text

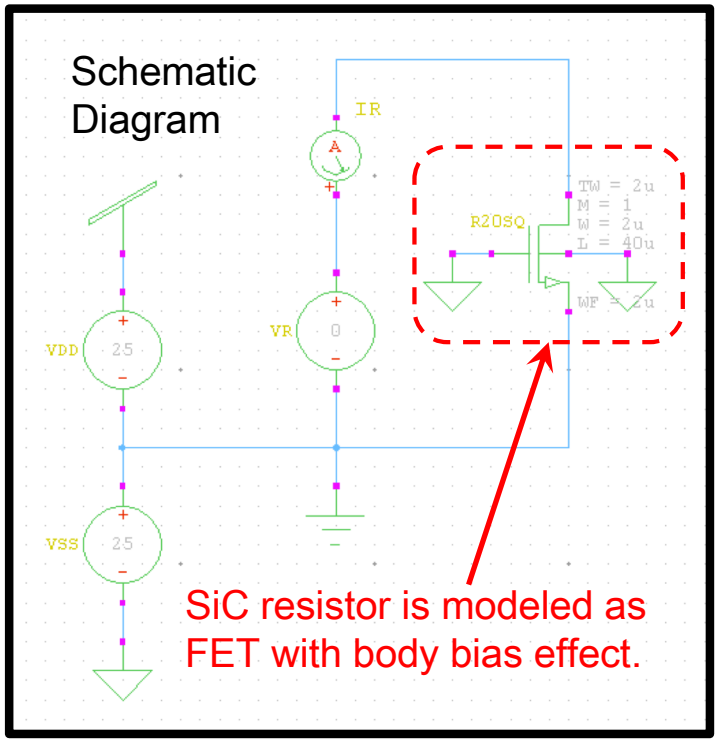
```
* NASA Glenn 20-Square SiC Resistor IV Simulation at 460C and VSS=-25V
.include "..\ICv12_Models\SiC_460C_10mm_v12_Models.txt"
MR20SQ N_1 Vss Gnd Vss RBodyBiasModel W=2u L=40u AS=81p AD=81p
VVDD Vdd Gnd  DC 25
VVR N_2 Gnd  DC 0
VVSS Gnd Vss  DC 25
VIR N_2 N_1 0v
.PRINT DC IR=I(VIR)
.dc VVR 0 40 1
.end
```

Included "SiC_460C_10mm_v12_Models.txt" file (corresponds to 2nd row of table in slide 10):

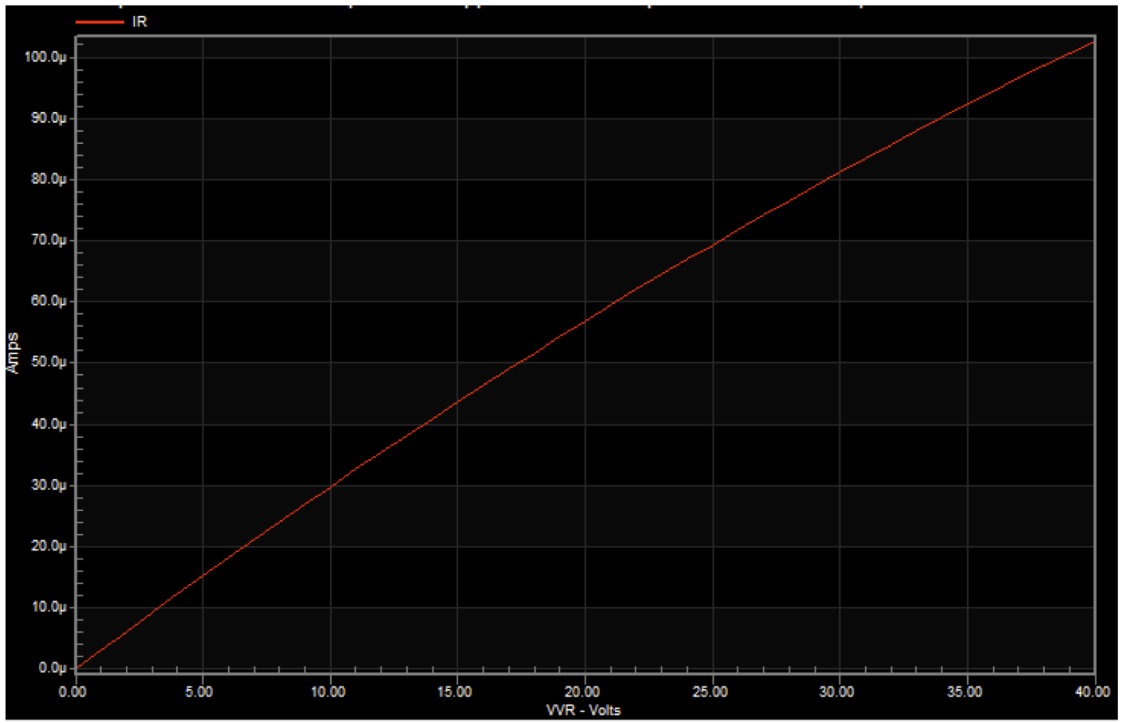
```
*SPICE Models for NASA JFET IC Version 12 T=733.0 K (460.0 C) and r=10.0 mm from wafer center.
.MODEL JFETModel NMOS LEVEL=1 VTO=-10.088 KP=2.393E-6 GAMMA=0.9207 LAMBDA=0.0200 RSH=0.000E+0
CJ=8.065E-5 PB=2.074 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.00E+0 PHI=1.037 RD=11464 RS=11464
.MODEL RSheetModel R RSH=1.295E+4
.MODEL RBodyBiasModel  NMOS LEVEL=1 VTO=-136.774 KP=5.647E-7 CJ=8.065E-5 PB=2.074 PHI=1.037
RSH=0.000E+0 GAMMA=1.00E-12 RS=1753 RD=1753 JS=1.00E-25
.MODEL RSourceImplant R RSH=607.0
```

NOTE: The "resistor" FET gate and body/bulk terminals are always connected to VSS supply!

Example SPICE Simulation of SiC IC Resistor I-V Characteristics



Simulation example for a 20-Square L=40µm x W=2um SiC resistor at T=460 °C.



SPICE Input Deck Text

```
* NASA Glenn 20-Square SiC Resistor IV Simulation at 460C and VSS=-25V
.include "..\ICv12_Models\SiC_460C_10mm_v12_Models.txt"
MR20SQ N_1 Vss Gnd Vss RBodyBiasModel W=2u L=40u AS=81p AD=81p
VVDD Vdd Gnd  DC 25
VVR N_2 Gnd  DC 0
VVSS Gnd Vss  DC 25
VIR N_2 N_1 0v
.PRINT DC IR=I(VIR)
.dc VVR 0 40 1
.end
```

Note the slight downward bend in the above SPICE-simulated I–V plot due to substrate body bias effect.

Key Online Technical References

Yearlong 500 °C Operational Demonstration of Up-Scaled 4H-SiC JFET Integrated Circuits (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180003391.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190001885.pdf

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014879.pdf
Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170001674.pdf

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160014886.pdf
Presentation: https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf

Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C (2016):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160005307.pdf

Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors (2018):
Article: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20180000657.pdf
Poster Presentation: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170009460.pdf