A Simple Control to Reduce the Voltage Stress of Non-Conducting Switches in Three-Level ANPC Converter

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***Abstract*—With the development of wide band-gap (WBG) technology, the switching speed of power semiconductor devices is increased, which makes circuits more sensitive to parasitics. For three-level active neutral point clamped (3L-ANPC) converters, the over-voltage of non-conducting switches can be an issue. This paper analyzes the multiple commutation loops in 3L-ANPC converter and summarizes the impact factors of the over-voltage for the non-conducting switch. It is found that the nonlinearity of the output capacitance of the device can significantly influence the over-voltage. A simple control without introducing any additional hardware circuit is proposed to attenuate the impact of the nonlinearity. With the proposed control, the peak over-voltage of the non-conducting switch can be reduced significantly. Multi-pulse test is conducted for a 3L- ANPC converter built with silicon carbide (SiC) MOSFETs. The testing results show that the peak over-voltage decreases from 892 V to 624 V with the proposed control. More detailed analysis and experimental results will be provided in the final paper.**

INTRODUCTION

Three-level (3L) converters are widely used in high power and medium voltage applications such as grid-tied inverters, motor drives, electric transportations and uninterruptible power supplies. Compared with conventional two-level (2L) converters, 3L converters own advantages such as lower EMI noise, lower required voltage rating for power semiconductor devices, better power quality, and higher control flexibility [1, 2]. Among the 3L topologies, the active neutral point clamped (ANPC) converter shown in Fig. 1 is a promising and popular candidate. All the switches in the converter can be actively controlled to achieve bidirectional power flow and high efficiency.

Different modulation schemes can be applied to control the 3L-ANPC converter [3-8]. In [3], two commonly used schemes are analyzed in detail, and the results show that the outer mode control can achieve lower switching loss compared to the inner mode control due to lower parasitics in commutation loops. The modulation of outer mode control for a single phase is plotted in Fig. 2. S_{1H} and S_{3H} operate complementarily at high switching frequency while S_{2H} operates at line frequency.

Owing to better switching characteristics of wide band-gap (WBG) power semiconductor devices like silicon carbide (SiC) MOSFETs and gallium nitride (GaN) HEMTs, the switching speed can be improved without increasing the switching loss. Nevertheless, the parasitics in the power loop have larger impact with the increase of switching speed. The higher dv/dt and di/dt can cause worse voltage and current spike on the power devices. Extensive work has been done to analyze and minimize the parasitics in switching loops of 2L converters [9-13]. However, not much research has been focused on 3L converters, which have multiple loops and are more complicated. In [14], the over-voltage of non-conducting switches in 3L-ANPC converters caused by long switching loops and reverse recovery is analyzed. However, the paper only gives a brief explanation for the phenomenon but no solution to reduce such over-voltage is provided.

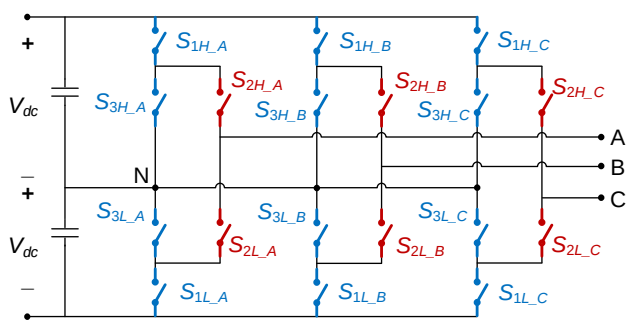


Fig. 1. Topology of 3L-ANPC converter.

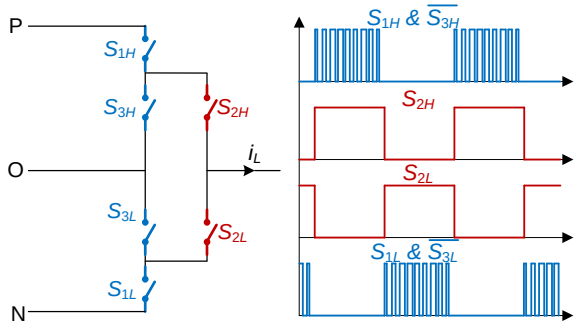


Fig. 2. Single phase and corresponding modulation.

To have comprehensive understanding of the over-voltage issue for the non-conducting switches in 3L-ANPC converters, this paper provides detailed analysis of multiple switching loops and finds the main impact factor of the over-voltage. Based on the analysis, a simple control method is proposed, and the over-voltage of non-conducting switches is reduced.

Loop Analysis

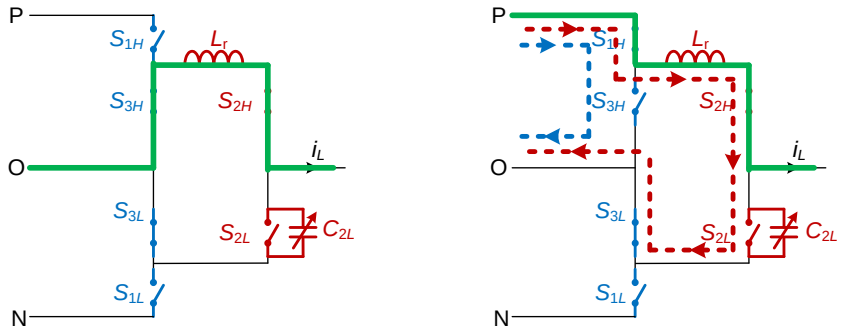
To simplify the analysis, operation of a single phase in Fig. 2 during one line cycle with conventional control is divided into four states as listed in Table I.

Table I. Operation states of single phase with conventional control.

	S_{1H}	S_{3H}	S_{2H}	S_{2L}	S_{3L}	S_{1L}
P	On	Off	On	Off	On	Off
O^+	Off	On	On	Off	On	Off
O^-	Off	On	Off	On	On	Off
N	Off	On	Off	On	Off	On

During the half line cycle with positive output voltage, the operation state change between P and O^+, which means that S_{1H} & S_{3H} operates at high frequency while S_{2H} & S_{3L} keep in on state and S_{2L} & S_{1L} are off. The commutation loop is plotted in Fig. 3. For instance, the power (solid green line) flows out of the phase and is constant during one switching cycle. Originally, the phase operates at O^+ state as shown in Fig. 3(a), and the current goes through S_{3H} and S_{2H}. During the state transition, S_{3H} is turned off first and the current flows through its body diode. Then S_{1H} is turned on to force the current path to change from S_{3H} to S_{1H}. The drain-source voltage of S_{3H} increases from 0 to V_{dc}. Therefore, a commutation loop exists between S_{1H} and S_{3H}, which is shown in dashed blue line in Fig. 3(b) and is similar to a conventional two-level phase leg. This loop has been widely analyzed and can be optimized by minimizing the loop area to reduce the influence of the loop parasitics.

However, there is an additional commutation loop as shown in dashed red line. Since S_{2H} and S_{3L} are in on state, S_{2L} is equivalently paralleled with S_{3H}. As a result, when the high switching frequency switch S_{3H} is commutating with S_{1H}, the drain-source voltage of the line switching frequency switch S_{2L} follows the drain-source voltage of S_{3H} even though S_{2L} is a non-conducting switch during the half line cycle.



(a) (b)

Fig. 3. Switching loop analysis during commutation. (a) O^+ state. (b) P state.

Over-Voltage in Non-Conducting Switch

Fig. 4 illustrates the equivalent circuit of the additional switching loop as well as the voltage response of S_{2L}. Because S_{2L} is always in off state during the half line cycle, it is represented by its output capacitance C_{2L}. The parasitic inductance of the loop is L_r. The drain-source voltage of S_{3H} is simplified to be a ramp pulse from 0 to V_{dc} and serves as the excitation of the loop. In all, the voltage across the non-conducting switch is the ramp response of a LC resonant network. The peak over-voltage of the non-conducting switch is mainly determined by three factors: dv/dt of v_{ds_3H}, inductance of L_r and capacitance of C_{2L}. Theoretically, the maximum peak voltage should be $2V_{dc}$ if L_r and C_{2L} both have constant value. Nevertheless, C_{2L} is the output capacitance of a power semiconductor device and has nonlinear value that

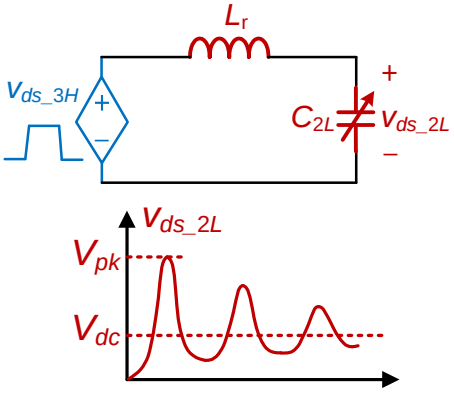


Fig. 4. Equivalent circuit and voltage response of additional switching loop.

changes with voltage. Dependent on different semiconductor material, the capacitance at low voltage can be 10-500 times higher than that at high voltage. From the perspective of energy, the voltage is inversely proportional to square root of capacitance. As a result, the peak voltage of the non-conducting switch can be much higher than $2V_{dc}$.

To reduce the impact of the intrinsic nonlinearity of the power semiconductor device, extra capacitors can be paralleled with the non-conducting switch. Unfortunately, it can significantly increase the C_{oss} loss as v_{ds_2L} is following v_{ds_3H} and C_{2L} is continuously charging and discharging. The other solutions to reduce the over-voltage with conventional control are reducing the dv/dt of v_{ds_3H}, reducing the loop inductance L_r and adding snubbers. Reducing the dv/dt of v_{ds_3H} means slowing down the switching speed of S_{1H} & S_{3H}, which increases the switching loss of the converter. Also, it is observed from Fig. 3(b) that within the additional switching loop, there are four switches included. Thus, this is a large loop with long loop length and it is hard to optimize L_r especially for discrete power semiconductor devices with bulky packaging. In terms adding snubbers, it not only increases the loss but also makes the circuit more complicated and reduces the reliability. Consequently, there is little room to reduce the over-voltage of the non-conducting switch with conventional control.

PROPOSED CONTROL STRATEGY

From the above analysis, the nonlinearity of the output capacitance of the power semiconductor device is one fundamental source of the high over-voltage. Note that for a typical power device, the output capacitance can be approximately divided into two regions. From 0 to around 1/10 of the rated voltage, the capacitance decreases rapidly, and this is the main nonlinear region. After that, the capacitance does not change much. Therefore, if the initial drain-source voltage of the non-conducting switch can be higher than the nonlinear region, the influence of the nonlinear capacitance can be avoided, and the over-voltage can be decreased.

To achieve such result, a simple control is proposed. Compared to the conventional control, the only change is to keep S_{3H} & S_{3L} off when they are not switching. Fig. 5 shows the circuit with the change of switch state highlighted.

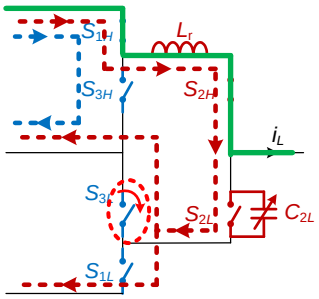


Fig. 5. Switching loop with proposed control.

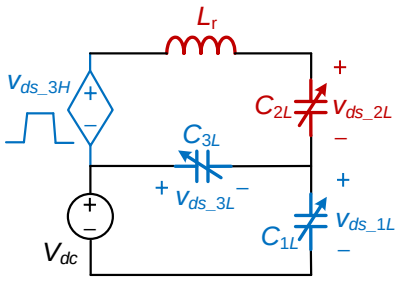


Fig. 6. Equivalent circuit of additional switching loop with proposed control.

With the proposed control, S_{2L} is no longer directly paralleled with S_{3H}. As both S_{1L} and S_{3L} are off during the commutation between O^+ and P states, they can be represented by the output capacitance and the equivalent circuit is shown in Fig. 6. This is a network including three nonlinear capacitance and one inductance. In steady state, L_r is neglected and the equivalent circuits in O^+ and P states are depicted in Fig. 7. From Fig. 7(a), C_{2L} is paralleled with C_{3L} and V_{dc} is distributed among the capacitance. Hence, there is initial voltage across C_{2L} before the turn-off of S_{3H}, which is helpful for avoiding the nonlinear region and reducing the over-voltage. Assuming that all the switches have the same parameters, the drain-source voltage of S_{2L} during O^+ is derived as

$$2V_{ds_2L_O+} \cdot C(V_{ds_2L_O+}) = (V_{dc} - V_{ds_2L_O+}) \cdot C(V_{dc} - V_{ds_2L_O+}) \tag{1}$$

where $C(v)$ is the voltage dependent capacitance value. From Fig. 7(b), the three capacitances share the voltage of two sources. The drain-source voltage of S_{2L} during P is

$$V_{ds_2L_P} \cdot C(V_{ds_2L_P}) = (2V_{dc} - V_{ds_2L_P}) \cdot C(2V_{dc} - V_{ds_2L_P}) - (V_{ds_2L_P} - V_{dc}) \cdot C(V_{ds_2L_P} - V_{dc}) + K_{O+} \tag{2}$$

where K_{O+} is a constant that is related to $V_{ds_2L_O+}$, which means that the voltage of current state is influenced by the voltage of last state.

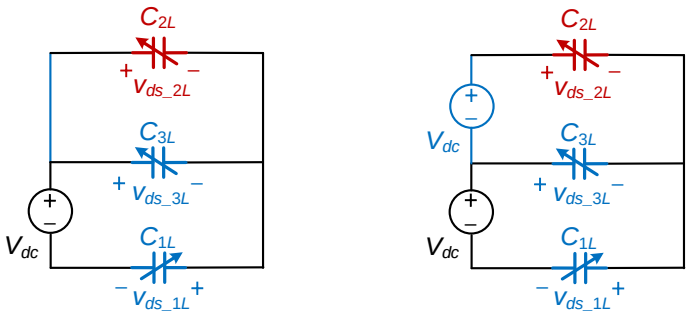


Fig. 7. Equivalent circuits with proposed control in steady state. (a) O^+ state. (b) P state.

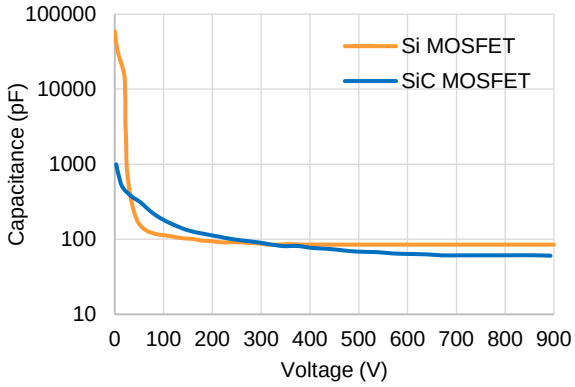


Fig. 8. Output capacitance of Si and SiC MOSFET.

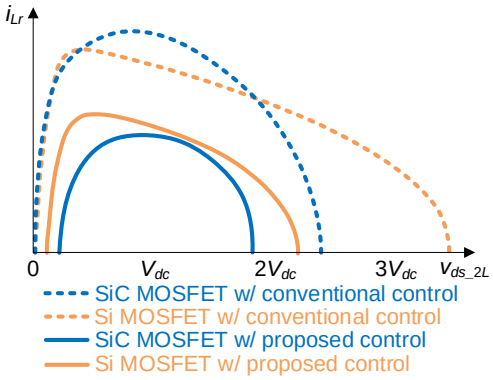


Fig. 9. State trajectory during transition from O^+ to P state with different devices and control.

Since the capacitance is nonlinear, (1) and (2) are difficult to solve and get the numerical result. Thus, the simulation based on the capacitance curve from datasheet is preferred. Fig. 8 plots the capacitance of one Si MOSFET and one SiC MOSFET with similar voltage and current rating. The nonlinearity of Si MOSFET is much higher than that of SiC MOSFET. Fig. 9 depicts the trajectory of the resonance between L_r and C_{2L}. With conventional control shown in dashed lines, the trace is not a circle due to the nonlinearity of the capacitance. The peak over-voltage is more than $2V_{dc}$ and the Si MOSFET has higher over-voltage because of the higher nonlinearity. With the proposed control and the initial voltage built at the beginning, the trace is more like a circle especially for the SiC MOSFET. The peak over-voltage is significantly reduced and is less than $2V_{dc}$ for the SiC MOSFET.

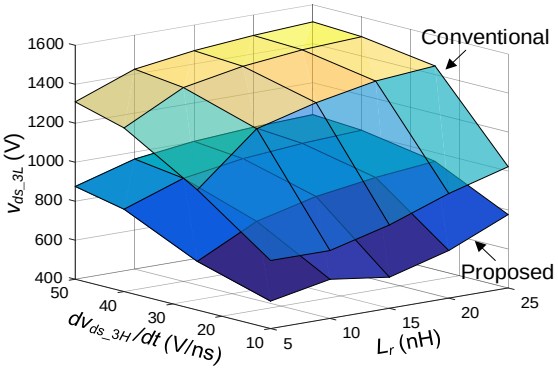


Fig. 10. Peak over-voltage comparison with different *dv*/*dt* and loop inductance.

Fig. 10 shows a comparison of the peak over-voltage with different *dv*/*dt* of S_{3H} and loop inductance between conventional and proposed control. Here a 900 V, 35 A SiC MOSFET is selected to analyze. In general, the peak over-voltage decreases greatly with proposed control. Therefore, higher *dv*/*dt* can be adopted for the high switching frequency switches with the same layout design, which can help reduce switching loss.

Testing Results

The SiC MOSFET C3M0065090J (900 V, 35 A) from Wolfspeed is selected to test the over-voltage and the proposed control. The test is based on a real 3L-ANPC converter that is shown in Fig. 11. Zoom-in picture of single phase and the loops analyzed above is highlighted in Fig. 12. The additional switching loop area (red curve) is much larger than that of the small loop (blue curve). According to the parasitic simulation of the PCB layout, the estimated loop inductance L_r is 35 nH. The DC bus voltage is 500 V, and the peak load current is 30 A.

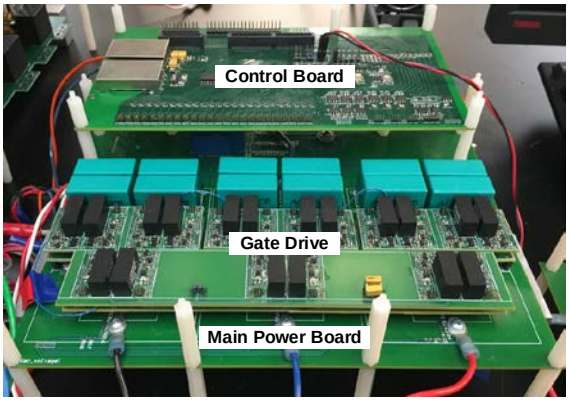


Fig. 11. Prototype of 3L-ANPC converter.

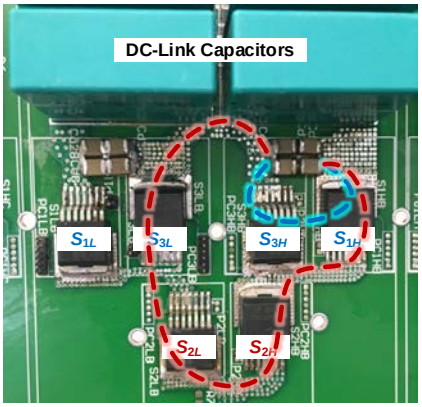
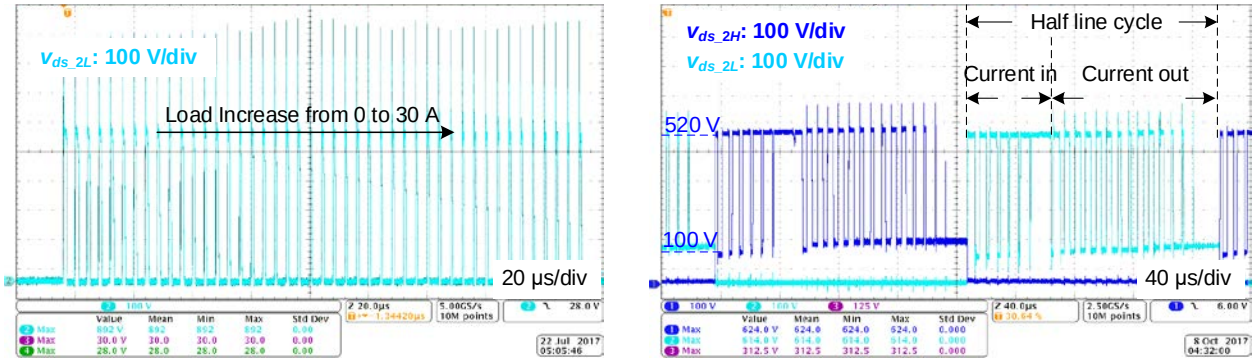


Fig. 12. Single phase and switching loops.

Fig. 13(a) illustrates the tested waveforms of the non-conducting switch with conventional control when the load current increases from 0 to 30 A with multiple pulses at 450 V bus voltage. The peak over-voltage of S_{2L} is 892 V, which is very close to the breakdown voltage of the device. In order to operate at full bus voltage, the switching speed of the MOSFETs has to be decreased to avoid damaging the non-conducting switches. Fig. 13(b) plots the waveforms with proposed control. The load current changes the direction at the middle of half line cycle. Because of the transition, the excitation (S_{3H} & S_{3L}) turns from active switch to synchronous switch and the *dv*/*dt* of the excitation changes. Therefore, the over-voltage before and after the transition of current direction is different. With the proposed control, the peak over-voltage is 624 V at full bus voltage, which shows significant improvement compared to conventional control. Meanwhile, it is also observed that the drain-source voltage during O^+ state is 100 V while that during P state is 520 V, which can match with the aforementioned analysis.



(a) (b)

Fig. 13. Waveforms of non-conducting switches. (a) with conventional control. (b) with proposed control.

CONCLUSIONS

This paper analyzes the multiple switching loops in 3L-ANPC converters and determines the causes for the over-voltage of non-conducting switches. The nonlinearity of the output capacitance of the power semiconductor devices plays an important role in introducing the over-voltage. To overcome such over-voltage, protect the device from damage and increase the switching speed, a simple control is proposed based on the conventional modulation scheme. It does not require any extra circuits or complicated control strategy, and the influence of the non-linearity of the output capacitance can be significantly reduced. With a single phase of a 3L-ANPC converter built with SiC MOSFETs, the multiple pulse test is conducted to compare the over-voltage of the non-conducting switches with conventional and proposed control. The testing result shows that the peak over-voltage is decreased from 892 V to 624 V with the proposed control when the bus voltage is 500 V. More detailed analysis and experimental results will be provided in the final paper.

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