Modeling of Multi-Loops Related Device Turn-On Overvoltage in 3L-ANPC Converters

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***Abstract*— The analytical model for the device drain-source turn-on overvoltage in three-level active neutral point clamped (3L-ANPC) converters is established in this paper. Considering the two commutation loops in the converter, the relationship between the overvoltage and the loop inductances is evaluated. The line switching frequency device usually exhibits higher overvoltage, while the high switching frequency device is not strongly influenced by the multiple loops. A 500 kVA 3L-ANPC converter using SiC MOSFETs is tested, and the model is verified with the experimental results.**

I. INTRODUCTION

Three-level active neutral point clamped (3L-ANPC) converter is a popular candidate for medium voltage and high power applications [1]. The topology of a 3L-ANPC converter is plotted in Fig. 1. The adoption of silicon carbide (SiC) MOSFETs makes it possible to run the converter at higher switching frequencies [2]. However, the higher di/dt and dv/dt during the switching transient also introduces worse voltage spikes because of the parasitics. These resonances and spikes not only deteriorate EMC, but also can cause device failure when they exceed the device ratings [3]. It is shown that for SiC MOSFETs operating at high switching speed, the drain-source overvoltage during turn-on is usually higher than turn-off [4]. This issue becomes even more severe and complicated in multi-level topologies since they have multiple commutation loops.

Extensive work has been conducted to analyze, model, and minimize power electronics device overvoltage during switching [3, 5-7]. However, they are mainly based on two level (2L) configuration and do not consider the multi-loop impact. Several studies have focused on switching loops in 3L-ANPC converters [8-11]. However, none of them provides an analytical model that can build the relationship between the overvoltage and the parasitics in the 3L-ANPC converter.

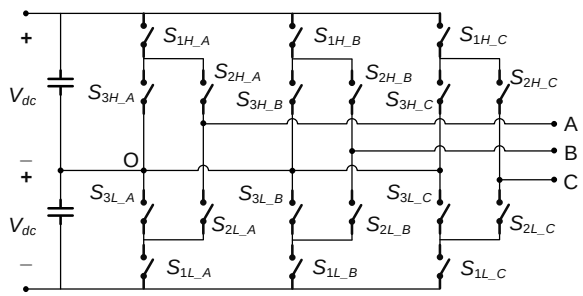

Fig. 1. Topology of 3L-ANPC converter.

This paper establishes the analytical turn-on overvoltage model for 3L-ANPC converters with a commonly used modulation, which considers the effect of multi-loops and non-linear device output capacitance.

II. MODULATION SCHEME AND LOOP ANALYSIS

For the analyzed modulation shown in Fig. 2, during half line period, the outer switch (S_{1L}) and the clamping switch (S_{3L}) operate complementarily at high switching frequency. The inner switches (S_{2H} and S_{2L}) also operate complementarily but at line switching frequency. As a result, the high switching speed commutation occurs between the outer and clamping switches (S_{3L} and S_{1L}). With the non-active clamping switch (S_{3H}) on, stable potential can be provided for the non-active outer and inner switches. However, as has been pointed out in [9-11], there is a multi-commutation loops issue in 3L-ANPC converters.

The equivalent circuit of a phase leg in the 3L-ANPC converter is illustrated in Fig. 3. Different busbar parts and parasitic inductances are highlighted. Since S_{2L} and S_{3H} are

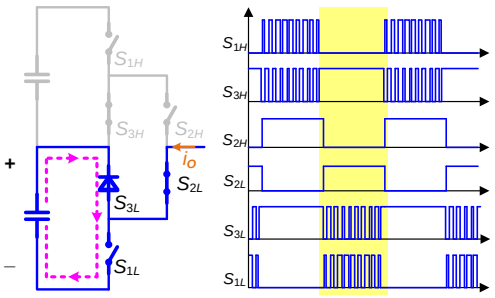

Fig. 4. Modulation scheme for 3L-ANPC converter phase leg.

on, S_{2H} is equivalently paralleled with S_{3L}. Note that S_{2H} is a non-active switch during the negative half line cycle. When the active switch S_{3L} commutates with S_{1L}, the drain-source voltage of S_{2H} follows that of S_{3L}. The parasitic inductance resonates with the output capacitance of S_{2H}. Therefore, both the short (pink) and long (green) commutation loops exist, and there is coupled influence between S_{3L} and S_{2H}.

Assume each busbar part is independent and is not coupled with other busbar parts, and each switch has the same stray inductance. The two loops share the neutral busbar, positive/negative busbar, the switch S_{1L} and the DC-link capacitor. The short loop contains the switch S_{3L} while the longer loop includes two pieces of middle busbar as well as the switches S_{3H}, S_{2H} and S_{2L}. When the load current flows into the phase leg and S_{1L} is the active switch, the equivalent circuit of the phase leg can be drawn in Fig. 4. L_1 is the shared loop inductance by two loops and equals to the sum of capacitor ESL L_C, neutral busbar inductance L_o, negative busbar inductance L_n, and one switch stray inductance L_s. L_2 is the sum of two middle busbar inductance $2L_m$ and three switch stray inductance $3L_s$. L_3 equals to one switch stray inductance L_s. The short loop inductance L_{st} is L_1+L_3 while the long loop inductance L_{lg} is L_1+L_2. R_1, R_2 and R_3 are the loop parasitic resistances. C_{3L} and C_{2H} are the output capacitances of S_{3L} and S_{2H}. i_3 and i_2 are the currents through S_{3L} and S_{2H}. S_{1L} is represented as a controlled voltage source.

Table I. Operation states of single phase 3L-ANPC converter with conventional control.

State	S_{1H}	S_{3H}	S_{2H}	S_{2L}	S_{3L}	S_{1L}
P	On	Off	On	Off	On	Off
O^+	Off	On	On	Off	On	Off
O^-	Off	On	Off	On	On	Off
N	Off	On	Off	On	Off	On

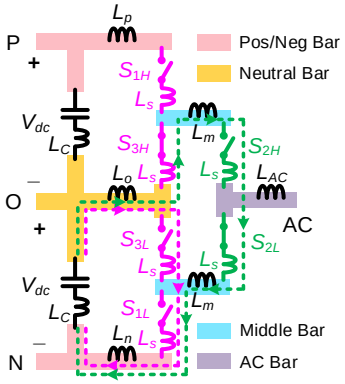

Fig. 2. 3L-ANPC converter single phase considering parasitics.

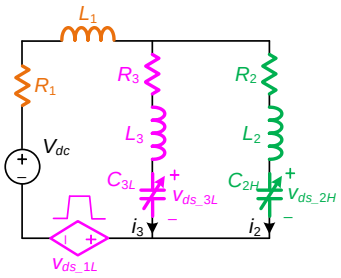

Fig. 3. Equivalent circuit of single phase leg during half line cycle.

III. Overvoltage Modeling and Analysis

The output capacitance of power semiconductor devices is non-linear and is dependent on the drain-source voltage. Based on different semiconductor material and device structure, the output capacitance at low voltage can be 10-500 times higher than that at high voltage. Because of this voltage dependency, it is difficult to directly derive the voltage response. Here, the state space analysis is implemented to build the analytical voltage response model in time domain. By applying the state space, the circuit model can be written in the format of:

$$\dot{X}(t) = AX(t) + BU(t) \qquad (1)$$

X=[i_3 i_2 v_{ds_3L} v_{ds_2H}]^T is the state vector. The analysis begins when the current commutation finishes and v_{ds_1L} starts to drop. At this moment, i_3=i_2=0 and v_{ds_3L}=v_{ds_2H}=0. So the initial state X_0=[0 0 0 0]^T. U=V_{dc}- v_{ds_1L} is the input vector. Here, v_{ds_1L} is assumed to drop linearly during turn-on. A and B are state and input matrix, and they can be derived as (2) and (3).

$$A=\begin{bmatrix} -\frac{(R_1+R_3)L_2+R_3L_1}{KL_2L_3} & -\frac{R_1L_2-R_2L_1}{KL_2L_3} & -\frac{L_1+L_2}{KL_2L_3} & \frac{L_1}{KL_2L_3} \\ -\frac{R_1L_3-R_3L_1}{KL_2L_3} & -\frac{(R_2+R_3)L_3+R_2L_1}{KL_2L_3} & \frac{L_1}{KL_2L_3} & -\frac{L_1+L_3}{KL_2L_3} \\ \frac{1}{C_{3L}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{2H}} & 0 & 0 \end{bmatrix} \quad (2)$$

$$B=\begin{bmatrix} \frac{1}{KL_3} & \frac{1}{KL_2} & 0 & 0 \end{bmatrix}^T$$

where

$$K=1+\frac{L_1}{L_2}+\frac{L_1}{L_3} \quad (3)$$

Based on the analytical model built above, the overvoltage of both high and line switching frequency switches can be evaluated. Fig. 5 illustrates the transient waveforms of 3L and 2L phase leg. The resonant frequencies of the high and line switching frequency devices are different. For high switching frequency device, the resonant frequency is close to that in a typical 2L phase leg, and is higher than the line switching frequency device.

The relationship between the loop inductance and the overvoltage of both the high and line switching frequency devices needs to be evaluated. The overvoltage percentage OV(%) is defined as (V_{ds_pk}-V_{dc})/V_{dc} to simplify the analysis. Based on the model, the relationship among the short loop inductance L_{st}, the ratio between long and short loop inductances L_{lg}/ L_{st}, and OV(%) is shown in Fig. 6. From the plot, the following conclusions can be made.

1) With the same inductance ratio of short and long loops, the increase of inductance value leads to higher overvoltage for both the high and line switching frequency devices.

2) Keeping the same short loop inductance, the larger long loop inductance results in higher overvoltage across the line switching frequency device. However, the overvoltage of the high switching frequency device reaches its peak when L_{lg}/ L_{st} is 3 to 4. Further increasing the long loop inductance does not cause higher overvoltage.

3) Generally speaking, the line frequency device exhibits higher overvoltage compared to the high switching frequency device especially with large L_{st} and inductance ratio. The only exception is when L_{st} is small (lower than 6 nH) and L_{lg}/ L_{st} is between 2.5 to 4. Hence, the overvoltage of the line switching frequency device requires more attention.

Fig. 7 shows the relationship between the overvoltage on the line switching frequency device and the voltage fall time of S_{1L} as well as the long loop inductance L_{lg}. Although the relationship is not purely monotonic, generally larger L_{lg} and lower t_{vf_1L} result in higher overvoltage.

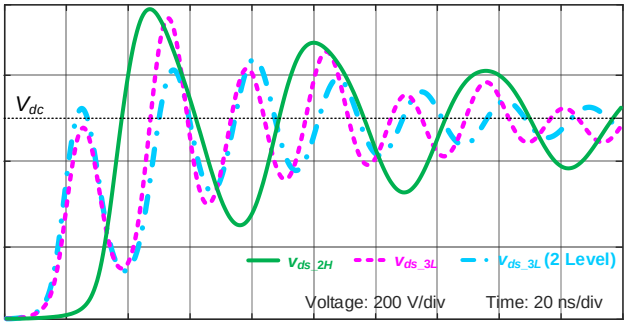

Fig. 5. Voltage transient waveforms with 3L and 2L phase leg based on established model.

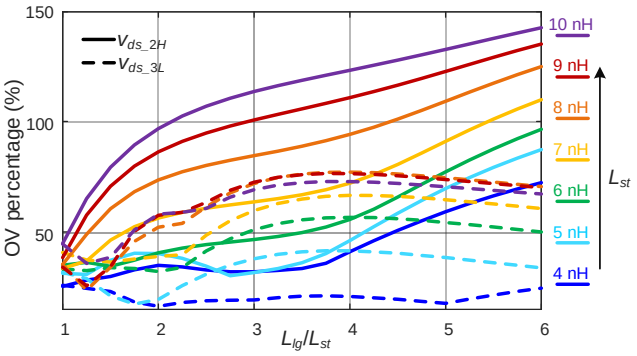

Fig. 6. Relationship among overvoltage, loop inductance ratio and short loop inductance.

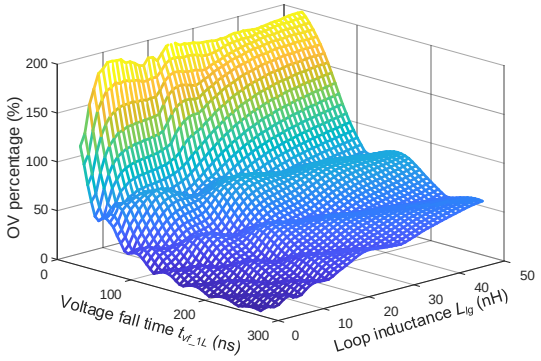

Fig. 7. Over-voltage of line switching frequency device under different L_{lg} and t_{vf_1L}.

IV. Experimental Results and Discussion

A 500 kVA 3L-ANPC converter is built to verify the analytical model. The DC bus input voltage is 1 kV. The switching frequency of the SiC MOSFETs is 60 kHz, and the output line frequency is 3 kHz. The 900 V HT-3000 series SiC MOSFET modules from Wolfspeed are used for all switches. The measured short and long loop inductances are 6.5 nH and 17.5 nH, respectively. The testing platform is

shown in Fig. 8.

The voltage waveform during the switching transient under full voltage and load condition is illustrated in Fig. 9. The applied gate resistance is 2.5 Ω, with which the dv/dt of v_{ds_1L} is 10 V/ns. The peak voltage of S_{3L} is 754 V, while that of S_{2H} is 736 V. The tested waveform is compared with the analytical model result. Generally, they can match with each other. The mismatch is mainly caused by three reasons: 1) the excitation is assumed to have an ideal trapezoidal shape in the model. However, the actual voltage rise and drop is not linear. 2) The coupling between different busbar parts is complicated, and it leads to errors when using a single inductance value to represent the inductance of each part. 3) The estimation of high frequency AC resistance is not accurate when the power modules and capacitors are included. Nevertheless, the analytical model is good enough to show the trend of the overvoltage.

V. Conclusions

An analytical model for the device turn-on overvoltage in 3L-ANPC converters is developed in this paper. Two commutation loops exist during the switching transient in the analyzed modulation, which results in coupling effect between the high and line switching frequency devices. According to the investigation with the established model, the line switching frequency device usually has higher overvoltage than the high switching frequency device. The high switching frequency device is not significantly influenced by the coupling effect of the line switching frequency device. The model is validated by the experiments with a 500 kVA 3L-ANPC converter.

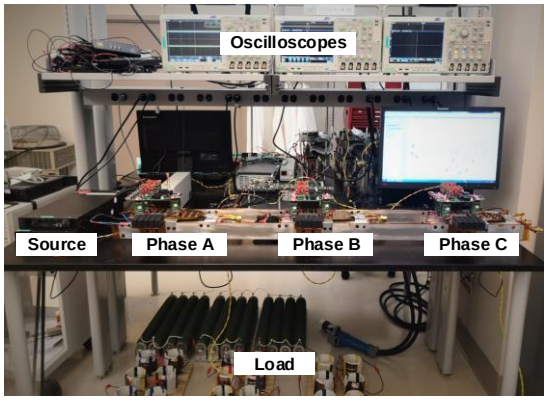

Fig. 8. Testing platform of 3L-ANPC converter.

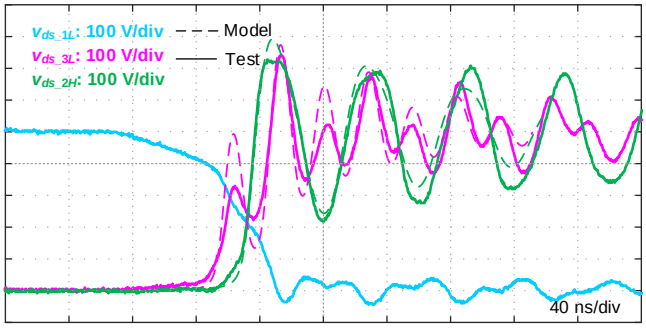

Fig. 9. Comparison of tested switching waveforms and model results.

Acknowledgment

The authors would like to thank The Boeing Company and NASA for their support of this research work. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

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