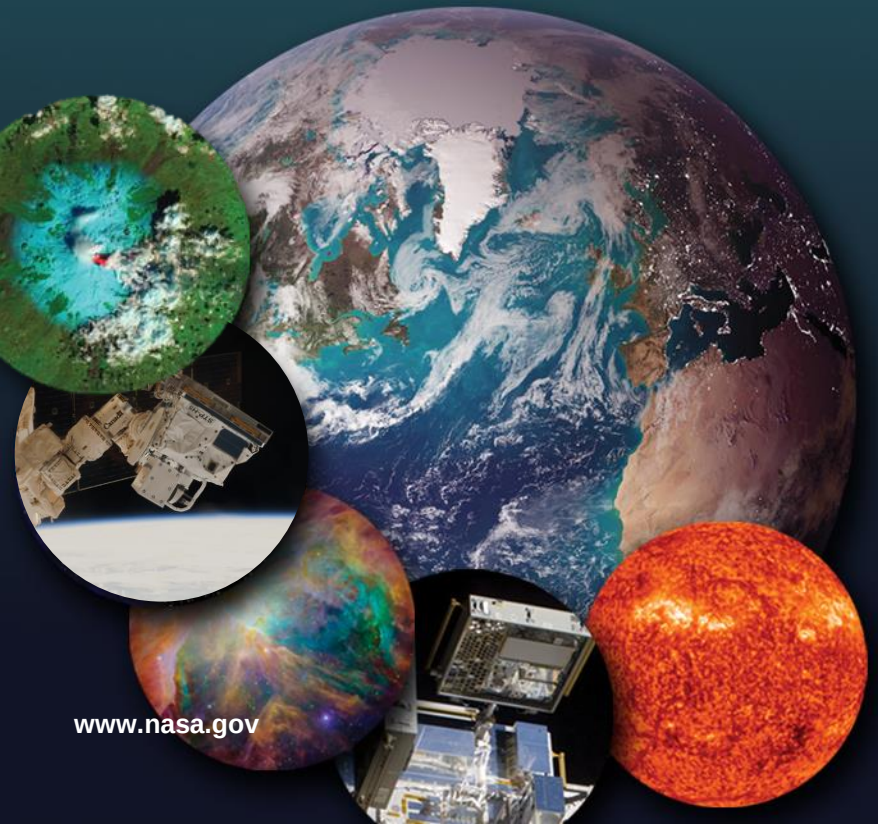
National Aeronautics and Space Administration

SpaceCube v3.0 Mini

NASA Next-Generation Data-Processing System for Advanced CubeSat Applications

SpaceCube



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NASA Electronic Parts and Packaging (NEPP) Program
2019 Electronics Technology Workshop

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www.nasa.gov

Acronyms

Acronym	Definition
BL-TMR	BYU-LANL TMR
cFE	Core Flight Executive
cFS	Core Flight System
CPU	Central Processing Unit
CSP	CHREC/CubeSat Space Processor
DSP	Digital Signal Processor
FF	Flip-Flop
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
ISA	Instruction Set Architecture
LEO	low-Earth Orbit
MGT	Multi-Gigabit Transceiver
PCB	Printed Circuit Board
RE	Recuring Engineering
SBC	Single-Board Computer
SEL	Single-Event Latchup
SEM	Soft Error Mitigation
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy

Outline

1. Introduction

2. SpaceCube Overview
   - SpaceCube Introduction
   - SpaceCube Approach
   - Mini Design Philosophy
   - Lessons Learned

3. SmallSat / CubeSats for Space
   - SmallSat/CubeSat Challenge
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   - Kintex UltraScale
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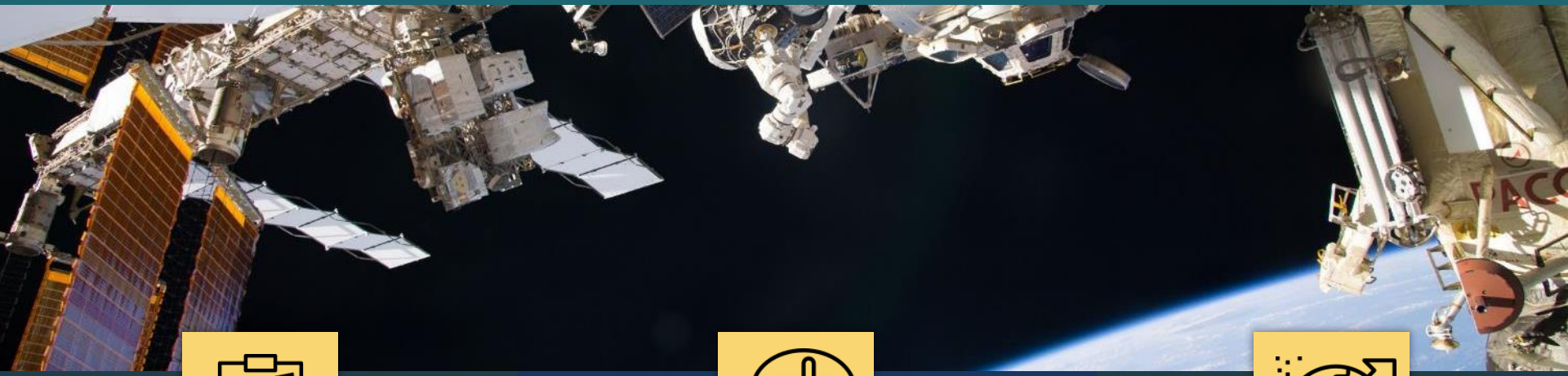
4. SpaceCube v3.0 Mini
   - Configuration Schemes
   - Fault-Tolerant Operation
   - Specification

Goals, Motivations, Challenges



Goals

Develop reliable, high-speed hybrid processor using **SpaceCube design approach** to enable next-generation instrument and CubeSat capability

Motivations

Many commercial CubeSat processor offerings primarily target benign LEO orbits and **do not strongly address** radiation concerns and parts qualification

Need exceptional capability to support complex applications such as artificial intelligence

Challenges

Managing PCB area restrictions for rad-hard components, balancing cost, educating mission designers for key reliability differences

SpaceCube Introduction

What is SpaceCube?

A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs

High performance reconfigurable science / mission data processor based on Xilinx FPGAs

- Hybrid processing …
  CPU, DSP, and FPGA logic
- Integrated "radiation upset mitigation" techniques
- SpaceCube "core software" infrastructure
  (cFE/cFS and "SpaceCube Linux"
  with Xenomai)
- Small "critical function" manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

SpaceCube is Hybrid Processing…

SpaceCube Heritage

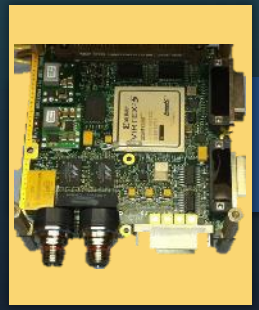
Closing the gap with commercial processors while retaining reliability

- **57+ Xilinx device-years on orbit**
- **26 Xilinx FPGAs in space to date (2019)**
- **11 systems in space to date (2019)**

SpaceCube is Mission Enabling…

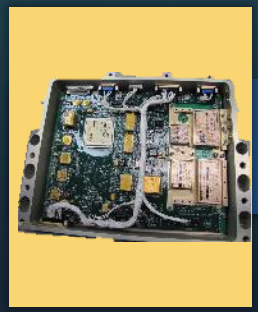
SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6



SpaceCube v1.5

SMART (ORS)



SpaceCube v2.0-EM

STP-H4, STP-H5

SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

SpaceCube Approach

01

The traditional path of developing radiation-hardened flight processor **will not work** …
they are always one or two generations behind

02

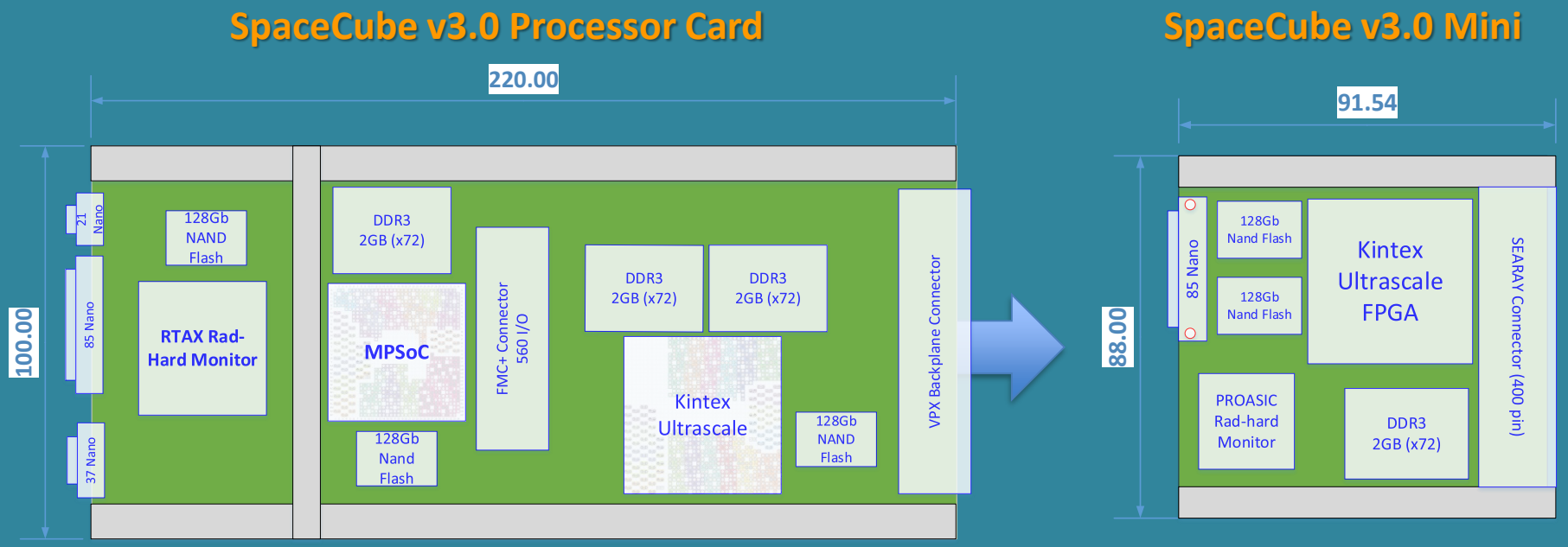
Use latest radiation-tolerant* processing elements to achieve massive **improvement** in "MIPS/watt" (for same size/weight/power)

03

Accept that radiation induced upsets may happen occasionally and just deal with them appropriately …
any level of reliability can be achieved via **smart system design!**

***Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation-induced destructive failures (latch-up)**

Mini Design Philosophy



Same Approach, Smaller Size

SpaceCube design approach applied to smaller form-factor

Key Design Reused

Much of UltraScale design and interface remain same between cards including DDR Pinout

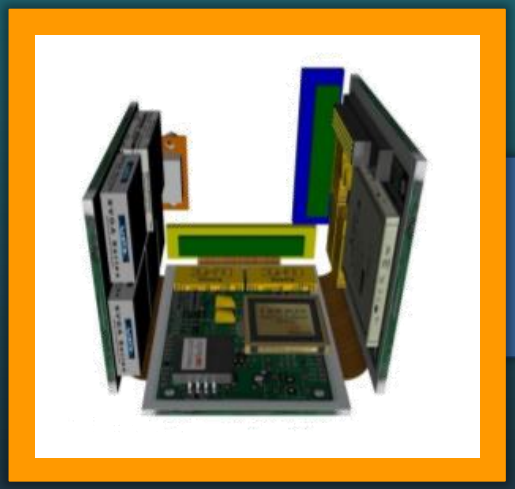
Supervision Requested

Radiation-hardened monitor architecture and code reusable

Trade in, Trade Out

EEE parts trades, analysis, and circuits extensively leveraged from main card design

Mini Form Factor Lessons Learned



SpaceCube Mini v2.0
Lessons Learned

CSPv1
Lessons Learned

Manufacturability
Difficult to manufacture due to rigid-flex and laser-drilled microvias. Tied to single vendor design.

Monitor Design
Aeroflex rad-hard monitor was effective, however, limited by FPGA resources preventing more robust design

CubeSat Connector
Samtec SEARAY connector provided flexibility and performance, same connector used with SpaceVNX (VITA 74.4)

Backplane Advantage
Backplane allows swapping of individual card as advances/ improvements are made and can easily incorporate new components

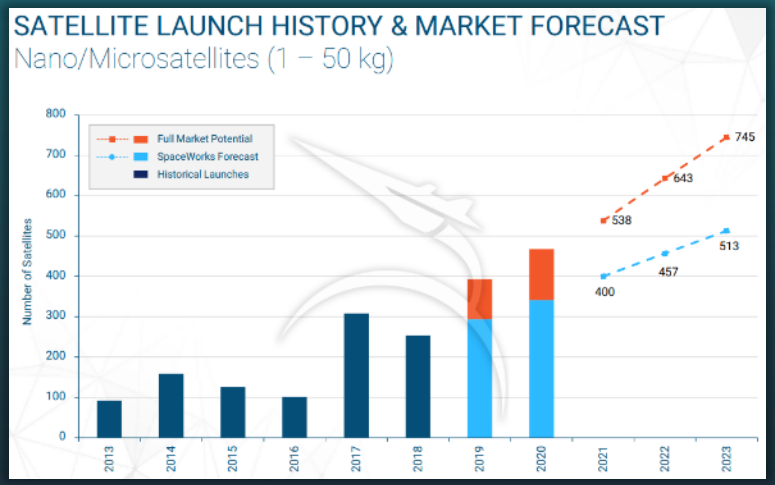
SmallSat/CubeSat Processor Challenge

Massively Expanding Commercial Market for SBCs

- Tons of commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc…)

Mission Developers Seeking Commercial Hardware

- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat "Kit" types of cards



"2019 Nano/Microsatellite Forecast, 9th Edition," SpaceWorks Enterprises, Inc., Jan 2019.

Not Designed With Harsh Orbit Considerations Beyond LEO

- Many vendors have performed limited radiation testing and largely support missions in more benign LEO orbits
- Mission is radiation test approach
- Little-to-no additional radiation testing or parts qualification
- No recommendations for fault-tolerant configurations of offered SBCs

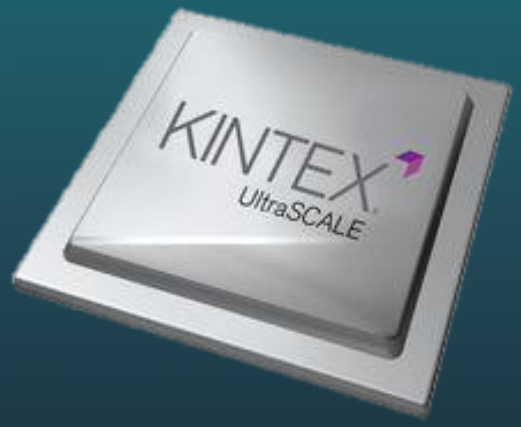
Xilinx Space Devices Compared

	SpaceCube v1.0		SpaceCube v2.0	SpaceCube v3.0	
	XQR4V (RT, 1.2V)		XQR5V (RHBD, 1.0V)	XQRKU060 (RT, 1.01V)	KU060 vs. V5
Resource	FX60	FX140	FX130	KU060	
Logic Cells	56,880	142,128	131,072	726,000	5.54x
CLB FF	50,560	126,336	81,920	663,360	8.10x
Max Distributed RAM (Kb)	395	987	1,580	9,180	5.81x
Total Block RAM (Kb)	4,176	9,936	10,728	38 Mb	3.54x
BRAM/FIFO ECC (36 Kb)	--------	--------	--------	1,080	N/A
DSP Slices	128	192	320	2,760	8.63x
MGT			18 @ 4.25 Gbps	32 @ 12.5 Gbps	5.23x
TID (krad)	300	300	1,000	120	(0.12)
SEL	>125	>125	>125	~80	(0.64)
Flow	V-Flow (QML-V)		B-Flow (QML-Q) V-Flow (QML-V)	B-Flow (QML-Q) Y-Flow (QML-Y Compilant)	N/A
Package	35 x 35 mm	40 x 40 mm	45 x 45 mm	40 x 40 mm	(0.78)

"Xilinx's Adaptive FPGAs for Space Applications" White Paper

Xilinx Kintex UltraScale XQRKU060

- First 20 nm FPGA for Space
  - Designed for SEU mitigation (>40 patents)
  - Deploys same commercial silicon mask set
  - Uses Vivado UltraFast Development



- Ruggedized 1509 CCGA
  - 40 mm x 40mm package
  - Footprint compatible A1517

- Product Space Test Flows
  - B-Flow (QML-Q Equiv.) and Y-Flow (QML-Y Compliant)

Lee, D., Allen, G., Swift, G., Cannon, M., Wirthlin, M., George, J. S., Koga, R., and K. Huey, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," IEEE Radiation Effects Data Workshop, July 13-17, 2015.

- Commercial Radiation Testing Results
  - Improved Xsect compared to 7 series
  - No observed classical SEL signatures

Berg, M., Kim, H., Phan, A., Seidleck, C., Label, K., and M. Campola, "Xilinx Kintex-UltraScale Field Programmable Gate Array Single Event Effects (SEE) Heavy-ion Test Report," NASA Electronic Parts and Packaging, 2017.

Fault-Tolerant Soft-Core Processing

Xilinx TMR MicroBlaze[1]

- Built-in Xilinx TMR solution for newer FPGAs
- Includes TMR SEM IP Core
- Vivado IP integrator for easy project creation

BL-TMR MicroBlaze[2]

- BYU-LANL TMR Tool (BL-TMR) provides automated TMR application
- Fault Injection on MicroBlaze performed for SpaceCube v2.0

BL-TMR RISC-V[3]

- RISC-V is a promising new ISA processor gaining popularity for Intel and Xilinx FPGAs
- Neutron radiation test of Taiga RISC-V
- 27% decrease in operational frequency, for 33x improvement in cross section

Resource Utilization of TMR Designs on KU040

Resource	MicroBlaze Stand Alone	Xilinx TMR MicroBlaze	BL-TMR MicroBlaze	BL-TMR RISC-V[3]
LUTs	3.29%	9.81%	15.58%	0.80 %
CLB FF	1.63%	4.77%	4.89%	0.20 %
BRAM/FIFO ECC (36 Kb)	12.50%	37.50%	37.50%	1.00 %
DSP Slices	0.31%	0.94%	0.94%	0.20 %
FMax	-----	0.95x	0.88x	0.73x

BL-TMR v6.3, MicroBlaze v11, 32-bit 5-stage, FPU, 32 Kb I/D, Vivado 2019.1,

[1]Microblaze Triple Modular Redundancy (TMR) Subsystem v1.0, https://www:xilinx:com/support/documentation/ip documentation/tmr/v1 0/pg268-tmr:pdf, Xilinx, 10 2018.

[2]http://reliability.ee.byu.edu/edif/

[3]A. Wilson and M. Wirthlin, "Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processors on Xilinx SRAM-based FPGAs," 12th Space Computing Conference, July 30 – August 1, 2019.

SCv3.0 Mini Booting Configuration

Selectable Configuration

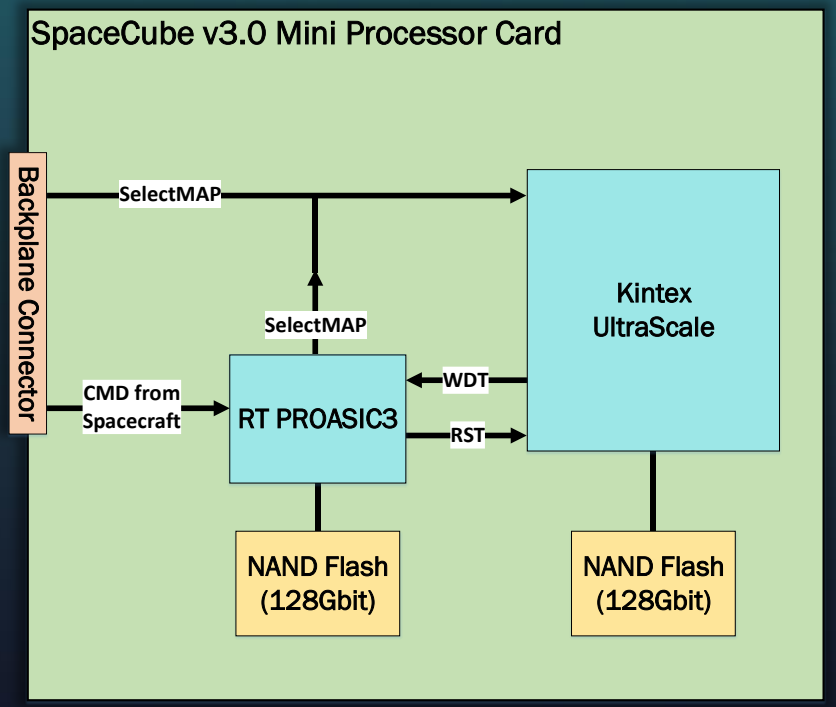
- Kintex configured via SelectMAP from backplane or on-board RTProASIC3 supervisor
- Dozens of configuration files stored with redundant copies across multiple internal dies

Robust RTProASIC Monitor

- Verifies configuration files are valid via page-level CRC checks
- Can reconstruct valid configuration file from several corrupted ones
- Internal FSM ensures Kintex programming and boot sequence is completed correctly
- Automatic program retry

Flexible Configuration

- Can be reconfigured via command from spacecraft to ProASIC
- Can change configurations in-flight to support dynamic mission requirements



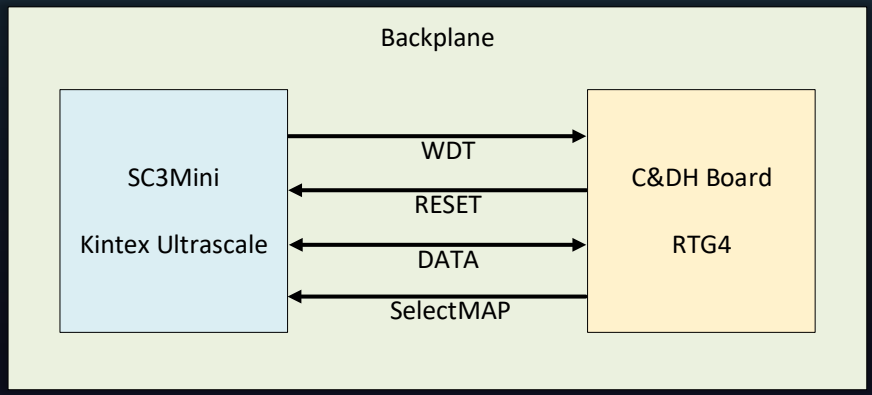
SCv3.0 Mini Fault-Tolerant Architecture

Stand-Alone Operation (RT-ProASIC)

- Scrubs Kintex configuration during operation via either:
  - Blind scrubbing (consistent time interval)
  - Smart scrubbing (readback scrubbing to check configuration and correct errors as they are detected)
- Scrubs configuration files in NAND flash memory

Companion-Card Operation (GSFC CubeSat Bus)

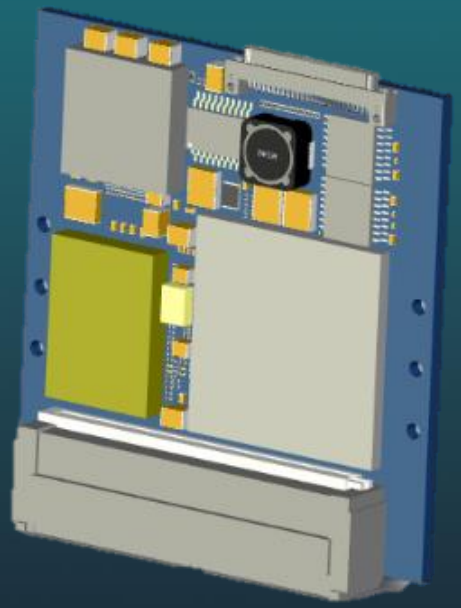
- Combines reliability of RTG4 with high performance of SCv3Mini to form flexible, reusable SmallSat/CubeSat bus
- RTG4 configures and monitors Mini over the backplane



SCv3.0 Mini High-Level Specifications

Overview

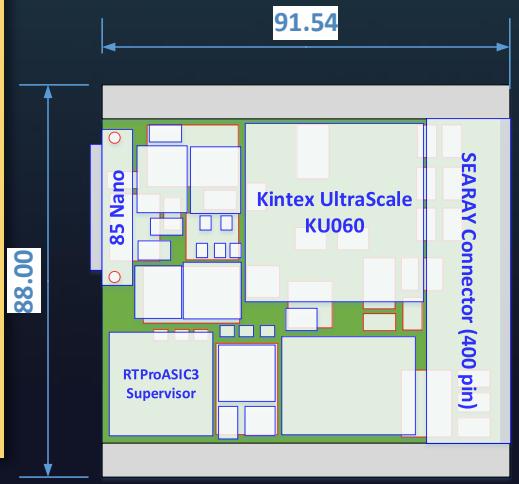
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus Dellingr-X



High-Level Specifications

1x Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 30x 3.3V GPIO
  - 2 RS-422/LVDS
  - SelectMAP Interface
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



Conclusions

SpaceCube is a MISSION ENABLING technology

- Delivers exceptional on-board computing power
- Cross-cutting (Earth/Space/Planetary/Exploration)
- Being reconfigurable equals BIG SAVINGS
- SpaceCube can be used in all mission applications
  … up to and including Class A
- Past research / missions have proven viability
- Ready for infusion into operational missions
- Next-Generation CubeSat design for artificial intelligence and machine learning applications

Thank you! Questions?

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Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)

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