Demonstration of 4H-SiC JFET Digital ICs Across 1000 °C Temperature Range Without Change to Input Voltages

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Abstract. Operational testing of prototype 4H-SiC JFET ICs across an unrivaled ambient temperature span in excess of 1000 °C, from -190 °C to +812 °C, has been demonstrated without any change/adjustment of input signal levels or power supply voltages. This unique ability is expected to simplify infusion of this IC technology into a broader range of beneficial applications.

Introduction

We have previously reported unique experimental demonstrations of 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) with two levels of interconnect that operate with excellent signal stability for over a year in 500 °C room air ambient [1,2] and weeks directly immersed in 460 °C, 9.4 MPa super-critical CO_2 Venus surface atmospheric conditions [3]. More recently, we have demonstrated short-term operation of these ICs at ambient temperature (T) exceeding 800 °C [4]. Despite these unprecedented high temperature demonstrations, the ability of this 4H-SiC IC technology to perform in additional relevant application environments, such as low-temperature or high-radiation, has not been previously reported. The ability of high temperature electronics to also function at very cold temperatures is very relevant to some envisioned applications. As an example, aircraft engines must reliably "cold-start" in arctic conditions (as low as -55 °C) despite the fact that they run hot.

This work reports electrical characterization of packaged 500 °C-durable 4H-SiC JFET ICs at cold ambient temperatures down to -190 °C (83 °K). A combined analysis including both low-T and high-T measurements is then presented. The combined results demonstrate IC operation across an unprecendented 1022 °C operating temperature span without any adjustments to input signal or power supply voltages.

Experimental

The SiC JFET ICs measured in this work were diced from prototype "Wafer 10.1" that has been previously described elsewhere [1,2,4] and commercially packaged in custom ceramic packages [5]. The most complicated IC selected for cold-testing was a 175-JFET "÷2/÷4 Clock" demonstration IC chip. As reported in [1,2], this technology demonstration IC provides a "base" frequency clock signal generator (a 21-stage ring oscillator) with electronically selectable divide by 2 or divide by 4 output signal frequency achieved using two D-type flip flops and control signal logic. Other devices cold-tested included a simple "MF" series NOT gate [6] and an n-type transmission line method (TLM) resistor test structure.

All digital logic functions were measured via digitizing oscilloscope with 10 MΩ passive probes, while DC source-measure units were employed for I-V characterization of the TLM structure. To facilitate more precise measurement of output logic levels (i.e., to mitigate frequency-dependent

waveform loading/distortion), the ÷2/÷4 frequency division IC logic functionality was operated and characterized using a 100 Hz square wave clock signal supplied by an external wave generator that overrode the on-chip ring oscillator clock input to the flip-flop logic [1,2]. By briefly disconnecting the external generator (via relay), the much higher-frequency on-chip clock (i.e., the 21-stage ring oscillator) signal was independently monitored, albeit with significant signal loading attenuation/distortion effects, using a dedicated AC-coupled oscilloscope channel. For all IC measurements at all temperatures, power supply voltages of V_{DD} = +25 V and V_{SS} = -25 V were maintained along with input logic signal levels of V_{IH} = 0 V representing logic 1/high and V_{IL} = -10 V representing logic 0/low.

The cold-testing was carried in a temperature-controlled refrigerated environmental chamber using ~ 2 m long wiring running between test articles inside the cold-chamber and instruments residing outside. The chamber was ramped down from room temperature to -190 °C (its low-temperature limit) and then re-heated to +100 °C (its high-temperature limit) before cooling back to room temperature. The rate of temperature ramp was confined to 3 °C/minute or less. Hot-testing of above 100 °C was carried out in ovens using separate chips from the same wafer. For purposes of succinct presentation of broader temperature behavior trends, the measured lower-temperature data original to this work (on chips denoted as #2 and #4) is presented in combination with previously measured high-temperature data from other Version 10.1 chips (denoted as #1 and #3) of identical design/layout. Chip #1 11-stage ring oscillator data was previously published in [4]. Since some relevant device properties have significant dependence upon radial device distance r from the wafer center as described in [7], the chip radial distances from the wafer center were as follows: $r_{\#1}$ = 21 mm, $r_{\#2}$ = 16 mm, $r_{\#3}$ = 15 mm, $r_{\#4}$ = 16 mm.

Results

Figure 1 compares 100 Hz operational test waveforms measured from the "MF" design NOT gates [6,7] at selected benchmark ambient temperatures. These waveforms demonstrated correct logic functionality with minimal changes despite the 1022 °C difference between minimum and maximum ambient temperature. Figure 2 compares NOT gate output high (V_{OH}) and output low (V_{OL}) voltage levels extracted from measured waveforms recorded at all ambient temperatures studied. Across the entire testing temperature range, the logic swing exceeds 8 V, and logic output voltages V_{OH} and V_{OL} at T = +810 °C and T = -190 °C differ by less than 2.1 V. The arrow annotations denote the direction of temperature ramp during data collection, but the chip #1 NOT gate experienced destructive failure

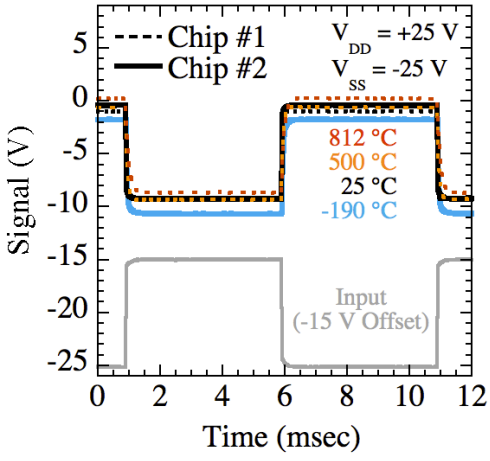

Fig. 1. 4H-SiC JFET IC NOT gate measured waveforms demonstrating functionality across more than 1000 °C temperature span with no changes to input voltages.

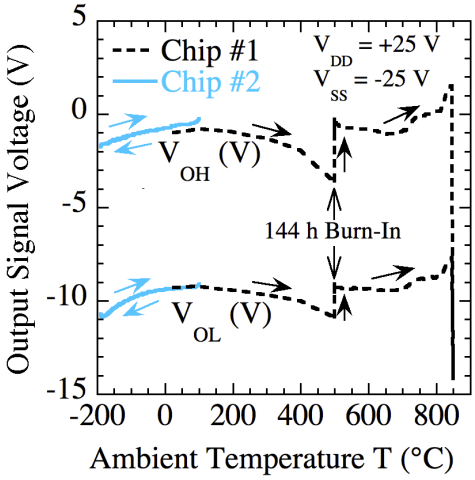

Fig. 2. 4H-SiC JFET IC NOT gate V_{OL} and V_{OH} vs. T measured in the cold-test chamber (solid, blue) and the hot-test oven (dashed, black). A 144 hour burn-in was conducted at 500 °C prior to T > 500 °C testing [4].

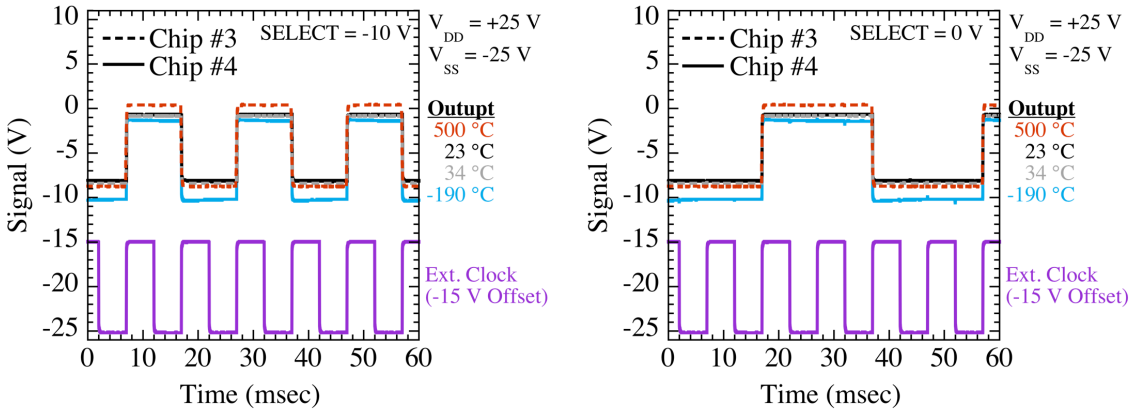

Fig. 3. Operational test waveforms from two packaged ÷2/÷4 clock ICs at selected temperatures driven by 100 Hz external clock input signal with SELECT input line set to -10 V (÷2 mode, left) or 0 V (÷4 mode, right).

during T ramp-up above 810 °C [4]. For the chip #2 cold-chamber test, there is negligible hysteresis of output voltage levels between ramp-up and ramp-down. The step discontinuity in high-temperature data for chip #1 arises from the 144-hour 500 °C burn-in conducted on that chip, an effect consistently noted in prior reported measurements of this IC technology [4,6,7].

Measured output waveforms from the clock IC driven by 100 Hz external clock input signal in ÷2 mode (i.e., with SELECT = -10 V) and ÷4 mode (i.e., with SELECT = 0 V) are shown in Fig. 3 for selected benchmark ambient temperatures. The results verify the ability of the substantially more complicated flip-flop frequency division logic to function at cold temperatures down to -190 °C. Likewise, the 21-stage ring oscillator on this chip (#4) also functioned across the entire -190 °C to +100 °C cold-chamber test range without any adjustment to power supply voltage. The temperature dependence of the 21-stage ring oscillator frequency is shown as one of the plots in Fig. 4.

The multi-device data set plotted in Fig. 4 illustrates the temperature dependence of measured ring oscillator frequency f_{OSC}, a metric of digital logic circuit speed (gate propagation delay), and its strong correlation with sheet conductivity G_{NSheet} (measured via TLM) of the n-type 4H-SiC channel incorporated in logic circuit resistors and transistors. For clearer direct comparison of the temperature dependence, the Fig. 4 plotted parameters are each normalized against their respective measured values at +100 °C. Strong and nearly identical temperature dependence is confirmed between f_{OSC} and G_{NSheet} across the multiple devices studied consistent with earlier JFET IC technology studies [4, 8]. Such behavior arises from the fact that logic gate propagation delays arise largely from charging and discharging of parasitic device capacitances associated with the device structure. While such capacitance effectively does not change with temperature, the rate of charging/discharging is

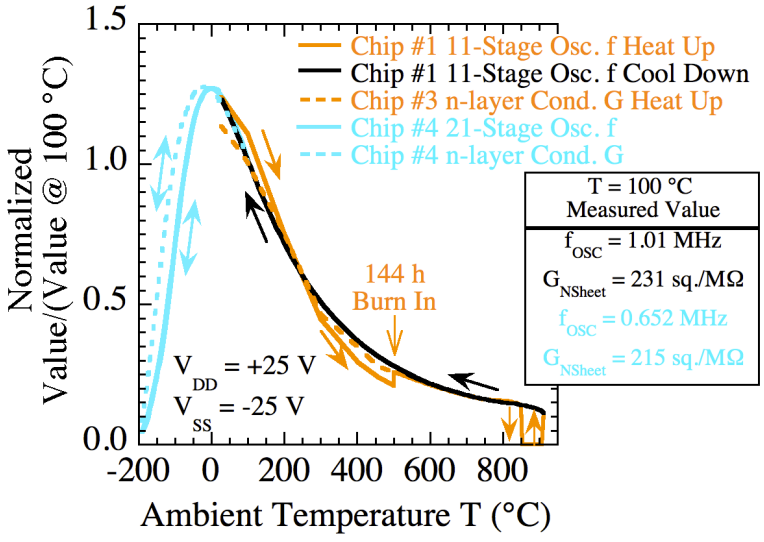

Fig. 4. Normalized plots of measured 4H-SiC JFET IC ring oscillator frequency (f_{OSC}, solid lines) and n-layer sheet conductance (G_{NSheet}, dashed lines) from the cold-test (blue) and hot-test (black, orange) confirming that these exhibit nearly the same T-dependence. Hot-test f_{OSC} data is from [4].

governed by current flow through the n-layer of the circuit resistors and transistors that exhibits strong temperature dependence.

The Fig. 4 temperature dependence is consistent with understood 4H-SiC n-channel conduction physics [9]. For cold conditions, 4H-SiC n-layer conductivity increases with temperature as dopant electroncs increasingly ionize to supply mobile carriers. After conductivity peaks, further temperature increases lead to thermal scattering that decreases electron mobility causing in decrease in n-layer conductivity. Further study is needed to ascertain the effect, if any, of IC self-heating on these measurements. The arrow annotations in Fig. 4 indicate whether data was taken during temperature ramp up or ramp down, but little dependence on temperature sweep direction is noted beyond the step at 500°C resulting from the 144 hour burn-in of the chip #1 ring oscillator. The continuity of 25 °C to 100 °C data from different tests/chips plotted in Figs. 2 and 4 indicates that similar behavior should be obtained if future work measures a single chip test over the entire -190 °C to +812 °C T span.

Summary Discussion

It should be noted that these 4H-SiC cold-testing results demonstrate a substantial improvement over similar cold-testing conducted on earlier-prototype 6H-SiC JFET digital ICs that were far less-complex, required adjusted input bias voltages, and failed to function at ambient T below -150 °C [8]. In contrast, the present work has demonstrated the operation of ICs across an extreme and unrivaled 1022 °C ambient temperature span (-190 °C to > +812 °C) without any change/adjustment of input signal levels or power supply voltages. The authors are unaware of prior reports of similar demonstrations of input-bias-independent IC functionality over such a large temperature span. These results are therefore a validation of the IC approach wherein both transistors and resistors are implemented using the same n-type 4H-SiC layer on the wafer [8,10]. This approach inherently offers straightforward and effective temperature compensation without adjustment of any input biases. The unique ability of 4H-SiC JFET ICs to function at both very low and very high temperature extremes without input bias adjustments should simplify technlogy infusion into a broader range of beneficial applications.

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