Pt:Ti Diffusion Barrier, Interconnect, and Simultaneous Ohmic Contacts to n- and p-type 4H-SiC

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Abstract. We report the initial results of using co-sputtered Pt:Ti 80:20 at. % composition ratio metallization as a diffusion barrier against gold (Au) and oxygen (O), as an interconnect layer, as well as forming simultaneous ohmic contacts to n- and p-type 4H-SiC. Having a single conductor with such combined multi-functional attributes would appreciably reduce the fabrication costs, processing time and complexity that are inherent in the production of SiC based devices. Auger Electron Spectroscopy, Focused Ion Beam-assisted Field Emission Scanning Electron Microscopy and Energy Dispersive Spectroscopy analyses revealed absence of Au and O migration to the SiC contact surface and minimal diffusion through the Pt:Ti barrier layer after 15 minutes of exposure at 800 ºC in atmosphere, thus offering potential long term stability of the ohmic contacts. Specific contact resistance values of 7×10^{-5} and 7.4×10^{-4} Ω-cm^2 were obtained on the n- ($N_d=7 \times 10^{18}$ cm^{-3}) and p- ($N_a=2 \times 10^{20}$ cm^{-3}) type 4H-SiC, respectively. The resistivity of 75 μΩ-cm was obtained for the Pt:Ti layer that was sandwiched between two SiO_2 layers and annealed in pure O ambient up to 900 °C, which offers promise as a high temperature interconnect metallization.

Introduction

Semiconductor metallizations are typically divided into four functional categories: ohmic contacts, diffusion barrier, interconnect, and bond pad. Conventionally, the appropriate metallization that posseses one of the above functional attributes is applied in the course of device implementation. For the ohmic contact, low specific contact resistance (SCR) on both the n- and p-type semiconductor are highly desirable in order to minimize junction power losses and excessive heating. Also, lowering the SCR ensures optimal output in semiconductor based sensors. The diffusion barrier metallization must be capable of preventing the migration of gold (Au) and oxygen (O) or other elements that are deleterious to the integrity of the ohmic contacts. With regard to the interconnect, one crucial attribute is to have low resistivity in order to minimize line power loss over long distances. The ohmic contact characteristic of a metal is driven largely by its work function, assuming the absence of Fermi level pinning surface states. The process of sequential formation of ohmic contacts on both semiconductor conductivities results in higher production costs, longer processing time, and fabrication complexity that could reduce yield.

A recently published report by the authors had demonstrated the concept of phase segregation annealing (PSA) of compositional Pt:Ti as a method of simultaneously forming ohmic contacts to n- and p-type surfaces [1]. In this present work, the primary goal was to further investigate the co-sputtered Pt:Ti as a single conductor metallization that posseses the combined attributes of low SCR simultaneous ohmic contacts to n- and p-type 4H-SiC, acts as a diffusion barrier against Au and O, and low resistivity interconnect to enable reliable device operation at high temperature in excess of 600 °C. This work is motivated by the need to reduce the fabrication process costs, time, and complexity of 4H-SiC sensors and electronics. The diffusion barrier characteristics of binary Pt/Ti metallization was previously studied extensively in silicon technology [2]. However, the high temperature diffusion barrier characteristics of compositional Pt:Ti against Au and O migration have not been investigated until now.

Experiment

Nitrogen-doped (n-type, 2 µm thick, N_d=1.7 x 10^{19} cm^{-3}) and aluminum-doped (p-type, 0.5 µm thick, N_a=1 x 10^{20} cm^{-3}) 4H-SiC epitaxial layers were homoepitaxially grown separately by chemical vapor deposition on the Si faces of basal (0001)-plane, 8° off-axis 4H-SiC semi-insulating substrates [3]. Aluminum (2 µm) was sputter deposited on each epilayer and rectangular transfer length method (TLM) patterns were photolithographically defined in the photoresist that was spun on the Al. Wet etching of the Al in H_3PO_4 at 50 °C for 3 minutes was performed, followed by photoresist dissolution, then reactive ion etching of the exposed SiC epilayer sections in a mixture of Argon (25 sccm) and SF_6 (15 sccm) at 400 W and a base pressure of 25 mT, stopping at the semi-insulating substrate. The residual Al mask was dissolved in hot H_3PO_4 and the samples were rinsed in de-ionized (DI) water. A 500 nm thick quartz (SiO_2) was sputter deposited on the samples, followed by standard lithography and reactive ion etching (RIE) to pattern and etch vias in the oxide, thus exposing the SiC contact regions on the TLM structures.

Since the complete details of the ohmic contact metallization processes have been reported in [1], only a brief description is presented here. Co-sputtering of a 300 nm film of Pt:Ti of 80:20 at. % ratio was performed, followed by a capping layer of 20 nm Pt to prevent premature oxidation. A 1 µm Al was sputter deposited for use as the etch mask. Photolithography was applied to define and pattern the ohmic contacts in the Al layer, followed by wet etching in H_3PO_4 at 50 °C for 2 minutes. The photoresist was then dissolved away in acetone, followed by stripping away of the residual Al in H_3PO_4 at 50 °C. Annealing of the samples was performed by rapid thermal process (RTP) in near vacuum at 1100 ºC for 5 seconds to complete the ohmic contact formation on the n- and p-type samples. For the second metallization, which was to serve as the diffusion barrier and interconnect, another layer of 300 nm layer of Pt:Ti of 80:20 at. % ratio was co-sputtered, followed by the Pt (20 nm) and Al (2 µm) depositions, photolithography, and etching processes descibed earlier. Finally, RTP annealing was performed at near vacuum and 800 ºC for 10 seconds. This final process provided second layer metallization traces to connect to the first layer ohmic contact metallization, which allows for the measurement of the interconnect resistivity between two ohmic contacts. A second 500 nm quartz oxide layer was deposited over the samples and the process of contact pholithography and RIE etch described above was repeated to open contact vias in the oxide, thus exposing the second level metallization. For bond pad metallization, a 100 nm layer of Pt:Ti of 80:20 at. % ratio was co-sputtered, followed by 1 µm Au deposition. The bond pad was patterned in the Au and wet etching was performed in 10:9:1 volume ratio of H_2O:HCl:HNO_3 at 40 ºC for about 2 minutes. This was followed by RIE to etch the Pt:Ti, and oxygen plasma cleaning of the photoresist to recover the Au surface. The actual and illustrative structures obtained after above processes are shown in Fig. 1 (a) and (b) for the TLM structure, diffusion barrier/burried interconnect, respectively.

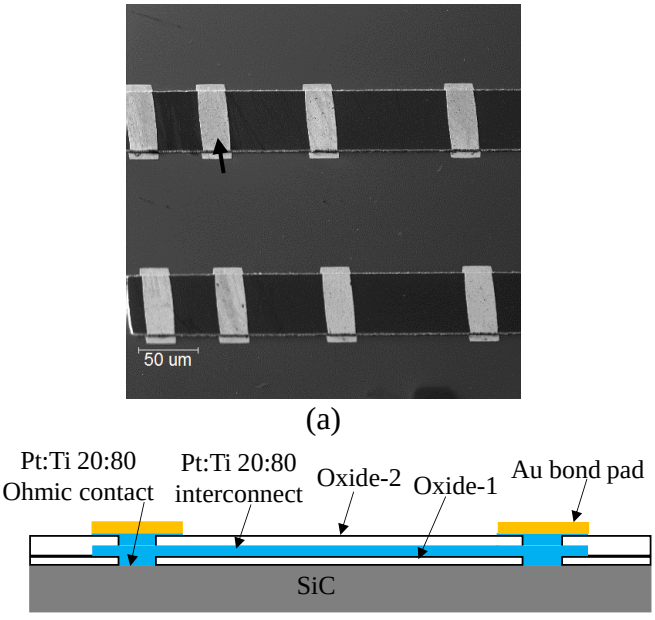
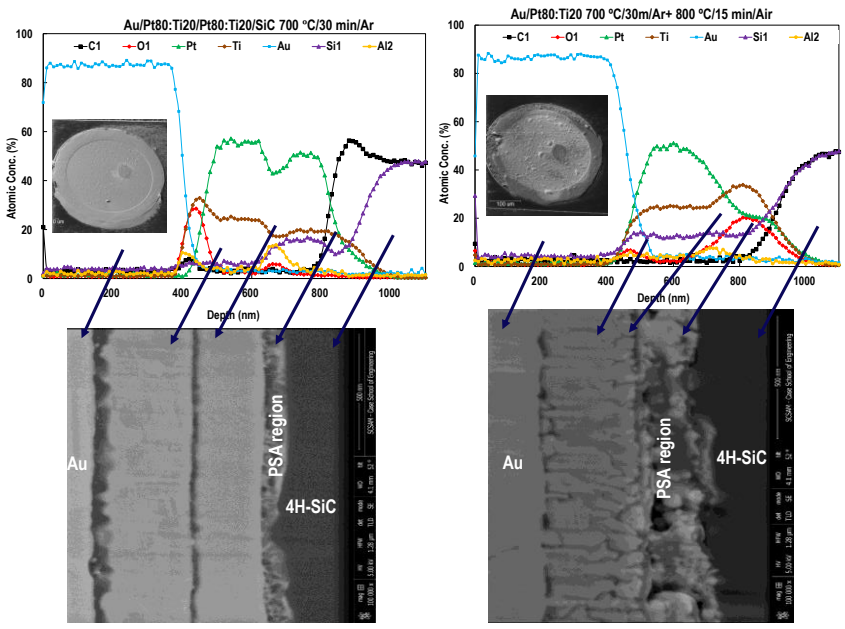


Fig. 1: a) Complete TLM structure with the Au capped Pt:Ti 80:20 at. % ratio ohmic contacts and diffusion barrier layers, and b) schematic cross section of the buried Pt:Ti 80:20 at. % ratio interconnect anchored between two contacts.

Two separate characterizations were performed: measurement of the diffusion of Au and O through the contacts and the measurement of the SCR and the resistivity of the second metallization interconnect (buried between the two SiO_2 layers) after thermal soak. For the Au and O diffusion study, samples were intially furnace annealed in Ar at 700 ºC for 30 minutes, followed by thermal soak in atmospheric oven at 800 ºC for 15 minutes. For the buried interconnect, sub-sets of samples were separately thermally soaked at 700, 800, and 900 ºC in pure O_2 ambient for 60 minutes.

Results and Discussion

After the 30 minutes Ar anneal at 700 ºC and 15 minutes thermal soak at 800 ºC in atmosphere, the SCR from the n- and p-type 4H-SiC TLM structures having doping levels of N_d=7 x 10^{18} cm^{-3} and N_a=2 x 10^{20} cm^{-3} were 7 x 10^{-5} and 7.4 x 10^{-4} Ω-cm^2, respectively. The Auger Electron Spectroscopy (AES) depth profile and corresponding Field Emission Scanning Electron Microscopy (FE-SEM) images of the sample after the 700 ºC anneal in Ar are shown in Fig. 2 (a). The top Au bond pad layer did not show any significant migration into the underlying co-sputtered Pt:Ti layers. The observed O between Au and the Pt:Ti was the result of Ti oxidation after the etching of the top oxide led to the exposure to atmosphere of the underlying Pt:Ti layer. The Al observed at the broad interface between the two Pt:Ti layers was the residual Al contact mask that was used during the etching of the first Pt:Ti layer. At the SiC interface is a mixture of TiC and silicides of Pt and Ti that forms the simultaneous ohmic contacts by PSA on the n- and p- conductivity surfaces [1]. The AES depth profile of the post-800 ºC treatment in air is shown in Fig. 2 (b). A presumed small Au migration (if not AES tailing effect) into the Pt:Ti diffusion barrier, but was effectively contained. The first Pt:Ti (ohmic contact) and the second Pt:Ti (diffusion barrier) layers have merged while the section of the ohmic contact layer on the 4H-SiC surface remaines intact. The residue O had shifted to the SiC interface in the form of a conductive oxide and intermixed with silicides of Pt and Ti. However, the measured SCR values remained unchanged. Compared to Fig. 2 (a), the surface morphology of the Au capping layer remained relatively smooth as seen in the inset SEM images.



(a) (b)

Fig. 2. The AES depth profile and corresponding cross section FIB-FE-SEM image of the co-sputtered Pt80:Ti20 at. % a) after ohmic contact and diffusion barrier formations, Au deposition and Ar anneal; b) after 800 ºC atmospheric exposure for 15 minutes. The Au migration was effectively stopped at the Pt80:Ti20 diffusion barrier layer.

The resistivity of the buried Pt:Ti interconnect after soak at 700, 800, and 900 °C in O ambient for 1 hour was 93.85-, 93.85-, and 75-μΩ-cm, respectively. The AES depth profiles after the thermal soaks at the above three temperatures are shown in Figs. 3 (a)-(c), respectively. The reaction zones are at the Pt:Ti/SiO_2 interfaces, and the prominent reaction was between Ti and SiO_2 to form titanium oxide and its silicide [4]. This reaction resulted in the gradual depletion of titanium within the Pt:Ti layer as the

temperature increased, thereby making the interconnect more Pt rich. This increase in Pt richness after 900 ºC correlates well with the decrease in the resistivity of the buried interconnect. For comparison, the resistivity of Pt and Ti are 10.6 and 42 μΩ-cm, respectively [5]. However, these metals in elemental forms are either too reactive or have poor adhesion to be used for interconnect metallization.

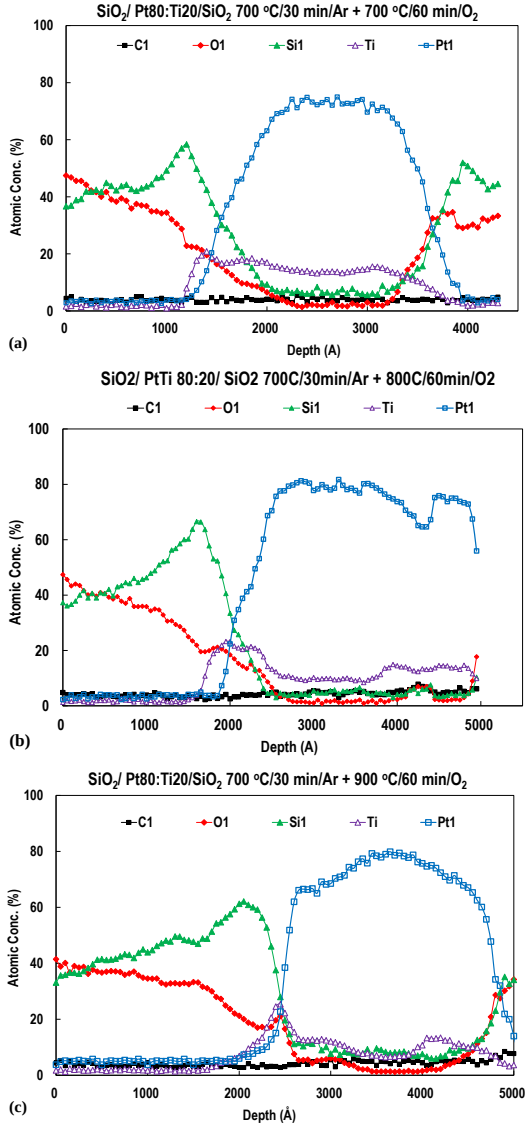


Fig. 3: AES depth profiles of the Pt:Ti 80:20 at. % ratio sandwiched between SiO_2 layers after 1 hour of thermal treatment in 6 slpm O flow at a) 700 ºC, b) 800 ºC, and 900 ºC.

Conclusion

The preliminary results from this work demonstrate the application of a single conductor metallization of co-sputtered Pt:Ti 80:20 at. % ratio having the combined attributes of enabling simultaneous ohmic contacts to n- and p-type 4H-SiC, as a diffusion barrier against Au and O at high temperature, and as a promising interconnect metallization. While the resistivity of the interconnect conductor is single-digit times higher than that of Ti and Pt at room temperature, it has a potential application as a low power loss interconnecting conductor, particularly considering its fabrication process compatibility and robustness for high temperature applications. To our knowledge this is the first reported demonstration of a single-conductor metallization that possesses the above stated combined attributes. The significance of this result is that it would enable the production of SiC sensors and electronic devices faster at lower production and material costs with minimal penalty in performance.

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