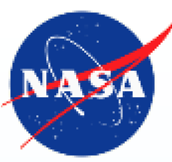


Standardizing Microprocessor and GPU Radiation Test Approaches

Edward J. Wyrwas

edward.j.wyrwas@nasa.gov

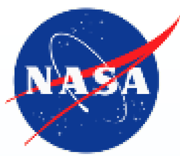
301-286-5213

SSAI, Inc / NASA GSFC NEPP

This work was sponsored by:

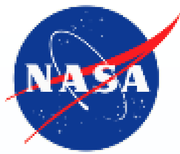
NASA Electronic Parts and Packaging (NEPP) Program

NASA Office of Safety & Mission Assurance



Acronyms

- Body of Knowledge (BOK)
- Complementary metal oxide semiconductor (CMOS)
- Commercial off-the-shelf (COTS)
- Device under test (DUT)
- Electrical, Electronic and Electromechanical (EEE)
- Energy (E)
- Error rate (λ)
- Field programmable gate array (FPGA)
- Fin Field-effect transistor (FinFET)
- Graphics Processing Unit (GPU)
- Joint Electron Device Engineering Council (JEDEC)
- Linear energy transfer (LET)
- Key Process Indicators (KPI)
- Mean time to failure (MTTF)
- Multi-Bit Upset (MBU)
- National Aeronautic and Space Administration (NASA)
- NASA Electronic Parts and Packaging (NEPP)
- Package-in-package (PIP)
- Package-on-package (POP)
- Single-Bit Upset (SBU)
- Single Event Effect (SEE)
- Single Event Functional Interrupt (SEFI)
- Single Event Upset (SEU)
- Single Event Upset Cross-Section (σ_{SEU})
- Single Instruction Multiple Data (SIMD)
- Society of Automotive Engineers (SAE)
- System on Chip (SOC)
- System on Module (SOM)
- Technical Operation Report (TOR)



Outline

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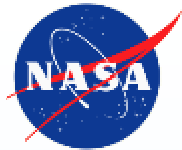
- High Performance Processing Components
- Application Environments and “Key Process Indicators”
- Design of Experiment
- Test Vectors
- Thoughts and Conclusions



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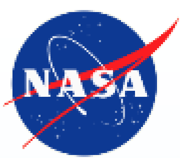
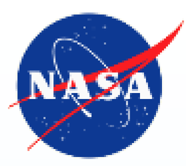


NEPP Mission Statement

Provide NASA's leadership for developing and maintaining guidance for the screening, qualification, test, and reliable use of Electrical, Electronic, and Electromechanical (EEE) parts by NASA, in collaboration with other government agencies and industry.



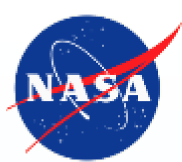
Radiation Assurance Requires Synchronous Integration

This is why radiation engineers tend to answer with "it depends…"

Image credits: NASA and other government sources

- Considerations summarized in these elements allow designers to effectively choose parts for their best performance in a given architecture
- Comprehension requires a complete synchronous picture of how technologies are to be used effectively
- Emphasizing one of these elements without understanding the others can compromise the integrity and performance of the parts and mission success

Adapted from Adapted from NASA Technical Report TM-2018-220074



Design Characterization & Qualification Trade Space

Abstraction → Efficiency (at what cost?)

System

Box

Board

Component

Component

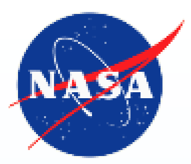
Subpart

Part

Part

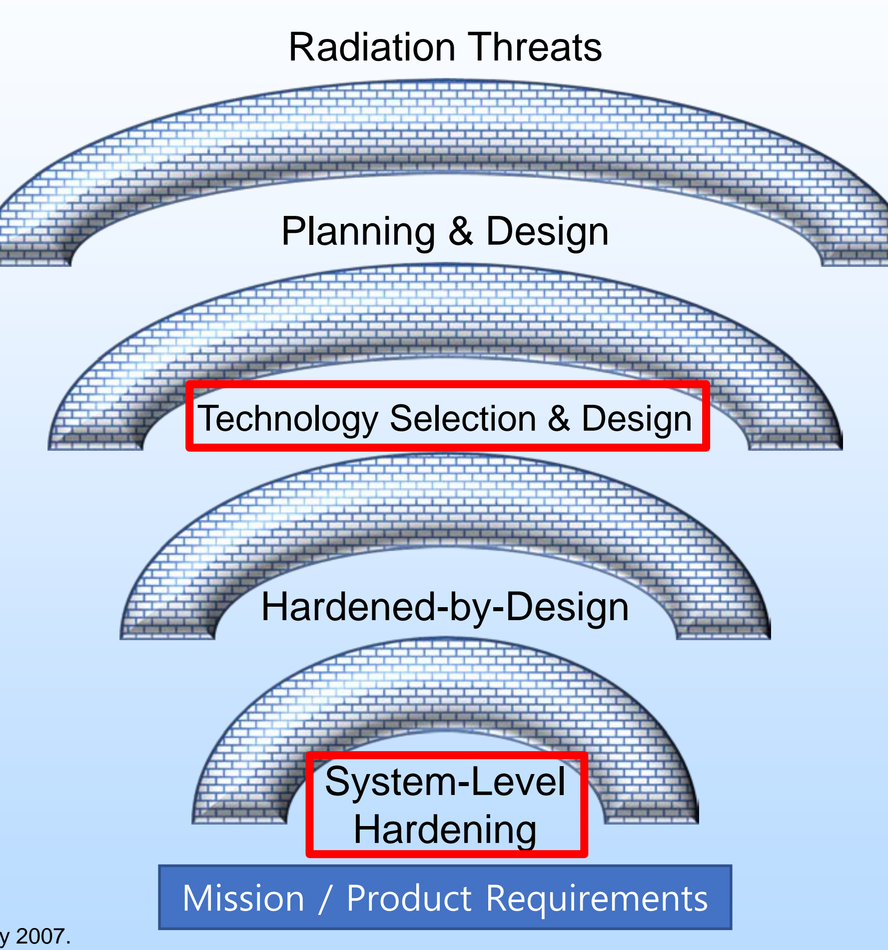
Part

Based on ISO 26262-11:2018(E) Fig. 2

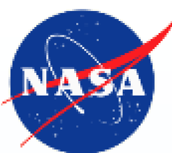


System-Level Assurance
(Space Users Perspective)

- Always faced with conflicting demands between
  - "Just Make It Work," and
  - "Just Make It Cheap"
- Many system-level mitigation strategies pre-date the space age (e.g., communications, fault-tolerant computing, etc.)
- Tiered approach to validation of mission / product requirements



R. Ladbury, *IEEE NSREC Short Course*, July 2007.



NEPP – Processors

State of the Art COTS Processors
- Sub 32nm CMOS, FinFETs, etc
- Samsung, Intel, AMD

"Space" FPGAs
- Microsemi RTG4
- Xilinx MPSOC+
- ESA Brave (future)
- "Trusted" FPGA (future)

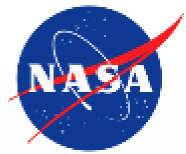
Graphics Processor Units (GPUs)
- Intel, AMD, Nvidia
- Enabling data processing

COTS FPGAs
- Xilinx Kintex+
- Mitigation evaluation
- TBD: Microsemi PolarFire

Radiation Hardened Processor Evaluation
- BAE
- Vorago (microcontrollers)

Best Practices and Guidelines

Partnering
- Processors: Navy Crane, BAE/NRO-
- FPGAs: AF SMC, SNL, LANL, BYU,…
- Microsemi, Xilinx, Synopsis
- Cubic Aerospace



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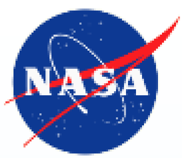
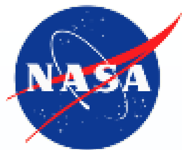


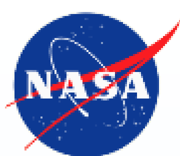
Modern Components

- We can no longer rely on FPGAs being as immune or resilient as their predecessors. They are complex mixed signal systems with compute engines.
- We may still use some legacy parts with well known reliability and radiation tolerances but we also test leading edge computational components
  - Microprocessors (e.g., x86, x64, ARM, Power Arch.)
  - GPUs (e.g., nVidia, AMD, Qualcomm)
  - Memories (e.g., 3D Xpoint, PCM, DDR3, DDR4, Flash)



Technology

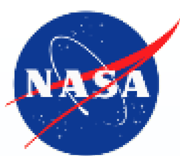
- Computational device families are converging
- Using high-level languages, applications are accelerated by running the sequential part of their workload on the CPU – which is optimized for single-threaded performance – and accelerating parallel processing on embedded engines or coprocessor devices
- Key computation pieces of mission applications can be computed using coprocessors and edge devices
  - Sensor and science instrument input
  - Object tracking and obstacle identification
  - Algorithm convergence (e.g., neural network, simulations)
  - Image processing
  - Data compression algorithms and encryption



FPGA vs GPU vs CPU

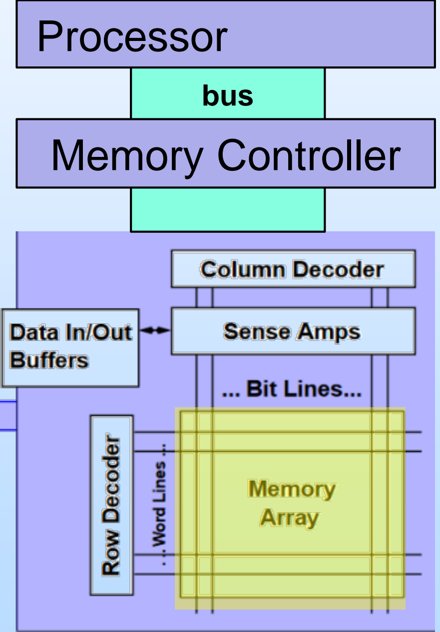
FPGA	GPU	CPU
Hardware	Software (bare-metal)	Software (+ OS)
Complete system	Accelerator is useless alone, **but ON when necessary**	Complete system
low-power	**it depends (low-power/operation)**	**+/- low-power**

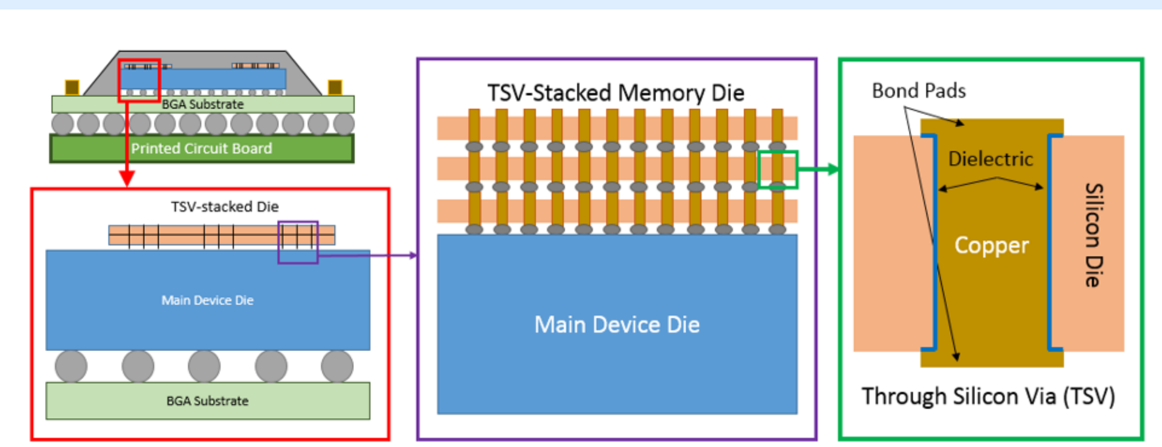
Floating-point operations (neural-net, image, radar)
High amount of data to analyze
High efficiency/high bandwidth applications

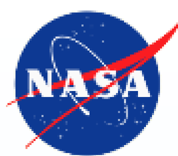


DDR Interface

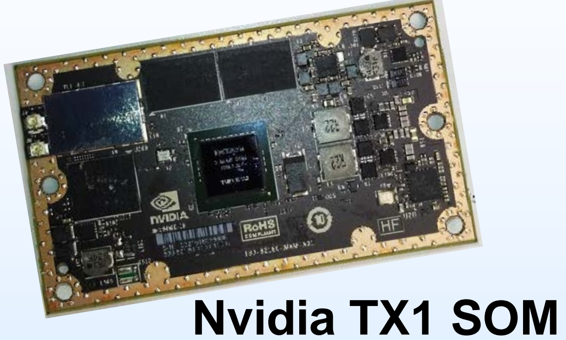
- Often found in PIP, POP and Stacked Die processors
- Multi-bit error correction features can be employed
- Cell disturbance via Rowhammer has manifested in DDR3 & DDR4 due to feature scaling
- Typical software model:
  1. Flight computers boot from ROM, but tend to run from RAM
  2. RAM permits *larger* data sets to be processed concurrently







COTS Devices



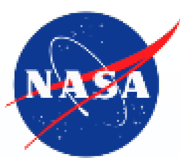
Nvidia TX1 SOM

Smart Phones

Intel Skylake Processor

Nvidia GTX 1050 GPU

AMD RX460 GPU



Evaluation Timeline

CPUs
- 14nm++ Intel (Intel)
- 10nm AMD (Global)

CPU with eGPUs
- 14nm++ Intel (Intel)
- 10nm AMD (Global)
- 10nm Qualcomm 835 (Samsung)

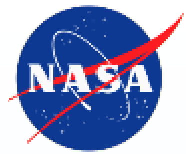
GPUs
- 14/16nm Nvidia GTX 1050/1080 (TSMC)
- 14nm AMD Radeon RX580/Vega (Global)
- 14nm Intel Discrete GPU (Intel)
- 14nm Low Power, AMD Radeon e917x (Global)
- 12nm Nvidia RTX 2080 (TSMC)

System on Chip
- 20nm Nvidia Tegra X1 (TSMC)
- 16nm Nvidia Tegra X2 (TSMC)
- 12nm Nvidia Tegra Xavier (TSMC)
- 10nm Qualcomm Snapdragon (Samsung)
- 7nm Qualcomm Snapdragon (Samsung)

*Radiation Testing (RT)
*Cold Block (CB) Adapter Development
*Test Feasibility Evaluation (FE)
*Continuation or
*Termination or

RT RT RT CB CB RT FE CB RT CB RT RT RT FE CB RT FE CB

H2FY19 FY20 FY21



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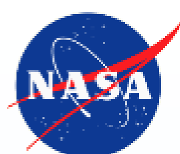
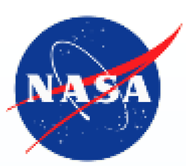


Aerospace Applications

ARAMIS: parallel processing to reduce the number of boards on aircrafts

COROT2: first GPU-powered satellite

GPU compresses images to send



Potential GPU Space Uses

GPUs can disclose A.I. for space exploration

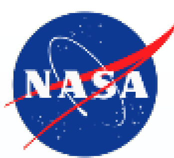
GPU-aided landing

-high amount of data to be processed in real-time

-Radar/communication in general

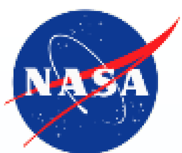
-Images compression/analysis

-Process data in space



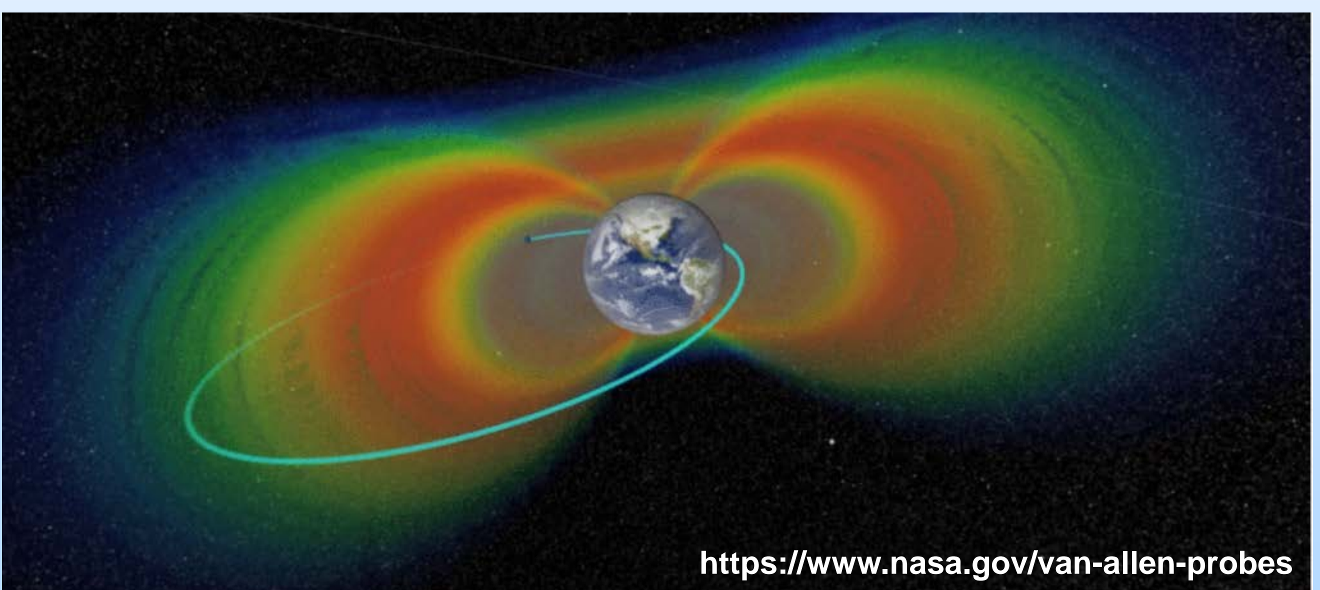
Semi-Autonomous Planetary Exploration

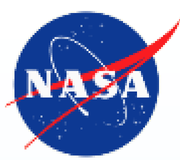
https://solarsystem.nasa.gov/news/472/10-things-mars-helicopter/



Energetic Particle Sources

- High-energy particles impact Earth's atmosphere and create air showers that generate a variety of particles (e.g., neutrons etc.) that reach ground level – fluxes are anisotropic
- Depends on latitude/longitude, atmospheric depth, and solar activity
- Process contamination in wafer fab materials
- Trace elements in packaging and in metallic (e.g., Pb) bumps
- ^{232}Th and ^{238}U are relatively abundant in terrestrial materials used in electronics processing and active enough to be a radiation effects concern





Linear Energy Transfer (LET)

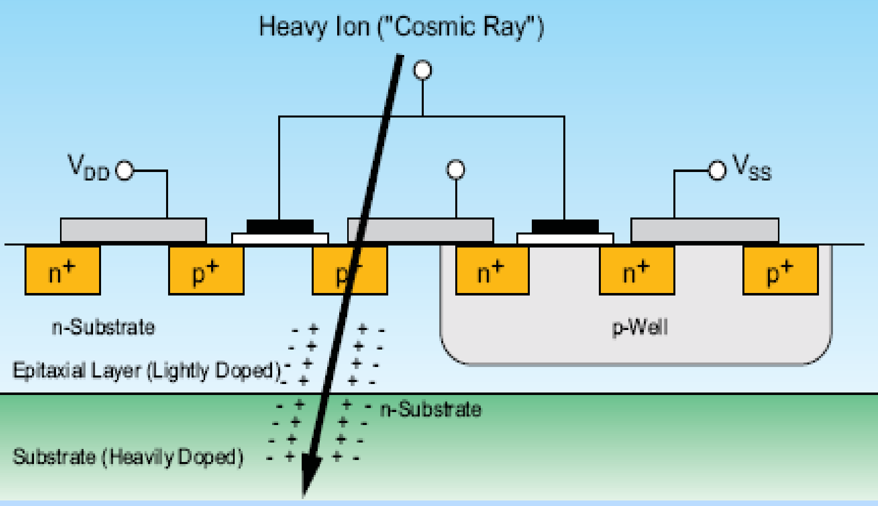
- LET characterizes the deposition of charged particles
- LET is based on average energy loss per unit path length (stopping power)
- Mass is used to normalize LET to the target material
- LET is the average energy deposited per unit path length

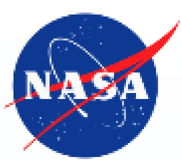
$$LET = \frac{1}{\rho}\frac{dE}{dx}$$

$$\left(MeV \frac{cm^2}{mg} \right)$$

Units

Density of target material





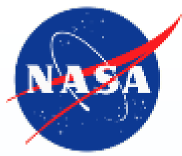
Characterizing SEUs

SEU Cross Sections (σ_{seu}) characterize how many upsets will occur based on ionizing particle exposure.

$$\sigma_{seu} = \frac{\#errors}{fluence}$$

Terminology:

- Flux (rate): Particles/(sec·cm^2)
- Fluence: Particles/cm^2
- σ_{seu} is calculated at several LET values



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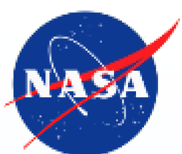


Types of Radiation Tests

2-photon Laser Testing

- Identify any extra-sensitive areas in the active area such that the characteristics of any events can be later evaluated against those results

Heavy-ion testing

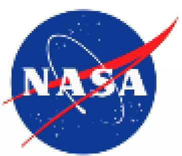
- Determine effects of different levels of Linear Energy Transfer (LET)
- Modern process technologies may be susceptible to destructive SEE
  - Heavy-ion testing is the only way to fully evaluate destructive SEE
  - If effects are apparent below 20 MeV.cm^2/mg, proton testing may be necessary

Proton testing

- Will evaluate SEE-induced transients, SEFIs, and accessible device power-states
- 200MeV protons generate secondary nuclear products with short range
- Not capable of reliably causing destructive events

Total Ionizing Dose (TID)

- In an accelerated environment, characterizes parametric variations and the long-term radiation effects on the device and determines whether dose-rate sensitivity exists



Pros and Cons

2-photon Laser Testing

- **Requires decapsulation/delidding, thinning and polishing**
- **Hard to draw direct comparisons to on-orbit performance**
- **Very focused energy deposition & visual localization of events**

Heavy-ion testing

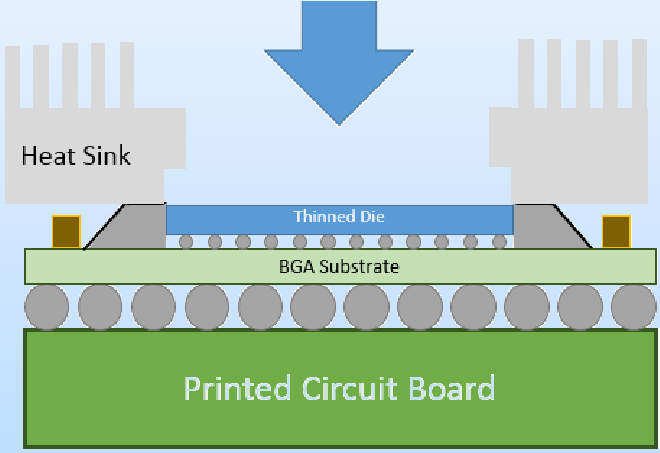
- **Requires decapsulation/delidding and sometimes thinning**
- **High LET, good range, good coverage**
- **Best comparison to on-orbit performance**

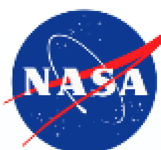
Proton testing

- **Broad beam or collimated ~1-2cm^2**
- **Limited LET, dependent on secondary interactions**
- **High accumulated dose, activation of test setup**
- **Simplest test preparation, may need to remove heat sink**

Total Ionizing Dose (TID)

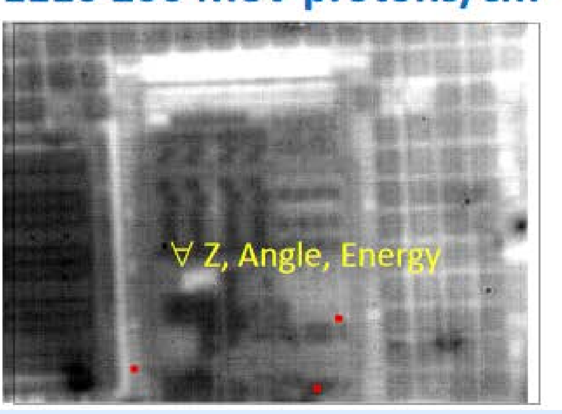
- **Hard to isolate a single component**
- **Often requires large sample size, potentially lot and wafer dependent**



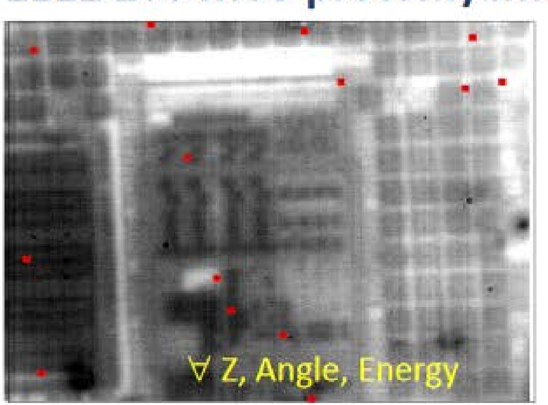


Coverage of Secondaries versus Heavy Ions

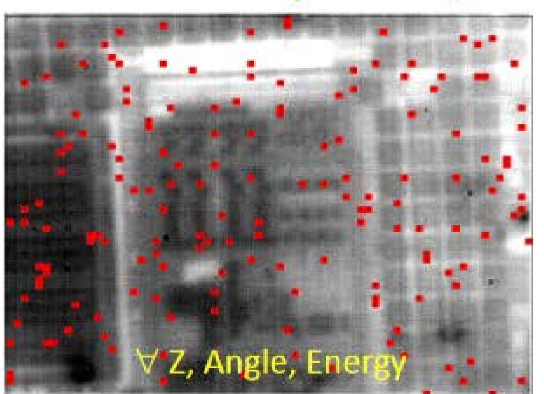
1E10 200 MeV protons/cm²

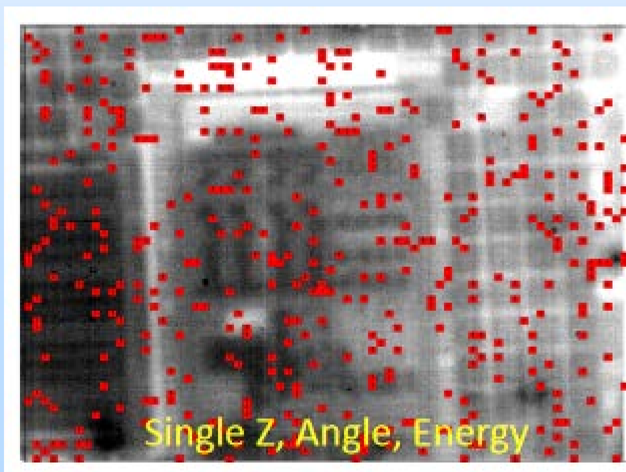


1E11 200 MeV protons/cm²



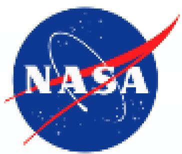
1E12 200 MeV protons/cm²





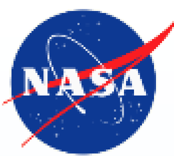
Coverage from 1E7 ions/cm²

Raymond L. Ladbury at the Single Event Effects (SEE) Symposium - Military and Aerospace Programmable Logic Devices (MAPLD) Workshop, La Jolla, CA, May 22-25, 2017



Test Setup

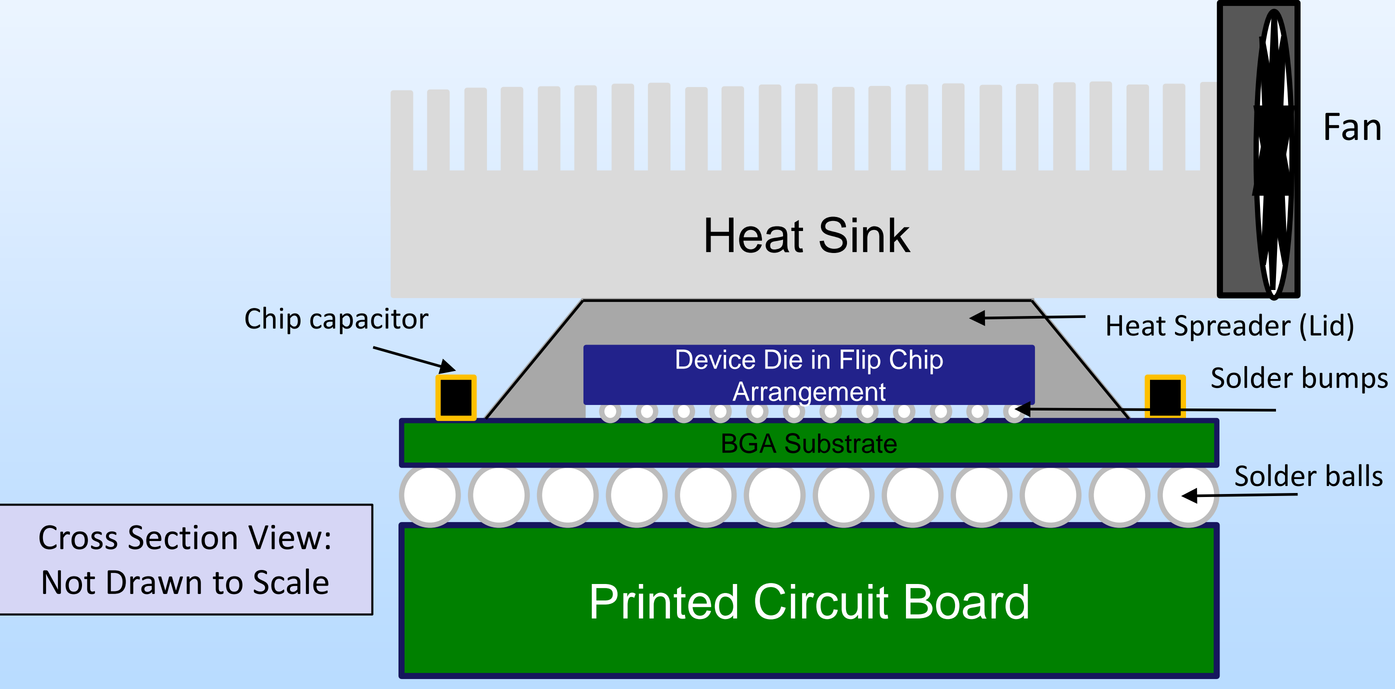
- Things to consider in the test environment
  - Physical location of payload and results
  - Data paths upstream/downstream
  - Control of electrical sources
  - Temperature control in a vacuum or air
- Things to consider in the device under test (DUT)
  - Is the die accessible?
  - What functional blocks are accessible?
  - Which functions are independent of each other?
  - Does it have proprietary or open software?
  - Operating system daemons

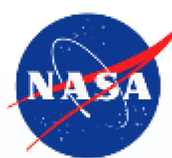


Design Requirement: Cooling

All processors that are >1W need a cooling solution

- Low power devices can use a passive cooler
- Mid to High power devices need active cooling (e.g., fan, water block)





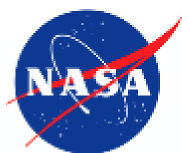
Designing a Standardized Cooler

Ambient Blower Fan

Extension Cables

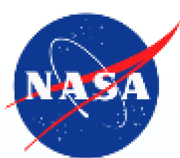
COTS System Board

Thermoelectric Cooling Plate

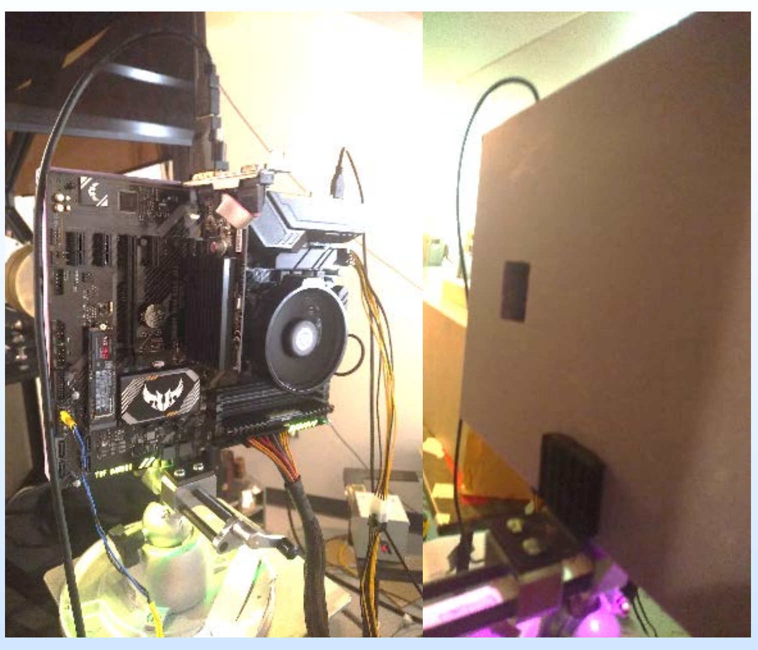


Test Environment

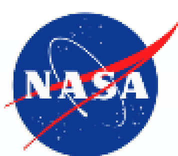
- **Beam line**
  - DUT testing zone where collateral damage can happen such as secondary neutrons
  - Shielding for everything non-DUT
- **Operator Area**
  - Cables, node control and extenders
  - Signal integrity at a distance > 50 ft
  - "Everything that was done in a lab, in front of you on a bench, now must be done from a distance…"



System Mounting



tripods, stands & open cases



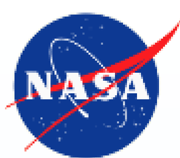
Laser or X-ray Environment

Windows Machine
- HWInfo

GPU

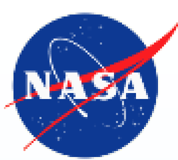
Linux NUC – Python Script, Logging from Power Supply Stack

DANGER
HIGH RADIATION AREA



Heavy-Ion Environment

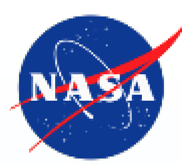
Heavy Ion Setup at The Cyclotron Institute at Texas A&M University



Proton Environment

Ted Wilcox (NASA GSFC) proton setup at Massachusetts General Hospital, Francis Burr Proton Facility

Lucite Blocks



Neutron Test Setup

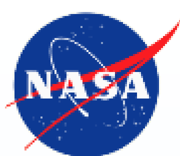
Paolo Rech (UFRGS, LANL) neutron setup at ChipIR Beamline

neutrons

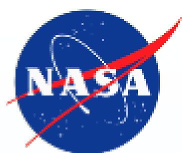
K40 – Kepler
28nm, Planar
ECC available

TX1 – Maxwell
20nm, Planar

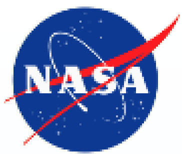
Titan X – Pascal
16nm, FinFET



Signal Integrity at a Distance

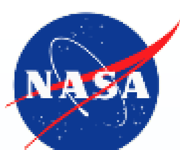


NEPP Standard Test Bench



Health Status

- What nodes in the system are accessible nodes?
- Can we make a system-level watch dog to monitor heartbeats from:
  - Network
  - Busses
  - Peripherals (input and output)
  - Electrical states
- Can we monitor at a “good enough” resolution to identify latch-up events?



Sampling using I2C hardware

Voltage Rails

12V

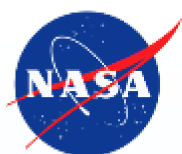
... lines...

5V

3.3V

+12V Current [A]

... noise...



Sampling using Software

GPU Load vs Temperature

100, 90, 80, 70, 60, 50, 40, 30, 20, 10, 0

12:10:05 PM

VDDC [V]

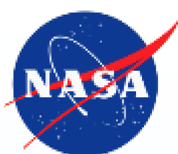
1.2, 1, 0.8, 0.6, 0.4, 0.2, 0

12:10:05 PM, 12:11:31 PM, 12:12:58 PM, 12:14:24 PM, 12:15:50 PM, 12:17:17 PM

TechPowerUp GPU-Z 2.8.0

Graphics Card | Sensors | Advanced | Validation

Sensor	Value
GPU Core Clock	139.0 MHz
GPU Memory Clock	202.5 MHz
GPU Temperature	17.0 °C
Fan Speed (%)	30 %
Memory Used	169 MB
GPU Load	3 %
Memory Controller Load	6 %
Video Engine Load	0 %
Bus Interface Load	1 %
PerfCap Reason	Idle
VDDC	0.6750 V



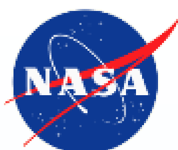
Sampling the Power Mains

Logger Lite - ryzen 1700 _rad 39.gmbl*

	Time (s)	Power (W)	Potential (Vrms)	Current (Arms)	VA (W)
489	489	35.6	120.9	0.317	37.9
490	490	35.5	120.9	0.317	38.2
491	491	35.5	120.8	0.317	38.2
492	492	35.4	120.8	0.316	37.9
493	493	35.4	120.9	0.319	38.4
494	494	35.5	120.7	0.433	38.6
495	495	49.7	120.7	0.434	51.2
496	496	49.6	120.9	0.321	52.4
497	497	35.7	120.8	0.317	40.1
498	498	35.6	120.8	0.327	38.2
499	499	35.6	120.8	0.317	38.9
500	500	35.6	120.9	0.317	38.2
501	501	35.5	120.9	0.318	37.9
502	502	35.4	120.9	0.316	38.2
503	503	35.4	120.9	0.317	37.9
504	504	35.4	120.8	0.317	38.2
505	505	35.3	120.8	0.316	37.9
506	506	35.4	120.9	0.318	38.6
507	507	35.3	120.9	0.316	38.4
508	508	35.3	120.9	0.326	37.9
509	509	35.4	120.8	0.316	38.9
510	510	35.3	120.8	0.316	38.2
511	511	35.3	120.9	0.315	37.9
512	512	35.3	120.9	0.331	37.9
513	513	35.4	120.8	0.325	38.9
514					

Real Power
35.4 W

Current (Arms) vs. Time (s)



Sampling at the Point of Load

CoPoSuM_MAIN_v1.0-rel.vi

File Edit Operate Tools Window Help

Continuous Power Supply Monitor

Rev 1.0-rel

EXIT

PS Type Simulation

Save Settings

Reset

SET

Recall Settings

Status?

Leave Pwr ON After Latch?

Master Latch Control

1 CH ALL CHs

CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
Voltage (V) 5	Voltage (V) 5	Voltage (V) 5	Voltage (V) 5
OVP (V) 10	OVP (V) 10	OVP (V) 10	OVP (V) 10
Current Limit (A) 1	Current Limit (A) 1	Current Limit (A) 1	Current Limit (A) 1
OCP Disable	OCP Disable	OCP Disable	OCP Disable
OCP Delay 0.001	OCP Delay 0.001	OCP Delay 0.001	OCP Delay 0.001

CH 1 OUT CH 2 OUT CH 3 OUT CH 4 OUT

EN 1 EN 2 EN 3 EN 4

ALL ON ALL OFF

Ch 1 Mon En Latch 1 Latch 1 0

Ch 2 Mon En Latch 2 Latch 2 0

Ch 3 Mon En Latch 3 Latch 3 0

Ch 4 Mon En Latch 4 Latch 4 0

635.501m 19:25:24 19:25:29

19:25:23 19:25:28

414.803m 19:25:24 19:25:29

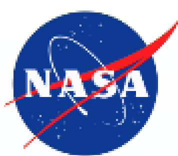
0.000 19:00:00 19:00:05

LOGGING ON OFF

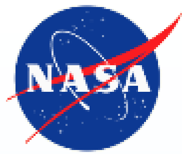
Heat Mon ON OFF

Digital IO 1 2 3 4 5 6 7

TAMU Beam Control

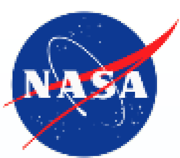


Plan ~~A B C~~ D



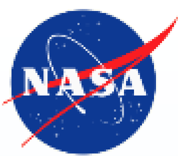
Outline

- NASA Electronic Part and Packaging Program (NEPP)
- High Performance Processing Components
- Application Environments and “Key Process Indicators”
- Design of Experiment
- **Test Vectors**
- Thoughts and Conclusions



Application Focused Payloads

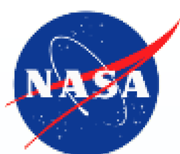
- Simulations
  - SDK Sample code
- Bit streams
  - Sensors or camera
  - Offline video feed
- Computational loading
  - LinPack
- Neural networks
  - Landsat image classification
- Display Buffer Output
  - RGBYWB Colors
  - Texture and Ray Tracing (Furmark)
- Encryption
  - SHA 256
- Benchmarks
- Easy Math
- Performance Corner tests
  - High/Low voltages
  - High/Low temperatures
  - Current limited



Software: Design Requirements

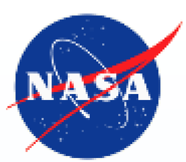
- **Does it need its own operating system?**

- **Instead of compiler optimizations for different device generations, can we create payloads and have normalization?**
  - **Can we run the same code on the previous generation and next generation of the device?**



Test Flow & Fault Tree

These bins are the classification of error signatures that we are trying to have the device under test fall into.



Silent Data Corruption vs Crash

Soft Errors in:
- data cache
- register files
- logic gates (ALU)
- scheduler

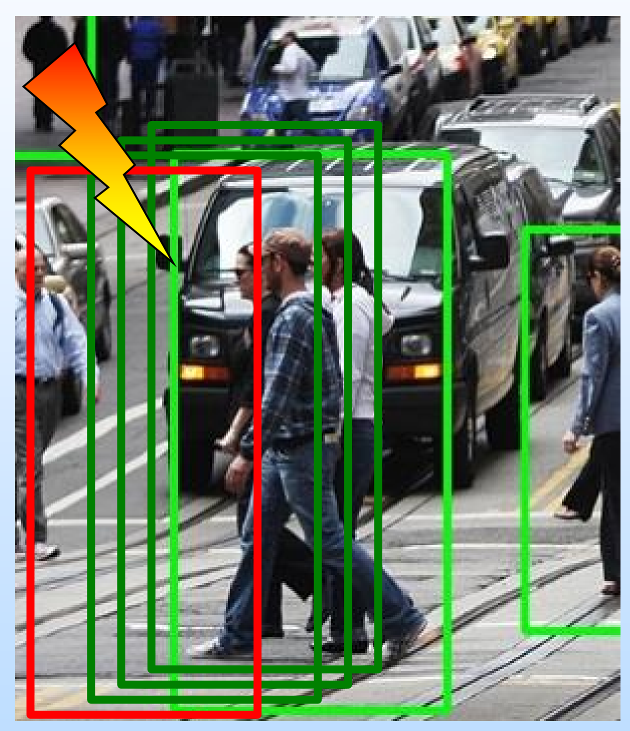
Silent Data Corruption: Output is corrupted (Can you tell?)

Soft Errors in:
- instruction cache
- scheduler / dispatcher
- bus controller

Crashes and Detected Unrecoverable Errors

What is Critical? Sometimes it's Fuzzy

Consider object detection. If there is a fault but at least 50% of the object is detected, should we consider it an error?

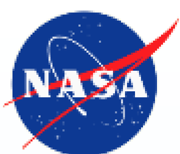


How can errors be classified?

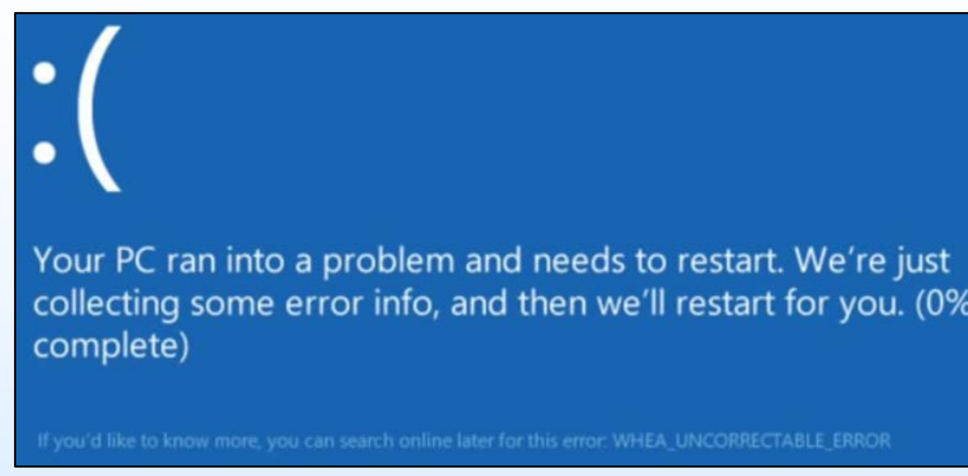
Precision: an object that is not present is detected (unnecessary vehicle stops)

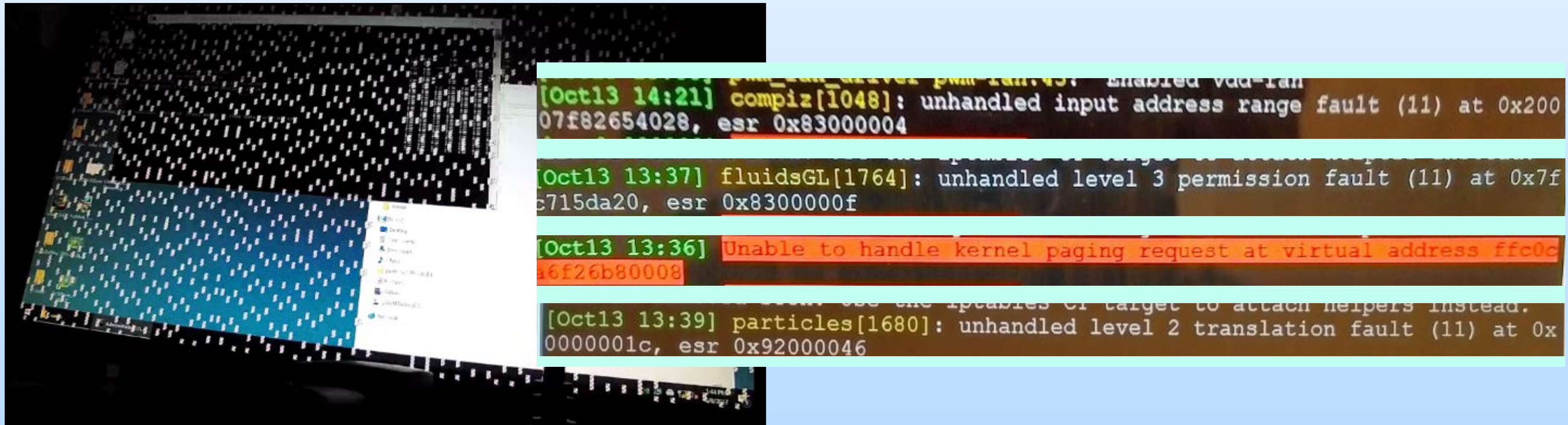
Recall during Inference: an object is missed (potentially resulting in a collision)

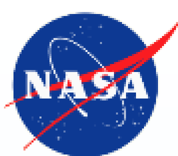
A standardized test bench must go beyond basic electrical behavior, i.e. cache upsets, but must extend to an application layer (see above).



What does a failure look like?







Latch up Signatures

nVidia TX2 in 200MeV protons

Current (Arms) during Monitored Activity

Normal operation during irradiation

Boot

Idle

UI

Idle

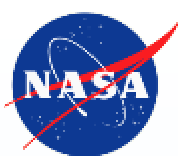
Computational Payload Loading

latchup event

reset

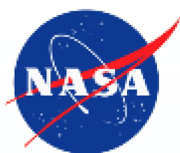
0.12
0.1
0.08
0.06
0.04
0.02
0

0 10 20 30 40 50 60 70 80 90 100



Latch up Signatures

nVidia TX2 in 200MeV protons



NEPP Standard Test Bench

Hardware Info Gathering
– Thermocouples

Power Supply Control Computer

GPU

Headless Display

Real Display

IP Camera

Interposer

Riser Cable

Power Supply A

Power Supply B

Motherboard

Software Info Gathering
– GPU (I, V, P)
– Motherboard (I, V, P)
– Memory dump
– System logs

Power Feed Switch Control

Network Access

Power Switch

Network Router

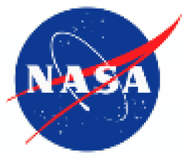
FTP storage

Operator Area

KVM

Laptop 1

Laptop 2



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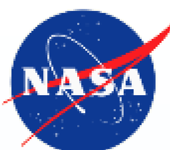
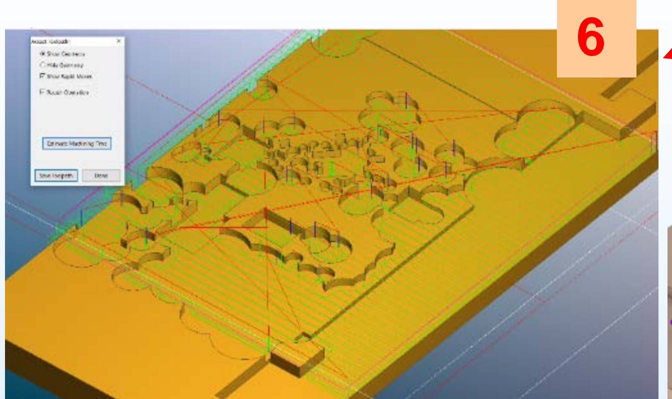
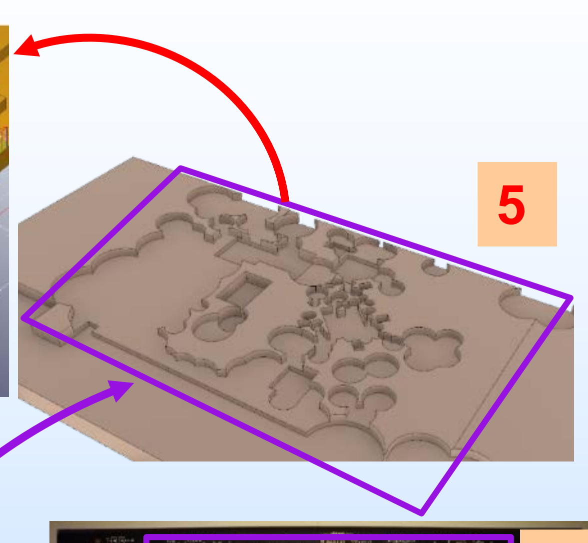


Rapid Test Preparation



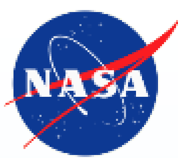


AMD e9173 GPU
(Clockwise from top right)

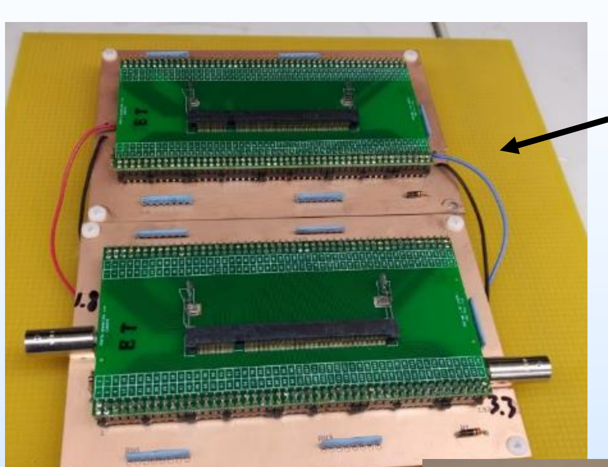
1) **As Received**
2) **Without fansink**
3) **Without Heatsink**
4) **Underside**
5) **Render of Adapter Plate**
6) **Toolpath settings**

Test Preparation:

- Software payloads are created offline
- Conduction cooling system is modular and portable
- Adapter plates are designed and fabricated in 3-5 business days



DDRx Test Readiness

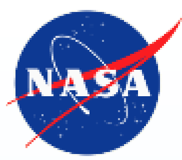


Voltage Bias Board

SPD Read and Write using microcontroller

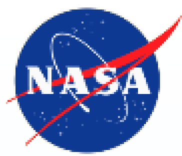
Supply current monitoring connects to LabVIEW for recording

JTAG tap connects to bus and allows PC software to exercise DDRx



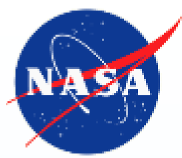
Thoughts

- Remember that space radiation, and modulation due to space weather, affects the terrestrial radiation environment – alpha particles are an additional environment
- Invoke a tiered approach for radiation effects assurance and maintain awareness that there are unknown unknowns due to rapid technology evolution
- Explore additional synergies within the community – we’re grappling with the same challenges as more advanced technologies enter our systems (e.g., reliability, availability, supply chain, etc.)



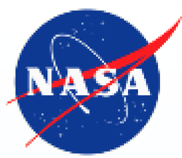
Thoughts

- NEPP and its partners have conducted proton, neutron and heavy ion testing on many devices
  - Have captured SEUs (SBU & MBU),
  - Have seen repeatable current spikes and latch up behavior,
  - Predominately have encountered system-based SEFIs
- Microprocessor and memory tests require a complex platform to arbitrate the test vectors, monitor the DUT (in multiple ways) and record data
  - None of these should require the DUT itself to reliably perform any other task outside of being exercised
- Every test is another learning experience and while improvements are always possible, preparation time may not be as abundant
- Prioritization during development is important



Conclusion

- The NEPP microprocessor and GPU testing has been standardized:
  - rapid development of cooling system for each DUT form factor and packaging type
  - system implementation using modular COTS' system and network components
  - public domain software that has been excessively tested by the community
  - payloads that can be easily updated to accommodate new DUTs while maintaining the ability to test older DUTs



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S. M. Guertin, “A guideline for SEE testing of SOC,” in Single Event Effects Symposium, San Diego, CA, May 2013. https://trs.jpl.nasa.gov/handle/2014/45991

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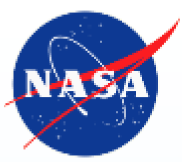

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  NASA Electronic Parts and Packaging (NEPP) Program

  NASA Office of Safety & Mission Assurance

- *Thanks is given to the NASA Goddard Space Flight Center's Radiation Effects and Analysis Group (REAG) for their technical assistance and support.*