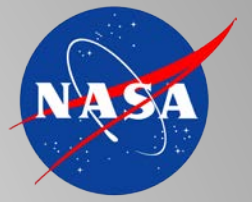


# Physics of Failure Approaches to Assessing Impacts of Assembly Level Rework Maintenance

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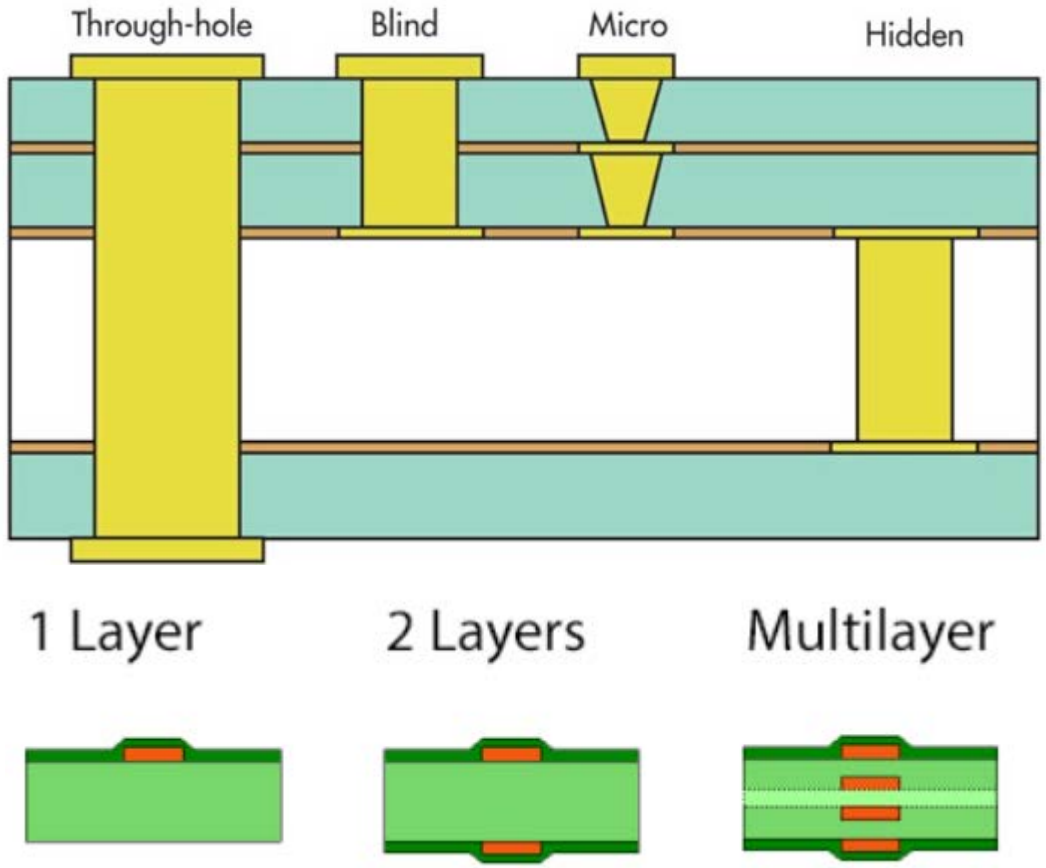
# Introduction

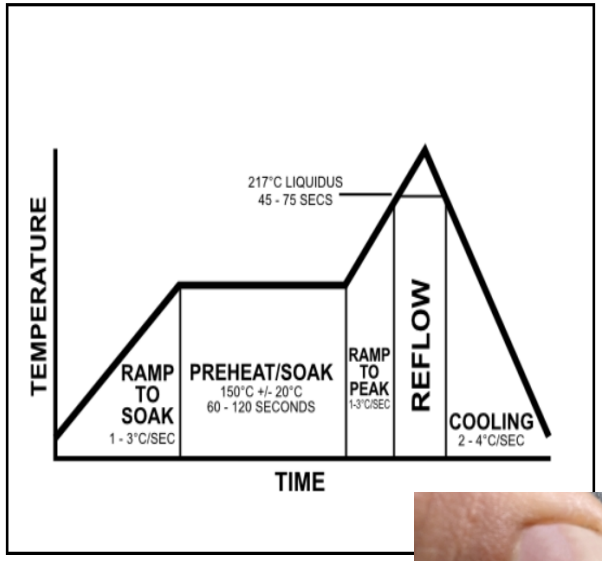
- The use of printed circuit boards has grown to dominate the Electronic Packaging industry.
- Printed circuit boards are now more complex with the inclusion of features( microvias, blind vias, buried vias), the increase of traces in each layer, and the increase in layer stack-up.
- All of these factors need to be considered when proposing the application of rework.



# Rework

- What is Rework?
  - The act of reprocessing in a manner that assures full compliance to applicable drawings/specification.
  - Maintenance " the upkeep of property or equipment" – Webster.

- Why Rework?
  - In situations where one or multiple component(s) were soldered incorrectly.
  - The removal or addition of one or multiple component(s) is necessary.



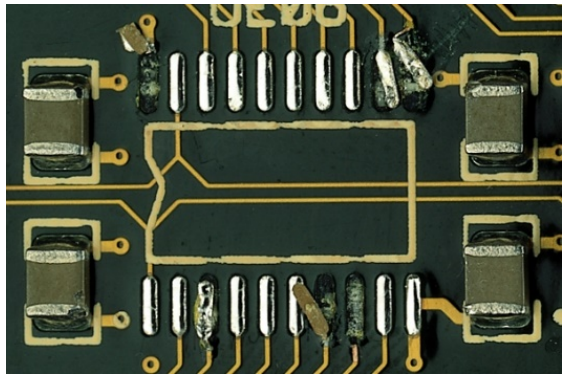

"World Leader." *CIRCUIT Technology Center*, www.circuitrework.com/.

# Motivation

- High temperatures and longer contact times with molten solder increase the risk of thermal degradation to the laminate and part leading to a higher risk of failure to the GSFC Mission Hardware.
  - Current rework guidelines for the number of allowable reworks for a component site need to be upgraded or better understood with solid research.
- This work is focused on establishing a limit on the number of reworks that can occur on selected component types without impacting the overall reliability of the assembly.
  - The outcomes will assist with developing guidelines for rework to be used in GSFC Mission printed circuit board assemblies.
- Current industry specifications, such as the J-STD-001F required that the hardware defects be documented prior to performing a rework.
  - However, the Standard does not provide a maximum or minimum number of reworks permitted on an assembly.
- Therefore, a clear guidance, based on research, is required to establish the threshold.

# Why Rework?

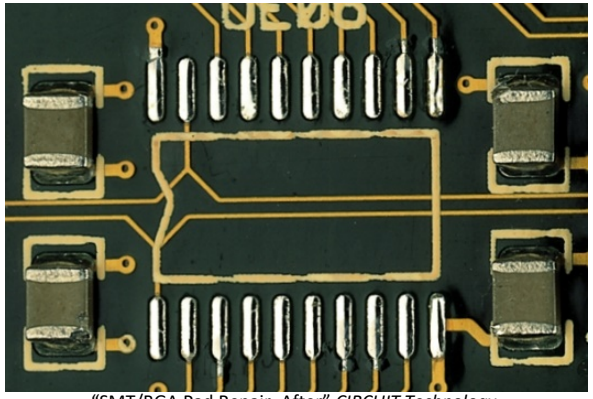
- Poor Solder joints
- Faulty Components
- Components broken due to natural wear, physical stress or excessive current.
- Machine malfunction or human error



"SMT/BGA Pad Repair. Before" *CIRCUIT Technology Center*, www.circuitrework.com/services/pads.html.

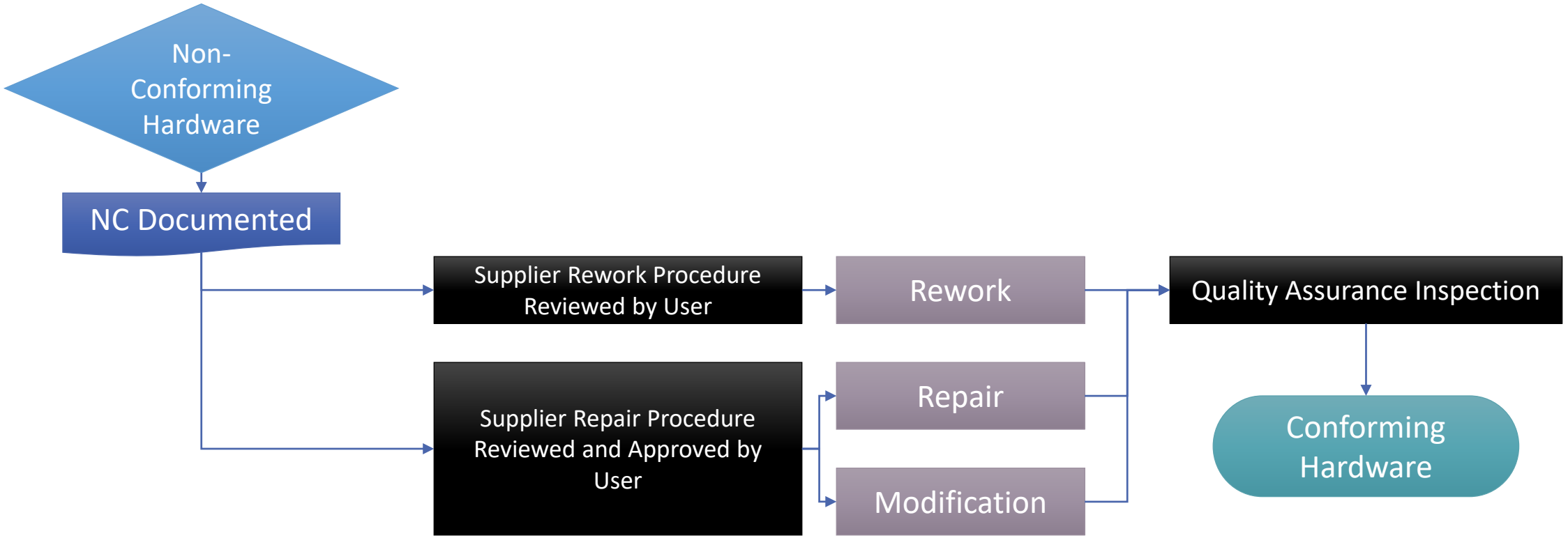
Before

After



"SMT/BGA Pad Repair. After" *CIRCUIT Technology Center*, www.circuitrework.com/services/pads.html.

# Rework Process Diagram



# Rework Snapshot at GSFC

- Currently, there are no rework or repair requirement standards, time limits, technical requirements defined at GSFC.
  - Each rework or repair request is processed via MRB discussion, and WOA review.
- The IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies has been adopted by many vendors, but the standard itself does not cover reliability issues post rework / repair.
- Most repair has non-standard configuration, such as stacking chip components, routing jumper wires close or overlapping the PWB edge, soldering a jumper wire onto a surface mount component's terminal, etc..
  - It would be good to provide some guidelines regarding to risks on these seemingly unreliable configurations.
- In addition, rework should consider if a part has been touched up or not. Currently, GSFC does not track hand soldering touch up of any part post machine soldering, for in-house or out-of-house build. Hand touch up was not treated as rework, yet it could pose similar risk to the PWA as a rework. The number of allowable hand touch ups shall be defined as well.

# Recent Experiences of Rework at GSFC

- A PWA with CCGA has cold soldering joint post convention reflow process. A rework was performed to reflow the assembly in a vapor phase reflow process. The CCGA cold soldering and voids were successfully removed. (This is an example of machine soldering rework.)

- Some rework could show perfect soldering joints, and pass post rework visual inspection. However, they may introduce latent failure, such as if the rework temperature exceeded the part allowed temperature, or PWA preheat was not performed. A strict process review/process control is needed to ensure the reliability of assembly being reworked.

# Risk associated with Rework

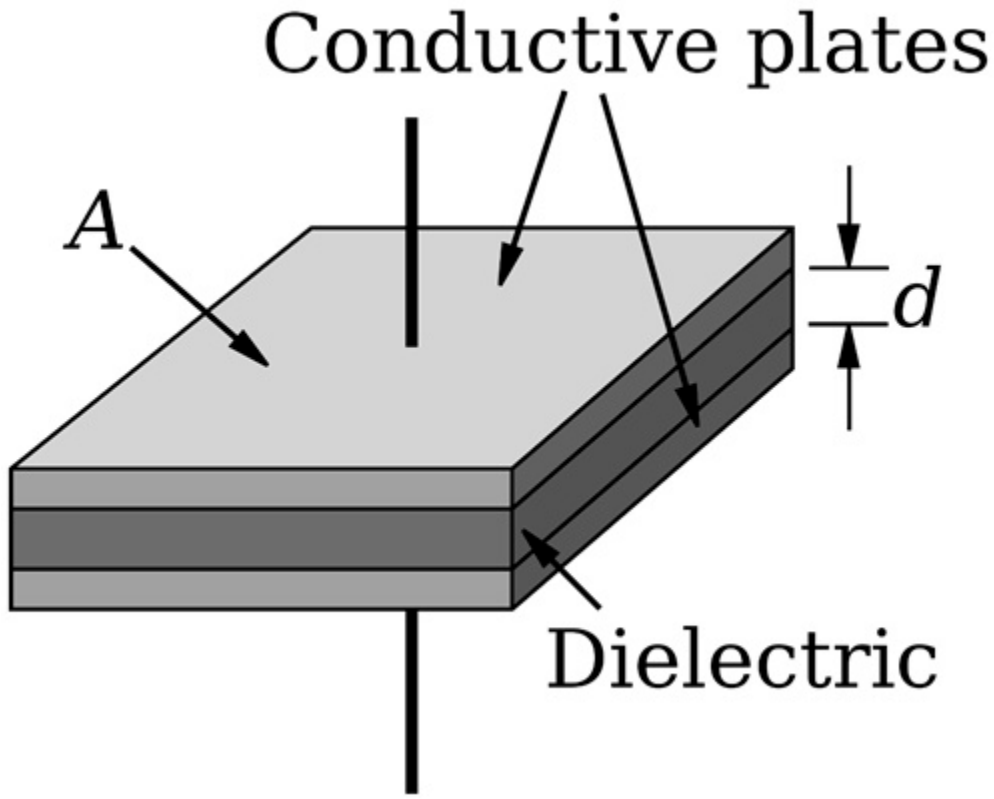
- Due to thermal excursion of from soldering there is a risk of surrounding components subjected to unanticipated heating.
  - This may cause erratic behavior of affected components, which can lead to a reduced life span or a short.
- Localized degradation of laminate material at or close to the rework site.
  - In the future can lead to delamination of the laminate.
- Board features  including microvias, plated through holes, blind vias, or buried vias experiencing localized stress concentration build-up due to thermal expansion mismatch.
  - Can lead to copper barrel or microvias cracking.

# Rework Reliability Research – Objective

- Determine the effects of assembly rework on the assembly reliability.
  - Effects of multiple rework – how does it affect IMC growth, interconnect reliability and laminate degradation?
- Quantify the effect of laminate degradation.
- How?
  - Measure capacitance  in Farad (F = Coulomb/Volt) of embedded capacitors in PCB after each rework cycle.
  - Back calculated the affected material properties.

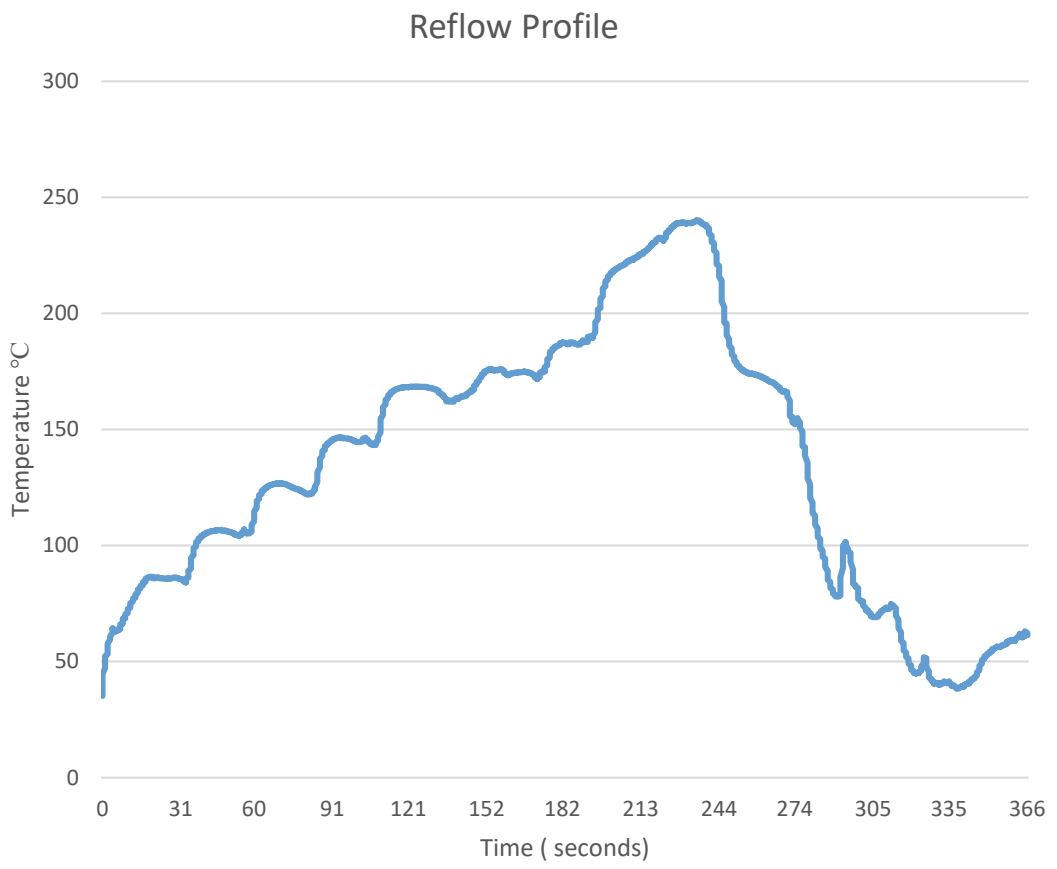
# Physical model of Capacitance

- *The capacitance of flat, parallel metallic plates of area A and separation d is given by the expression below where*
- $C = \frac{K\varepsilon_0 A}{d}$
- $\varepsilon_0 = 8.854 \times 10^{-12}\ {}^{F}/_{m} =$ permittivity of space
- K = dielectric constant of material between plates



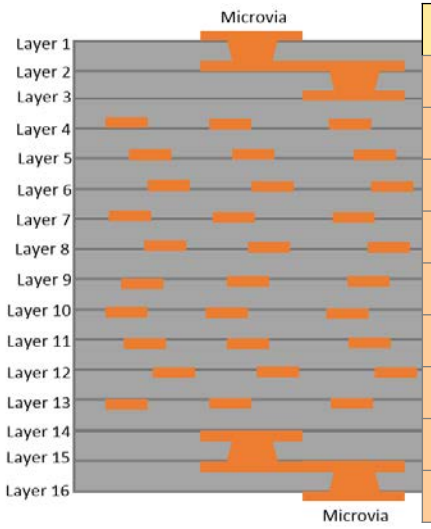
# Assembly Build - Outline

- Build 10 assemblies
- Rework 8 assemblies - 1st rework
- Rework 6 assemblies - 2nd rework
- Rework 2 assemblies - 3rd 4th 5th rework
  - Two assemblies will go through three reworks to get a total of 5 reworks.

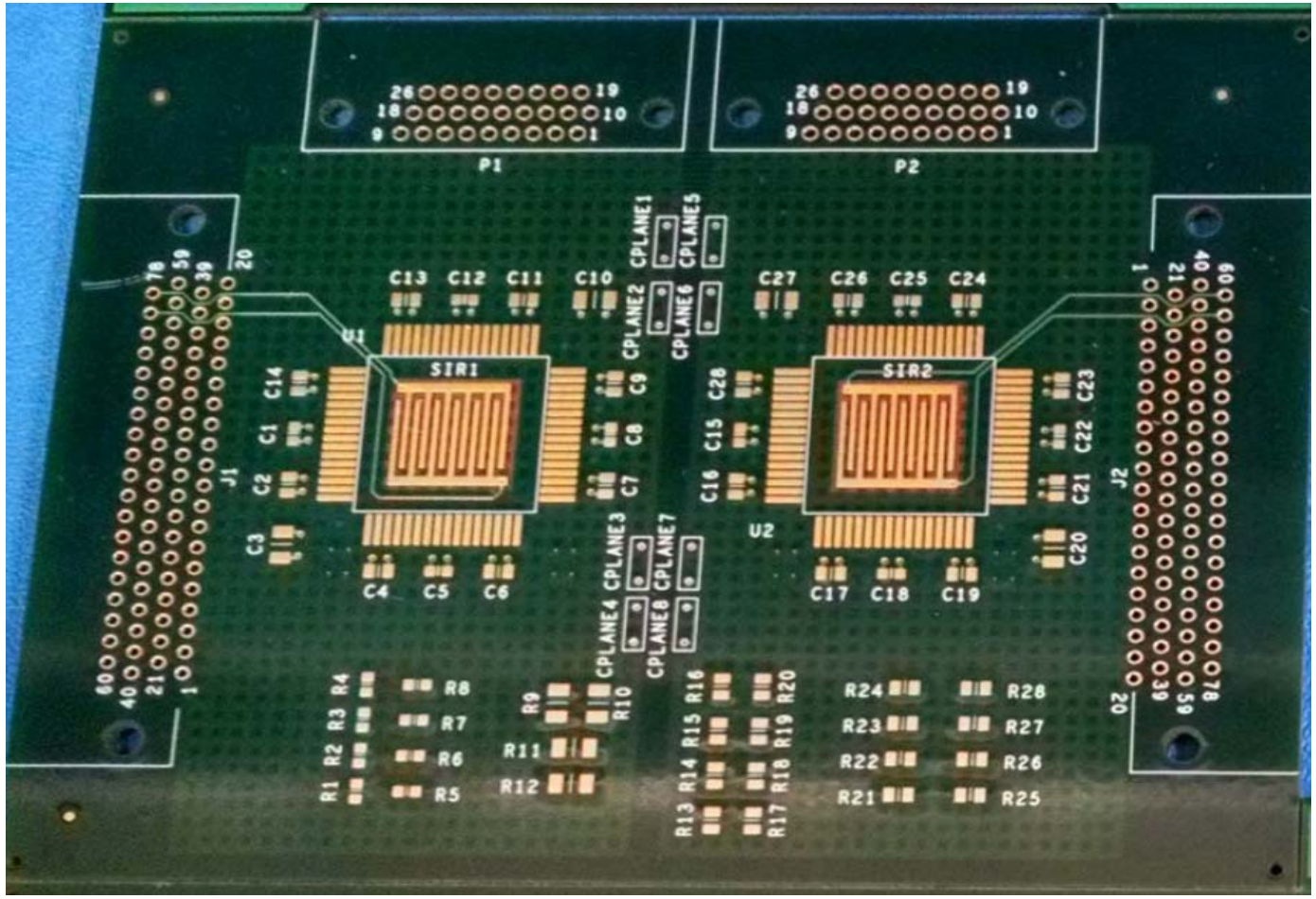


# Rework Reliability - Board Design

- PCBs are 4” x 5” are made from Polyimide and have an ENIG finish. The PCB layer stack up is 16 layers. The PCB has two microvias laminations on both top and bottom.




| Item | Qty | Part | Type |
|---|---|---|---|
| 1 | 2 | CQFP | 64 Pin 1mm |
| 2 | 8 | Capacitor | 603 |
| 3 | 16 | Capacitor | 805 |
| 4 | 4 | Capacitor | 1206 |
| 5 | 8 | Resistor | 603 |
| 6 | 16 | Resistor | 805 |
| 7 | 4 | Resistor | 1206 |
| 8 | 2 | D-Sub | 26 Pin |
| 9 | 2 | D-Sub | 78 Pin |



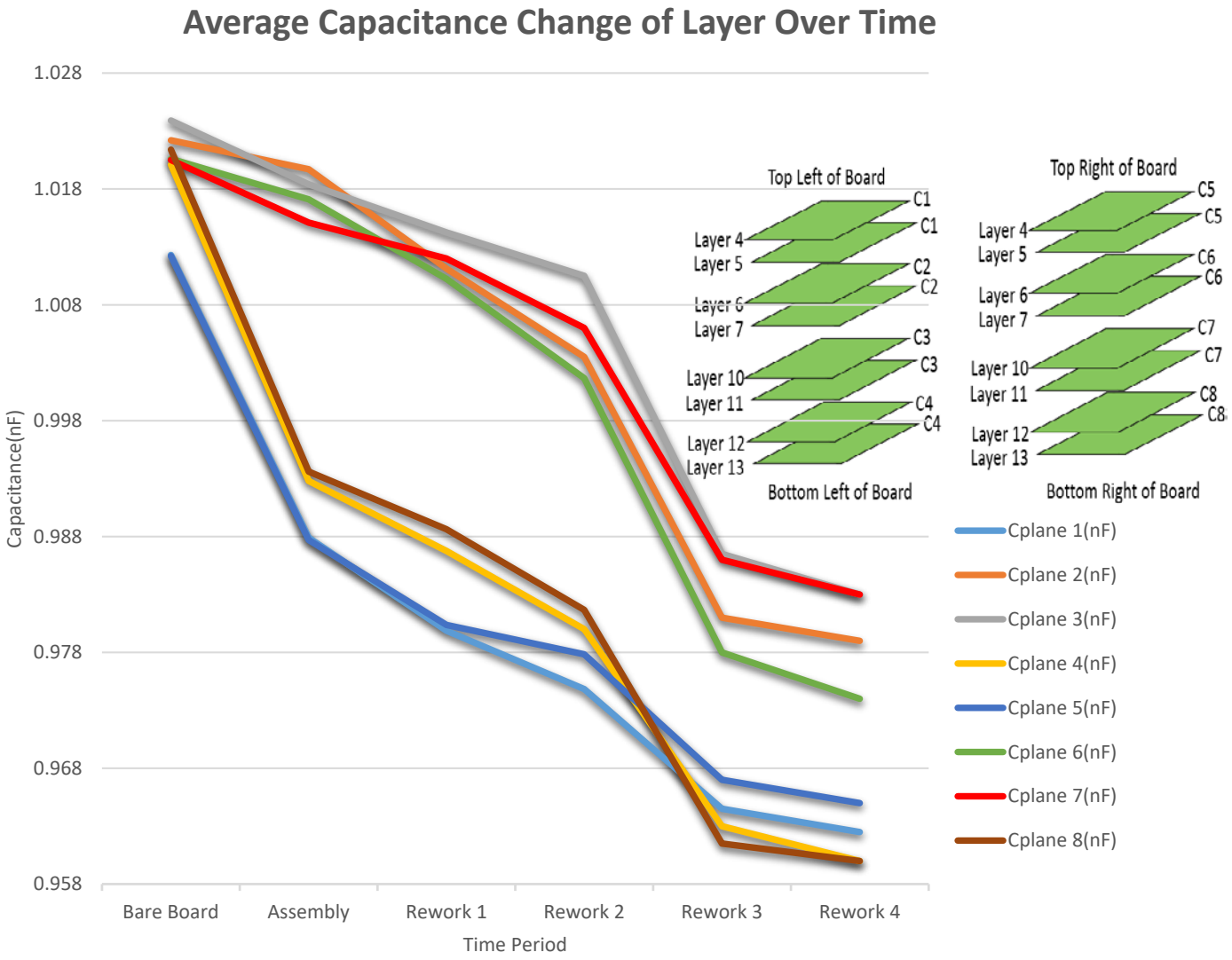
# PCB Stack up

- -Layer 4(Capacitor 1&5)
- -Layer 5(Capacitor 1&5)
- -Layer 6(Capacitor 2&6)
- -Layer 7(Capacitor 2&6)
- -Layer 10(Capacitor 3&7)
- -Layer 11(Capacitor 3&7)
- -Layer 12(Capacitor 4&8)
- -Layer 13(Capacitor 4&8)

| Layer | | Layer Thickness | | Copper Type | Dk | Df@1Ghz | Description | | |
|---|---|---|---|---|---|---|---|---|---|
| Soldermask | | 0.5 | | | 4.7 | 0.022 | | | |
| TOP | 1 | 2.5 | | 1/2 + Plating | | | Primary | Top | Fan-Outs and Wires |
| | PP | 2.5 | | | 3.72 | 0.015 | Pre-Preg 1 | | |
| SIGNAL | 2 | 0.85 | | 3/8 + Plating | | | Signal 1 | Signal | CQFP, Micovia, Resistor Wiring |
| | PP | 3.8 | | | 3.68 | 0.016 | Pre-Preg 2 | | |
| SIGNAL | 3 | 1.25 | | 3/8 + Plating | | | Signal 2 | Signal | |
| | PP | 5 | | | 3.7 | 0.016 | Pre-Preg 3 | | |
| PLANE | 4 | 1.2 | | 1 | | | Plane 1 | Plane | **Capacitor Plane1/5** |
| | CORE | 5 | | | 3.8 | 0.015 | Core 1 | | |
| PLANE | 5 | 1.2 | | 1 | | | Plane 2 | Plane | |
| | PP | 4.5 | | | 3.7 | 0.016 | Pre-Preg 4 | | |
| PLANE | 6 | 1.2 | | 1 | | | Plane 3 | Plane | **Capacitor Plane2/6** |
| | CORE | 5 | | | 3.8 | 0.015 | Core 2 | | |
| PLANE | 7 | 1.2 | | 1 | | | Plane 4 | Plane | |
| | PP | 5.5 | | | 3.7 | 0.016 | Pre-Preg 5 | | |
| SIGNAL | 8 | 0.6 | | H | | | Signal 3 | Signal | Capacitor Wiring (Wide Traces) |
| | CORE | 10 | | | 3.8 | 0.015 | Core 3 | | |
| SIGNAL | 9 | 0.6 | | H | | | Signal 4 | Signal | |
| | PP | 5.5 | | | 3.7 | 0.016 | Pre-Preg 6 | | |
| PLANE | 10 | 1.2 | | 1 | | | Plane 5 | Plane | **Capacitor Plane3/7** |
| | CORE | 5 | | | 3.8 | 0.015 | Core 4 | | |
| PLANE | 11 | 1.2 | | 1 | | | Plane 6 | Plane | |
| | PP | 4.5 | | | 3.7 | 0.016 | Pre-Preg 7 | | |
| PLANE | 12 | 1.2 | | 1 | | | Plane 7 | Plane | **Capacitor Plane4/8** |
| | CORE | 5 | | | 3.8 | 0.015 | Core 5 | | |
| PLANE | 13 | 1.2 | | 1 | | | Plane 8 | Plane | |
| | PP | 5 | | | 3.7 | 0.016 | Pre-Preg 8 | | |
| SIGNAL | 14 | 1.25 | | 3/8 + Plating | | | Signal 5 | Signal | |
| | PP | 3.8 | | | 3.68 | 0.016 | Pre-Preg 9 | | CQFP, Micovia, Resistor Wiring |
| SIGNAL | 15 | 0.85 | | 3/8 + Plating | | | Signal 6 | Signal | |

# Results I

- Capacitance is decreasing after each Rework cycle.
- The rate of change of capacitance is not uniform for all 8 layers being measured.
- There is a .02 nF gap between a set of four planes that continues after each rework
- Inner Layers (Layer 6, Layer 7, Layer 10, Layer 11) show in a similar capacitance changes when expose to rework.
- Outer Layer (Layer 4, Layer 5, Layer 12, Layer 13) show in a similar capacitance changes when expose to rework.

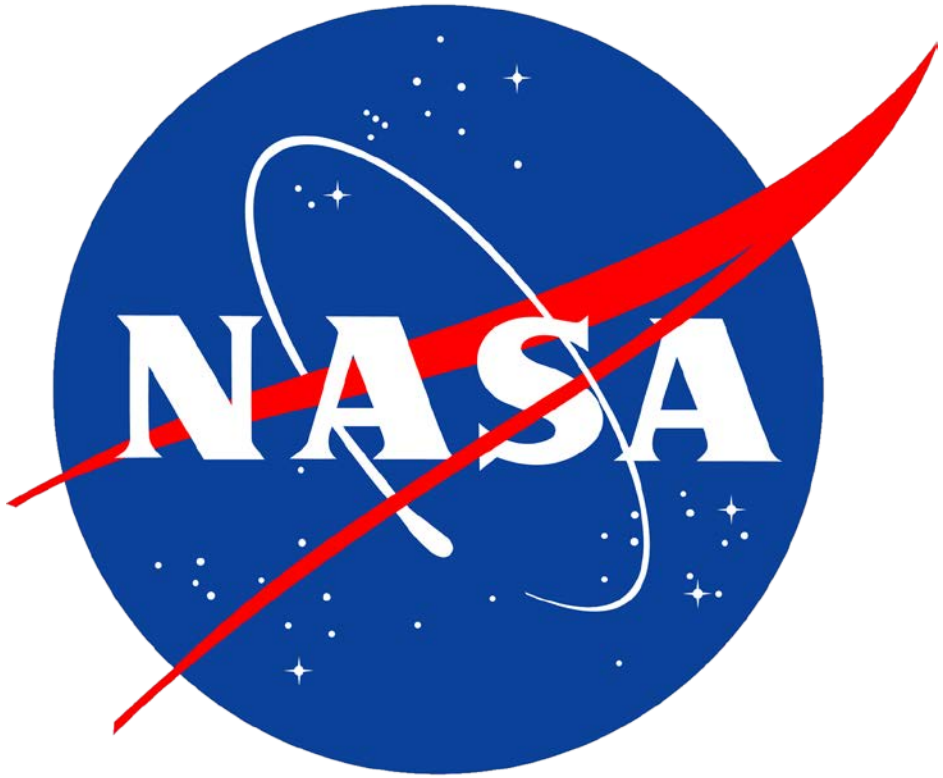


# Conclusion

- The effects of assembly rework on the assemblies' reliability has been quantified through laminate degradation.
- The data show that rework causes degradation of capacitance, which implies that the dielectric constant is strongly susceptible to rework.
- Reduction of the dielectric constant increases high-speed electrical performance of PCB.
- However this improvement may very likely cause a shorter electrical performance life period for a PCB and this will have negative impacts on reliability.

# Further Work

- More testing will be done on the 26 connector pin in an attempt to assess the effects of rework on surrounding components.
- Flux testing will be done on space were a Quad Flat Pack is removed in order to observe susceptibly to short.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