Proton Testing of AMD Ryzen 3 1200 Microprocessors

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Acronyms

ATE	Automated Test Equipment
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input Output System
BOM	Bill of Materials
BSOD	Blue Screen of Death
Cat5e	Category 5e (enhanced) specification
COTS	Commercial Off the Shelf
CPU	Central Processing Unit
CUDA	Compute Unified Device Architecture
CUFFT	CUDA Fast Fourier Transform library
DDR3	Double Data Rate 3
DDR4	Double Data Rate 4
DHCP	Dynamic Host Configuration Protocol
DRAM	Dynamic random-access memory
DUT	Device Under Test
EGL	Embedded-System Graphics Library
ES	Embedded Systems
FinFET	Fin Field-Effect Transistor
GB	Gigabyte (1 billion bytes)
GPU	Graphical Processing Unit
GUI	Graphical User Interface
HDMI	High-Definition Multimedia Interface
I/O	Input Output
IPv6	Internet Protocol version
JPL	Jet Propulsion Laboratory
LINPACK	a linear algebra library written in Fortran

MC	Machine Check
MGH	Massachusetts General Hospital
NEPP	NASA Electronic Part and Packaging
NSWC	Naval Surface Warfare Center
NVMe	Non-Volatile Memory Express
OpenCL	Open Computing Language
OpenGL	Open Graphics Library
OS	Operating System
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
RAM	Random Access Memory
REAG-ID	Radiation Effects and Analysis Group Identifier
RJ45	Registered Jack #45
SATA	Serial Advanced Technology Attachment
SDK	Software Development Kit
SDM	Software Developer Manual
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SKU	Stock Keeping Unit
SNTP	Simple Network Time Protocol
SOC	System on Chip
SOM	System on Module
SRAM	Static Random Access Memory
SSD	Solid State Drive
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus

I. Introduction

Commercial processors are an intense topic of interest for the space community. As technologies and manufacturing processes have advanced in response to the free market demand, the resulting innovations offer a tantalizing set of benefits to space users. These are: high-performance, low-cost, and a trend toward better radiation tolerance as feature sizes shrink.

However tantalizing these benefits may appear, there is usually a caveat that hinders the mass adoption of these products in space missions. In particular, the power and thermal consumption of the processor. A relatively trivial problem for terrestrial users, where countermeasures like air conditioning, heat-sinks and fans are plentiful, these power and heat obstacles can not only make these processors impractical for spacecraft, but also impractical to test within modern facilities without specially fabricated heat-removal options as developed for GPU testing.

Manufacturers stipulate that their processors are not intended for high-reliability applications. This fact is generally understood when it comes to designing potential spacecraft. However, this major limitation does not preclude the community from characterizing the technology. The change in process from planar to three-dimensional design, on its own, warrants further study, given how relatively young it is. The complexity of these commercially available FinFET devices has a significant impact on their testability. These devices contain billions of transistors with a high layer of abstraction between device input/output (IO) and the transistor level response. In addition, the devices require significant on-board circuitry such as proprietary power management integrated circuits (PMICs), DDR3 and DDR4 dynamic random access memory (DRAM), and often proprietary low level boot code.

Single-Event Effects (SEE) testing was conducted on the AMD Ryzen 3 1200 microprocessor; herein referred to as device under test (DUT). The goal of this work is to provide a baseline on radiation susceptibility data for the DUT. While not all radiation-induced errors are critical, the effects on the application need to be considered. More so, failure of the device and an inability to reset itself should be considered detrimental to the application. Radiation effects on electronic components are a significant reliability issue for systems intended for space.

The testing that has been conducted covered three types of test vectors: Linear Algebra and graphics memory and output buffer. Except in the case of a single event functional interrupt (SEFI), the test vectors employed in this round of testing were created to target the cache memory and control logic of the DUT. Because the device was recoverable upon a power cycle of the computer system, its use in a radiative environment may be possible given a hardware or software watchdog routine to detect an error and reset the device.

II. Device Under Test (DUT)

The DUT utilized is a modern state-of the-art SOC.

Table 1: Part Identification Information[1]

Quantity	1
Vendor	AMD
Part Model	Ryzen 3 1200
Codename	Zen
REAG ID	19-023
Manufacturer	Global Foundries
Technology	14nm FinFET
Packaging	Flip Chip, BGA, Socketed
Clock Speed	3.1 GHz
Cache Density	Cache L1: 96K (per core) Cache L2: 512K (per core) Cache L3: 8MB (shared)
Thermal Design Power	65 W
Memory Supported:	DDR4

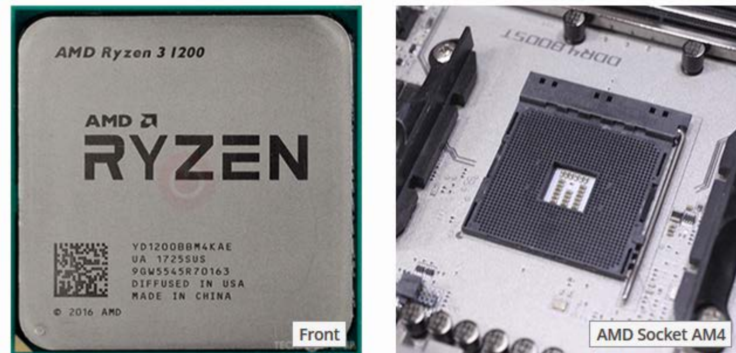

Figure 1. Processor as depicted on TechPowerUp.com

III. Facilities Utilized

Testing was conducted at Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center on June 2nd, 2019 using 200-MeV protons.

IV. Test Setup

a. Hardware

The DUT relies on a typical computer setup in order to be used. Here, the following platform bill of materials (BOM) was utilized (Table 2) along with Newegg part numbers. The operating system was Windows 10 x64.

[1] https://www.techpowerup.com/cpudb/1899/ryzen-3-1200

Table 2: Computer Platform - Bill of Materials

Newegg.com Part #	Description
N82E16813119107	ASUS TUF X470-Plus Gaming AM4 AMD X470 SATA 6Gb/s USB 3.1 HDMI ATX AMD Motherboard
N82E16819113446	AMD RYZEN 3 1200 4-Core 3.1 GHz (3.4 GHz Turbo) Socket AM4 65W YD1200BBAEBOX Desktop Processor
N82E16820236072	CORSAIR Vengeance LPX 64GB (4 x 16GB) 288-Pin DDR4 SDRAM DDR4 3000 (PC4 24000) Desktop Memory Model CMK64GX4M4C3000C15
N82E16817139084	CORSAIR HXi Series HX750i 750W 80 PLUS PLATINUM Haswell Ready Full Modular ATX12V & EPS12V SLI and Crossfire Ready Power Supply with C-Link Monitoring and Control
9SIA12K77Z5902	SAMSUNG 970 PRO M.2 2280 1TB PCIe Gen3. X4, NVMe 1.3 64L V-NAND 2-bit MLC Internal Solid State Drive (SSD) MZ-V7P1T0BW

The computer was operated nominally from a distance of 140 ft. Video was sent via onboard High-Definition Multimedia Interface (HDMI) port over Ethernet to the operator control hallway. The system was controlled using Universal Serial Bus (USB) devices (keyboard and mouse) over Ethernet. The system motherboard was mounted to an ATX footprint milled into borated polyethylene to absorb scattered neutrons which are a result of proton collisions within materials in the beam's path (i.e. heatsink).

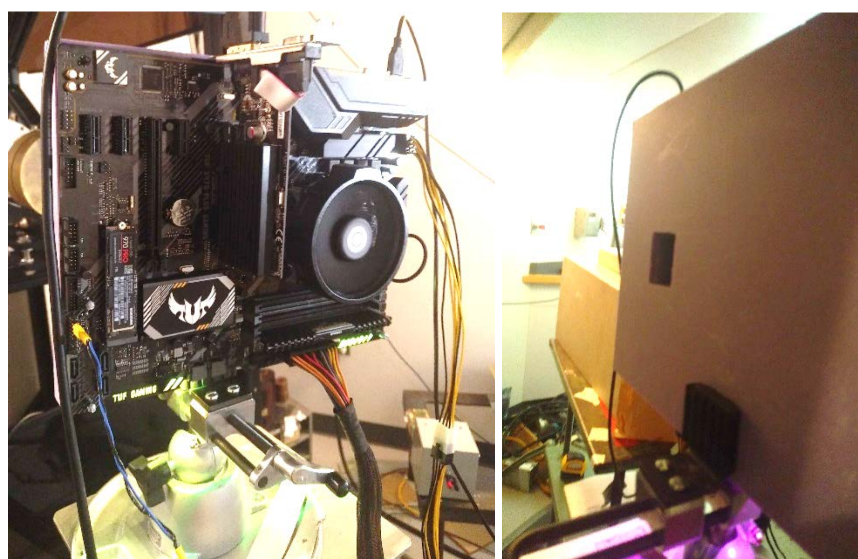

Figure 2: Test fixture and cabling: Motherboard is front side (left), Borated Polyethylene is reverse (right)

b. Software

An Operating System (OS), based on the "Windows to Go" concept introduced by Microsoft with the Windows 8 product, was installed onto the Solid State Disk (SSD) which was chosen for speed and low power requirements. Instead of Windows 8.1, Windows 10 x64 was selected. The advantage of this setup was to be able to run natively from the onboard Serial Advanced Technology Attachment (SATA) interface AND/OR the USB 2.0 or 3.0 ports, if needed. This SSD was connected to the motherboard via the M.2 slot.

During in-situ exposure, the system was booted to Windows. A freeware hardware information tool, HWiNFO64, was utilized to record DUT performance statistics and power consumption during the irradiation. When a desired fluence level was reached, or when failure behavior occurred, the beam was

stopped and the system was power cycled. A full load of software stressors consisted of using the graphical stress test tool FurMark simultaneously with the LINPACK stress test. Logging continued until the stress test calculation was completed.

Table 3: Software Used in Test Bench

Software	Function
Microsoft Windows 10 x64	Commercially available 64-bit Operating System configured to be "portable".
HWiNFO64	Freeware 64-bit Hardware Monitoring Tool and On-Board Sensor logger. Used with Corsair "i" series power supplies to monitor rail voltages and current consumption during idle and under loading conditions.
Intel Optimized LINPACK Library	Freely available mathematical stress computation and benchmarking software. 32 and 64-bit binaries are maintained by Intel with optimizations tailored to specific features on Intel products
Geeks3D.com "FurMark"	Freeware graphical stress tool – causes integrated graphics and logic accelerator capabilities to consume power and dissipate heat
Splinterware System Scheduler	"Free Version" of the software tool was utilized to automate software steps that would otherwise require interaction (i.e. key presses, custom log naming, dismissal of dialog windows)

The test was conducted on different quantities (or pairs) of CPU cores as configurable in the motherboard UEFI BIOS. Each of the following test conditions was utilized during the test campaign for each CPU core configuration. The operational status of the Windows operating system was purposely involved as the idle test condition. This allows the analysis in post processing to reduce or remove any contribution the operating system has on the application's radiation susceptibility cross section.

Test Conditions

- Idle (HWiNFO)
- Math (HWiNFO + Linpack)
- Full (HWiNFO + Linpack + Furmark)

The hardware monitoring program HWiNFO64 was run during all testing and monitored various on-die sensors such as temperature, voltage and power dissipation [[2]]. The LINPACK program was used to stress the processor components involved in matrix multiplication [[3]]. The FurMark program applied computational stress to the on-die graphical processing unit (GPU) [[4]]. The Full test condition was not employed in this test campaign. The Furmark test stresses the GPU which is not under test here.

V. Failure Modes

Three types of failure events can be recorded during the test campaign. These events are indicative of the sensitivity of the hardware to the radiation and the fault resilience of the operating system to failure of instructions, memory fetches and architecture microcode running in the background. While further analysis is required to identify the failing operating system or hardware component when the event occurred, a brief explanation of these event types is provided.

[2] [Online] http://www.hwinfo.com [Accessed: Jan-2019].

[3] J. Dongarra, et al., "Linpack benchmark." *Encyclopedia of Parallel Computing*. Springer US, 2011. 1033-1036.

[4] [Online] https://geeks3d.com/furmark/ [Accessed: Jan-2019].

The first event type was that of a processor machine check (MC) error which was logged by the operating system. Each recorded machine check error was logged as a 64-bit value and was decoded using the vendor specific hardware manuals. The decoded value was able to indicate whether the error was "corrected" or "uncorrected" and the functional block within the microprocessor from which the error originated. A mixture of corrected and uncorrected machine checks was observed. All uncorrected machine checks led directly to a system crash. Some of the corrected machine checks produced a system crash as well, but the majority of the corrected machine checks were recorded without a system crash and with no noticeable change in operation from the OS.

The corrected machine checks logged during the tests decode to either an L1 or L2 cache error according to the documentation. Further decoding of the machine checks indicate a specific cache operation associated with each event. It is unclear however if the error resulted from a bit flip in a SRAM cell within the cache or an upset in other circuitry involved with the operation of the cache. Note that cache level naming convention is adopted from the Intel SDM which lists the levels as L0, L1, and L2 with L0 being the lowest level cache.

The second event type was a system crash where the OS would become either unresponsive, shut itself down, or reboot itself. After the system crash was observed and the system was restarted, the operating system and its idle behavior was assessed to determine if latent damage had occurred.

The third event type is hardware failure. Multiple sets of the test platform and spare hardware are present at the test facility. This enables real time debug and diagnosis when any component within the hardware bill of materials becomes suspect or exhibits "hard failure" during irradiation. In general, the computer fails to boot.

VI. Results

Table 4: Test Run Parameters and Results

Run#	# Cores	Test Mode	Time of run (s)	Flux (p+/sec)	Effective Fluence (p+)	Dose rad (Si)	SEFI Cross section (cm^2)	Flux (p+/sec)
1	4	IDLE	77.4	7.09E+07	5.49E+09	318.28	1.82E-10	1
2	4	IDLE	30.6	6.57E+07	2.01E+09	116.52	4.98E-10	1
3	4	IDLE	120	6.74E+07	8.09E+09	468.87		
4	4	IDLE	52.8	6.79E+07	3.59E+09	207.92	2.79E-10	1
5	4	IDLE	120	7.06E+07	8.47E+09	491.15		
6	4	MATH	82.2	7.06E+07	5.80E+09	336.40	1.72E-10	1
7	4	MATH	22.2	7.13E+07	1.58E+09	91.69	6.32E-10	1
8	4	MATH	1.8	7.92E+07	1.43E+08	8.26	7.02E-09	1
9	4	MATH	82.2	6.22E+07	5.11E+09	296.33	1.96E-10	1
10	4	MATH	72.6	5.90E+07	4.28E+09	248.24	2.34E-10	1
11	2	IDLE	120	6.13E+07	7.36E+09	426.74		
12	2	IDLE	111	6.22E+07	6.90E+09	400.23	1.45E-10	1
13	2	IDLE	64.8	6.55E+07	4.25E+09	246.19	2.35E-10	1
14	2	IDLE	120.6	6.60E+07	7.96E+09	461.55	1.26E-10	1
15	2	IDLE	120	7.07E+07	8.49E+09	491.93		
16	2	MATH	1.2	9.99E+07	1.20E+08	6.95	8.35E-09	1
17	2	MATH	9.6	7.72E+07	7.41E+08	42.95	1.35E-09	1
18	2	MATH	81.6	7.79E+07	6.35E+09	368.34	1.57E-10	1
19	2	MATH	27.6	8.03E+07	2.22E+09	128.48	4.51E-10	1
20	2	MATH	2.4	8.77E+07	2.11E+08	12.21		

Table 5: Summary of Test Campaign Results

Ryzen 3 1200	Flux (p+/sec)	Effective Fluence (p+)	SEFI Cross section (cm^2)
min	5.90E+07	1.20E+08	1.26E-10
max	9.99E+07	8.49E+09	8.35E-09
average	7.17E+07	4.46E+09	1.33E-09
standard deviation	9.84E+06	2.98E+09	2.61E-09

VII. Discussion

The methodology used for testing was a “best effort” method to replace traditional custom bias boards and expensive automated test equipment (ATE), albeit a method that has been refined over a few investigations. The SoC manufacturer is able to afford both the ATE equipment and the manpower to develop the test vectors due to commercial sales volumes (i.e., free market economics). However, being a commercial entity, the manufacturer also is not compelled to disseminate any hint of radiation hardness or related capability, other than by way of legal (author-paraphrased) disclaimer: “We’re not liable if you irradiate our products.” The radiation test houses, unfortunately, are not able to afford such measures and this is a novel compromise to accommodate.

During the irradiation of these devices, elements of the processor appear to have operated improperly (incorrect thermal die reading, degraded state) but the processor instructional architecture continued to produce the correct LINPACK results after numerous stress tests.

The superior performance of the DUT during the LINPACK stress testing may be an unintended side effect of the device’s power management strategy when it encounters degraded thermal readings. As the strategy works to reduce the perceived overheating, it begins to reduce performance of its logic units by throttling power. Execution of the FurMark test ends up being delayed due to the slowed response time of the CPU issuing instructions to the GPU. This reduction in graphical power allows the instructional architecture to focus on LINPACK calculation. By contrast, performance of the control device suffers because the LINPACK calculation is able to be interrupted by more frequent FurMark test cycles.

VIII. Summary

We have performed a series of proton irradiations on commercial off the shelf (COTS) microprocessors, utilizing system-level tests that are conducted with commercial and free software tools. This work is a continuation of previous efforts supported by the NASA Electronic Part and Packaging (NEPP) Program and builds upon successful collaborations with NSWC Crane, Jet Propulsion Laboratory (JPL) and other entities. The authors look forward to future tests on these parts.