Proton Testing of nVidia Jetson TX2

E.J. Wyrwas[1]

NASA Goddard Space Flight Center
Code 561.4, Radiation Effects and Analysis Group
8800 Greenbelt RD
Greenbelt, MD 20771

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[1]SSAI Inc, Greenbelt, MD USA

1. Acronyms

BGA	Ball Grid Array
Cat5e	Category 5e (enhanced) specification
CPU	Central Processing Unit
CUDA	Compute Unified Device Architecture
CUFFT	CUDA Fast Fourier Transform library
DHCP	Dynamic Host Configuration Protocol
DRAM	Dynamic random-access memory
DUT	Device Under Test
EGL	Embedded-System Graphics Library
ES	Embedded Systems
GPU	Graphical Processing Unit
GUI	Graphical User Interface
HDMI	High-Definition Multimedia Interface
IPv6	Internet Protocol version
MGH	Massachusetts General Hospital
OpenGL	Open Graphics Library
OpenCL	Open Computing Language
RAM	Random Access Memory
RJ45	Registered Jack #45
SDK	Software Development Kit
SEE	Single Event Effects
SKU	Stock Keeping Unit
SNTP	Simple Network Time Protocol
SOC	System on Chip
SOM	System on Module
SRAM	Static Random Access Memory

2. Introduction and Summary of Test Results

Single-Event Effects (SEE) testing was conducted on the nVidia Jetson TX2 System on Chip (SOC); herein referred to as device under test (DUT). Testing was conducted at Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center on June 2, 2018 using 200 MeV protons. This testing trip was purposed to provide a baseline assessment of the radiation susceptibility of the DUT and to compare its performance with its predecessor, the Jetson TX1. While not all radiation-induced errors are critical, the effects on the application need to be considered. More so, failure of the device and an inability to reset itself should be considered detrimental to the application. Radiation effects on electronic components are a significant reliability issue for systems intended for space.

The testing that has been conducted should be considered a very partial test vector. While it was possible to induce upsets in the nVidia Jetson TX2, we lack insight into which element within the device experienced the upset. Further testing may include memory mapping vectors in SRAM and DRAM, and a bus-level test as these were the majority of the upset events recorded. Because the device was recoverable upon a power cycle, its use in a radiative environment may be possible given a hardware or software watchdog routine to detect an error and reset the device.

3. Device Tested

The nVidia Jetson TX2 System on Chip (SOC) was provided on a modular printed circuit board connected to a main carrier board by a 400-pin connector. The SOC itself is the device under test (DUT).

Figure 1: Nvidia Jetson TX2 System on Module (representative device)

Table 1: Part Identification Information

Quantity	2
Part Model	Jetson TX2
Part Number	REAG ID# 19-021
Manufacturer	nVidia
Technology	20nm
Packaging	Flip Chip, BGA
Module SKU	699-83310-1000-D01
Module Serials	0425018002797 (DUT1) 0423318020233 (DUT2)
Carrier Board SKU	945-82771-0000-000
Carrier Board Serials	0420219008112 0423318089692

The version of Ubuntu Linux that is pre-installed on the DUT's flash memory should be considered feature-lite as it is an embedded version based on the ARM 64-bit platform compiled specifically for the Tegra SOC. Very few sensors are accessible within Ubuntu as the hardware does not enumerate with

compatible drivers in the Ubuntu tools. However, the temperature of the GPU and CPU are both accessible. The GPU temperature is used in this study which is designated as thermal zone #2 in the virtual devices in Ubuntu.

4. Test Facility

Facility: Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center
Flux: $1.0 \times 10^7 - 1.0 \times 10^8$ protons/cm^2/sec
Fluence: $2.4 \times 10^8 - 4.0 \times 10^9$ protons/cm^2
Ion species: Proton, 200 MeV

5. Test Setup

Because the DUT is a fully operable computer system, an in-situ testing environment is necessary to replicate a field application. This configuration consists of a DUT with an operating system, software applications and the underlying hardware. An external arbitration computer operating over a closed network was used to interrogate the device, execute remote commands and monitor the DUT health.

A. Software

Software was devised to remotely execute Linux shell commands that would otherwise be manually typed into the local terminal of the DUT. The purpose of this software was to instigate and record a set of commands sent to the DUT, the system's response in terms of system temperature and processor utilization, and any errors occurring during the testing. A screenshot is provided in the following figure.

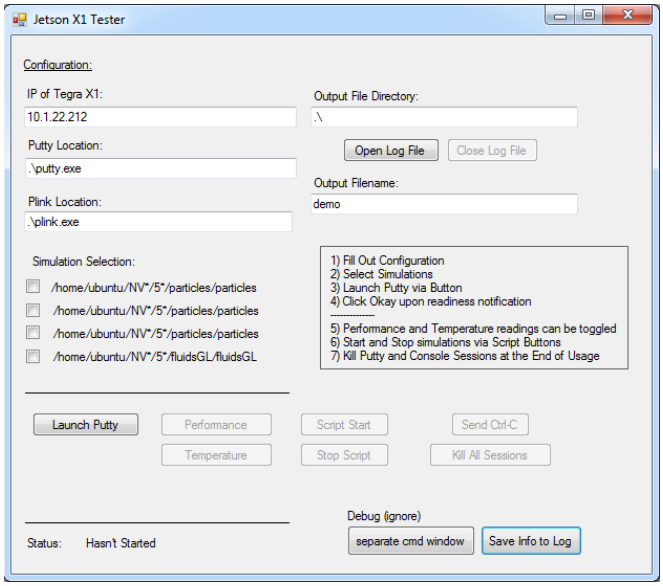

Figure 2: Screenshot of Jetson X1 tester software

The software was written in Visual Basic dot Net using the Visual Studio 2015 programming environment from Microsoft. This arrangement permitted use of both Windows and Linux commands while within a user friendly graphical interface and allowed portability of the application. Furthermore, it allowed repeatability during test as any pausing of the scripts or intervals between commands were consistent.

The logical flow of software tasks was as follows:

1. User configurable DUT network address
2. User configurable record file location and filename
3. Local-sourced terminal client location (PuTTY[1] and Plink[2])
4. Simulation selection for workload deployment
5. Options to enable/disable record files and workload

The simulations that are deployed on the DUT are sample code runtimes from the nVidia Corporation's software development kit (SDK) for CUDA version 10. This code was used as part of this test protocol as it is highly optimized for the DUT by the vendor. Further, no claims can be made that custom code deployed on the DUT is responsible for errors experienced during testing. Future testing can compare the results of this baseline test with code that is vendor independent.

B. Test Vector

Matrix arithmetic was utilized as the primary payload for System on Chip (SOC) testing as it exercised both the ARM CPU cores and the nVidia GPU cores. This application payload performs additions independently on the CPU and GPU, then compares the results. Any discrepancies are recorded in-situ and quantified during post processing.

Two simulations were selected for the GPU performance and buffer test: particles and fluidsGL. Particles uses CUDA to simulate and visualize a large set of particles and their physical interaction. FluidsGL is an example of fluid simulation using CUDA and CUFFT, with OpenGL rendering. A tertiary Ubuntu Linux environment was required to upgrade the DUT to the latest firmware (kernel version 4.9-tegra, L4T version r32.2) and monitor the DUT during lab bench evaluation prior to the test trip.

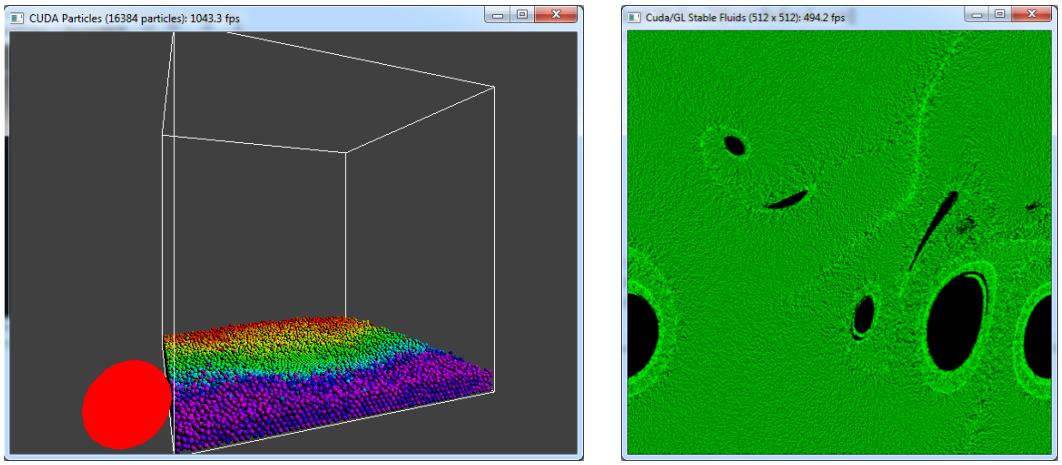

Figure 3: nVidia CUDA Samples (Particles and FluidsGL, left and right, respectively)

The goal of running these specific simulations was to assure low CPU usage (across all cores) and high GPU usage (as reported by grid usage) on the DUT. The selection of these simulations was based on GPU performance results as determined by the nVidia CUDA Profiler software (from nVidia Corporation) which was used to evaluate the consumption of system resources of the TX1. This software permitted evaluation of the simulation software threads in regards to core affinity, RAM usage, and CPU to GPU

[1] www.putty.org; PuTTY is an SSH and telnet client, developed originally by Simon Tatham for the Windows platform. PuTTY is open source software that is available with source code and is developed and supported by a group of volunteers.

[2] a command-line interface to the PuTTY back ends

offloading. Further, the output buffer to the display (graphics as humans see them) was monitored for pixel artifacts, horizontal and vertical frame rate synchronization and overall failure to update the frame buffer.

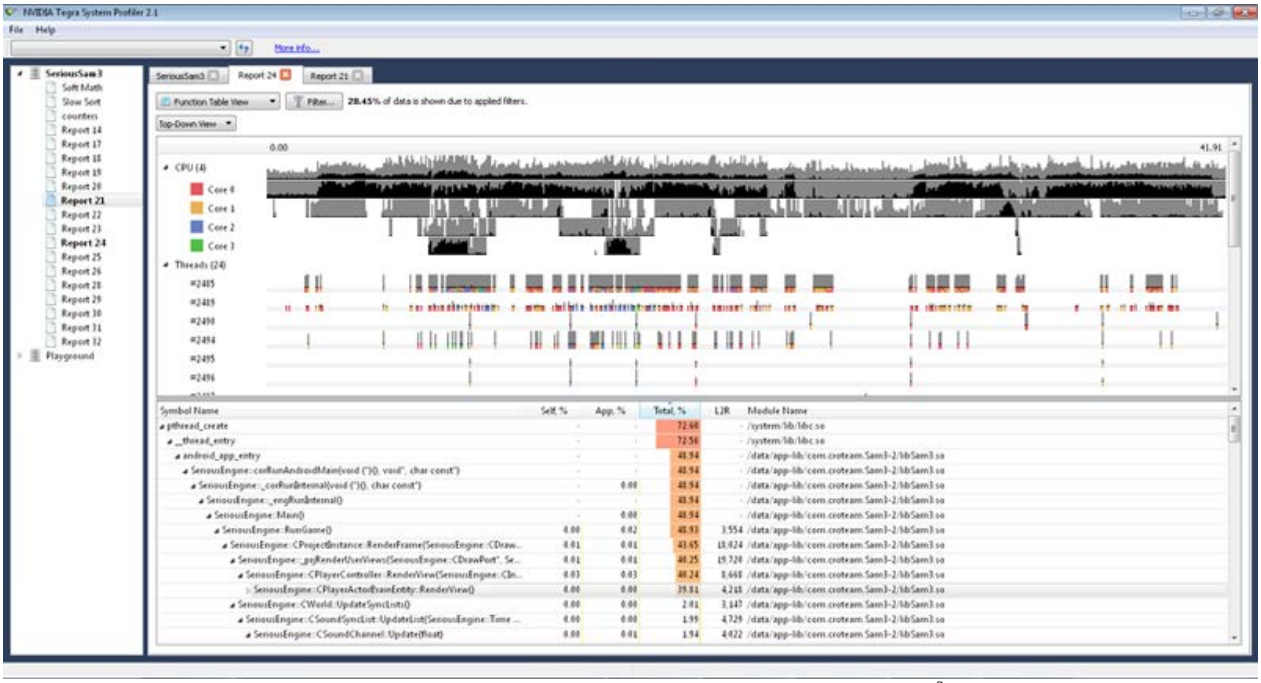

Figure 4: nVidia Tegra System Profiler, Representative Example[3]

C. Hardware

The DUT is found in the center of a metal core module that is used to sink the heat from the components. Due to the orientation of the module on the system board, the beam was aligned to the backside of the system board, through the thermal sink and onto the SOC. A secondary fan-sink is located on the component side of the module. There was sufficient clearance around the SOC and no components were present on the secondary side of the system board within the z-axis of the SOC. This was advantageous as it allowed some radiation mitigation to other system components such as the power management and flash memory components.

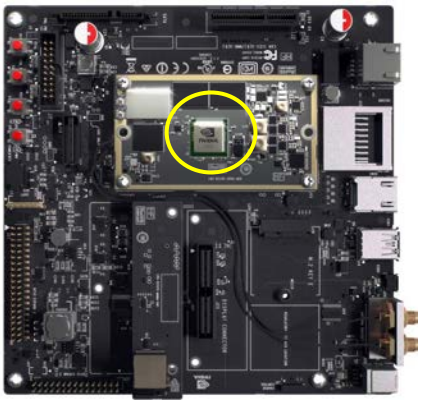

Figure 5: nVidia Image of Jetson TX1 System, with Tegra System on Chip marked[4]

[3] Image courtesy of https://developer.nvidia.com/tegra-system-profiler

[4] Image courtesy of http://www.anandtech.com/show/9779/nvidia-announces-jetson-tx1-tegra-x1-module-development-kit

Lucite bricks were used to shield the power supply of the DUT from scattered neutrons which are a result of proton collisions within materials in the beam's path. Unlike prior TX1 tests, an HDMI over Ethernet connection was used with the DUT during testing to monitor the Linux environment from the operator area (~140 feet away). Further, both a power line mains electrical monitor and a point of load power supply with in-situ measurement capability were used to record any electrical latch-up or latch-up like behavior. The computer which runs the Jetson X1 tester software is considered the arbiter system. A router provided a DHCP service on a closed network. A network switch was utilized to provide an isolated medium between the arbiter and the DUT. Network communication was performed over a CAT5e cable from the DUT to the switch and the arbiter to the switch.

6. Test Procedure and Results

Each run was conducted using a fresh session of the tester software and was performed after a power cycle of the DUT. A "kill all" command is contained in the tester software to ensure no remnant processes (ones that are utilized in the test sequence) are running prior to testing at both the arbiter machine and the DUT. The beam was engaged after the simulation software was running and at least one set of performance and temperature measurements were saved to the run's log file.

Thermal dissipation due to application loading, stress profiles and impinging radiation particles were consistent with prior TX1 results. The DUT experienced a thermal loading of approximately 25°C during full load, 10°C during idle and 20°C during partial load, all above room temperature.

Single-Event Functional Interrupts (SEFI) occurred during all runs. Only two instances occurred where pixel artifacts coincided with a SEFI. All SEFIs required the system to be reset through a power cycle. The second DUT experienced pixel artifacts and a catastrophic failure during its first test run. This failure follows the module and is currently undergoing root cause analysis. DUT1 received ~680 rad(Si) dose and DUT2 received ~60 rad(Si) dose. The results from this test campaign and a comparison summary with the Jetson TX1 are provided in Table 2 and Table 3.

Table 2: Testing Results

Run#	S/N	Test Mode	Time of run (s)	Flux	Effective Fluence	Dose rad (Si)	SEU Cross section
1	425018002797	Math/Simulation	51	5.09E+07	2.59E+09	94.43	3.85E-10
2	425018002797	Math/Simulation	19.2	7.20E+07	1.38E+09	50.31	7.23E-10
3	425018002797	Math/Simulation	55.2	5.95E+07	3.28E+09	119.45	3.05E-10
4	425018002797	Math/Simulation	36	1.11E+08	4.01E+09	145.77	2.50E-10
5	425018002797	Math/Simulation	48	5.60E+07	2.69E+09	97.73	3.72E-10
7	425018002797	Math/Simulation	22.2	5.45E+07	1.21E+09	43.99	8.27E-10
8	425018002797	Math/Simulation	10.2	5.47E+07	5.58E+08	20.30	1.79E-09
9	425018002797	Math/Simulation	15.6	5.03E+07	7.84E+08	28.53	1.28E-09
10	425018002797	Math/Simulation	24	9.99E+06	2.40E+08	8.72	4.17E-09
11	425018002797	Failure to load Linux	0				
12	425018002797	Math/Simulation	172.8	1.10E+07	1.89E+09	68.91	5.28E-10
13	423318020233	Math/Simulation	147	1.09E+07	1.61E+09	58.57	6.21E-10
		min		9.99E+06	2.40E+08		2.50E-10
		max		1.11E+08	4.01E+09		4.17E-09
		average		4.92E+07	1.84E+09		1.02E-09
		std dev		3.01E+07	1.18E+09		1.14E-09

Table 3: Comparison of Jetson TX1 and TX2

	Flux (p+/sec)		Fluence (p+)		Cross Section (cm^2)	
	TX2	TX1	TX2	TX1	TX2	TX1
min	9.99E+06	1.03E+06	2.40E+08	9.24E+06	2.50E-10	2.65E-09
max	1.11E+08	2.83E+07	4.01E+09	3.77E+08	4.17E-09	5.05E-07
average	4.92E+07	4.38E+06	1.84E+09	1.33E+08	1.02E-09	6.22E-08
std dev	3.01E+07	7.75E+06	1.18E+09	1.11E+08	1.14E-09	1.21E-07