Room Temperature Radiation Testing of a 500 °C Durable 4H-SiC JFET Integrated Circuit Technology

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Abstract— **Total ionizing dose (TID) and single-event effect (SEE) room-temperature radiation test results are presented for developmental prototype 4H-SiC junction field effect transistor (JFET) semiconductor integrated circuits (ICs) that have demonstrated prolonged operation in extremely high-temperature (500 °C) environments. The devices tested demonstrated over 7 Mrad(Si) TID tolerance and no destructive SEE susceptibility.**

Index Terms**—integrated circuit (IC), junction field effect transistor (JFET), radiation, silicon carbide (SiC), single-event effects (SEE), total ionizing dose (TID)**

I. Introduction

THE Jovian moons and planet Venus continue to be scientific priorities for exploration [1]. Missions designed to meet these objectives must operate in severe environments. The total ionizing dose rate near the Jovian moon, Europa, is approximately 300 times that at Earth's geostationary orbit [2] for standard 100-mil Al shielding. The Venus surface environment consists of a highly reactive chemical media at about 9.3 MPa (92 times Earth's atmospheric pressure) and about 460 °C [3]. Commercial silicon carbide (SiC) semiconductor power devices as well as prototype SiC bipolar junction transistor (BJT) integrated circuits (ICs) have been shown to be robust to total ionizing dose [4, 5]. Recent generation prototype SiC junction field effect transistor (JFET) ICs developed at NASA Glenn Research Center (GRC) have operated successfully for one year at 500 °C in air [6, 7]. This same technology was more recently reported to operate for two months with the chips unprotected (no package lid and no cooling) from Venus surface atmospheric conditions in a test chamber [8].

In this work, the radiation tolerance of the NASA GRC prototype 4H-SiC JFET devices and integrated circuits was experimentally evaluated at room temperature. Total ionizing dose testing of ring oscillators, operational amplifiers, and individual n-channel JFETs was conducted up to 7 Mrad(Si). These same devices, as well as a flip-flop and a clock signal generator with electronically selectable divide-by-2 or divide-by-4 output signal frequencies, were exposed to heavy ions up to a silicon linear energy transfer (LET(Si)) of 86 MeV-cm^2/mg.

This developmental NASA GRC JFET IC device technology is depicted in simplified cross section in Fig. 1, and features n-type 4H-SiC epilayer-channel JFETs and resistors integrated with two levels of $TaSi_2$ metal interconnect and SiO_2 dielectric layers. The top dielectric layers of the stack, comprising a 67 nm Si_2N_3 layer sandwiched between 1 µm thick deposited SiO_2 3 and SiO_2 4 layers, protect the underlying $TaSi_2$ interconnect metal from oxidizing during high temperature operation [9].

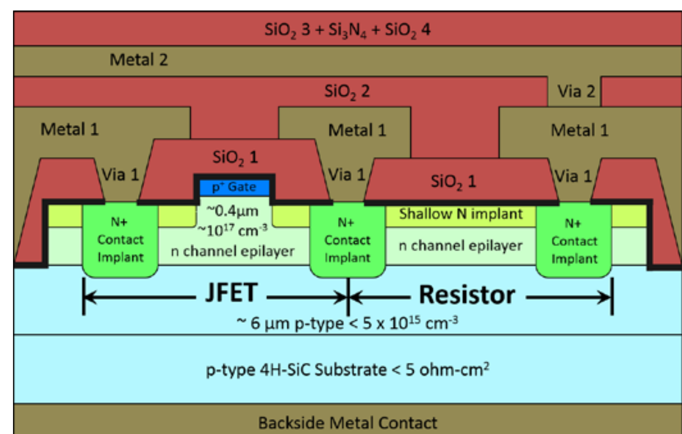

Fig. 1. Simplified schematic cross section of SiC JFET and resistor device structure with two levels of interconnect.

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II. Test Samples

The devices tested in this study came from "Wafer 10.1" and "Wafer 10.2" fabricated at NASA GRC using "IC Version 10" 6 µm dimension process technology described in [6, 7, 9, 10]. During normal circuit operation, the substrate of this technology is biased at the V_{SS} supply voltage of approximately -25 V.

A. Ring Oscillator

Ring oscillator devices under test (DUTs) consist of an 11-stage ("LF" layout design [11]) ring of NOT gates plus 3 output buffer stages (an "LF" stage feeding 2 "MF" stages [11]), and are made of 28 JFETs. The output when measured with non-negligible cable and probe capacitive loading effects is an approximately 1 MHz, 100 mV triangular wave. IC samples were packaged in 12-pin metal cans, but no package lid was present for SEE testing. Sample size for TID tests was 6, including 1 un-irradiated control. One additional sample was used for SEE testing.

B. Operational Amplifier

The operational amplifiers (op amps) tested have a 2-stage differential input and a voltage gain up to 50 with on-chip resistors. The op amp is composed of 10 JFETs, with similar stage architecture as shown in [9]. Samples were packaged in 12-pin metal cans, but no package lid was present for SEE testing. Sample size for TID tests was 7, including 1 un-irradiated control. Three additional samples were used for SEE testing.

C. JFET

The JFETs tested were n-channel normally-on integrated devices, with 192 µm/6 µm W/L gates. The normal operating voltages of these JFETs include a gate-source voltage (V_{GS}) of -10 V to 0 V and a drain-source voltage (V_{DS}) of up to 40 V. Samples were packaged in 12-pin metal cans, but no package lid was present for SEE testing. Sample size for TID tests was 7, including 1 un-irradiated control. Three additional samples were used for SEE testing.

D. Clock Circuit

The clock circuit was the most complex circuit tested. It consists of a 21-stage ring oscillator that provides a "base" frequency, with electronically selectable divide-by-2 or divide-by-4 output frequencies achieved using two D-type flip flops and control signal logic. There is also a "Clock In" signal input that (when optionally desired) enables frequency division to be conducted (by the same D flip-flops) on an externally provided "base" clock signal instead of the on-chip "base-clock" provided by the 21-stage ring oscillator. Detailed circuit architecture can be found in [10]. The clock IC is composed of 175 JFETs. IC samples were packaged in custom high-temperature co-fired ceramic (HTCC) packages without package lids. Four samples were used for SEE testing.

E. Flip Flop

These flip flops are identical to those used in the clock circuit and are composed of 25 JFETs [10]. Samples were packaged in custom high-temperature co-fired ceramic (HTCC) packages without package lids. Two individual D-type flip flop samples comprising combination logic gates were used for SEE testing.

III. Experimental Methods

A. Total Ionizing Dose Testing

Samples to be irradiated were mounted on a custom test board which was then positioned inside a PbAl box in a gamma radiation chamber. Test equipment was placed on a bench outside the chamber and included Keithley 2400 and 2410 source meters, an Agilent E3647A dual power supply, and a Tektronix TDS3014 oscilloscope. The DUTs were connected to the test equipment via 50' BNC cables using a Keithley 7001 switch box to enable individual DUT measurements between dose steps. Un-irradiated control devices were placed on an electrostatic discharge (ESD) mat near the test equipment and interfaced via clip leads. All equipment was controlled by a custom LabVIEW program. After the final dose step and measurement, control samples were mounted on the test board in the chamber and re-measured via the 50' BNC leads. During irradiation, all parts were biased according to Fig. 2. Table I gives the dose steps. Testing occurred over a period of 4 days; during overnight periods (indicated by an asterisk in Table I), the dose rate was reduced by about half that of the daytime rate of 152.6 krad(Si)/hr. Following each dose step, measurements were taken after a 15 minute anneal period.

At the completion of the test, all samples were shipped back to NASA GRC, resulting in a 2 week period of unbiased anneal during transport. Samples were re-measured at GRC over a period of approximately 1 week during which the samples remained biased.

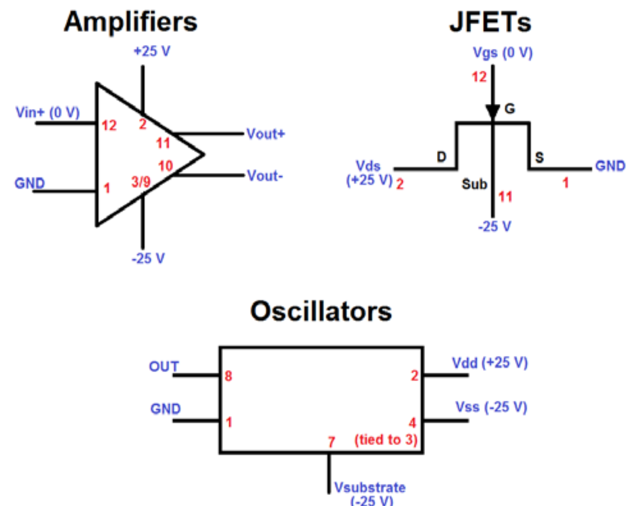

Fig. 2. Pinout block diagrams showing bias conditions during irradiation.

B. Heavy-Ion Testing

Heavy-ion test data were taken at Lawrence Berkeley National Laboratory (LBNL) in vacuum using the 10 MeV/amu tune. Test equipment was placed just outside the vacuum chamber and included the equipment used for TID testing, as well as a Fluke 271 function generator and a Tektronix MSO5204 oscilloscope (in place of the TDS3014). Equipment was controlled remotely by custom LabVIEW programs. Ions used during the testing are given in Table II. LET and range values were calculated using the SRIM code [12]. Ion flux remained below $2x10^5$ $cm^{-2}\cdot s^{-1}$, and fluence per run was typically $1x10^7$ cm^{-2}.

TABLE I
TOTAL IONIZING DOSE STEPS

Run # *reduced dose rate*	Cumulative Total Dose [krad(Si)]
1	100
2	200
3	300
4	500
5	1000
6*	2000
7	2500
8	3000
9*	4100
10	5000
11*	6171
12	7000

TABLE II
HEAVY ION BEAM PROPERTIES

Ion	Energy [MeV]	Range in Si/SiC [µm]	Surface LET in Si/SiC [MeV-cm2/mg]
Ne	216	175/126	3.5/3.4
Ar	400	130/89	9.7/10
Cu	659	108/74	21/22
Ag	1039	90/61	48/50
Xe	1232	90/61	59/62
Au	1956	106/72	86/90

1) JFET

JFETs were biased under maximum off-state stress, with V_{GS} = -10 V and V_{DS} = 40 V on the drain. The test circuit specified for discrete MOSFETs in MIL-STD 750, TM1080 [13], was adapted to these IC JFETs. During irradiation, the drain and gate currents were continuously monitored by the source meters and recorded. After each beam run, the drain current (I_D) as a function of V_{GS} was measured at V_{DS} = 20 V, and the shorted-gate drain current (I_{DSS}) was measured. Fluence for each beam run was increased to $1x10^8$ cm^{-2} due to the small transistor size.

2) Operational Amplifier

Each op amp DUT was configured as shown in Fig. 3. Jumpers enabled testing in a closed-loop unity gain configuration or in an open loop configuration. V_{DD} and V_{SS} were optimized for each op amp and were nominally 30 V and -20 V. The substrate voltage was tied to V_{SS}. Tests were conducted primarily in DC mode with inputs grounded; however, some runs were conducted with a 5 kHz, 1 V peak-peak sine wave signal on one input with the other grounded. The output was monitored by oscilloscope.

3) Clock Circuit

Each clock IC was configured as shown in Fig. 4. The “Select” pin controls the frequency of the clock circuit output: -10 V toggles a single D flip flop to output a divide-by-2 frequency; 0 V toggles two flip flops resulting in a divide-by-4 output. Test were performed with this select pin grounded (÷4 mode). A jumper at the “Clock In” node was left open to test the full clock circuit. Additional tests were conducted with this jumper closed and a 1 kHz square wave external clock signal supplied using a signal generator. In this configuration, the flip flops and control logic are isolated from the internal ring oscillator. For all tests, V_{DD} was 26 V and both the substrate voltage and V_{SS} were held at -26 V.

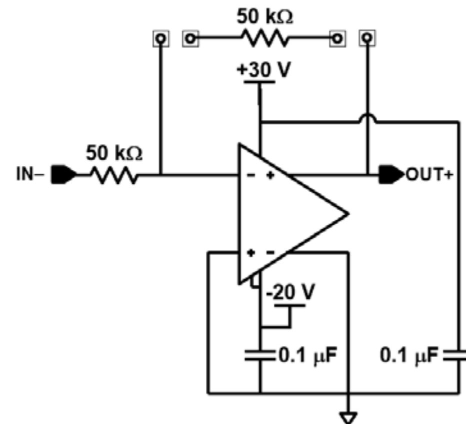

Fig. 3. Circuit configuration for SEE testing of op amps.

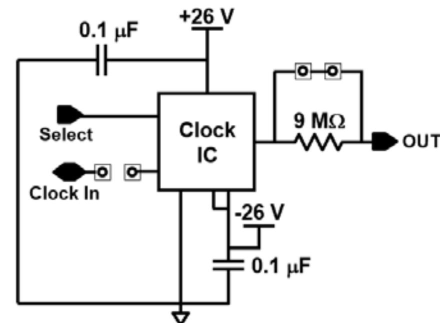

Fig. 4. Circuit configuration for SEE testing of clock circuit.

4) Ring Oscillator

The ring oscillator test circuit is shown in Fig. 5. During testing, the output jumper was shorted, bypassing the output resistor. V_{DD} was 26 V and both the substrate voltage and V_{SS} were held at -26 V.

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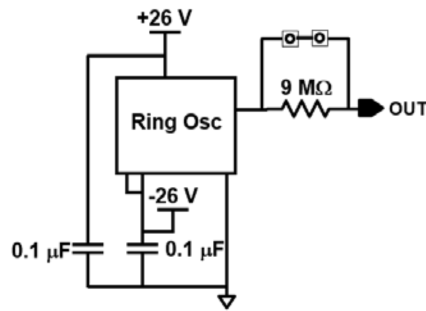

Fig. 5. Circuit configuration for SEE testing of ring oscillator.

5) Flip Flop

Individual D flip flops were configured as in Fig. 6. During testing, a divide-by-2 mode was used whereby a 1 kHz 0 V to -10 V square wave signal was applied to the "Clock In" pin and the Q-bar output was fed to the D input pin. Both Set-bar and Reset-bar pins were tied to ground; V_{DD} was 26 V and both the substrate voltage and V_{SS} were held at -26 V. The Q output was monitored by oscilloscope.

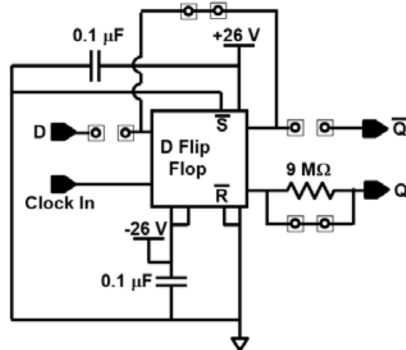

Fig. 6. Circuit configuration for SEE testing of D flip flop.

IV. Results

A. JFET

1) Heavy-ion tests

JFET DUTs were irradiated with Ag, Xe, and Au ions at normal incidence. No destructive events occurred.

2) Total ionizing dose tests

Overall, the change in JFET performance as a function of total dose was minimal. The change in I_{DSS} was within ±1.5% of the initial values, with a general trend toward increasing values. Transconductance remained unchanged. Pinch-off voltage (V_p) showed a small increase with dose, but the change remained within 2%. Most of the increase in V_p occurred below 1 Mrad(Si). The most notable change with dose occurred in the subthreshold region of the I_D vs. V_{GS} curves, where a subthreshold "hump" developed (Fig. 7). After remaining unbiased for two weeks, the subthreshold "hump" diminished or disappeared, re-emerging in subsequent measurements of the irradiated devices after the JFETs remained under bias.

B. Operational Amplifier

1) Heavy-ion tests

Irradiation with Au ions did not result in any destructive events. No changes to the power supply currents were observed. Single-event transients (SETs) were observed, but were negative-going and typically only a few nanoseconds and tens of millivolts in size when irradiated with Ar, Cu, and Ag. Under irradiation with Au, a large, positive-going 400 mV, 150 µs transient was recorded.

2) Total ionizing dose tests

The gain of the op amps generally decreased with dose. The variability in the gain of the test parts remained within 21% of the initial values, whereas the variability of the control part remained within 1% of the initial value. Annealing at room temperature (2 weeks unbiased during shipping to GRC; 1 week biased at GRC) had little impact. The offset voltage of the irradiated DUTs remained within 9% of the initial value. The initial performance of the pristine op amps showed substantial part-part variability. The poorer performing op amps suffered greater degradation with dose (Fig. 8 vs. Fig. 9, for example).

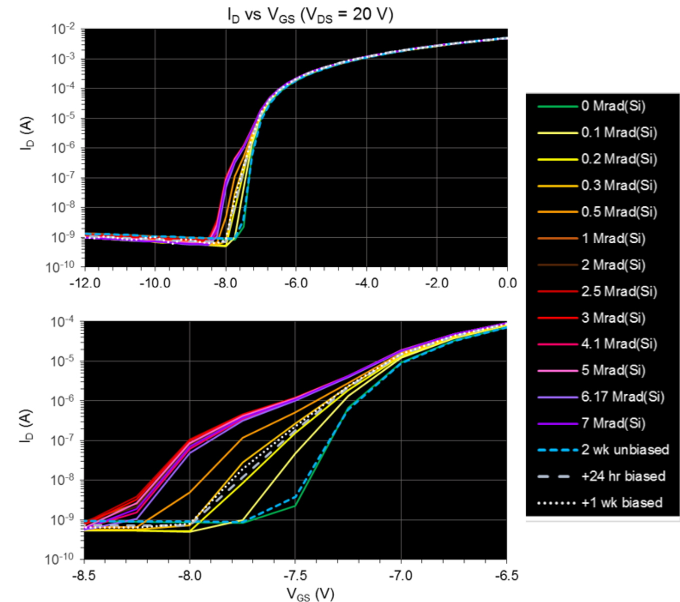

Fig. 7. Typical JFET I_D vs. V_{GS} curve as a function of dose (V_{DS} = 20 V). Subthreshold region replotted in lower panel. Broken lines are after 2 weeks unbiased anneal, and subsequent 24 hour and 1 week biased anneals.

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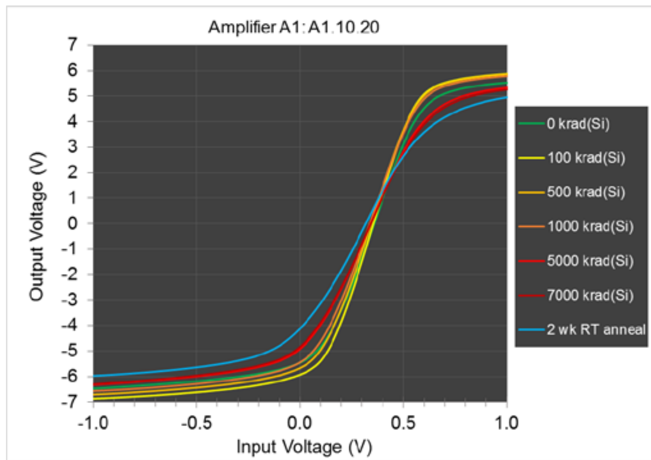

Fig. 8. Op amp DUT "A1" output vs. input voltage at select dose steps. Green line = pre-rad measurement; blue line = after 2-week unbiased anneal.

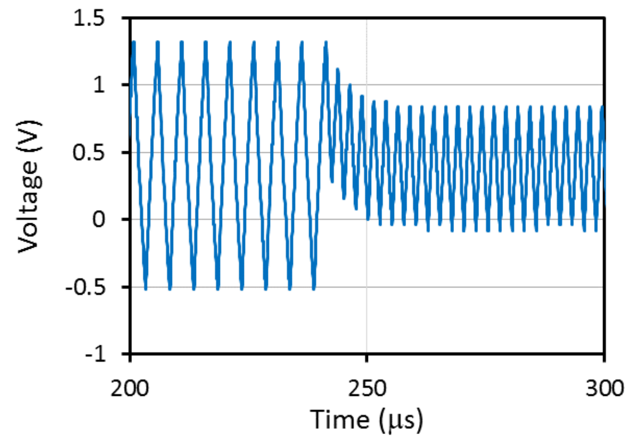

Fig. 10. Example SEU in clock circuit under Cu irradiation. Output changes from ÷4 to ÷2 clock.

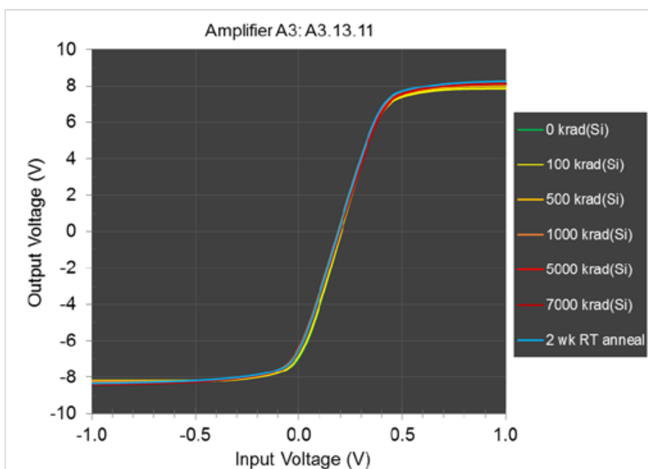

Fig. 9. Op amp DUT "A3" output vs. input voltage at various dose steps.

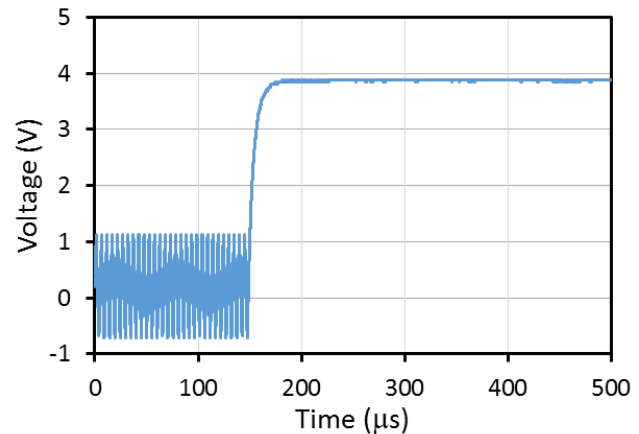

Fig. 11. Example SET in clock circuit under Cu irradiation. Output changes from a ÷4 clock to a higher DC voltage.

C. Clock Circuit

Irradiation with Au ions did not result in any destructive events. Clock frequency was set to divide by 4 for all runs. Single-event upsets (SEUs) or transients (SETs) occurred in which the clock frequency toggled to divide by 2 (Fig. 10), or else maintained a high constant voltage for beyond the oscilloscope window of a few hundred µs (Fig. 11). This elevated steady voltage would then return the baseline divide-by-4 state (Fig. 12). No upsets were recorded under Ne (LET(Si) = 3.5 MeV·cm^2/mg), but were found with Ar (LET(Si) = 9.7 MeV·cm^2/mg) and heavier ions.

Application of an external square-wave clock to bypass the internal ring oscillator resulted in similar upsets and transients. (Figs. 13-14).

D. Flip Flop

Individual D flip flops were irradiated with Au ions under the configuration shown in Fig. 6. No SEUs or SETs were measured, suggesting that the upsets and transients occurring in the clock circuit result from events in the control logic.

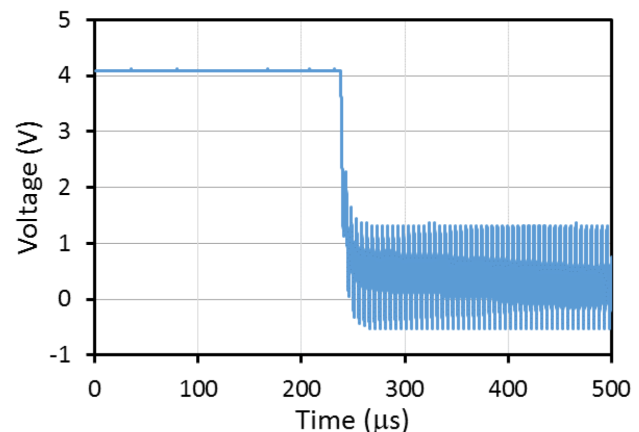

Fig. 12. Example SET in clock circuit under Au irradiation. SET is captured as the output changes back from a high DC voltage to a ÷4 clock.

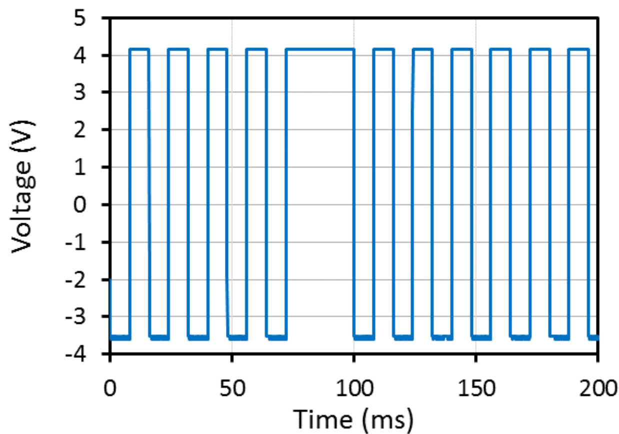

Fig. 13. Example of SET in clock circuit with external clock applied. Output signal remains high for an additional clock cycle during irradiation with Ar.

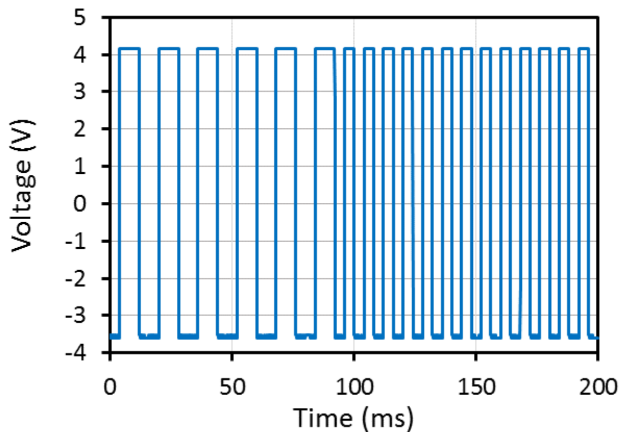

Fig. 14. Example SEU in clock circuit with external clock applied. Output signal toggles from ÷4 to ÷2 clock during irradiation with Ar.

V. Summary

In this work, prototype 4H-SiC JFET ICs developed at NASA GRC for harsh environmental conditions were evaluated for total ionizing dose tolerance and heavy-ion SEE susceptibility. The devices tested demonstrated over 7 Mrad(Si) TID tolerance and no destructive SEE susceptibility at the maximum test LET(Si) of 86 MeV-cm^2/mg. SEUs and SETs occurred in the clock circuit; onset LET(Si) was between 3.5 MeV-cm^2/mg and 9.6 MeV-cm^2/mg.

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References

[1] National Research Council, *Vision and Voyages for Planetary Science in the Decade 2013-2022*. Washington, DC: The National Academies Press, 2011.

[2] I. Jun and H. B. Garrett, "Comparison of high-energy trapped particle environments at the earth and jupiter," *Radiation Protection Dosimetry,* vol. 116, pp. 50-54, 2005.

[3] A. T. Basilevsky and J. W. Head, "The surface of Venus," *Reports on Progress in Physics,* vol. 66, pp. 1699-1734, 2003/09/10 2003.

[4] M. Steffens, S. K. Höffgen, and M. Poizat, "Total ionizing dose tests of Power Bipolar Transistors and SiC power devices for JUICE," in *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2017, pp. 1-5.

[5] S. S. Suvanam, S. Kuroki, L. Lanni, R. Hadayati, T. Ohshima, T. Makino, *et al.*, "High Gamma Ray Tolerance for 4H-SiC Bipolar Circuits," *IEEE Transactions on Nuclear Science,* vol. 64, pp. 852-858, 2017.

[6] P. G. Neudeck, D. J. Spry, M. J. Krasowski, N. F. Prokop, G. M. Beheim, L.-Y. Chen*, et al.*, "Yearlong 500 °C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT),* vol. 2018, pp. 000071-000078, 2018.

[7] D. J. Spry, P. G. Neudeck, D. Lukco, L. Y. Chen, M. J. Krasowski, N. F. Prokop*, et al.*, "Prolonged 500°C Operation of 100+ Transistor Silicon Carbide Integrated Circuits," *Materials Science Forum,* vol. 924, pp. 949-952, 2018.

[8] P. G. Neudeck, L. Chen, R. D. Meredith, D. Lukco, D. J. Spry, L. M. Nakley*, et al.*, "Operational Testing of 4H-SiC JFET ICs for 60 Days Directly Exposed to Venus Surface Atmospheric Conditions," *IEEE Journal of the Electron Devices Society,* vol. 7, pp. 100-110, 2019.

[9] D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim*, et al.*, "Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT),* vol. 2016, pp. 000249-000256, 2016.

[10] P. G. Neudeck, D. J. Spry, M. J. Krasowski, N. F. Prokop, G. M. Beheim, L.-Y. Chen*, et al.*, "Year-long 500°C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits," *Journal of Microelectronics and Electronic Packaging,* vol. 15, pp. 163-170, 2018.

[11] D. J. Spry, P. G. Neudeck, L. Chen, D. Lukco, C. W. Chang, and G. M. Beheim, "Prolonged 500 °C Demonstration of 4H-SiC JFET ICs With Two-Level Interconnect," *IEEE Electron Device Letters,* vol. 37, pp. 625-628, 2016.

[12] J. F. Ziegler and J. P. Biersack. *The Stopping and Range of Ions in Matter*. Available: http://www.srim.org

[13] MIL-STD-750-1A, "Test Methods for Semiconductor Devices," ed: United States Department of Defense, Aug, 2016.