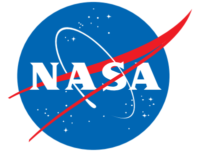


Experimental Study on Mitigation of Lifetime-Limiting Dielectric Cracking in Extreme Temperature 4H-SiC JFET Integrated Circuits

D. J. Spry[1], P. G. Neudeck[1], and C. W. Chang[2]

1 NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

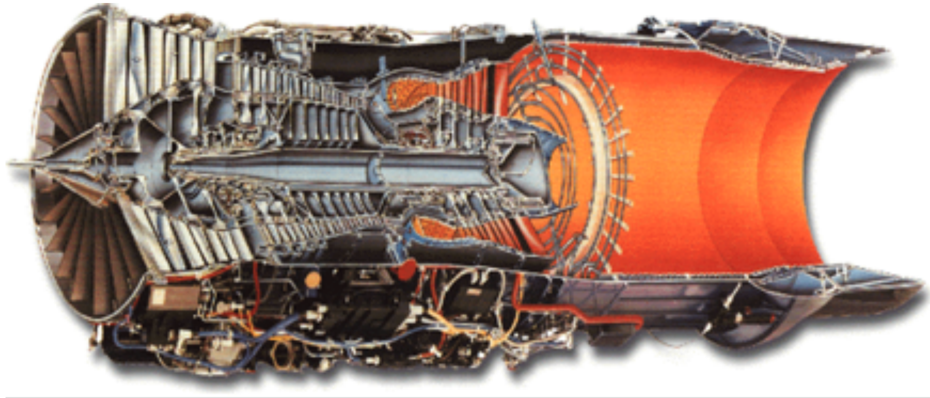
2 Vantage Partners LLC, NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

E-mail: David.J.Spry@nasa.gov

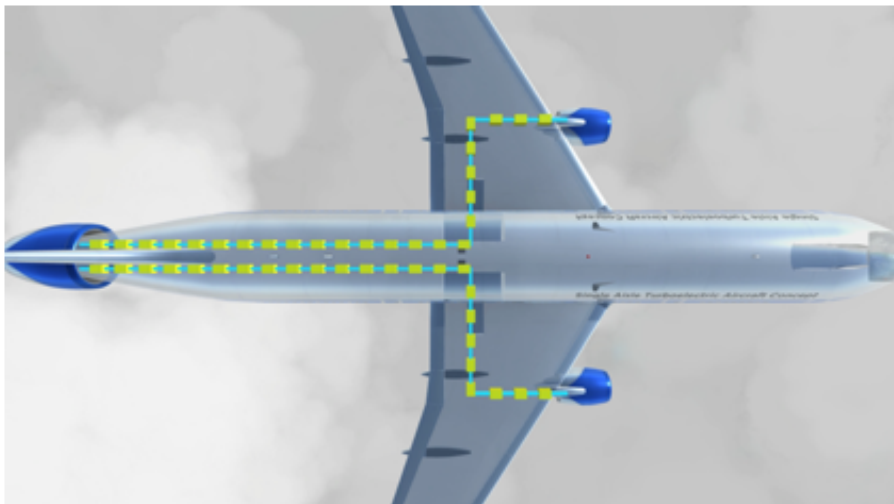
SiC Electronics Benefits to NASA Missions

Aeronautics Research Mission Directorate ARMD

Intelligent Propulsion Systems

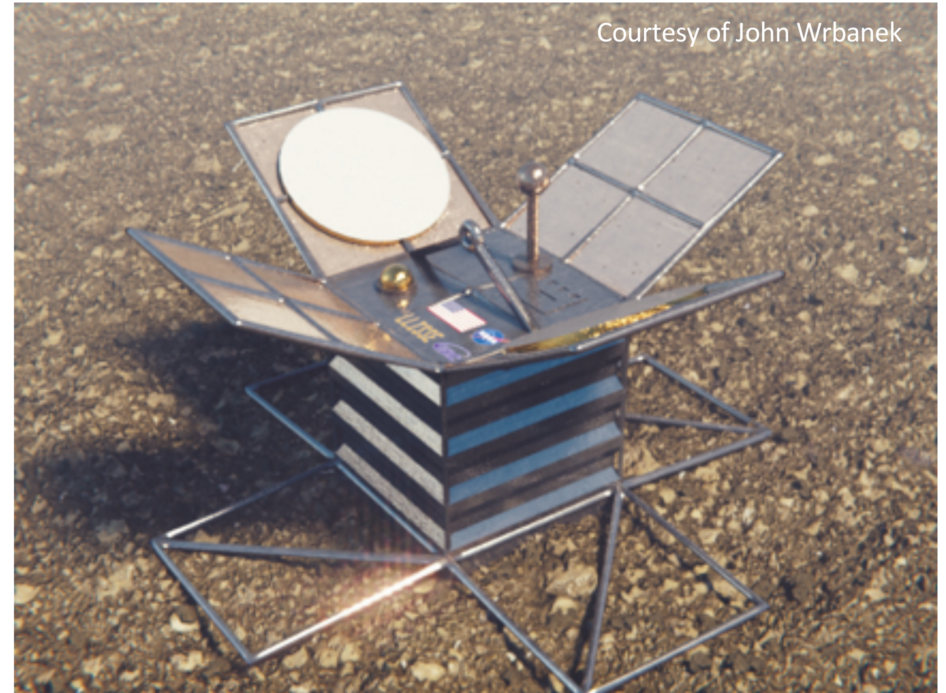


Hybrid Electric & Turbo Electric Aircraft



Space Mission Directorate SMD Venus Surface Exploration

LLISSE = Long-Life In-Situ Solar System Explorer[1]

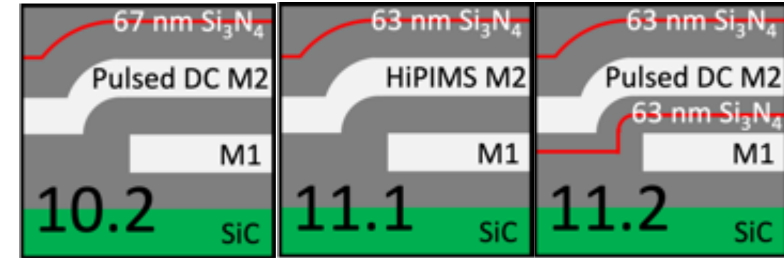


9.4 Mpa = 92.7 times Earth pressure
460 °C + chemical composition found at the surface of Venus (CO_2, N_2, SO_2, H_20, CO, OCS, HCl, HF, and H_2S)

[1]T. Kremic, et al., 48th Lunar and Planetary Science, 2017, 2986.

JFET IC Wafer 10.2 vs 11.1 vs 11.2 Process

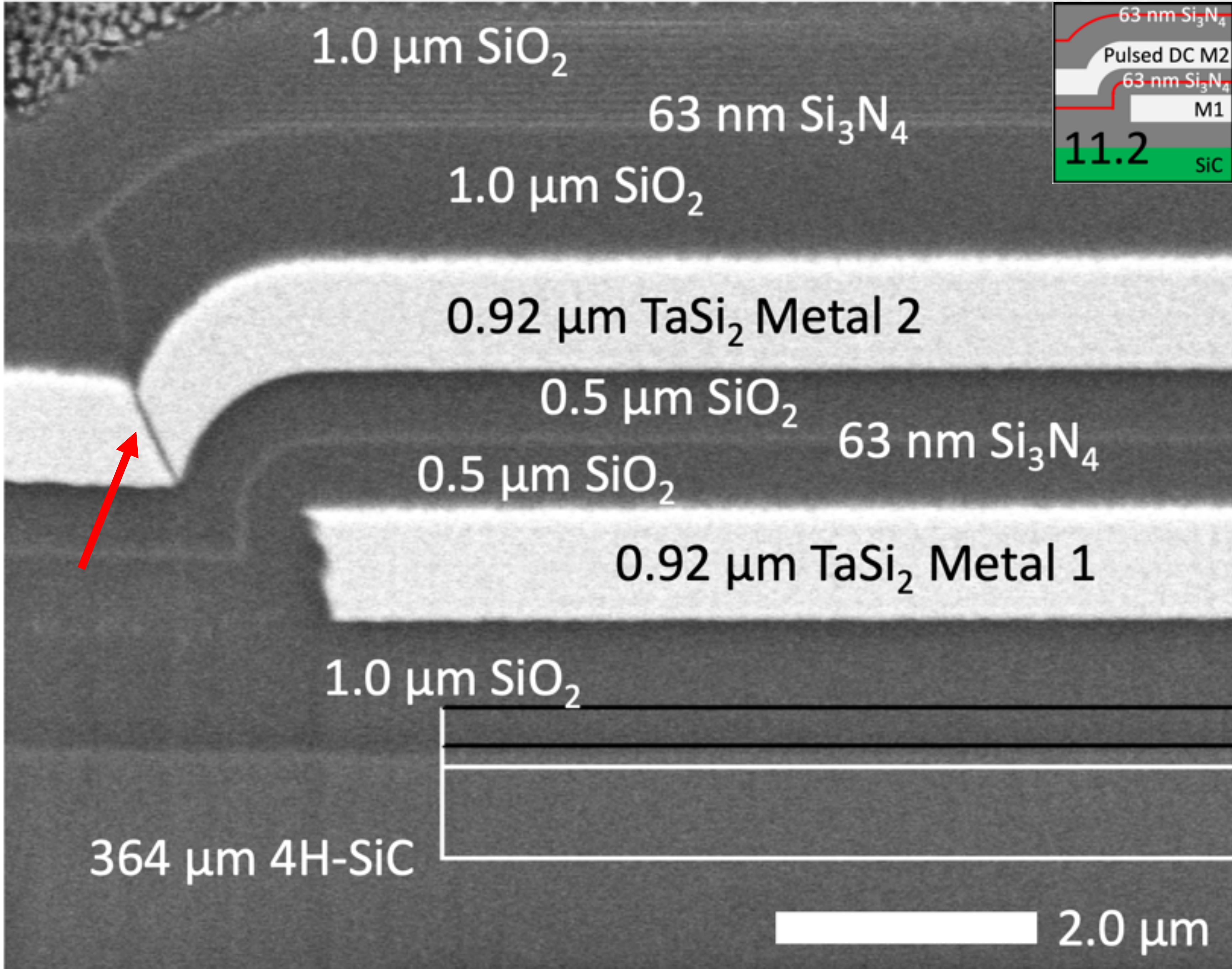
- 10.2 - Pulsed-DC $TaSi_2$ and 1 Si_3N_4 layer above Metal 2
- 11.1 - HiPIMS $TaSi_2$ and 1 Si_3N_4 layer above Metal 2
- 11.2 - Pulsed-DC $TaSi_2$ & Two Si_3N_4 layers
  - -above Metal 2
  - -between Metal 1 and Metal 2



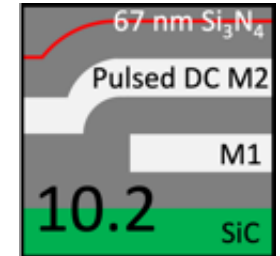
4H-SiC n-mesa
1 µm SiO_2
67 nm Si_3N_4
1 µm SiO_2
0.8 µm $TaSi_2$ Metal 2
1 µm SiO_2
50 nm Ti + 0.2 µm $TaSi_2$ + Metal 1
p+ Gate > 10^{20} cm^{-3}
0.8 µm $TaSi_2$ Metal 1
1 µm SiO_2
~ 0.4 µm 1 x 10^{17} cm^{-3}
Al Field Implant
6.8 x 10^{11} cm^{-2}
Phosphorous Contact
Implant 1.78 x 10^{15} cm^{-2}
Nitrogen Self-Aligned
Implant 7 x 10^{12} cm^{-2}
10 µm
6-8 µm p-type < 5 x 10^{15} cm^{-3} on p-type 4H-SiC
67 nm Si_3N_4
Pulsed DC M2
M1
10.2
SiC

SiO_2 deposited at 720 °C by LPCVD using TEOS and 63nm stoichiometric Si_3N_4 deposited also at 720 °C by LPCVD using DCS and NH_3.

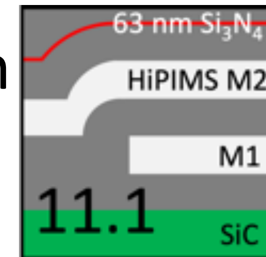
JFET IC Wafer 11.2 -Metal 2 Crack

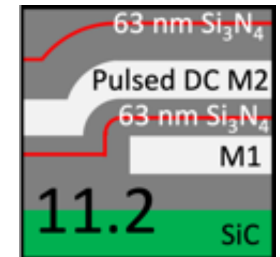


JFET IC Wafer 10.2 vs 11.1 vs 11.2 Layout

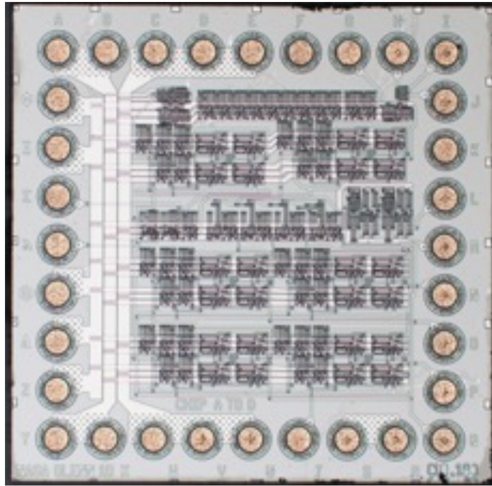


- 10.2
  - 3 X 3 mm, active area 2 X 2 mm,
  - 6 µm gate & resistors, 175 transistors
  - >10,000 hours at 500 °C in air ambient
  - 9 die versions
  - Die tested in the report
    - **Chip 1 A to D**
    - **Chip 3 Clock IC ÷2 ÷ 4** (some non-working)
- 11.1 & 11.2
  - 4.65 X 4.65mm, active area 3.55 X 3.55 mm
  - 6 µm gate, 3 µm resistors, 348 transistors
    - most complex ~1000 transistors
  - 19 die versions
  - Die tested in this report
    - **Chip 7 Shift Registers** (non-working)
    - **Chip 13B LLISSE RF Transmitter & Ring Oscillators**

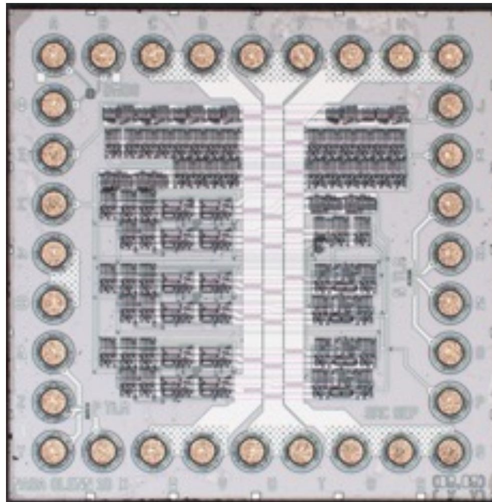


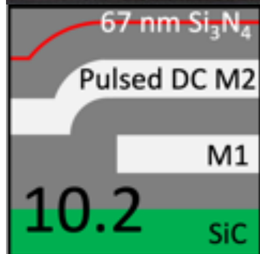


10 cycles 10 hrs. at 500 °C Pre-Test Images

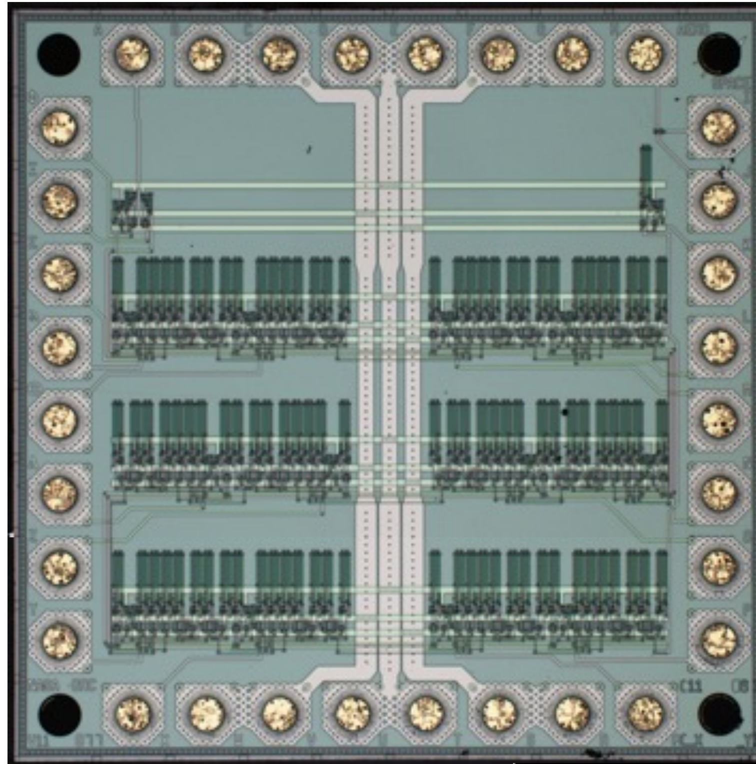


Chip 1 A to D

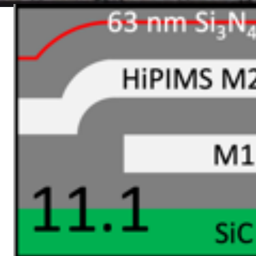


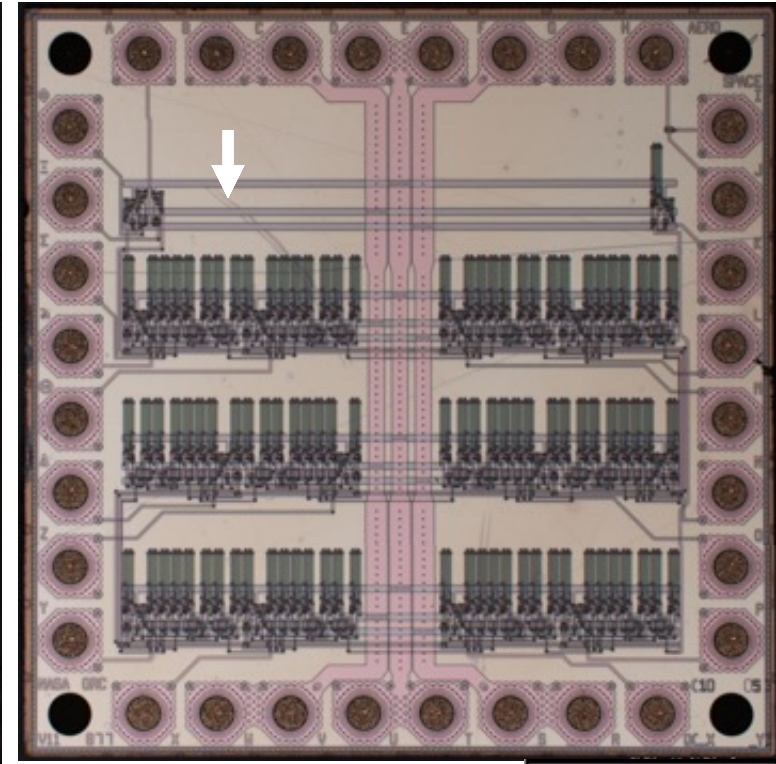


Chip 3 Clock

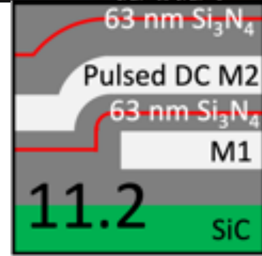


Shift Register



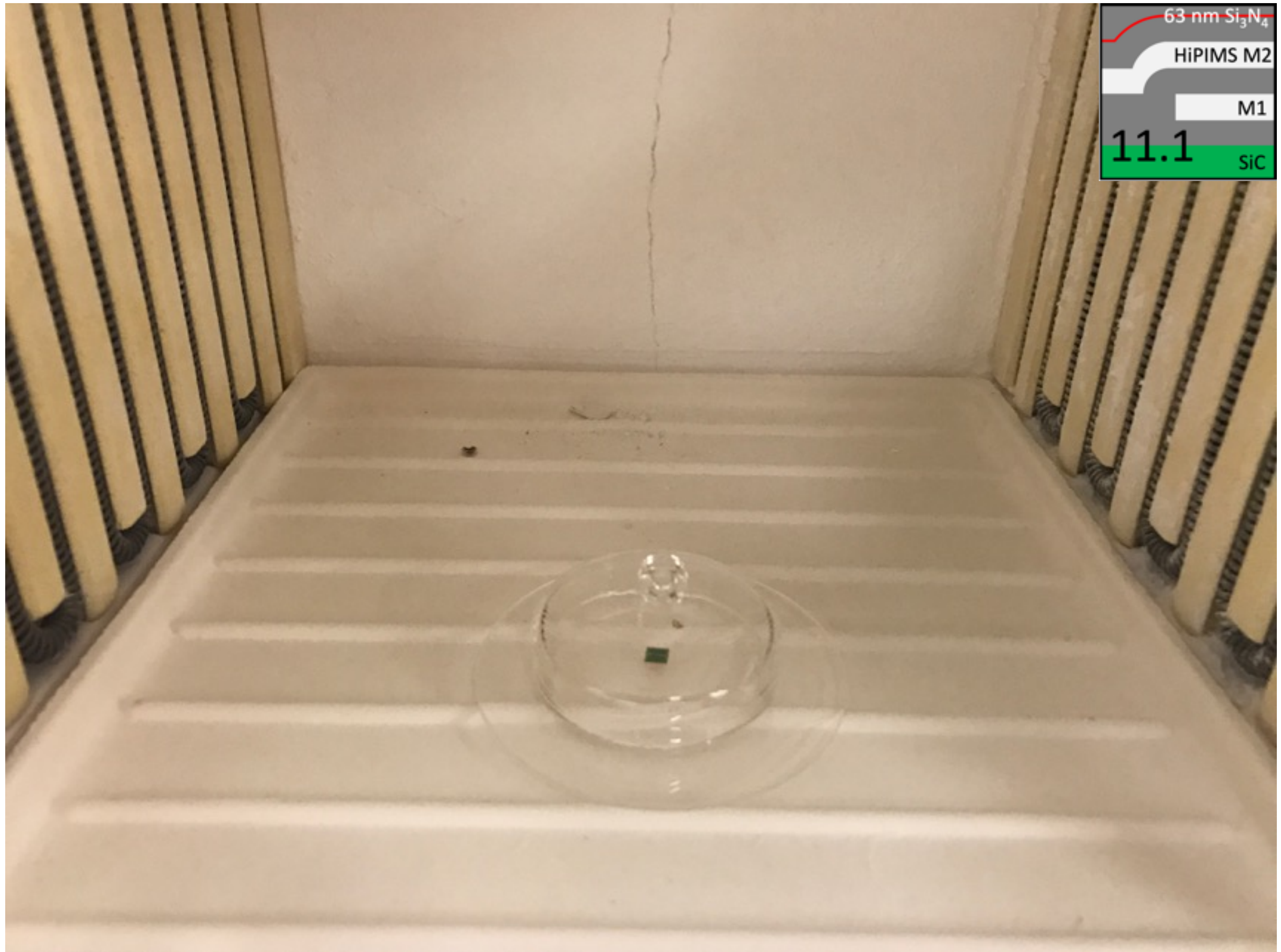


Shift Register

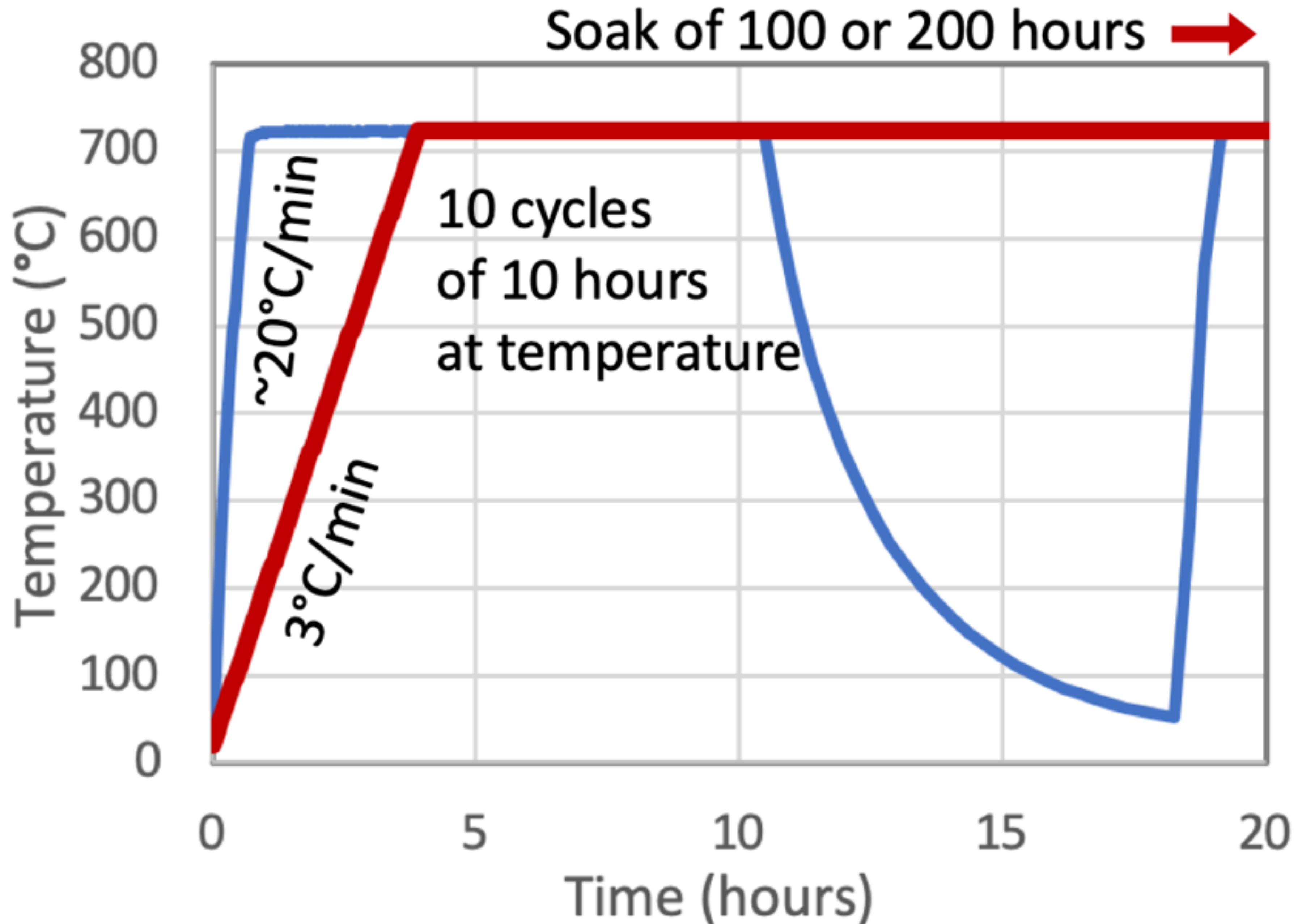


1 mm

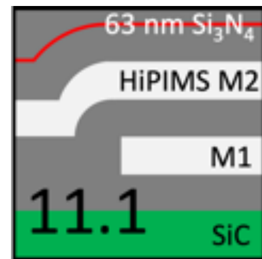
Unpackaged, Quartz, in Air Ambient Ovens



10 cycles 10 hrs. / 100hrs. / 200hrs.
500, 600, 720, and 800 °C



Graded Results of Thermal Testing

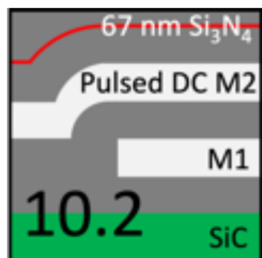


Version 10.2 C1 Anolog to Digital	500 °C	600 °C	720 °C	800 °C
100 hours	1	1	3	3
200 hours	1	2	3	3
10-10hr cycle	1	2	3	

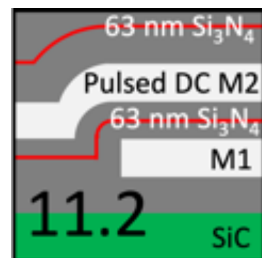
Version 11.1 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	1	3	3	3
200 hours	3	3	3	3
10-10hr cycle	2	3	3	

Version 10.2 C3 Clock ÷2 ÷4	500 °C	600 °C	720 °C	800 °C
100 hours	1	0	3	0
200 hours	2	2	3	3
10-10hr cycle	1	2	3	

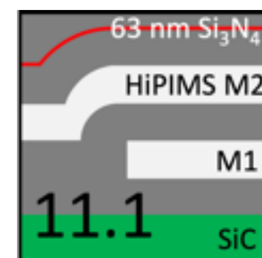
Version 11.2 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	0	0	0	1
200 hours	0	2	0	3
10-10hr cycle	0	0	0	



Grade	Score	Description
Good	0	No cracks
Problem	1	TaSi2 not dicolored
Fail	2	TaSi2 very discolored
Ugly	3	Dieletric pealed



Closer look at 10-10hr cycle 500 °C

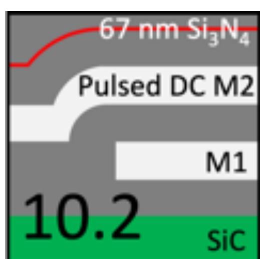


Version 10.2 C1 Anolog to Digital	500 °C	600 °C	720 °C	800 °C
100 hours	1	1	3	3
200 hours	1	2	3	3
10-10hr cycle	**1**	2	3	

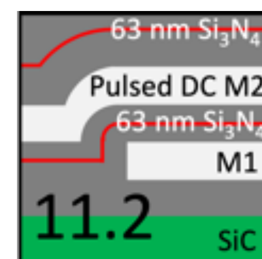
Version 11.1 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	1	3	3	3
200 hours	3	3	3	3
10-10hr cycle	**2**	3	3	

Version 10.2 C3 Clock ÷2 ÷4	500 °C	600 °C	720 °C	800 °C
100 hours	1	0	3	0
200 hours	2	2	3	3
10-10hr cycle	**1**	2	3	

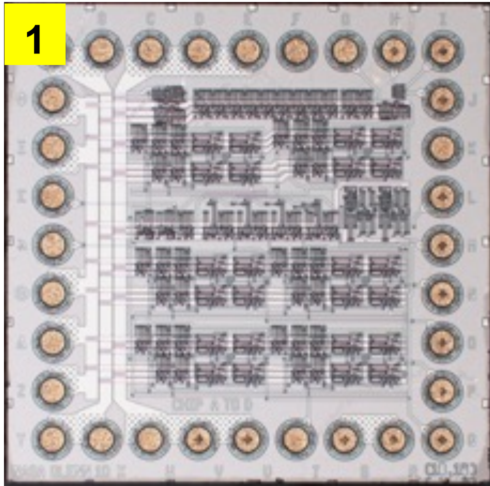
Version 11.2 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	0	0	0	1
200 hours	0	2	0	3
10-10hr cycle	**0**	0	0	



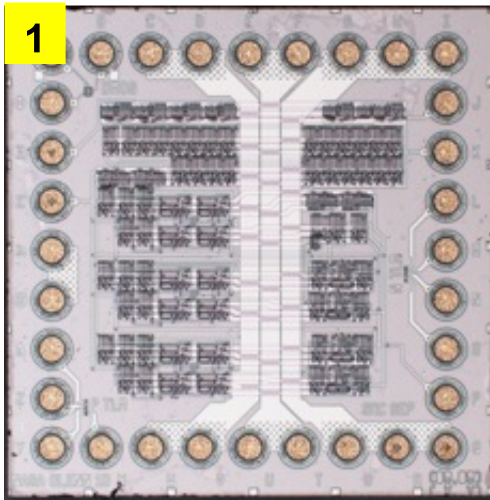
Good	0	No cracks
Problem	1	TaSi2 not dicolored
Fail	2	TaSi2 very discolored
Ugly	3	Dieletric pealed

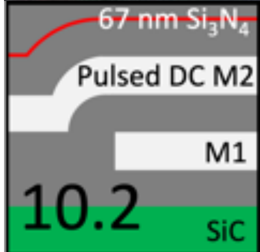


10 cycles 10 hrs. at 500 °C Post-Test Images

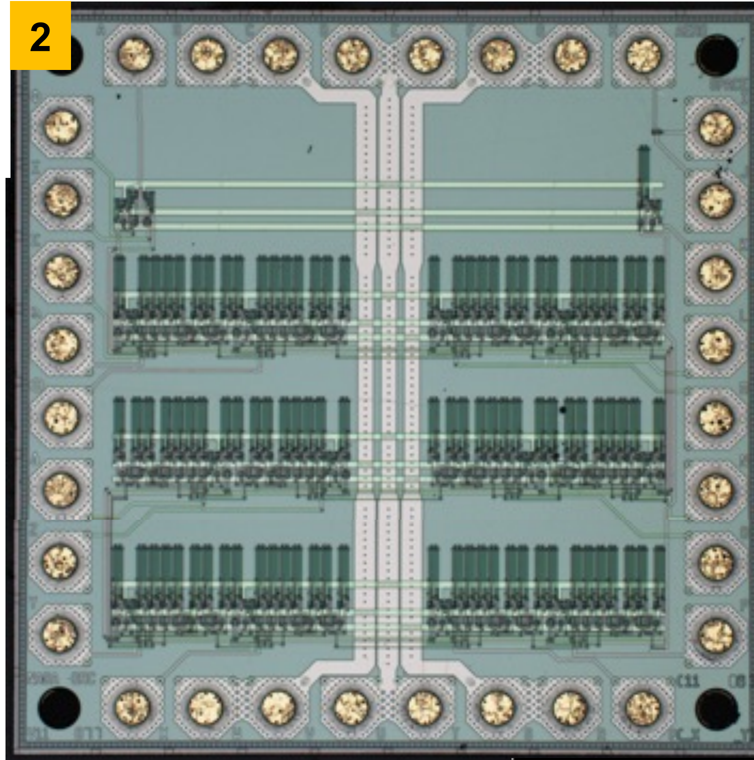


Chip 1 A to D

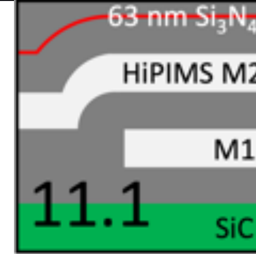


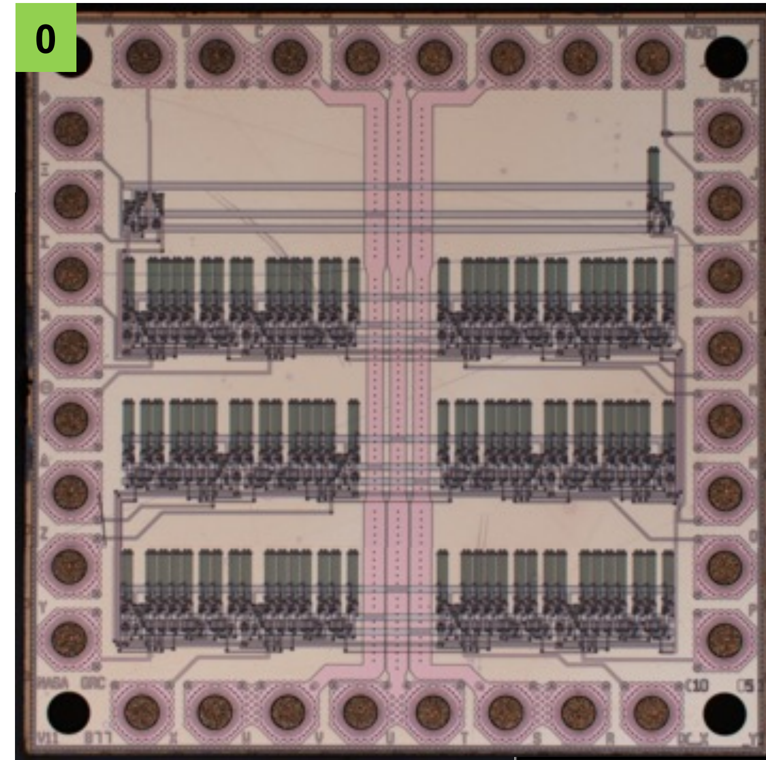


Chip 3 Clock

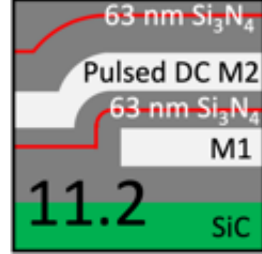


Shift Register



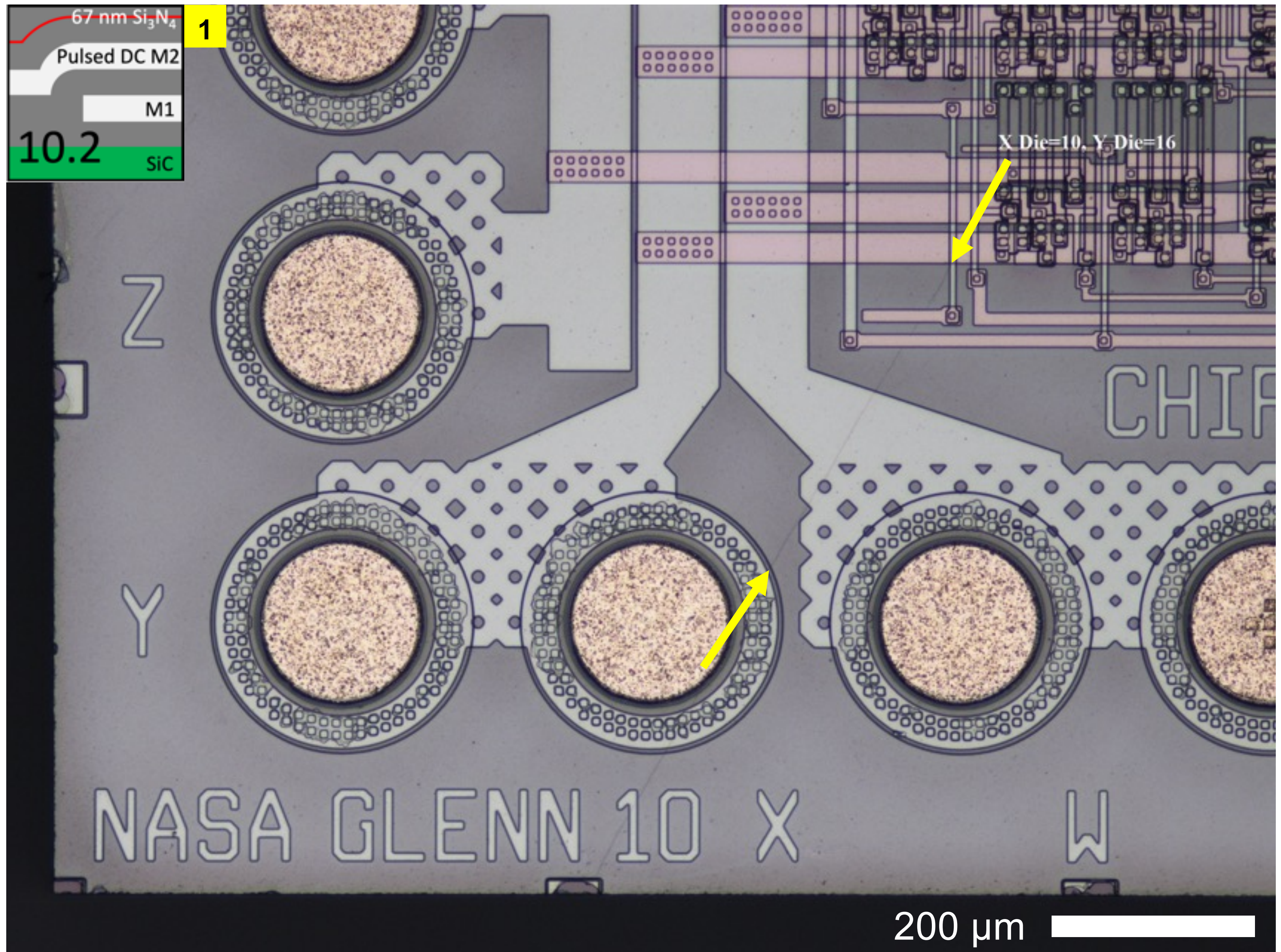


Shift Register

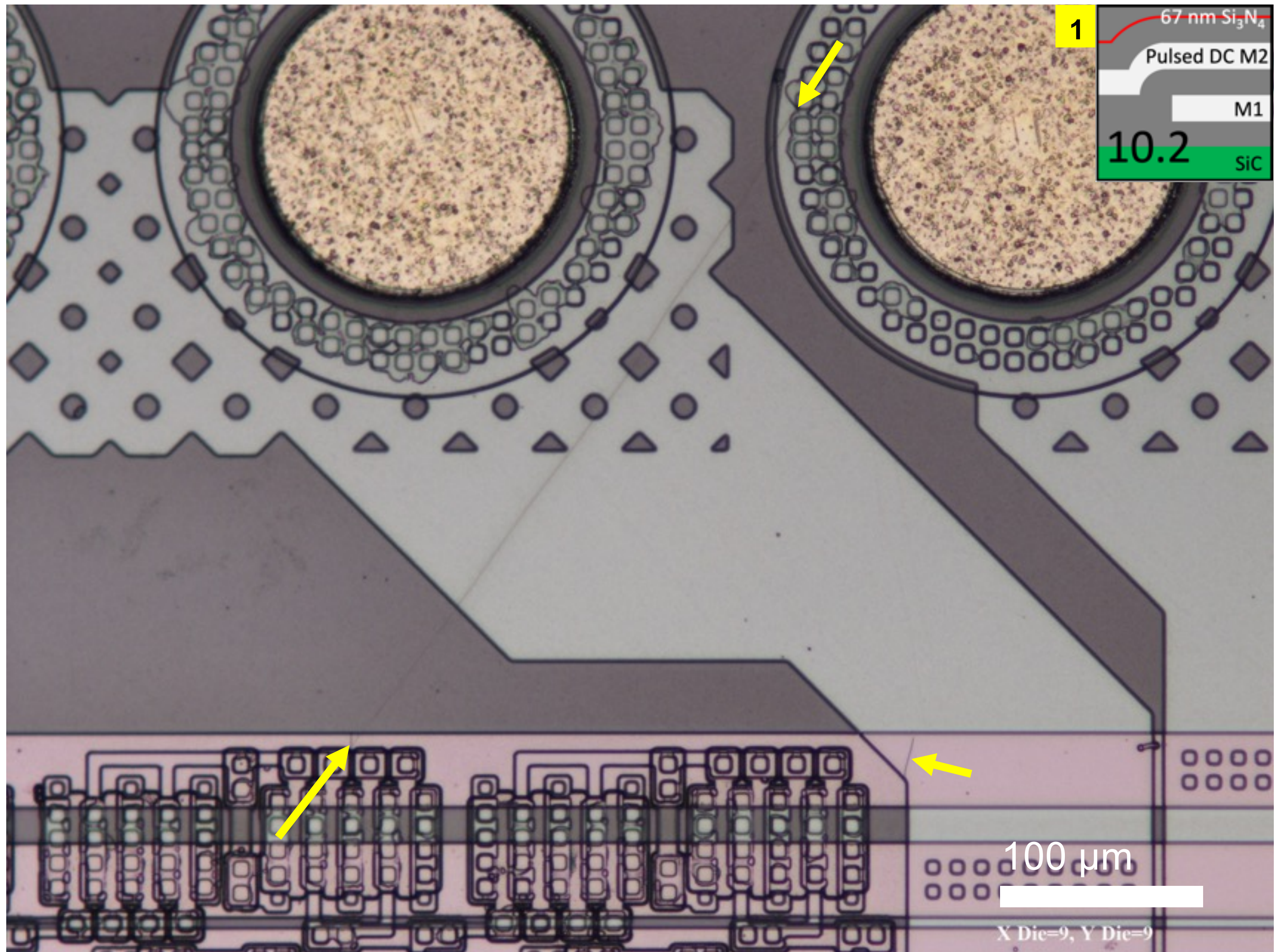


1 mm

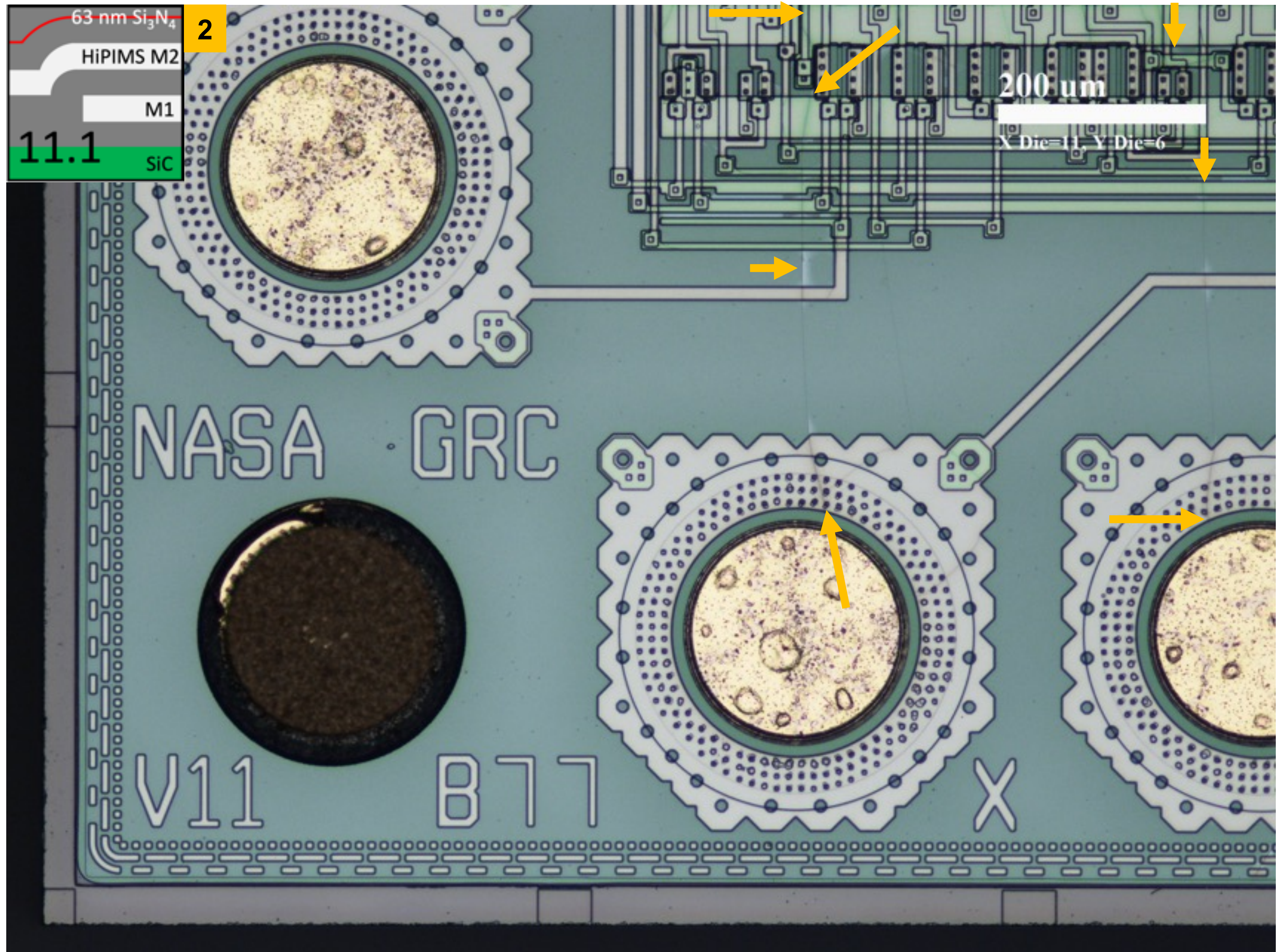
10 cycles 10 hrs. at 500 °C 10.2 Chip 1



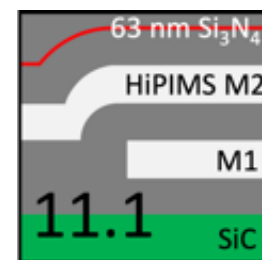
10 cycles 10 hrs. at 500 °C 10.2 Chip 3



10 cycles 10 hrs. at 500 °C 11.1 Chip 7



Closer look at 10-10hr cycle 720 °C

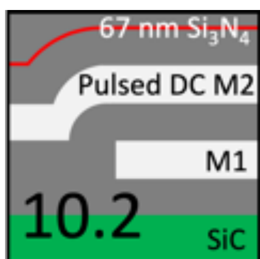


Version 10.2 C1 Anolog to Digital	500 °C	600 °C	720 °C	800 °C
100 hours	1	1	3	3
200 hours	1	2	3	3
10-10hr cycle	1	2	3	

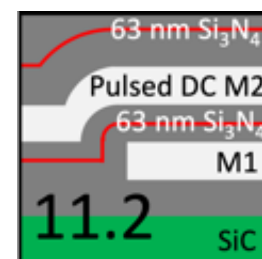
Version 11.1 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	1	3	3	3
200 hours	3	3	3	3
10-10hr cycle	2	3	3	

Version 10.2 C3 Clock ÷2 ÷4	500 °C	600 °C	720 °C	800 °C
100 hours	1	0	3	0
200 hours	2	2	3	3
10-10hr cycle	1	2	3	

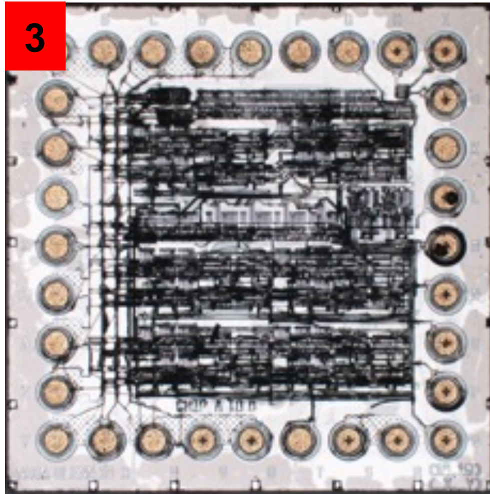
Version 11.2 C7 Shift Register	500 °C	600 °C	720 °C	800 °C
100 hours	0	0	0	1
200 hours	0	2	0	3
10-10hr cycle	0	0	0	



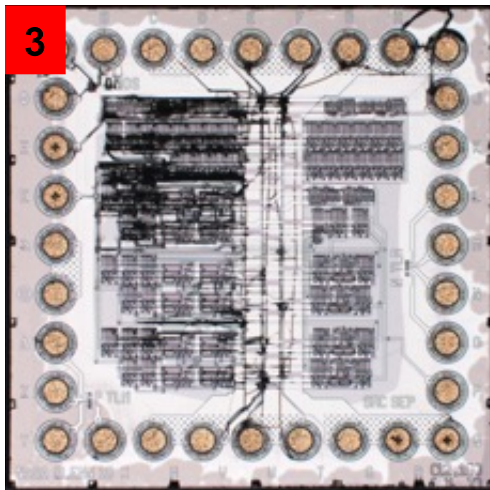
Good	0	No cracks
Problem	1	TaSi2 not dicolored
Fail	2	TaSi2 very discolored
Ugly	3	Dieletric pealed

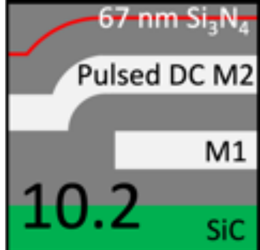


10 cycles 10 hrs. at 720 °C Post-Test Images

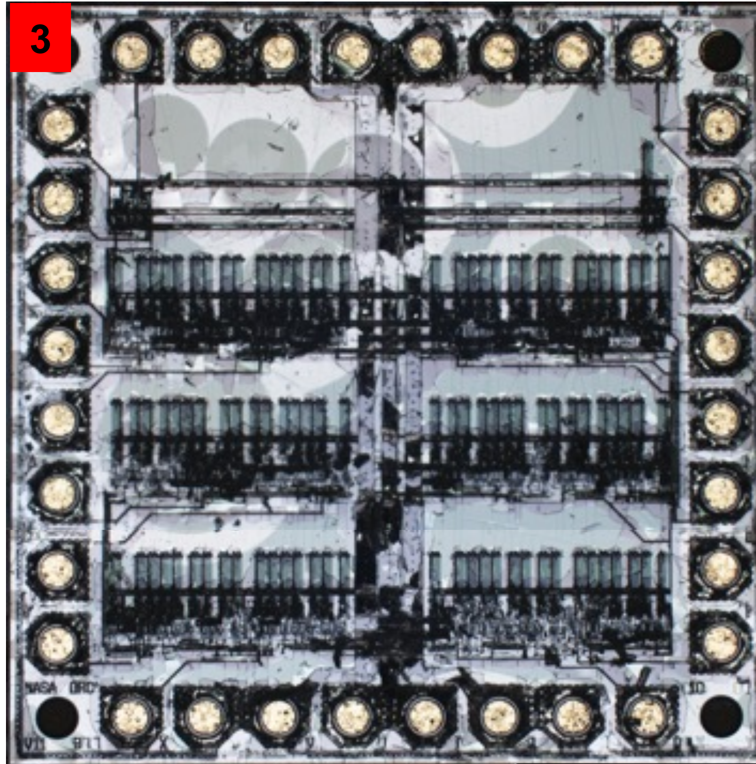


Chip 1 A to D

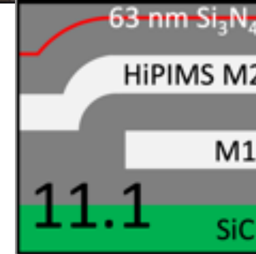


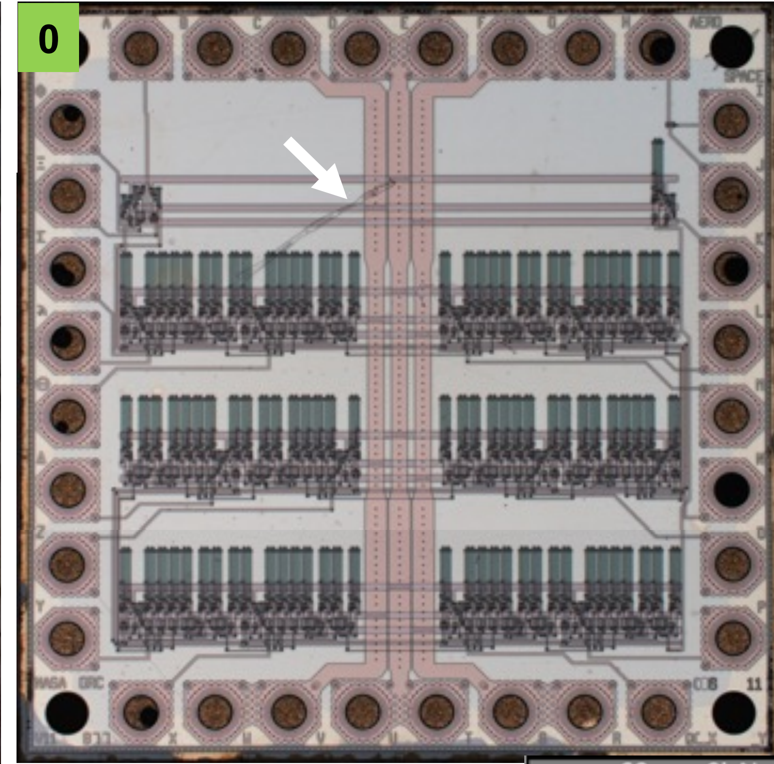


Chip 3 Clock

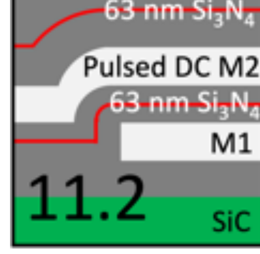


Shift Register



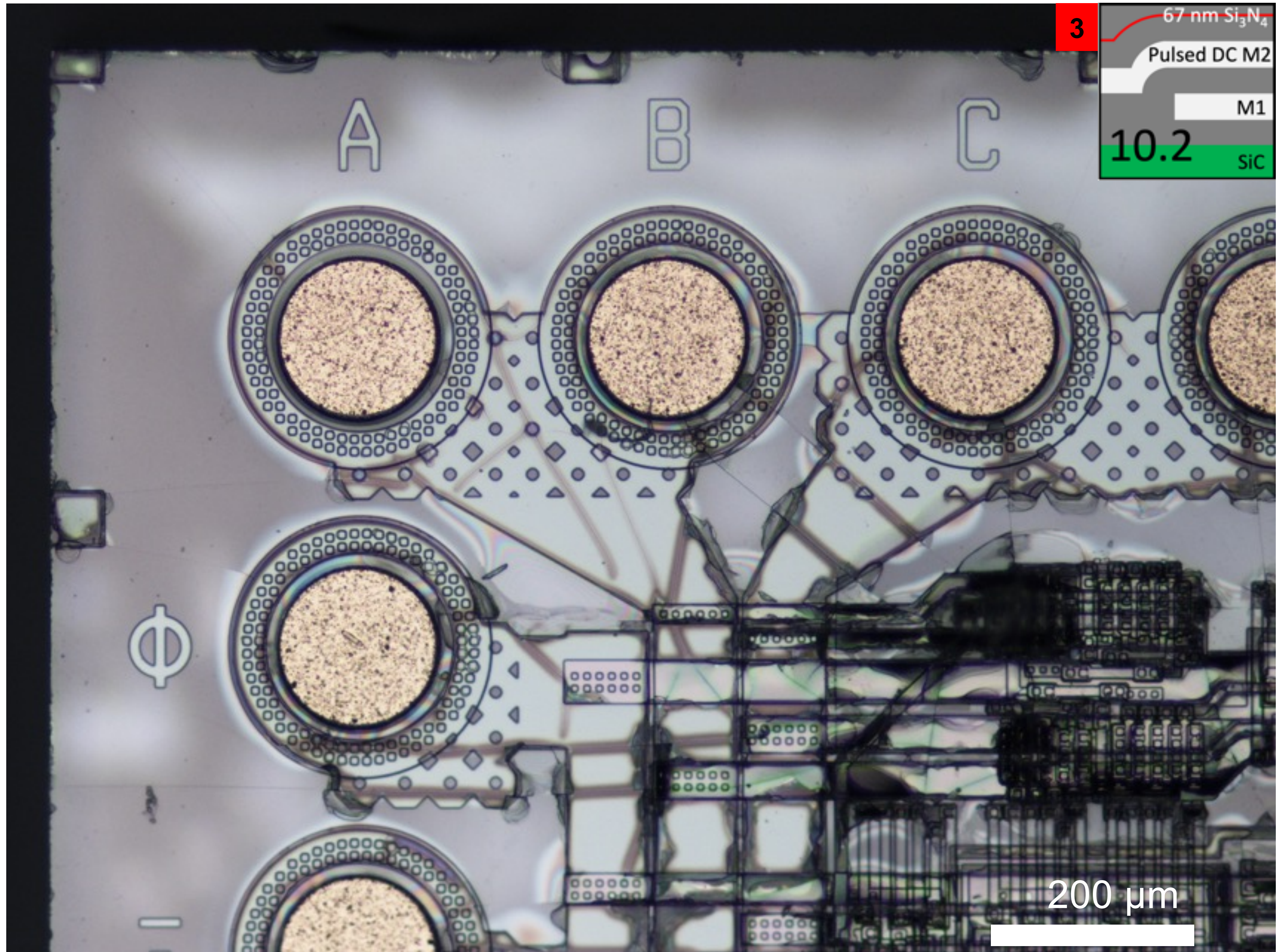


Shift Register

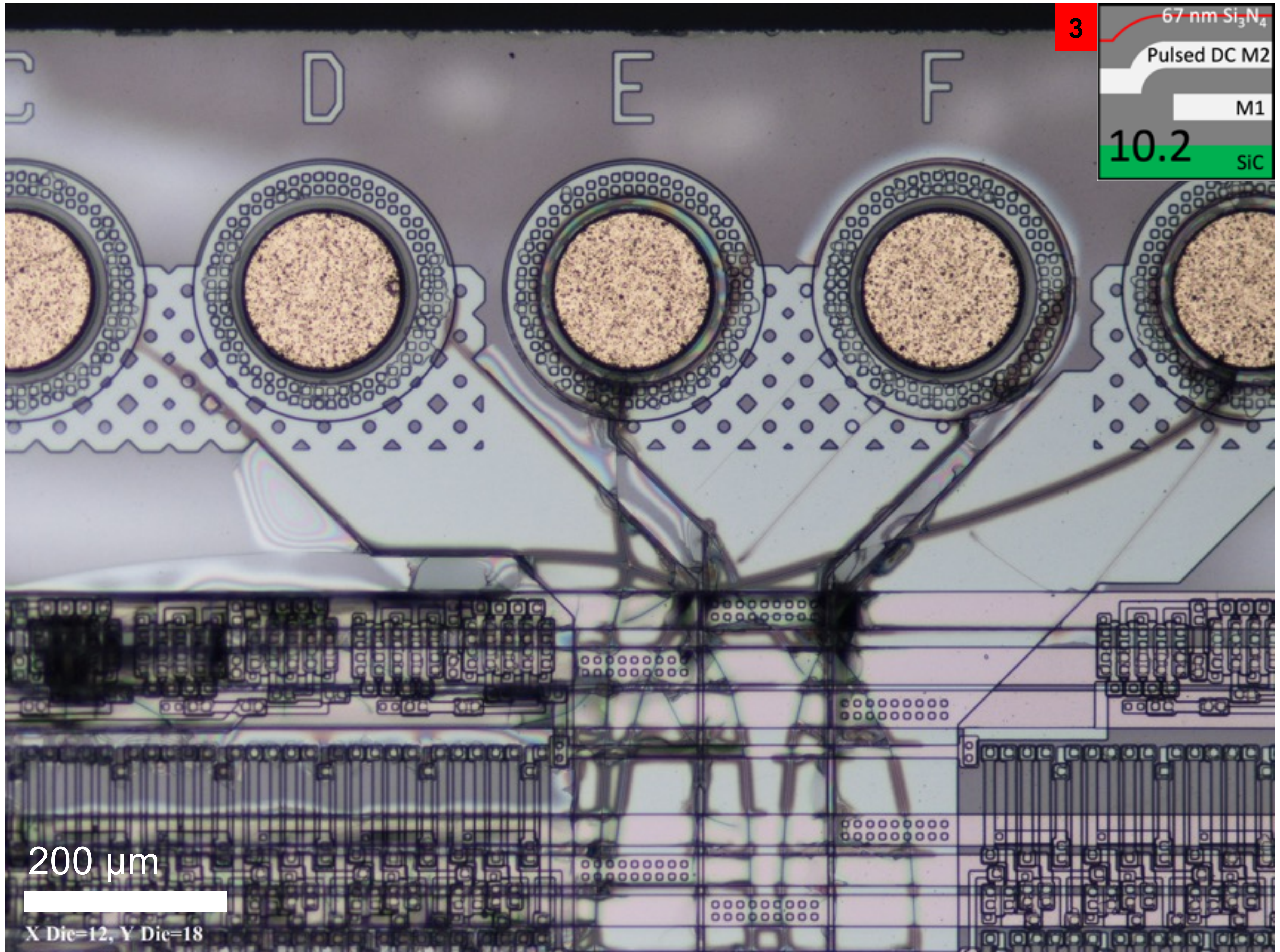


1 mm

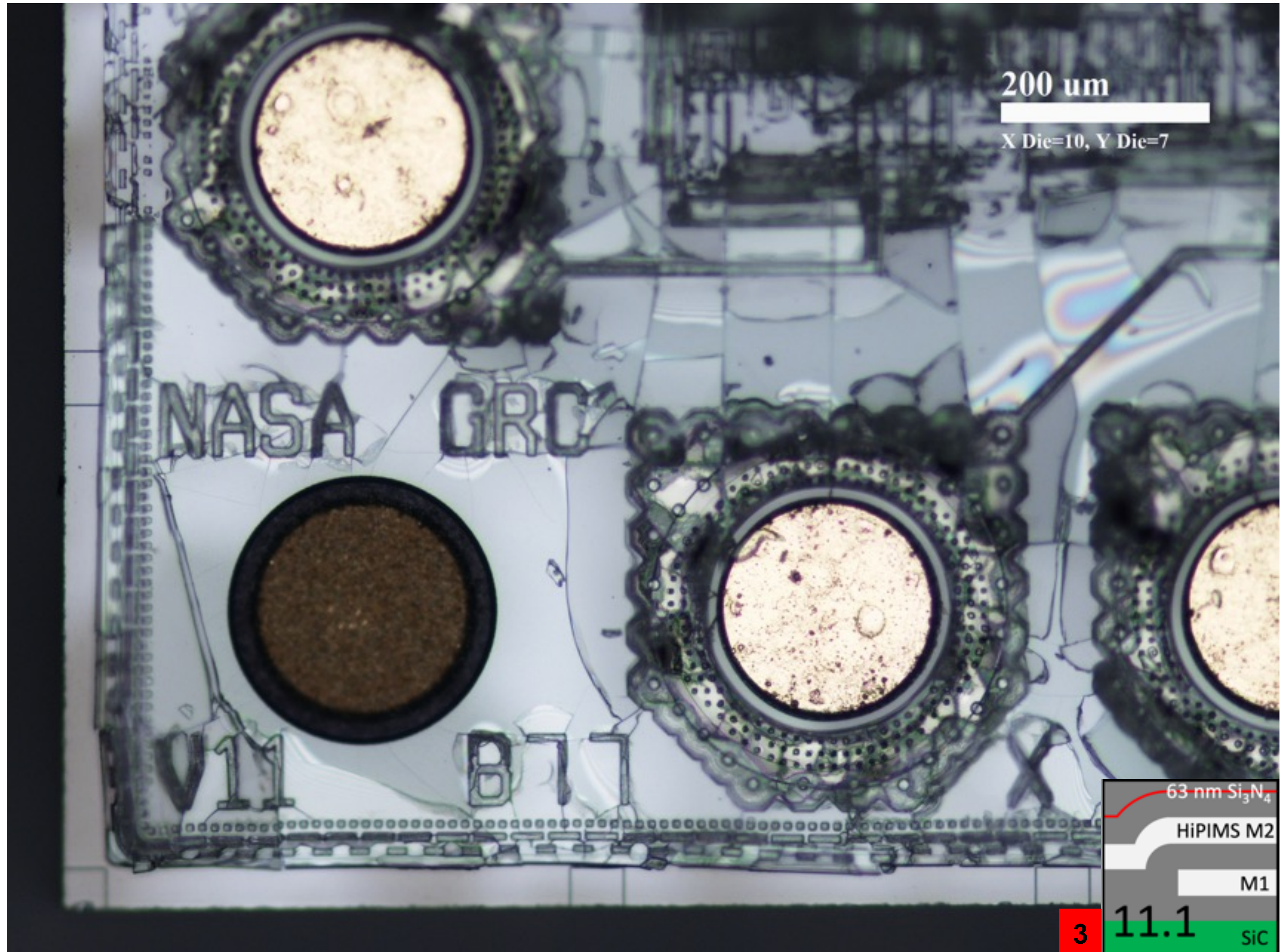
10 cycles 10 hrs. at 720 °C 10.2 Chip 1



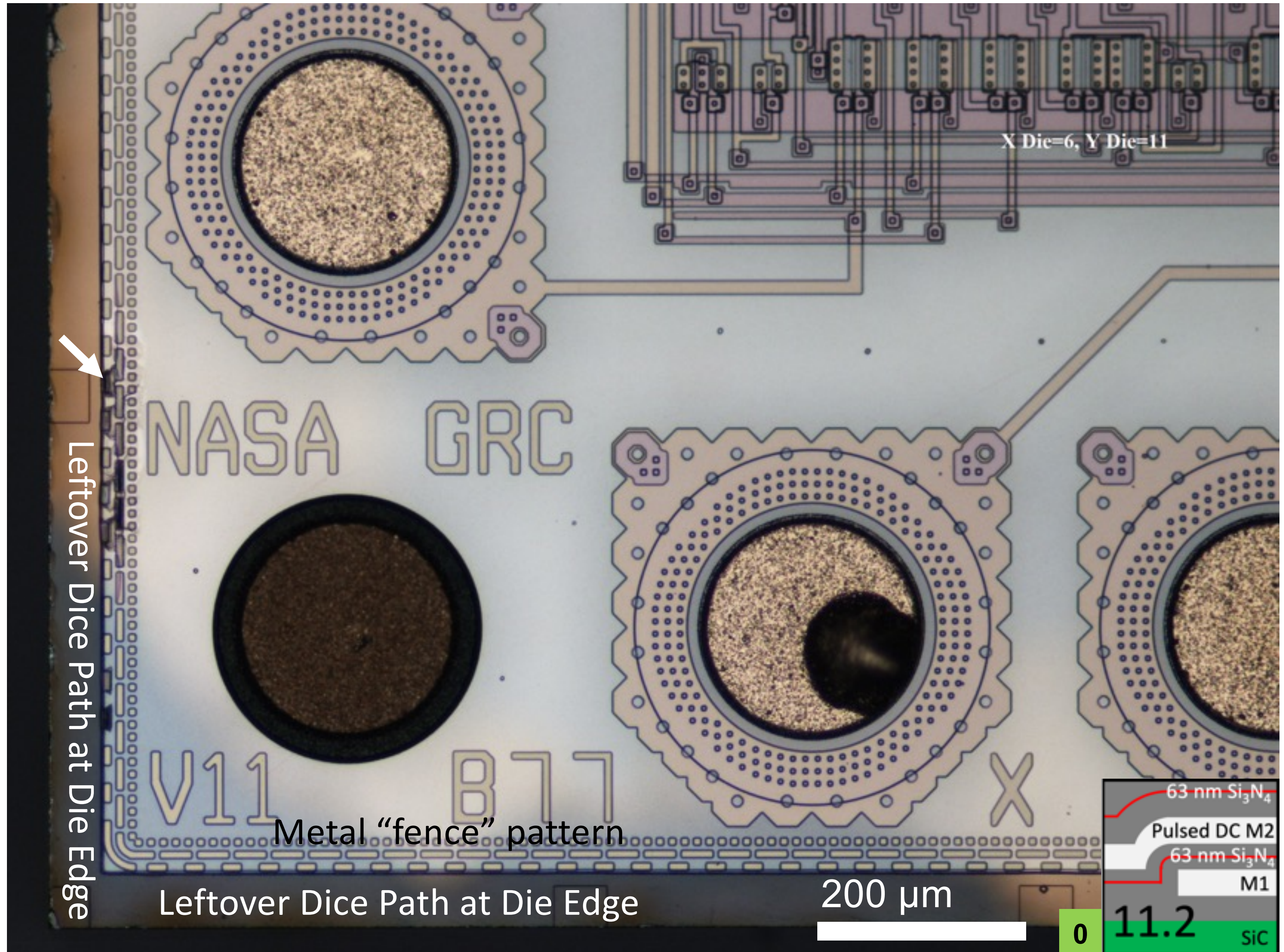
10 cycles 10 hours at 720 °C 10.2 Chip 3



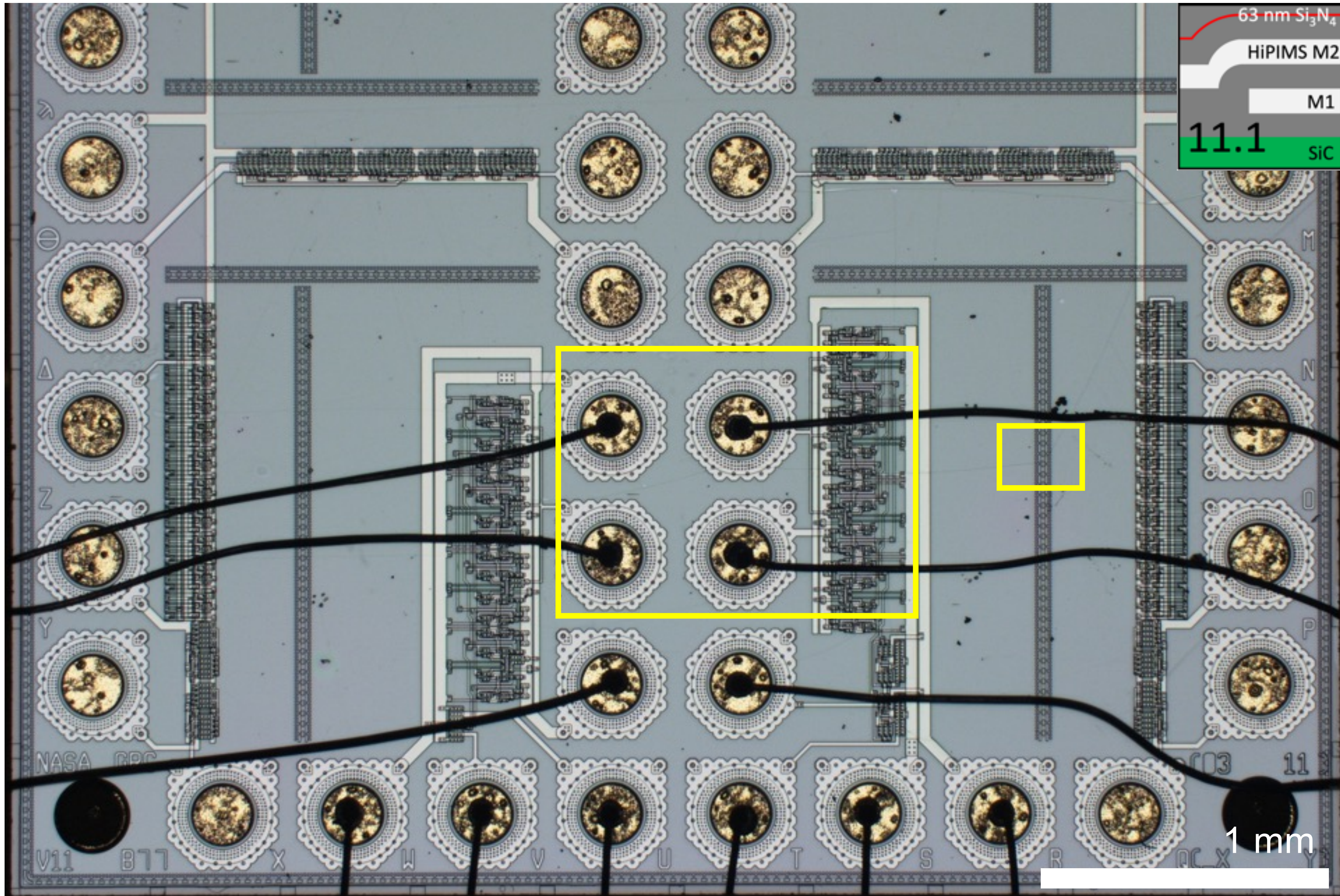
10 cycles 10 hours at 720 °C   11.1 Chip 7



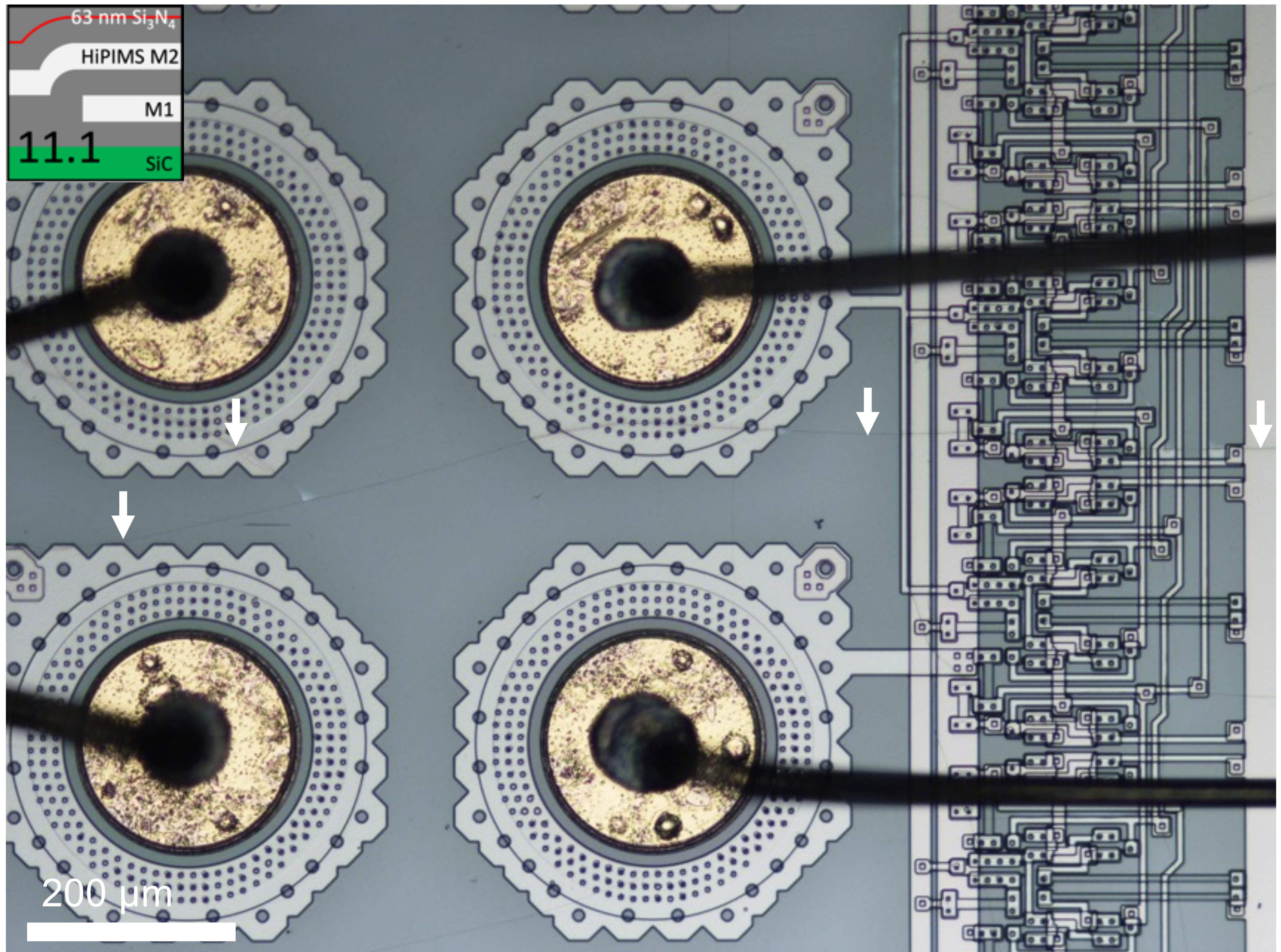
10 cycles 10 hours at 720 °C 11.2 Chip 7



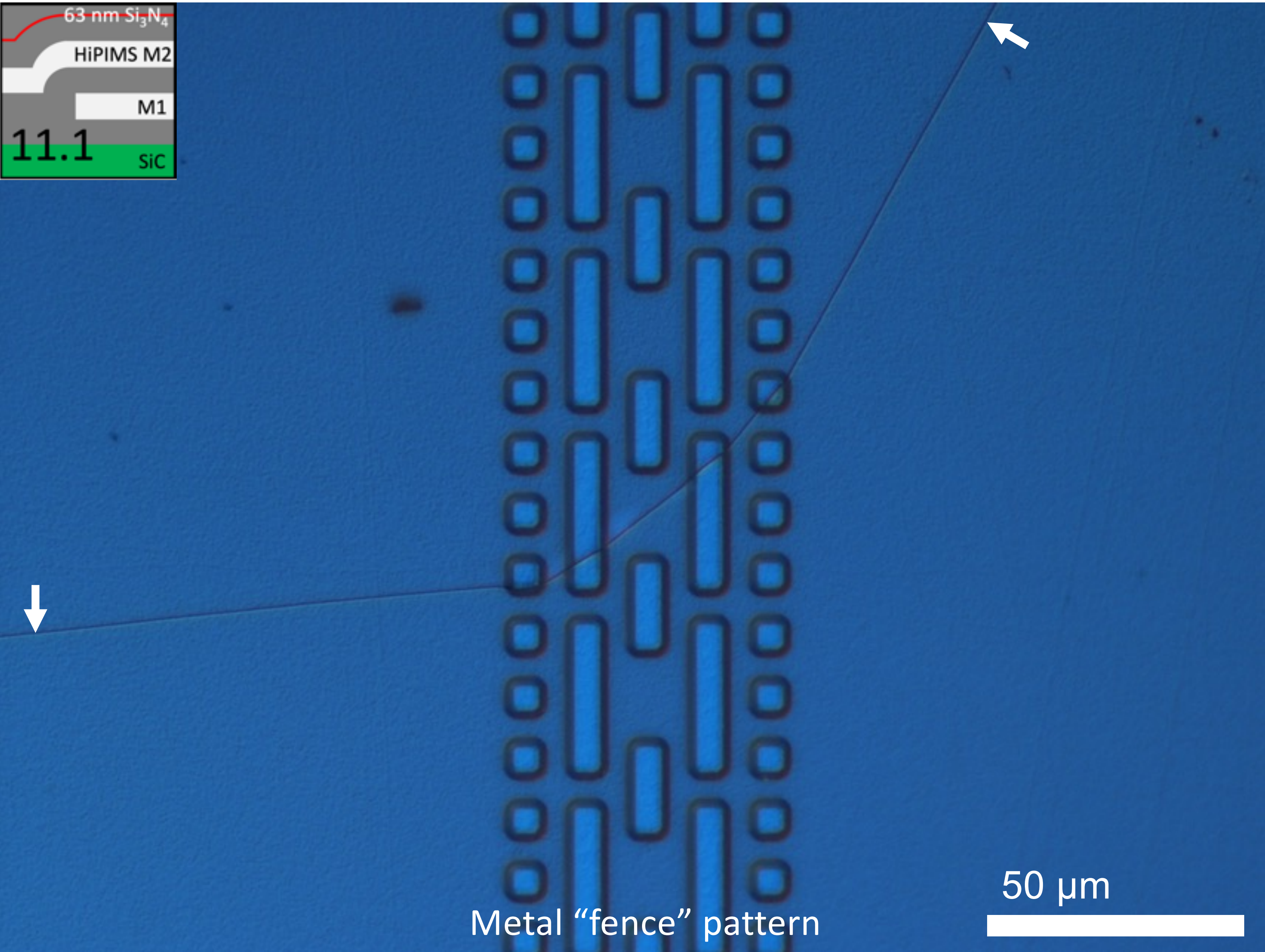
Electrical Failure 5th cycle 500 °C 10.2 Chip 13B



Electrical Failure 5th cycle 500 °C 10.2 Chip 13B



Electrical Failure 5th cycle 500 °C 10.2 Chip 13B



Summary

- The addition of a second LPCVD stochiometric Si_3N_4 layer reduced the amount of dielectric cracking.
- Etching through to bare SiC between die, reduces dielectric cracks form dicing process.
- Adding a metal 1 “fence” pattern deflected dielectric cracks from propagation into neighboring devices.

Acknowledgements

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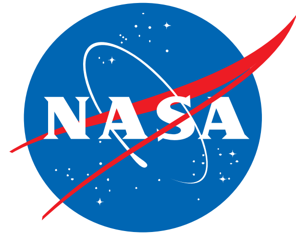
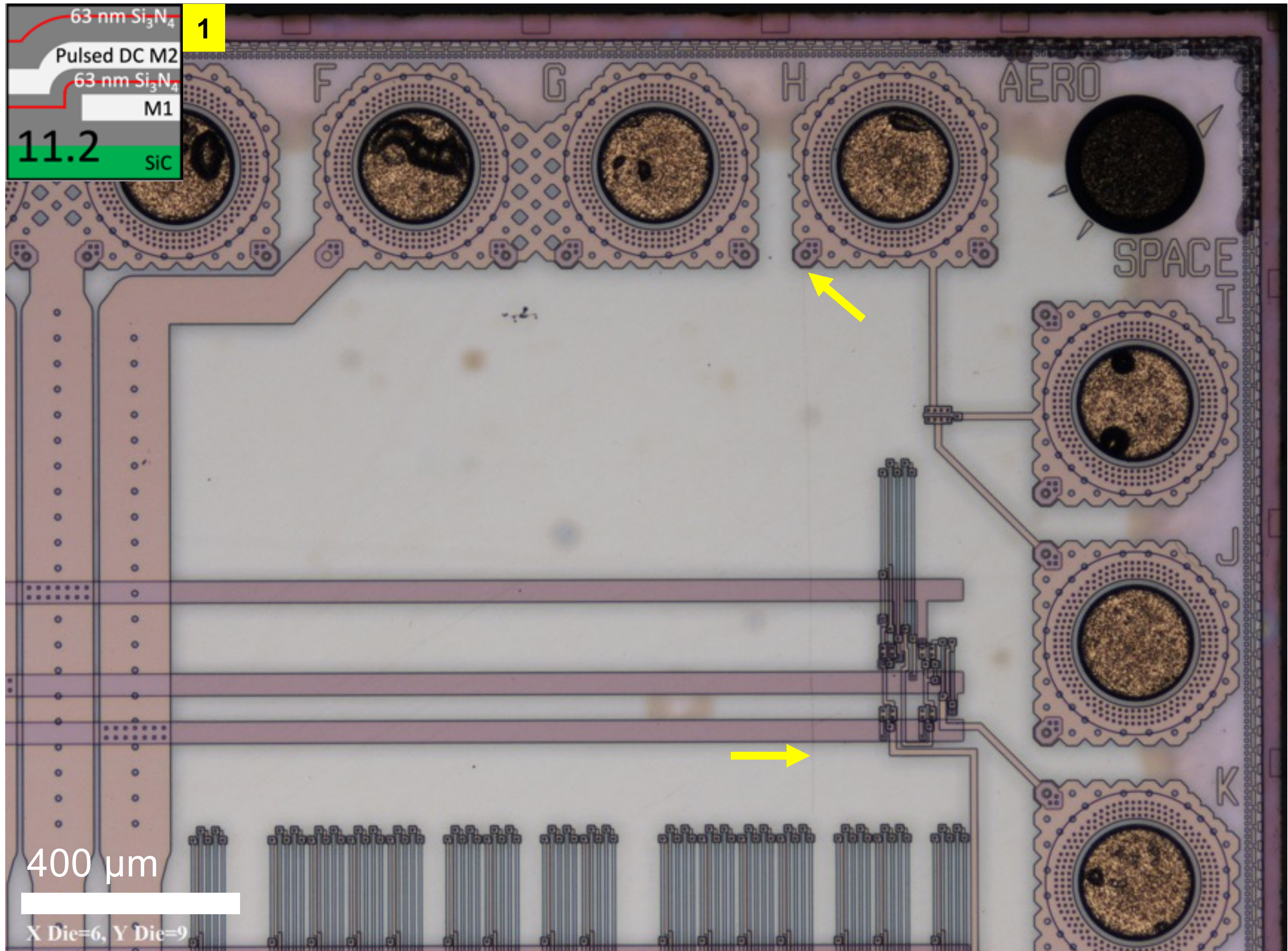
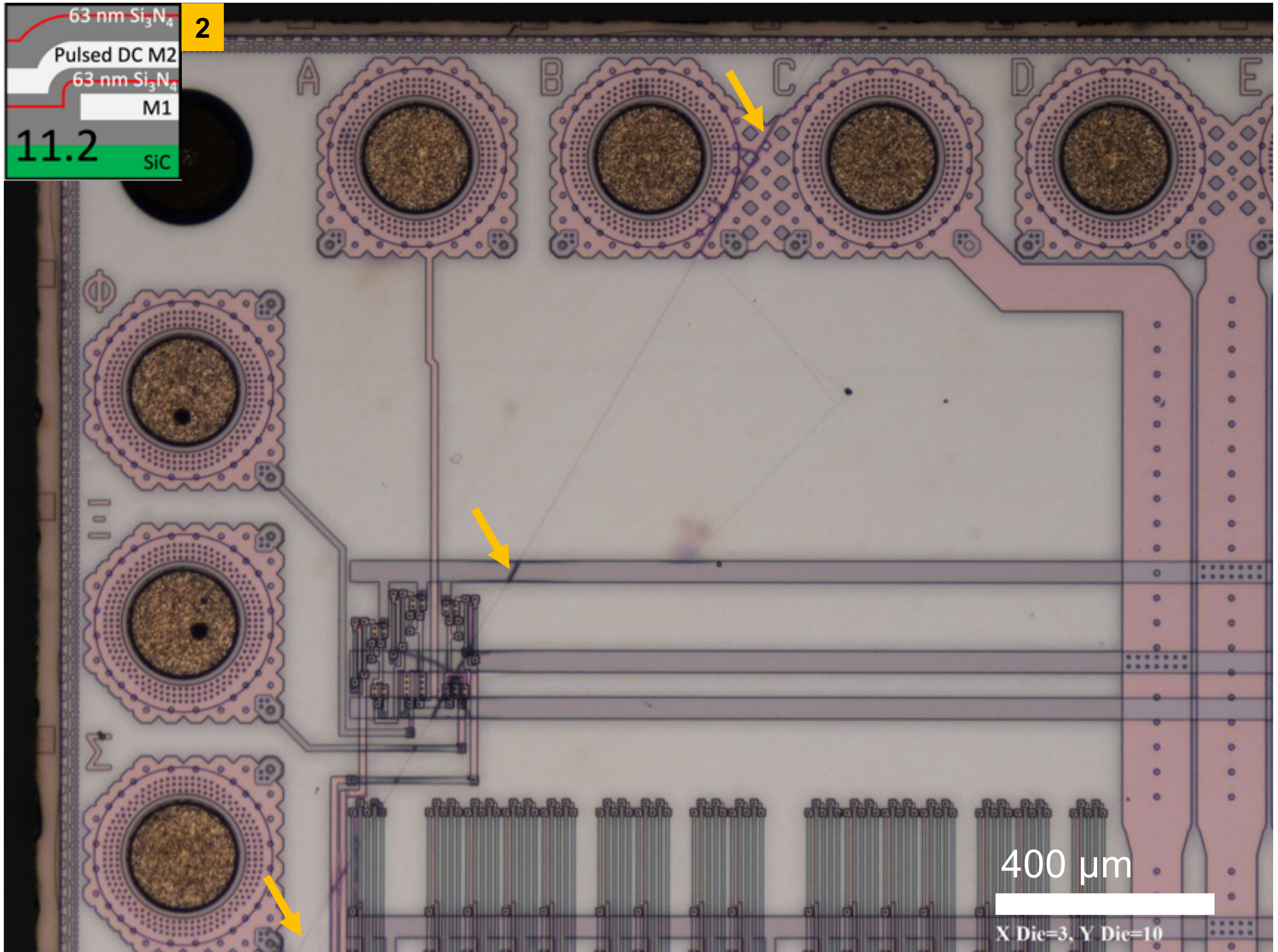

NASA

100 hours at 800 °C Post-Test

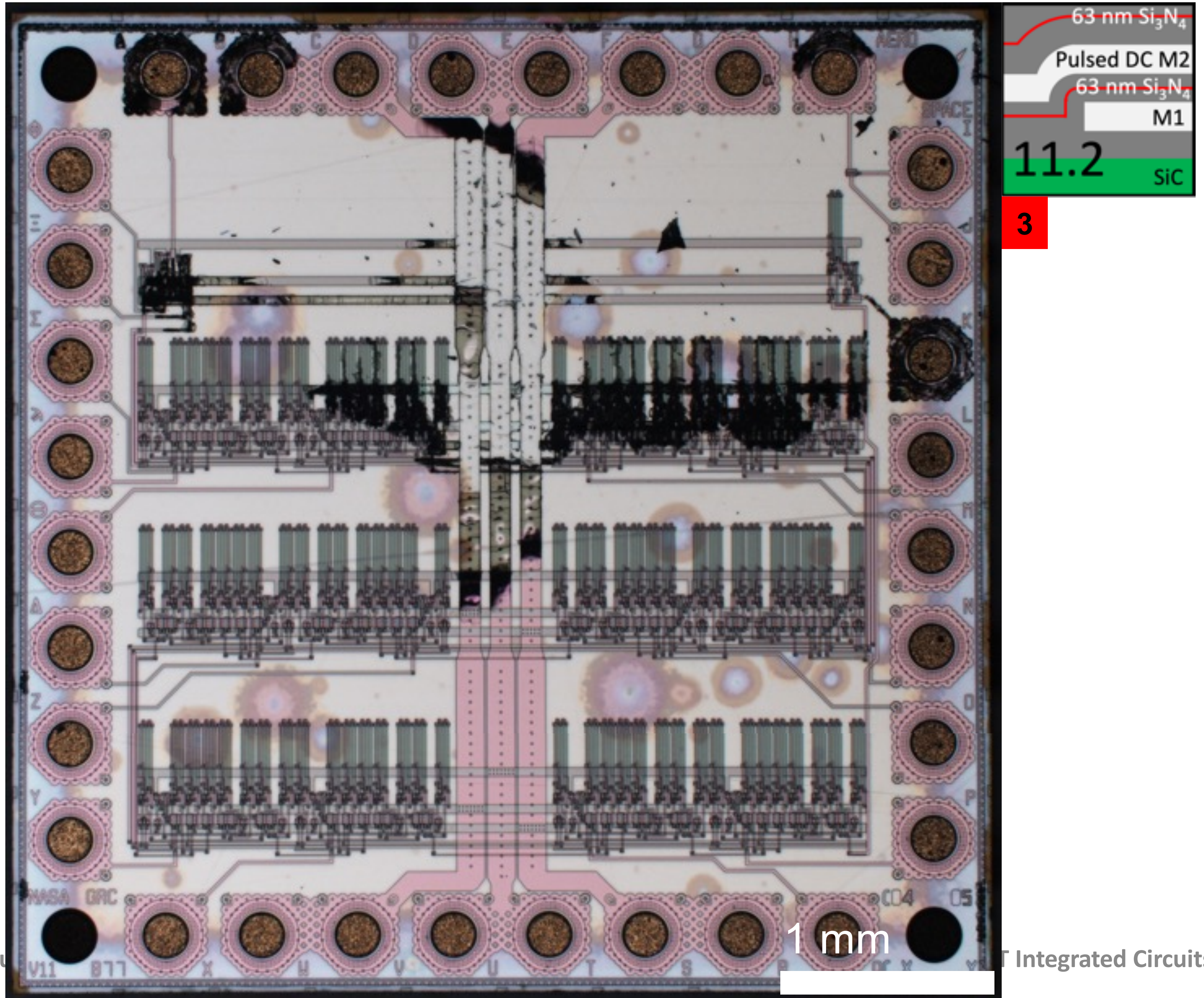


200 hours at 600 °C Post-Test

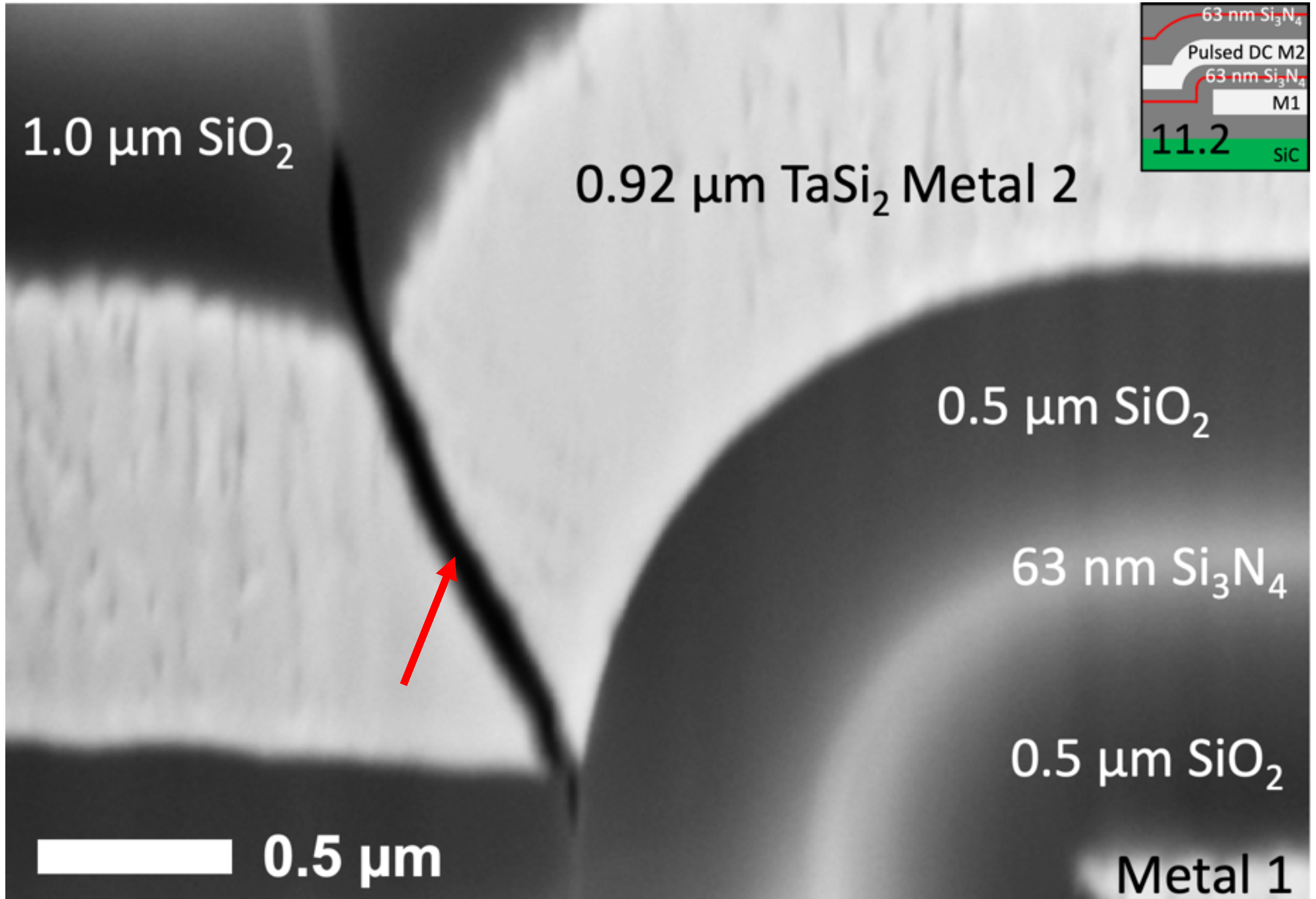


200 hours at 800 °C Post-Test

11.2

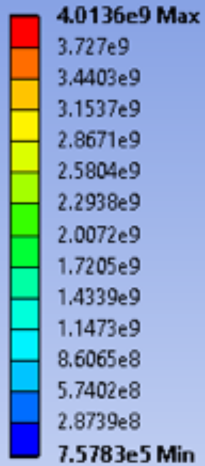


JFET IC Wafer 11.2 -Metal 2 Crack Zoom-in



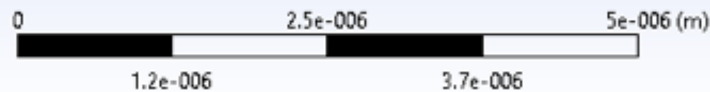
Max Stress Point Ansys FEA 10.2 and 11.1

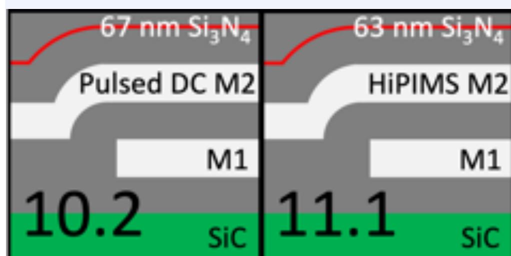
C: Static Structural
Equivalent Stress 2
Type: Equivalent (von-Mises) Stress
Unit: Pa
Time: 1
9/17/2019 4:08 PM



ANSYS
R18.2

Max



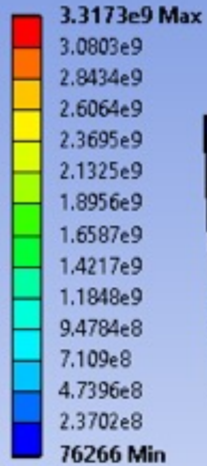


Max Stress Point Ansys FEA

11.2

E: Static Structural - mesh curv wrefine 720 to 22C
Equivalent Stress 2
Type: Equivalent (von-Mises) Stress
Unit: Pa
Time: 1
9/17/2019 4:05 PM

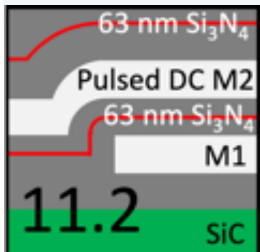
ANSYS
R18.2



Max

Y
X

1e-006
3e-006

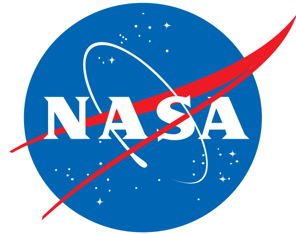


Future Work

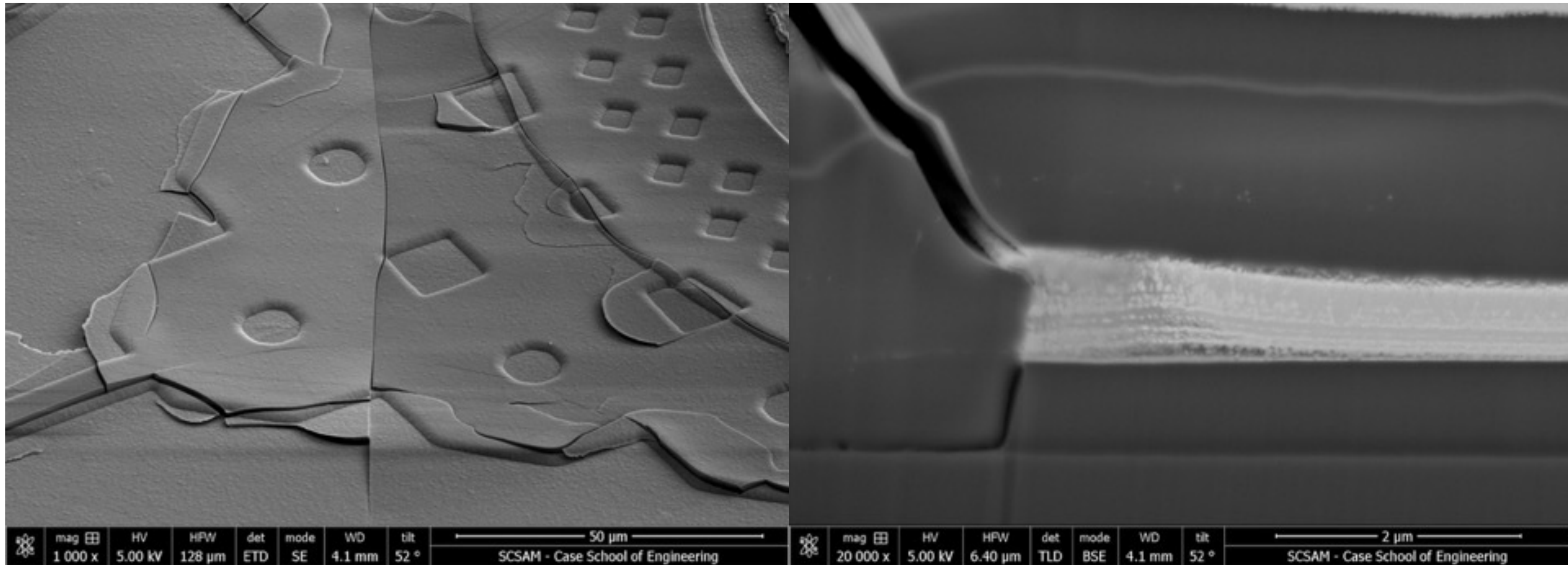
Current work was SiO_2 deposited at 720 °C by LPCVD using TEOS and 63nm stoichiometric Si_3N_4 deposited also at 720 °C by LPCVD using DCS and NH_3.

Make test metal insulator metal MIM capacitors to evaluate:

- 3 stoichiometric silicon nitride layers
- Thicker Si_3N_4 layers
- Stoichiometric Si_3N_4 deposited at 800 °C instead of 720 °C
- Low-stress silicon nitride layers
- High Temperature (HT) SiO_2 with dichlorosilane (DCS) and ammonia NH_3.
- Oxynitride
- HT oxide in same run as stoichiometric Si_3N_4
- Other precursors for stoichiometric Si_3N_4 such as trisilylamine (TSA) or neopentasilane (NPS) + NH_3 for use with TEOS in a sign tube LPCVD

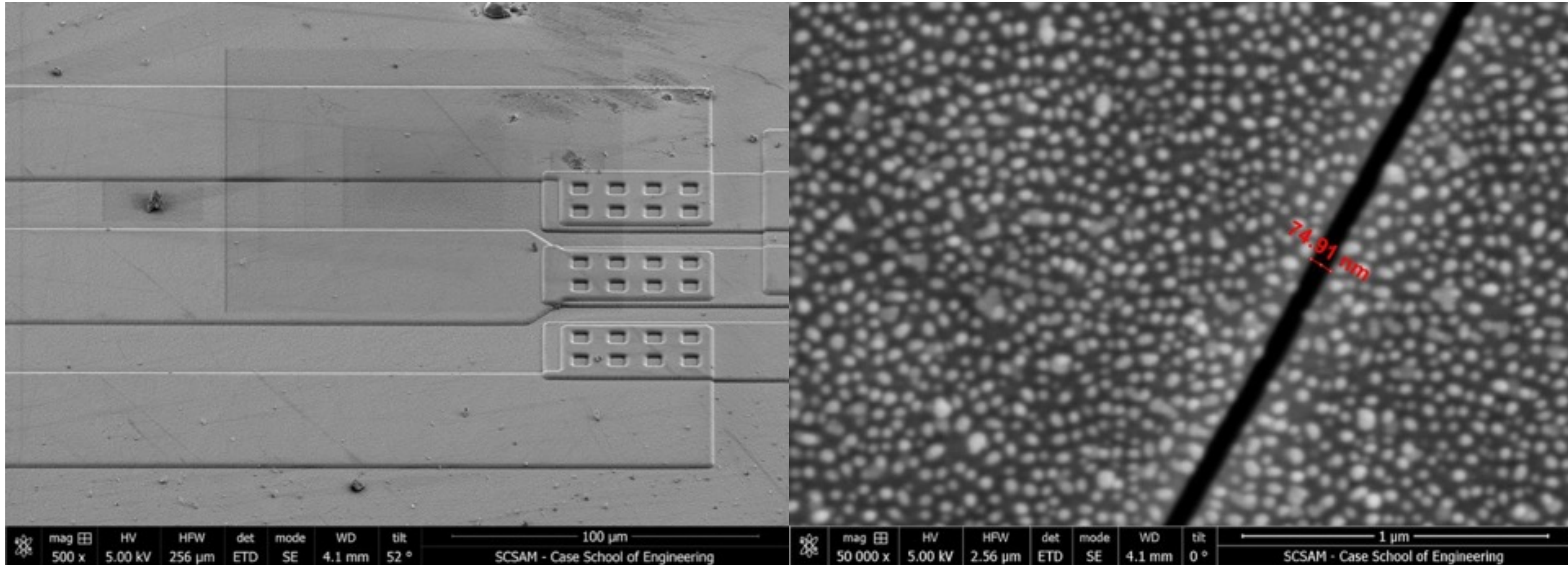


Typical Crack Propagation in Earth Air



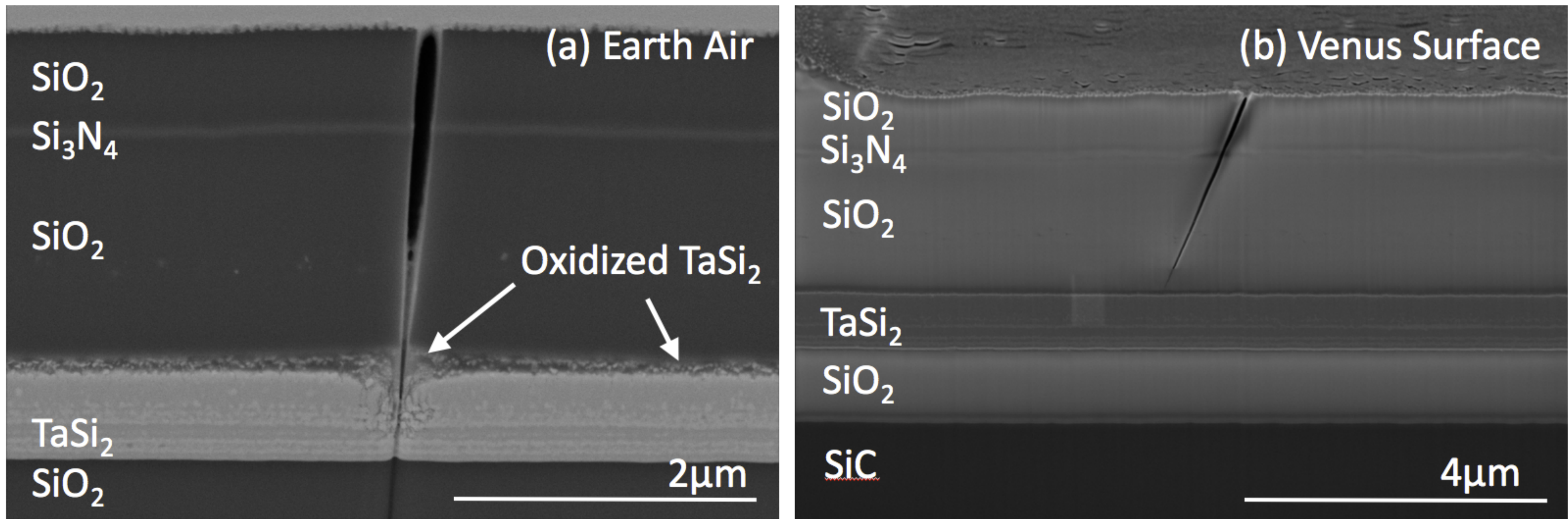
- This sample was at 727 °C sample and a old (Version 9.2) design. Same kind of behavior when seen on some 500 °C samples.
- Cracks related to dicing, handling, design rules, and bonding.
- Various degrees of oxidation and pealing seen.
- Oxidation of $TaSi_2$ surface can be many 10s of microns wide.

Crack at Venus Surface Conditions



- Only one crack seen on entire sample exposed to Venus.
- Found via optical microscope and then examined on SEM. Hard to find with FESEM.
- Very small (~ 75 nm) when viewed from the top.

Venus Environment Durability FIB FESEM



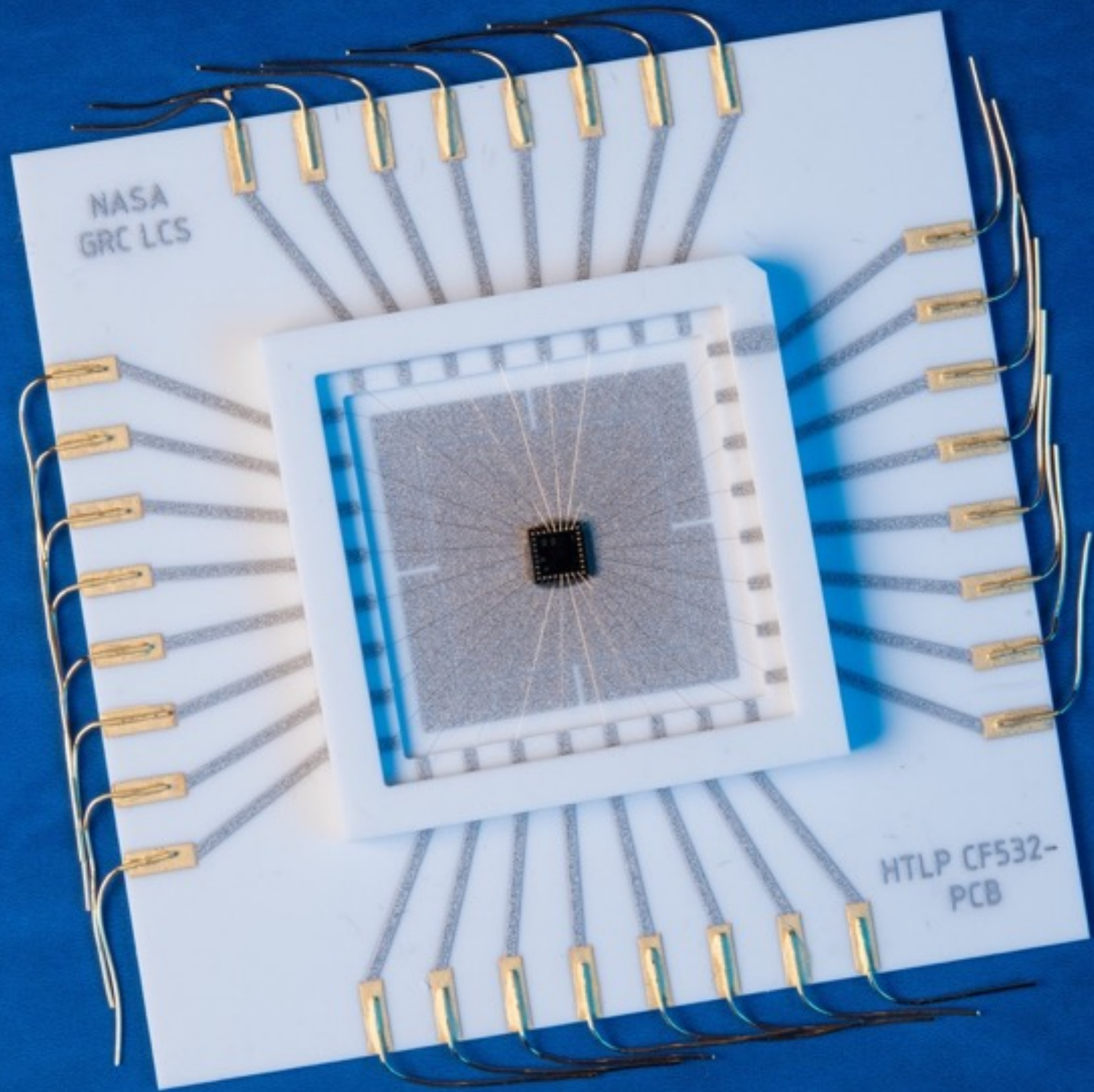
(a) Crack typical of prolonged T ≥ 500 °C testing in air (727 °C for this sample)

- In Earth environment, the crack allows the top surface of the $TaSi_2$ film to oxidize which exacerbates failure.

(b) Crack in IC sample tested in Venus surface condition.

- In Venus environment, the crack reaches the top of the $TaSi_2$ but does not propagate through the $TaSi_2$ and there is no observable evidence of $TaSi_2$ film oxidation.

STARC-ABL: Single-aisle Turboelectric AiRCraft with Aft Boundary Layer propulsion


NASA
GRC LCS
HTLP CF532-
PCB