Mechanisms of Heavy Ion-Induced Single Event Burnout in 4H-SiC Power MOSFETs

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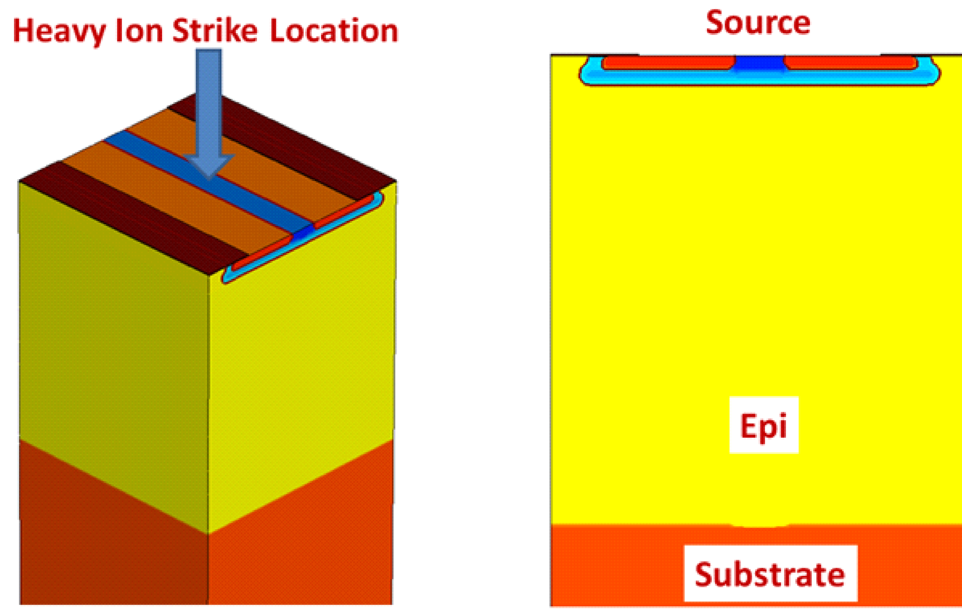
Introduction

Silicon Carbide (SiC) power MOSFETs are capable of operating at higher temperatures, voltages, and switching frequencies than silicon. This makes SiC desirable to NASA for future space missions and electric aircraft propulsion technologies. However, experimental tests have shown that SiC devices are susceptible to single event effects, especially single event burnout (SEB) caused by heavy ions. SEB can occur at applied voltages of less than half the device rating.

This work uses 3-dimensional electrothermal device simulations to explore the mechanisms of SEB in MOSFETs and proposes new designs that can survive SEB at higher blocking voltages.

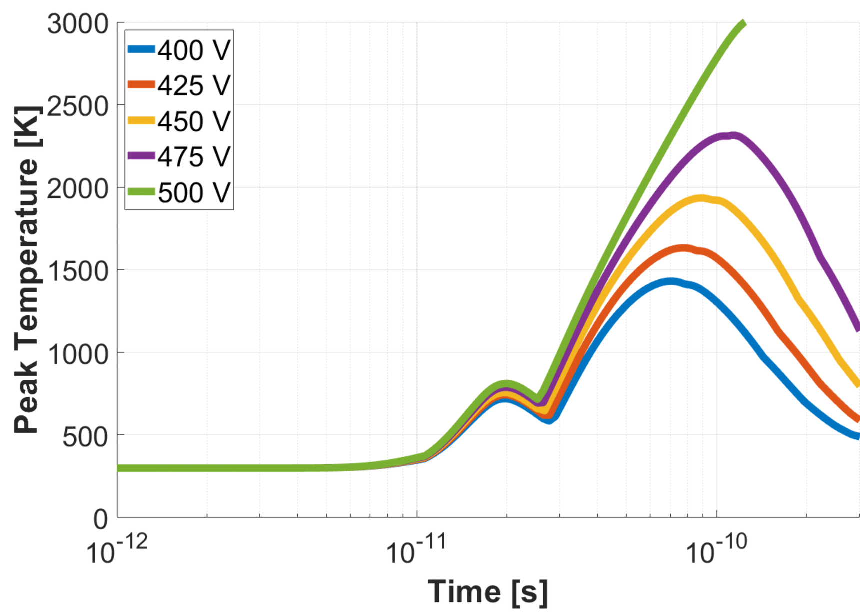
Baseline Model

- Commercially available power MOSFET rated for 1200 V with a specific on-resistance (Ron,sp) of 3.68 mΩ-cm^{-2}
- 10 µm thick epitaxial layer at doped n-type 6×10^{15} cm-3 on a 40 µm n+ substrate

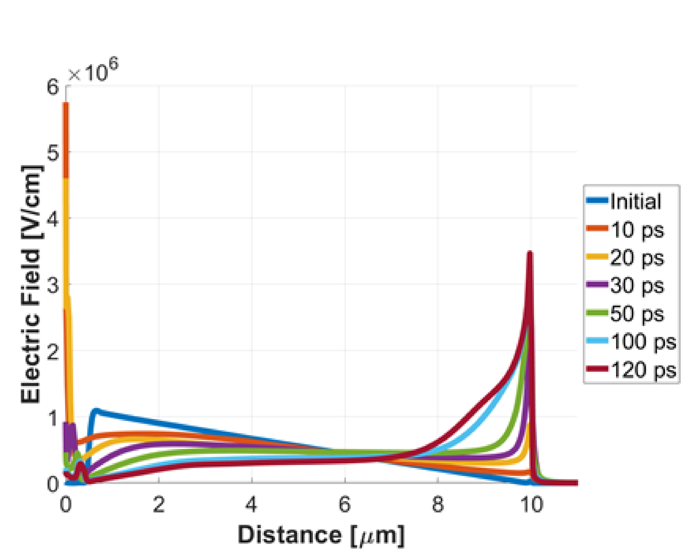


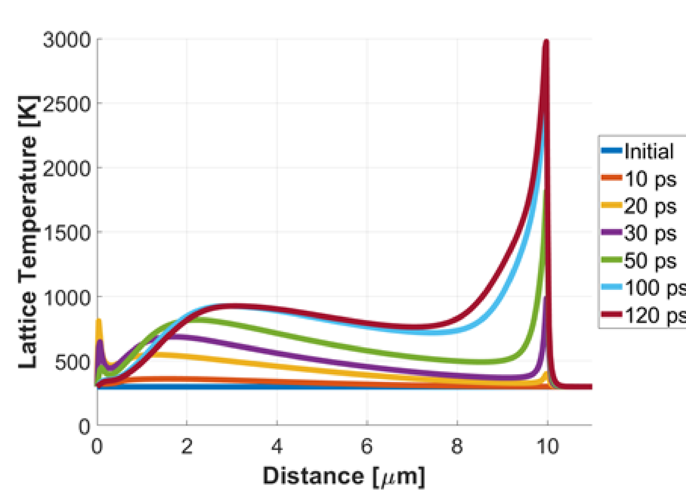
SEB Simulation

- Silver ion strike at a Linear Energy Transfer (LET) of 46 MeV-cm^2/mg in the center of the source contact region
- Burnout is assumed when the temperature reaches 3000 K anywhere
- Device fails between 475 and 500 V
  - ◊e-h plasma formation from heavy ion strike
  - ◊Transit of e-h carriers to modulate electric field causing an electric field peak that persists at the epi/substrate interface
  - ◊Enhanced electric field causes significant impact ionization and localized heating at the epi/substrate interface until thermal destruction

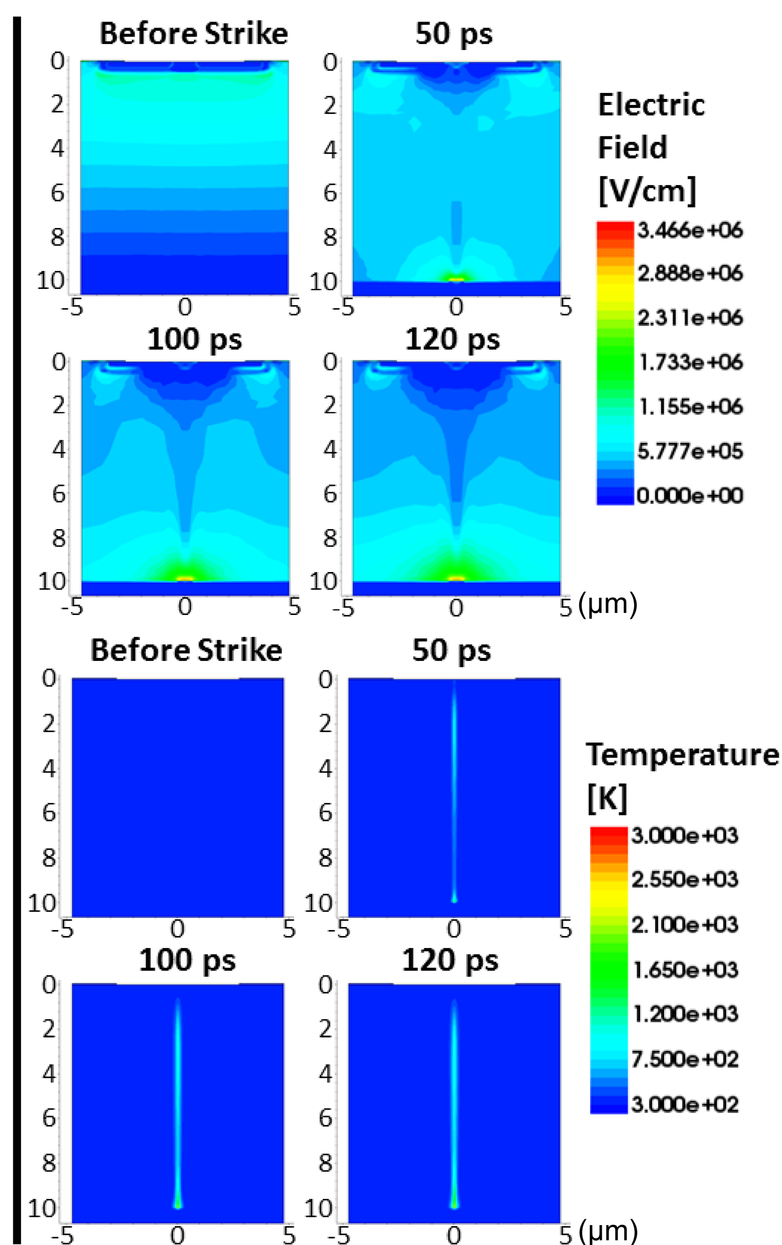


Along heavy ion track





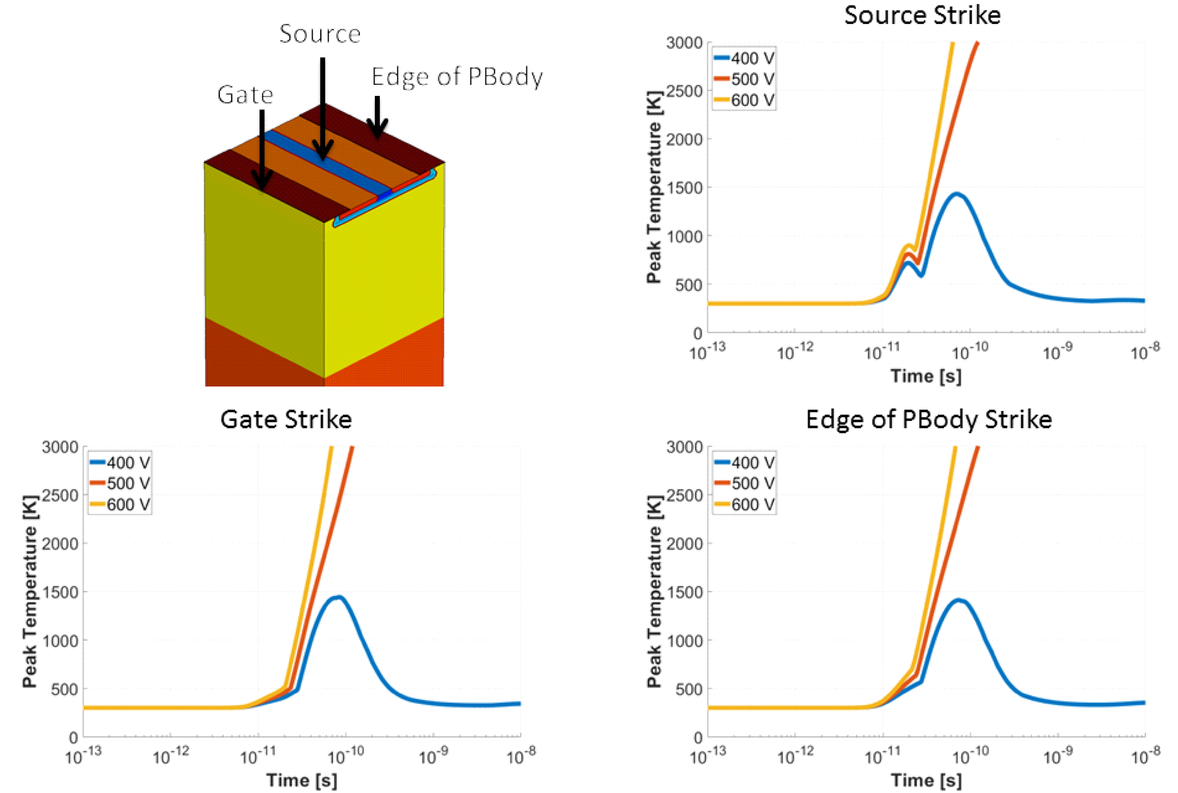
2-D



Simulated time evolution for electric field and lattice temperature of MOSFET a blocking voltage of 500 V

Strike Locations

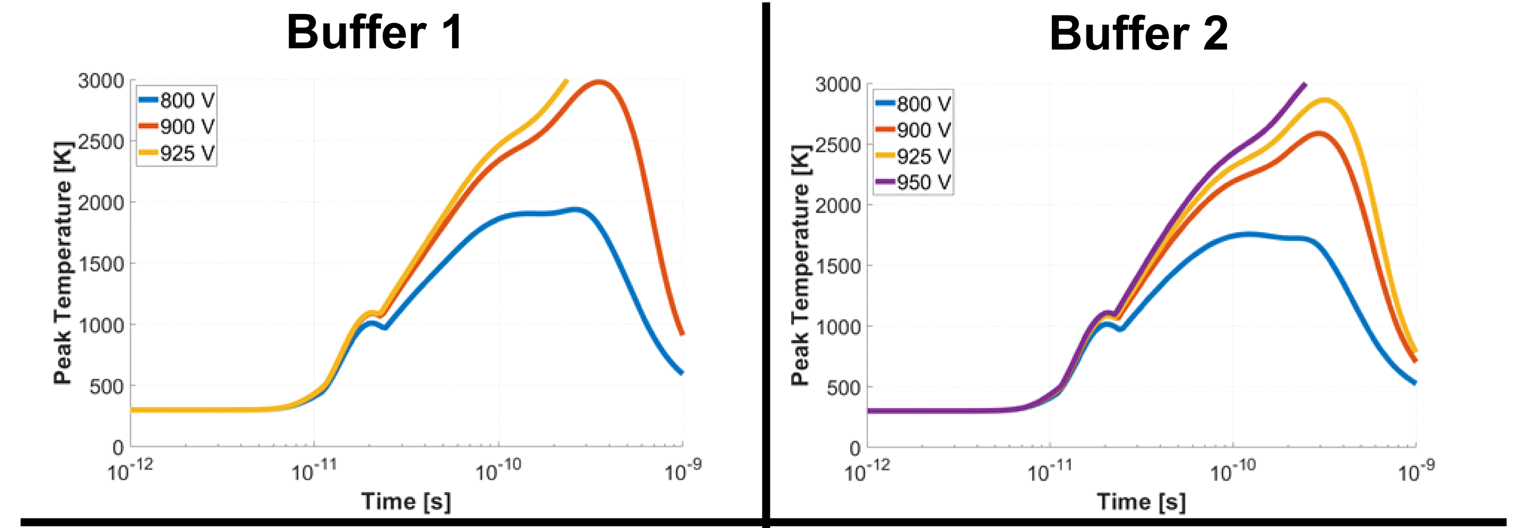
- 3 locations investigated: Center of P+, gate, and edge of P-Body

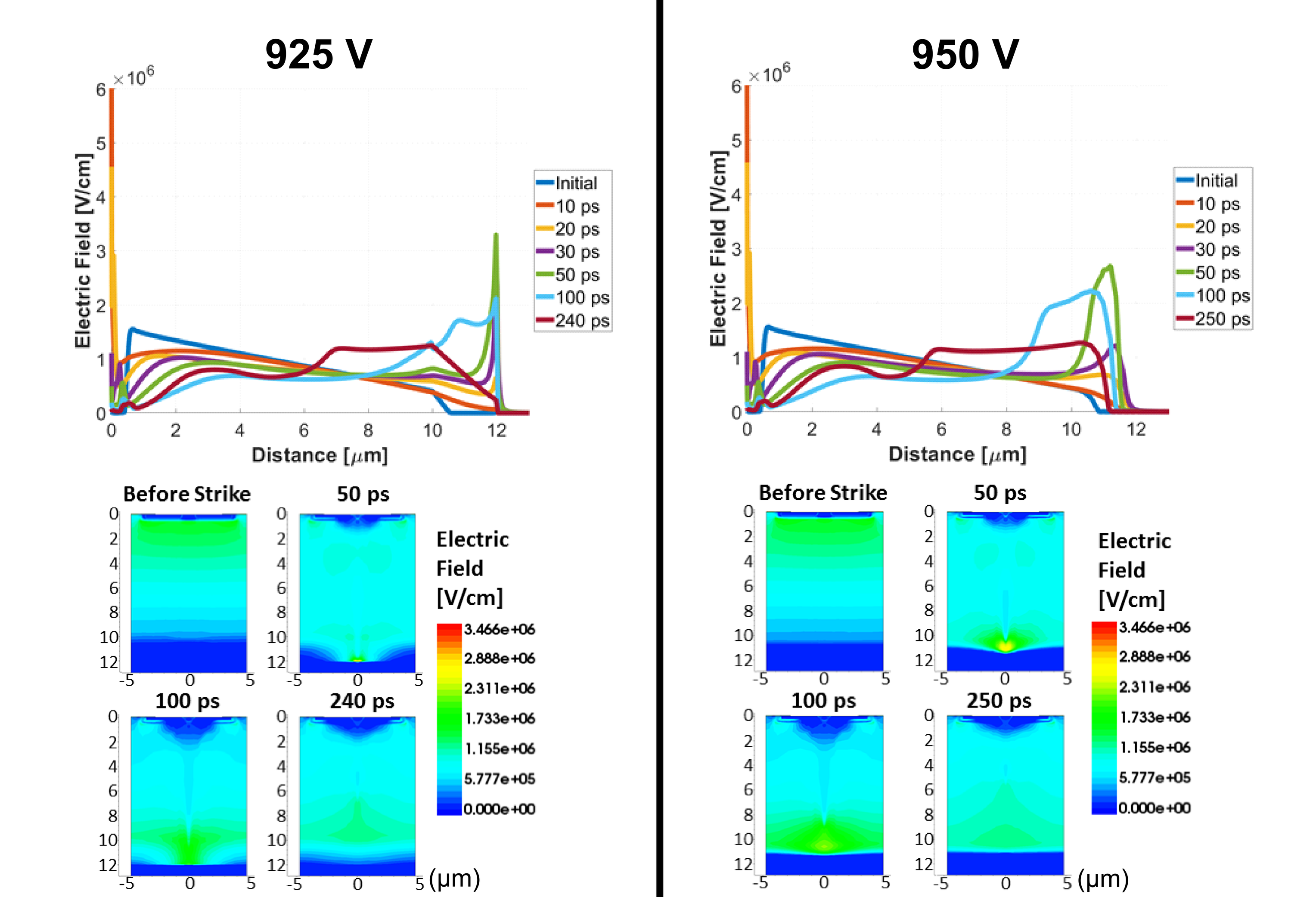


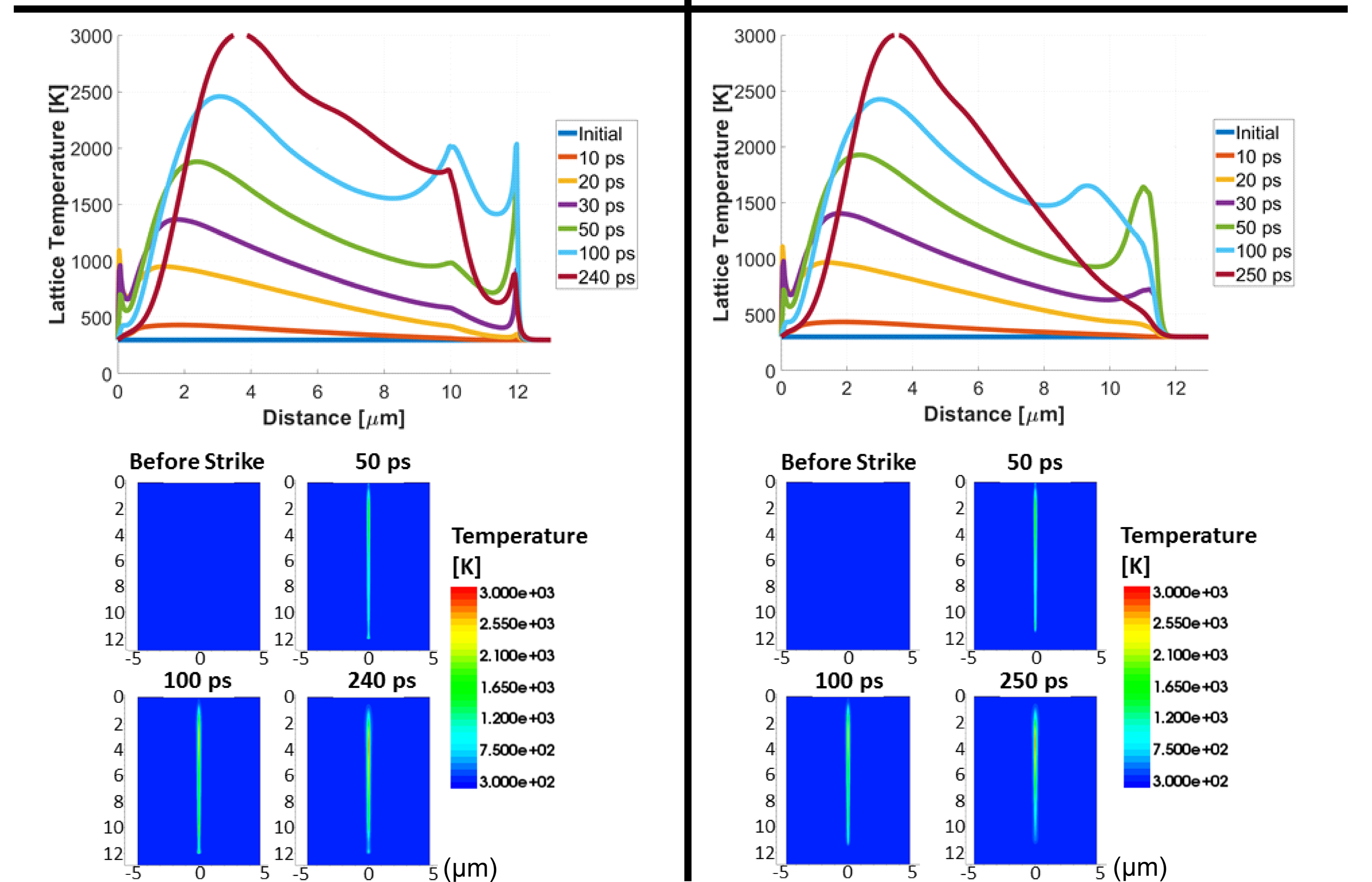
- No dependence found between strike location and SEB

Improved Designs

- 2 µm additional, N-type layer inserted in between the original epi layer and substrate
- SEB threshold voltage was raised to over 900 V
- Electric field enhancement at epi/substrate interface has been suppressed
- Failure of device is due to excessive heating from an accumulation of carriers at a depth of 3 to 4 µm below top surface







Summary

- Failure of commercial design is due to the electric field at the epi/substrate interface is high enough to cause significant impact ionization, which in turn causes significant heating and eventual failure
- Creation of two buffer designs were investigated and allowed for the device to operate at over 900 V before SEB occurred and this is due to the reduction of the electric field at the epi/substrate interface

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