Detector channel combining results from a high photon efficiency optical communications link test bed

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ABSTRACT

The National Aeronautics and Space Administration (NASA) Glenn Research Center (GRC) is developing a low cost, scalable, photon-counting receiver prototype for space-to-ground optical communications links. The receiver is being tested in a test bed that emulates photon-starved space-to-ground optical communication links. The receiver uses an array of single-pixel fiber-coupled superconducting nanowire single-photon detectors. The receiver is designed to receive the high photon efficiency serially concatenated pulse position modulation (SCPPM) waveform specified in the Consultative Committee for Space Data Systems (CCSDS) Optical Communications Coding and Synchronization Blue Book Standard. The optical receiver consists of an array of single-pixel superconducting nanowire detectors, analog phase shifters for channel alignment, digitizers for each detector channel, and digital processing of the received signal. An overview of the test bed and arrayed receiver system is given. Simulation and system characterization results are presented. The data rate increase of using a four-channel arrayed detector system over using one single pixel nanowire detector is characterized. Results indicate that a single-pixel detector is capable of receiving data at a rate of 40 Mbps and a four-channel arrayed detector system is capable of receiving data at a rate of 130 Mbps.

Keywords: Optical communications, pulse position modulation, waveform, superconducting nanowire detectors

1. INTRODUCTION

The National Aeronautics and Space Administration (NASA) is planning to use the Consultative Committee for Space Data Systems (CCSDS) Optical Communications High Photon Efficiency (HPE) Standard[1] in future missions requiring photon-counting optical communication systems. These missions include the Optical Artemis-2 Orion (O2O)[2] communications demonstration on the first crewed flight of the Artemis program as well as the Psyche[3] mission into deep space. The CCSDS HPE standard uses pulse position modulation (PPM) concatenated with a convolutional code (code rates 1/3, 1/2, and 2/3).

The NASA Glenn Research Center (GRC) implementing a low-cost photon-counting receiver using commercial off the shelf (COTS) components in order to decrease the cost of implementing the system. The receiver is designed to be compatible with the CCSDS Optical Communications HPE telemetry link, with a 500 ps slot and data rates up to 530 Mbps. Previous test results[4] indicated that a single superconducting nanowire single-photon counting detector (SNSPD) is capable of receiving the PPM-32, code rate 1/3, 1 ns slot, 40 Mbps mode. Higher photon flux rates are needed for lower PPM orders, smaller slot widths, and higher data rates. One issue with utilizing SNSPDs is that at higher photon flux rates, photon detection efficiency decreases due to detector blocking. This is because after a photon is detected, a SNSPD is blocked, during which time a photon cannot be detected. This time period is called detector reset time. Due to detector blocking, an arrayed detector system is therefore required to receive higher photon flux rates and increase the data rate.

Detector arraying simulation and test bed results are compared in this paper. A test bed which emulates the space-to-ground communications link is described in Section 2. Simulation results are presented in Section 3 and test bed system test results are presented in Section 4.

2. TEST SETUP

The arrayed SNSPDs are part of an optical communications test bed for photon-starved optical communications links. The test bed, shown in Figure 1, consists of the field programmable gate array (FPGA) based software defined radio (SDR) transmitter, which implements the CCSDS HPE optical communications waveform[5], a variable attenuator for path loss emulation, and an array of SNSPDs which feed into a digitizer and post processing software receiver. A description of the system follows.

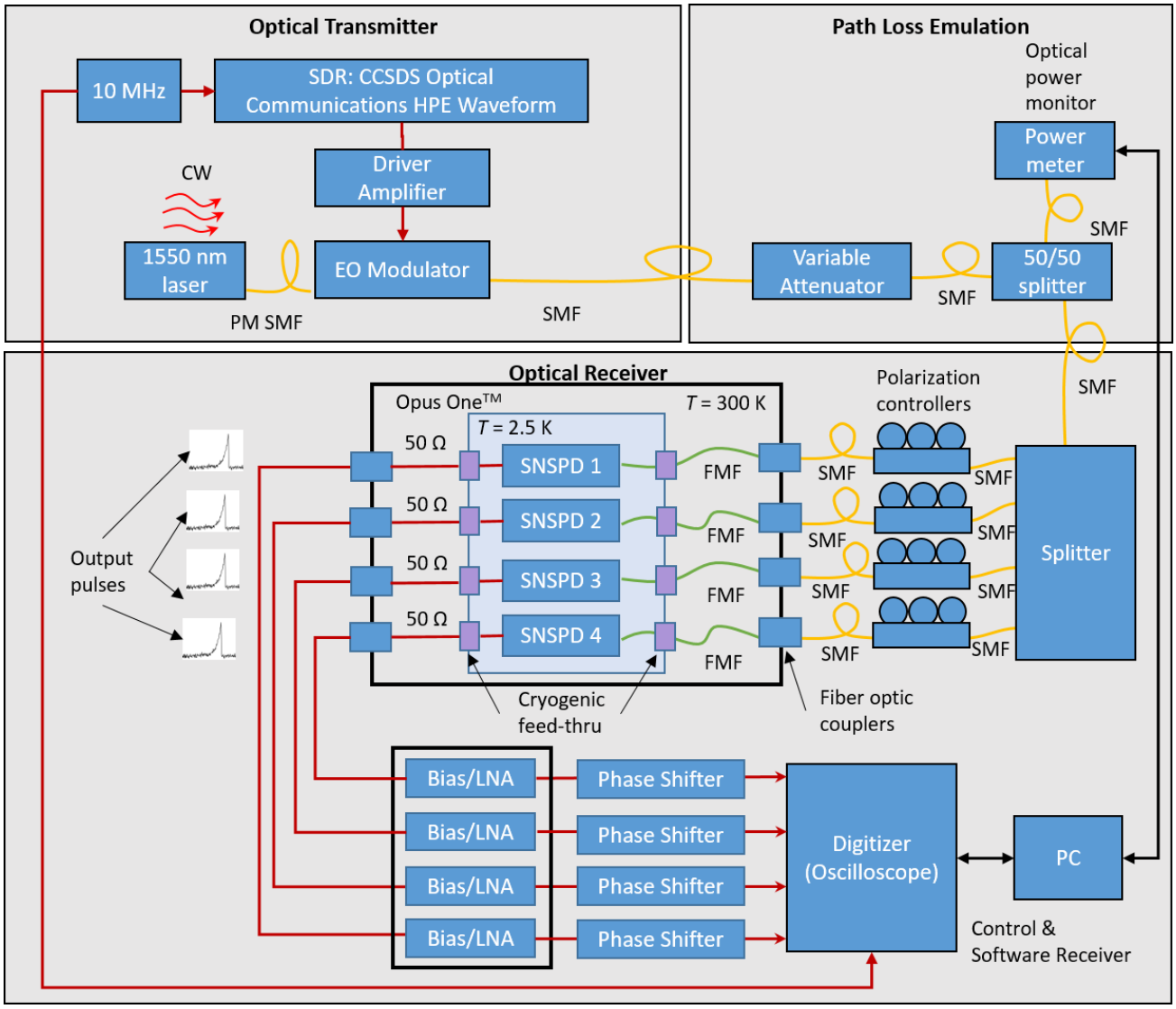


Figure 1. Block diagram of the SNSPD array within the optical communications system test bed.

2.1 Optical transmitter

The CCSDS HPE telemetry link waveform is implemented on a Xilinx Virtex 7 FPGA. PPM orders ranging from PPM-4 to PPM-256 and code rates 1/3, 1/2, and 2/3 are implemented. The data source consists of a pseudorandom bit stream (PRBS) 2^{23} -1 pattern. The channel interleaver is bypassed as no fades are inserted in this test. Pulses are transmitted out of the FPGA using a gigabit transceiver (GTX) at a rate of 10 GSps. The smallest slot width implemented is 500 ps. Inside the FPGA, each 500 ps PPM slot is up-sampled by 5 and processed using a shaping algorithm. Transmitter pulse shaping is necessary to reduce inter-slot interference and is accomplished by zeroing out the last 2 up-sampled GTX pulses so that the transmitted slot fits within the PPM slot. Figure 2 shows the transmitted pulse, sampled at 20 GHz, compared to the 500 ps PPM slot.

In order to generate the optical pulses, the signal transmitted out of the FPGA is sent to a driver amplifier and then into a high extinction electro-optic (EO) modulation which is driven by a continuous wave (CW) laser.

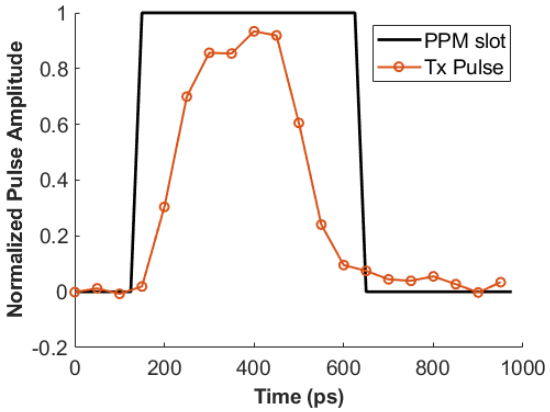


Figure 2. Transmitted pulse compared to the PPM slot.

2.2 Path loss emulation

The path loss for this test bed is emulated using a variable attenuator. A 50/50 fiber splitter is used to monitor the power of the signal before it goes in to the optical receiver. The power measurement is used to calculate the received power into the detectors. No fading or scintillation is inserted in this test setup.

2.3 Optical receiver

The receiver splits the incoming signal into four paths, and each path is connected to a single-pixel SNSPD. Each path consists of a polarization controller, SNSPD, detector bias circuitry, low noise amplifier (LNA), and phase shifter. A 4-channel oscilloscope samples the detector pulses.

The SNSPDs are single-pixel detectors from the Quantum Opus, Opus One™ system. The detectors are optimized for a wavelength of 1550 nm. The SNSPDs are polarization sensitive and the polarization controller is used to optimize the polarization into the detectors. The system comes with bias circuitry and a room-temperature 500 MHz bandwidth LNA for each detector. Prior to use, the detector performance was characterized[6]. The root mean squared (RMS) jitter for each detector channel (Ch 1 = 45.6 ps, Ch 2 = 46.2 ps, Ch 3 = 40.2 ps, Ch 4 = 48.6 ps), detector pulse rise time (90/10 = 850 ps), detector reset time (25 ns), and detector blocking loss were measured. The detector blocking loss is directly related to the input photon flux. This characterization of the detection blocking loss vs. the input photon flux for each detector channel is shown in Figure 3.

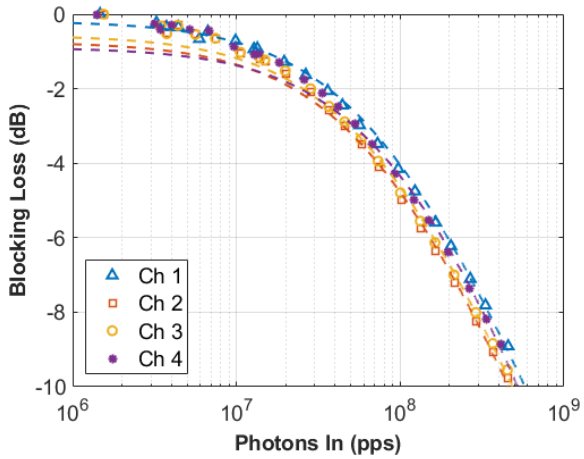


Figure 3. Detection blocking loss increases as the input photon flux increases.

Phase shifters are used to align the outputs of the each detector, as the optical and electrical path lengths internal to the detector system are not the same. If the detector channels are not aligned, inter-slot interference occurs. Prior to data collection, detector alignment is accomplished using a femtosecond laser as the detector input and shifting the phase of the detector output pulses until they are aligned visually on the oscilloscope.

Detector output pulses are sampled at a rate of 2 GHz using the oscilloscope. A sample rate of 2 GHz was chosen because a COTS 8-channel analog to digital converter (ADC) is available to use when this receiver is implemented in a real-time system. The detector pulse rise time (90/10) is 850 ps. Since a sampling frequency of 2.4 GHz is required to sample the rising edge with at least 2 samples on the edge, additional jitter is introduced.

The receive waveform is implemented in software to post process the digital samples. First, an estimate of the slot and symbol phase relative to the start of the oscilloscope samples is performed on one channel using the method described by Rogalin[7]. The slot and symbol phase estimate is used to linearly interpolate between the ADC samples at the slot and symbol boundary. Jitter is introduced in this process on each channel. The detector jitter, interpolator jitter, and total jitter is given in Table 1. The total jitter is calculated by adding the detector and interpolator jitter using the root sum squared method.

Table 1. System Jitter

Detector Channel	Detector Jitter (ps RMS)	Interpolator Jitter (ps RMS)	Total Jitter (ps RMS)
1	45.6	39.4	60.3
2	46.2	33.3	57.0
3	40.2	35.9	53.9
4	48.6	32.6	58.6

After slot and symbol phase recovery, photons in each slot are counted using a threshold on the detector pulse rising edge and then the channels are digitally combined. The detected average photons per signal slot (K_s) and the detected average background photons per slot (K_b) are calculated. Codeword alignment is performed, the codewords are decoded using the Bahl, Cocke, Jelinek and Raviv (BCJR) algorithm[8], and a bit error rate is calculated. A block diagram of this waveform is given in Figure 4.

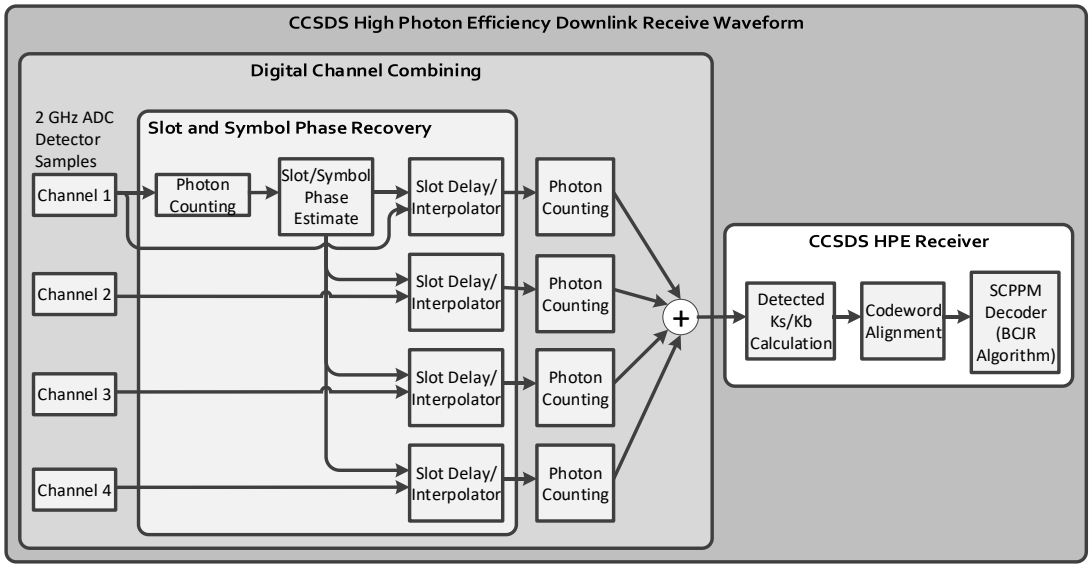


Figure 4. Block diagram of receive waveform with digital channel combining.

3. SIMULATION RESULTS AND DESCRIPTION

A model of the photon-counting test bed is implemented in software. The model includes the CCSDS HPE transmit waveform, a Poisson channel model, and the receive waveform model. The receiver model is the same as the post-processing receiver used in the system tests and described in section 2.3. In addition, effects including detector blocking and total jitter are modeled for each detector channel. Detector blocking is implemented after the Poisson channel by starting with the first detection and deleting subsequent detections that are within 25 ns (reset time) after the first detection. After the reset time ends, the next detection is found and the process repeats. Photons are placed within the slot with a uniform distribution and then total jitter is added from that point using a normal distribution. A block diagram of the model is shown in Figure 5.

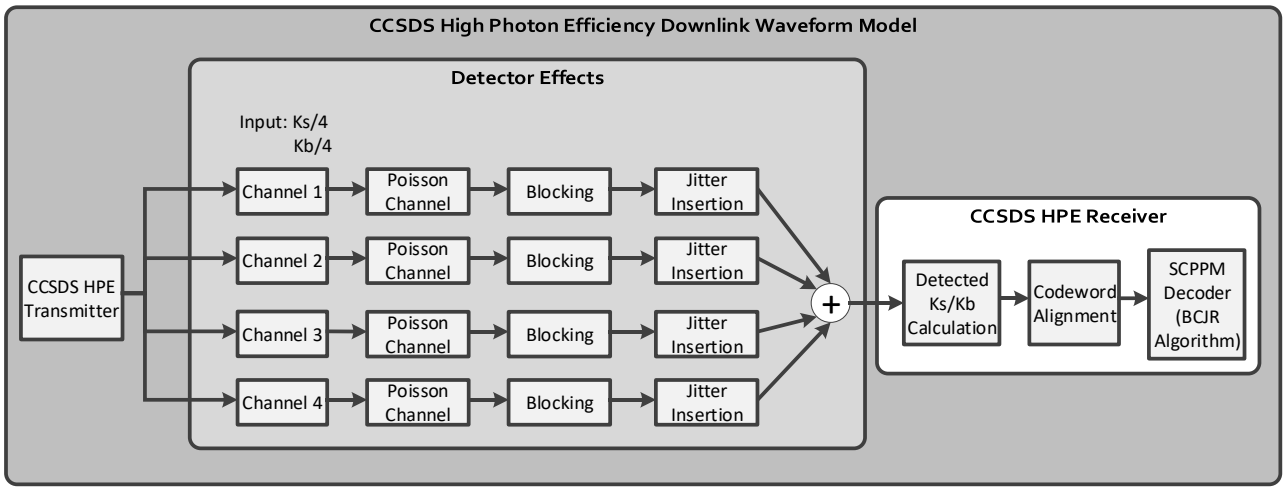


Figure 5. Block diagram of CCSDS HPE transmitter and photon counting receiver model. The model includes detector effects such as blocking loss and jitter insertion.

3.1 Symbol and slot phase estimation results

The first step in the software receiver is to estimate the symbol and slot phase. Each symbol contains M slots in which there is one signal pulse and an additional M/4 guard slots in which there is never a signal pulse. This feature enables symbol and slot synchronization in the receiver. When photons are received, the first M slots contain signal photons and noise photons and the last M/4 slots only contain noise photons. The phase alignment algorithm[7] includes summing the photon counts in each respective slot over many symbols. This results in a histogram of photon detections per slot, which is used to calculate the symbol boundary, the average signal photons per signal slot (K_s), and the average background photons per slot (K_b). K_b is calculated from the average of the guard slots over the number of symbols. K_s is calculated by subtracting K_b from the average of the signal slots scaled by M. A slot histogram with $K_s = 0.8$, $K_b = 0.001$, and no system effects is shown in Figure 6 (a). The signal slots and the guard slots form a uniform distribution.

The slot histogram distribution changes when detector effects are included in the model. When detector blocking is included, as shown in Figure 6 (b) with 1 detector, the signal slots are not uniformly distributed across the first M slots. Less detections occur at the beginning of a symbol than at the end on average. This effect decreases when using 4 detectors (Figure 6 (c)) instead of 1 detector. The plots also show that there are more photon detections when using 4 detectors instead of 1 detector. When jitter is added, as shown in Figure 6 (d) (1 detector) and (e) (4 detectors), inter-slot interference occurs, and this can be seen in an increase in photon counts in the guard slots adjacent to the first and last signal slot. Results are shown in Figure 6 (f) when both detector blocking, detector jitter, and a slot phase offset are included in the simulation. The slot phase offset occurs when the receiver is not perfectly aligned to the beginning of the symbol or when each detector channel is not perfectly phase aligned. This results in inter-slot interference. The phase offset is shown in the plot because the first guard slot is larger than the last. Detector blocking, system jitter, and phase misalignment impact

the calculation result for K_s and K_b. K_s is lower on average in the first slot of the symbol than in the last signal slot due to blocking. K_b is higher in guard slots adjacent to signal slots due to jitter or slot phase misalignment.

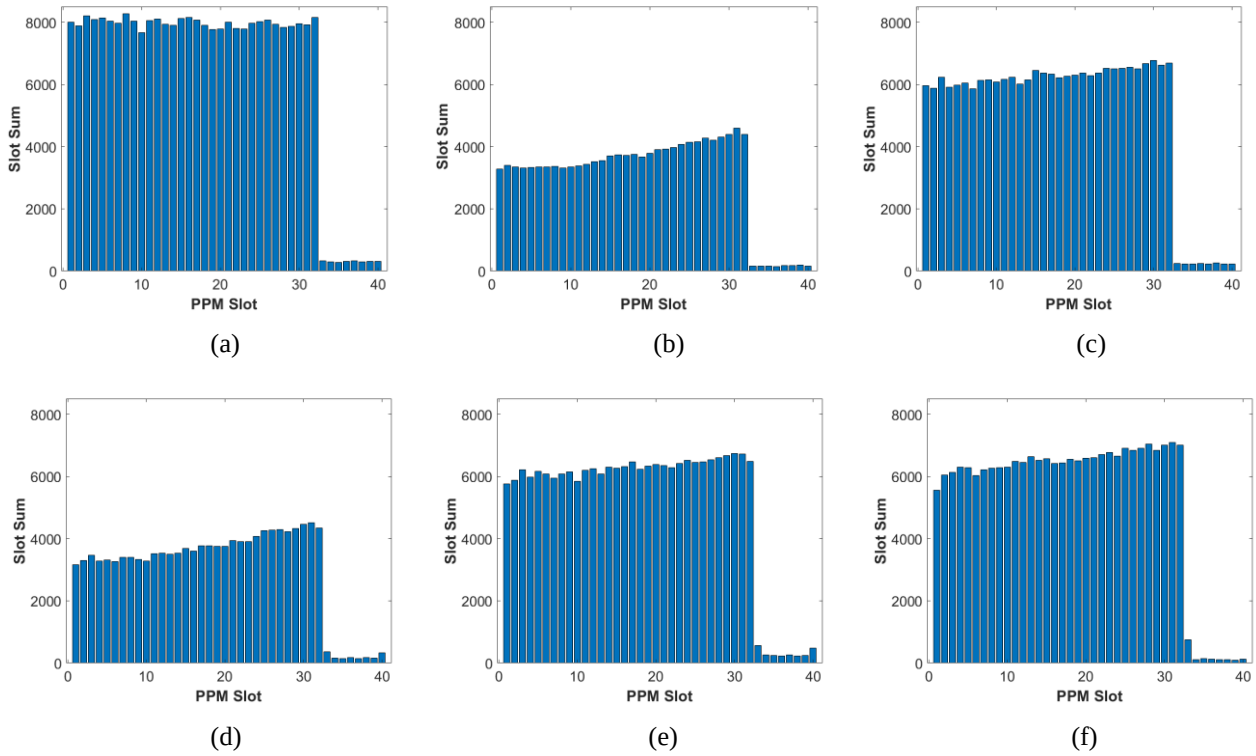


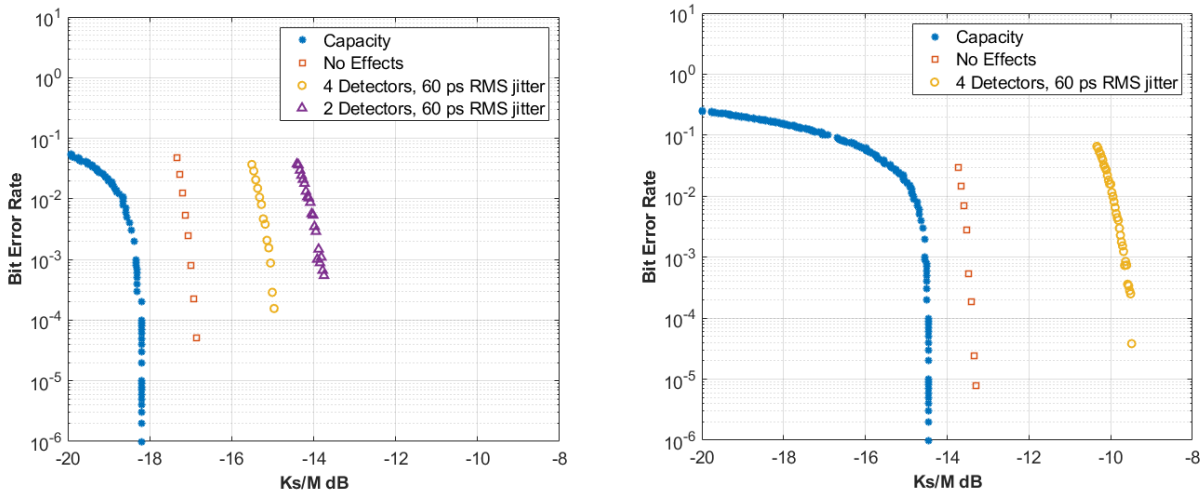
Figure 6. Slot phase estimation histogram results over 100 codewords for the PPM-32, code rate 1/3, 0.5 ns slot, mode with K_s=0.8 and K_b=0.001. (a) no additional effects; (b) 1 detector, 25 ns detector blocking; (c) 4 detectors, 25 ns detector blocking; (d) 60 ps RMS system jitter, 1 detector, 25 ns detector blocking; (e) 60 ps RMS system jitter, 4 detectors, 25 ns detector blocking; (f) 60 ps RMS system jitter, 4 detectors, 25 ns detector blocking, with a slot phase offset

3.2 Bit error rate (BER) curve simulation results

Simulation results are presented for the PPM-32, code rate 1/3, 0.5 ns slot, 81 Mbps mode and for the PPM-16, code rate 1/3, 0.5 ns slot, 130 Mbps mode. Detector blocking (25 ns) and system jitter (60 ps RMS) effects are also included. The detector channels are perfectly aligned in the simulation. The background photon counts per slot are K_b = 0.001 for PPM-32 and K_b=0.01 for PPM-16. The input signal photon counts (K_s) are varied to produce a BER curve. Each point on the curve is simulated using 1,000 codewords. The number of detector channels simulated is 2 and 4. The PPM capacity BER curve[9, 10] was also simulated using the Monte Carlo method.

The PPM-32 mode results are shown in Figure 7(a). The capacity, baseline with no additional effects, 4 detectors, and 2 detectors BER curves are plotted. When the number of detectors is limited to 4, the curve shifts 2 dB to the right from the baseline. The 4 detector simulation performs 0.8 dB better than the 2 detector simulation. The simulation results indicate this mode should be able to successfully close the link with at least 2 or more detectors.

The PPM-16 mode simulation results are shown in Figure 7(b). The capacity, baseline, and 4 detector BER curves are plotted in this figure. When 4 detectors are used, the curve shifts to the right by 4 dB compared to the baseline curve. The simulation results indicate this mode should successfully close the link with at least 4 or more detectors.



(a) (b)

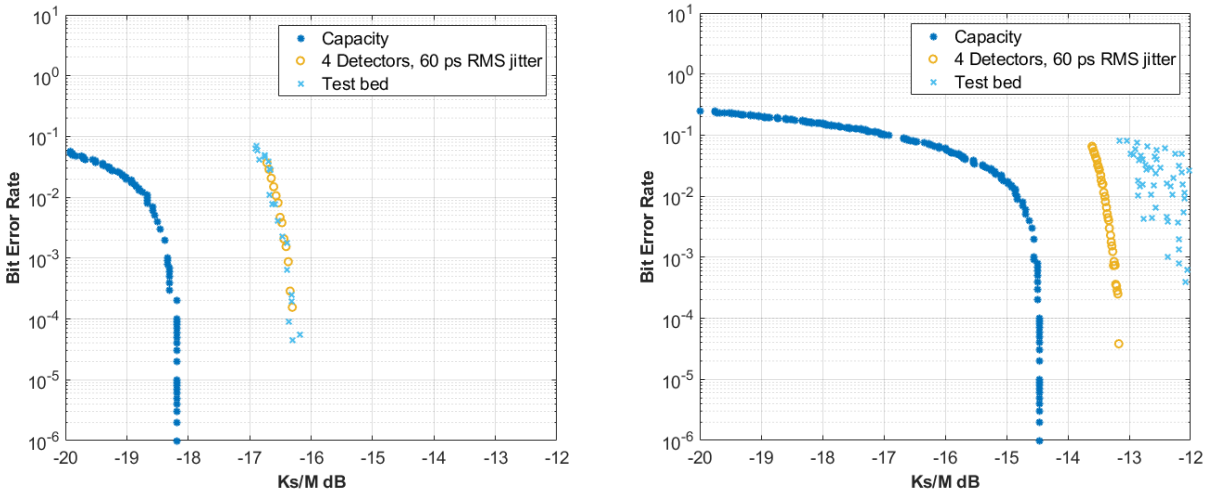
Figure 7. Simulation results for (a) PPM-32, code rate 1/3, 0.5 ns slot, 81 Mbps mode; Kb=0.001 and (b) PPM-16, code rate 1/3, 0.5 ns slot, 130 Mbps mode; Kb=0.01

4. SYSTEM TEST RESULTS AND DESCRIPTION

System testing was conducted using the PPM-32, code rate 1/3, 0.5 ns slot, 81 Mbps mode and the PPM-16, code rate 1/3, 0.5 ns slot, 130 Mbps mode. Four SNSPD channels were used for both tests. BER curve results are presented in Figure 8 (a) for PPM-32 and Figure 8 (b) for PPM-16. The K_s in these figures is the detected photons per signal slot, which is calculated in the software receiver. The capacity, simulation, and test bed results are plotted.

Receiver metrics were calculated for both modes. The received symbol and slot phase was calculated for each data point on the curves. For PPM-32, the channels were aligned to within an average of 10% of a slot (50 ps). For PPM-16, the detector channels were aligned to an average of 14% of a slot (70 ps). Detection efficiency was calculated from the measured input power and the detector blocking loss characterization results. The detection efficiency of the PPM-32 mode was ~70% and was ~30% for the PPM-16 mode. The detection efficiency is lower for the PPM-16 mode because the detected photon flux rate needed to close the link requires operating the detectors in the region of lower efficiency.

The results in Figure 8 (a) for PPM-32 show that the test bed data matches the simulated data very well. The testing results for the PPM-16 mode are spread out over 1 dB and are shifted 1 dB to the right of the simulated curve. The test bed results indicate that perhaps there was more jitter in the system than expected. This could be due to time walk[11] of the detector pulses. At higher photon flux levels, such as those used in the PPM-16 mode, the pulse heights vary more, but have the same rise time. For the threshold-based photon counting method used in this paper, this amplitude variance creates a time walk, in which the detection time varies with the pulse amplitude. This looks like additional jitter to the receiver.



(a) (b)

Figure 8. System testing BER curve results compared to simulation results from the (a) PPM-32, 0.5 ns slot, code rate 1/3, 81 Mbps mode; K_b=0.001; (b) PPM-16, 0.5 ns slot, code rate 1/3, 130 Mbps mode; K_b=0.01

5. CONCLUSION AND FUTURE WORK

A photon counting test bed with a SNSPD array-based receiver has been simulated and implemented in a test bed. The system is designed to transmit and receive the CCSDS Optical Communications HPE telemetry link waveform. Simulation results indicate that detector arraying is necessary for the PPM-32, code rate 1/3, 0.5 ns slot, 81 Mbps mode and the PPM-16, code rate 1/3, 0.5 ns slot, 130 Mbps mode. The PPM-32 mode should need least 2 detectors and the PPM-16 mode should need at least 4 detectors to close the link. The PPM-32 and PPM-16 modes were both successfully received with 4 detectors in the photon counting test bed. By using an array of 4 detectors, the data rate increased to 130 Mbps from 40 Mbps with a single detector. Simulation results match the test bed data for PPM-32, but are 1 dB different for PPM-16. A possible cause includes increased jitter due to detector pulse time walk at high photon flux rates. This problem will be investigated in the future.

Improvements can also be made in the detector blocking and efficiency model. The model presented in this paper utilizes a fixed time for detector blocking. Detector efficiency loss is not simulated, but could be applied after the simulation by scaling the input K_s. The model could be improved by incorporating detector blocking and efficiency as a function of the time since the last detection.

ACKNOWLEDGEMENTS

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