Radiation-Hard Parallel Readout Circuit for Low-Frequency Voltage Signal Measurements

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ABSTRACT

NASA Goddard Space Flight Center (GSFC) has successfully developed and tested a custom-designed low-noise multi-channel digitizer (MCD) application specific integrated circuit (ASIC) for operation in harsh radiation environments. The MCD-ASIC is optimized for low-frequency and low-voltage signal measurements from sensors and transducers. It has 20 input channels where each channel is comprised of auto-zeroed chopper variable-gain amplifier, post amplifier, and a second order ΣΔ modulator. ΣΔ analog-to-digital converter (ADC) relies on oversampling and noise shaping to achieve high-resolution conversion. However, the MCD-ASIC requires digital filtering and decimation to convert the output single bit streams from the ADC to useful data words. A parallel digital platform such as a field-programmable-gate-array (FPGA) is highly suitable to fully leverage the capabilities of the MCD-ASIC. The FPGA controls the MCD-ASIC via serial peripheral interface (SPI) protocol and acquires data from it. A Python-script communicates with the FPGA board through a USB interface on a cross operating platform. Using this architecture, the system is capable of monitoring up to 20 voltage readout channels simultaneously in a real-time manner. Each channel's parameters can be programmed independently allowing maximum user versatility. In this paper, we present analysis of the analog front-end, the implementation of the digital processing unit on the FPGA, and provide noise performance results from the MCD-ASIC readout.

Keywords: ASIC, FPGA, amplifier, low-frequency, ADC, thermopile detectors, parallel readout, radiation hard

1. INTRODUCTION

A fully custom radiation-hardened-by-design MCD-ASIC [1,2] was fabricated using theTowerJazz Semiconductor's 180 nm CMOS CA18HD process node for the near-DC front-end readout of a thermopile focal plane array on a remote sensing instrument concept for a future NASA Europa Mission, *i.e.*, "Thermal Imager for Europa Reconnaissance and Science (TIMERS)" [3]. Over the last few years, the ASIC has matured to a third-generation chip and is currently the baseline readout scheme for thermopile detectors on net flux radiometer concepts for the gas and ice giant planets [4-6]. In previous chip generations the ASIC was operated by a micro-controller, although simple to operate, it limited the readout to only one channel at a time, *i.e.,* serial mode. To fully unlock the maximum capabilities of the ASIC, an FPGA has been implemented to the system architecture in order to readout in parallel mode.

Thermopile detectors are two terminal devices, sensitive in the long wavelength infra-red spectral region that outputs a voltage proportional to the incident infrared radiation power. These detectors show no *1/f* noise or offset drift, and can achieve a system Noise Equivalent Temperature Difference ≤ 60 mK at 300 K, 30 Hz, *f*# /1.0 (many references in the literature). In the thermopile detector readout system described here, the analog front-end of ASIC is optimized for low-frequency signal measurement. Amplification before digitizing is the most common pre-processing step in such an application. The thermopile output voltage's frequency is usually less than 100 Hz and can be classified as a low-frequency measurement. Unfortunately, the presence of thermal noise or $1/f$ noise in the amplifier chain and ADC are the most dominant sources contributing to the loss of signal fidelity. Simple averaging/integrating will not eliminate the $1/f$ noise near the DC region since it requires unpractical large number of sampling to reduce the variance. In this manuscript, a description of the end-to-end readout circuit and its mixed-signal processing techniques to overcome such shortcomings is presented, *i.e.*, the MCD-ASIC under FPGA control, along with its frequency response and noise characterization.

1.1 The Multi-Channel Digitizer Third Generation (MCD3G) ASIC

The MCD3G-ASIC (hereafter called ASIC) is a 180 nm CMOS system on a chip, with a die size of 1 mm^2. It includes 20 channels which contain variable-gain zero-offset amplifier with ΣΔ ADC to digitize a microvolt level signal and 6 transimpedance amplifiers (TIA) for current measurement. The ASIC employs two mechanisms to suppress the offset voltage and thermal noise [7, 8]. Moreover, the chip has 10 Digital-to-Analog Converters (DAC), 8 bias current generators which can be used for sensor biasing, and a crystal stabilized oscillator that is not used in this application. The ASIC's analog front-end is designed for maximum versatility; therefore, most of its functionality is programmable by the controller block, which is accessible via an SPI port. For low power consumption, the ASIC uses 1.8V CMOS technology with supply current less than 200 mA. Figure 1 shows the ASIC architecture block diagram and its highlighted features are shown in Table 1.

Table 1. Highlighted features of the ASIC.

Type	Feature	Note
ANALOG/MIXED SIGNAL FEATURE	40x Input, High Resolution Digitizer	Interlace mode can read up to 40 Input by multiplexing
	6x Transimpedance Amplifiers	Transimpedance Amplifier for current measurement
	21x 16-bit Sigma Delta ADCs	20 ADCs for data acquisition, 1 for housekeeping
	10x 8-bit Buffered Output Voltage DACs	Bias voltage generator
	8x thermistor bias outputs	For temperature measurement
	Crystal stabilized oscillator (up to 20MHz)	For stand-alone operation
	Timing Generator with programmable clock divider	For chopping circuit
	Bandgap reference and temperature sensor	Housekeeping data
	Low Gain (1/6/12/25) and High Gain (> 25) Modes	Variable gain amplifier for versatile analog input
	User defined ΣΔADC speed/resolution (Max fCLK=2MHz)	Programmable modulation speed
	Chopper Stabilized with Optional Auto-Zero	To reduce 1/f noise and offset of non-idea amplifier
	Radiation Hardened by Design (TID > 10 Mrad; no SEL up to 174MeV-cm2/mg; SEU protection mode)	For space instrument development
DIGITAL FEATURE	SPI compatible serial control port	Slave mode only
	Master Reset and Global Power down	Asynchronous reset
	21x 1-bit ADC Outputs	1.8V CMOS technology
	LVDS Clock Input and Muxed Data Output	For long distance data transfer
POWER	Single 1.8 V Supply Operation Supply current: 2 mA to 200mA @ 1.8 V Power-Down: < 100 µA	Low power Consumption

1.2 ZEM5310 FPGA Evaluation Platform for Multi-Channel Data Acquisition

Recently, there has been a trend in the implementation of reconfigurable instrumentation based on FPGAs [9]. The high flexibility and high computational resource with real-time deterministic response makes FPGA's outstanding candidates for digital, time-critical back-end applications. With their fully programmable nature, the interface to a custom ASIC can be easily developed. Commercially available, off-the-shelf FPGA boards provide a cost-effective platform for application development. The ZEM5310 FPGA evaluation board from Opal Kelly Inc. with its high-speed on-board memory and extensive I/O capabilities makes it suitable for multi-channel data acquisition system like the ASIC described here. Moreover, the vendor provides a rich set of support libraries, including USB 3.0 driver and board support packages for Python. These libraries enable an easy way to access the internal data for debugging and analysis. With the peak performance of the USB 3.0 at 340 MiB/s, pairing the ASIC with the ZEM5310 FPGA module is an optimal solution for parallel data acquisition for rapid measurement instrumentation with versatile analog inputs. Its block diagram is shown Figure 2. The highlighted features of ZEM5310 FPGA are shown in Table 2.

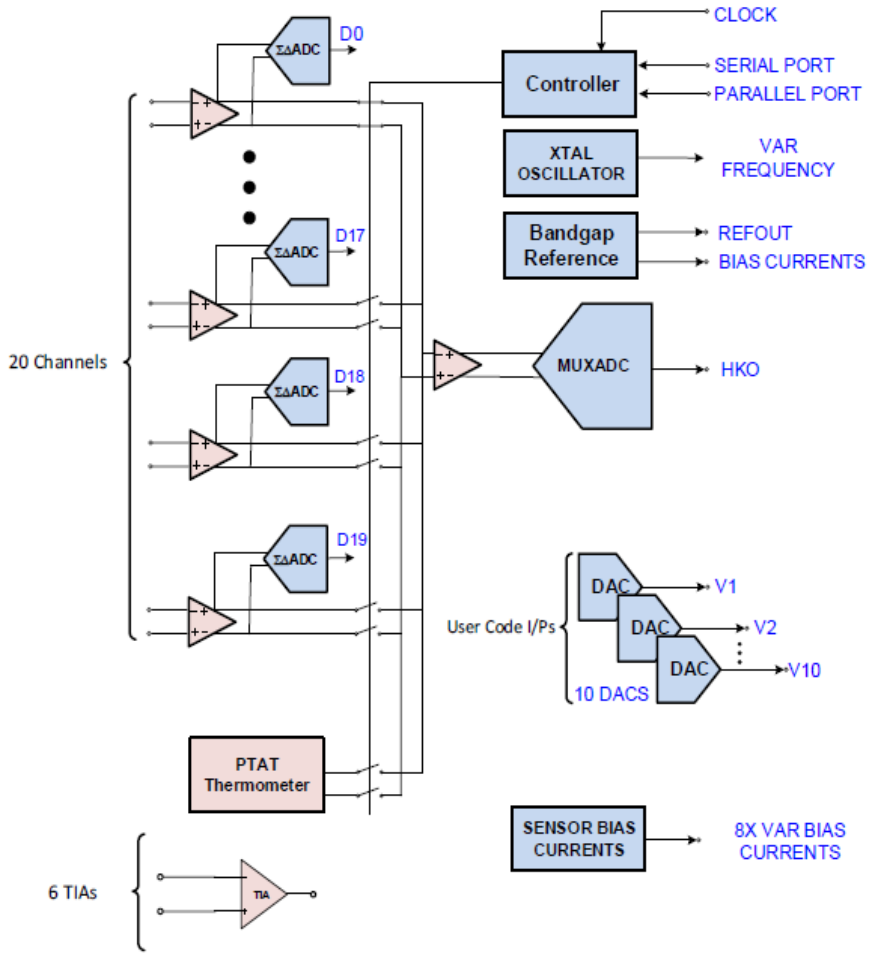


Figure 2. General Block Diagram of the MCD3G ASIC.

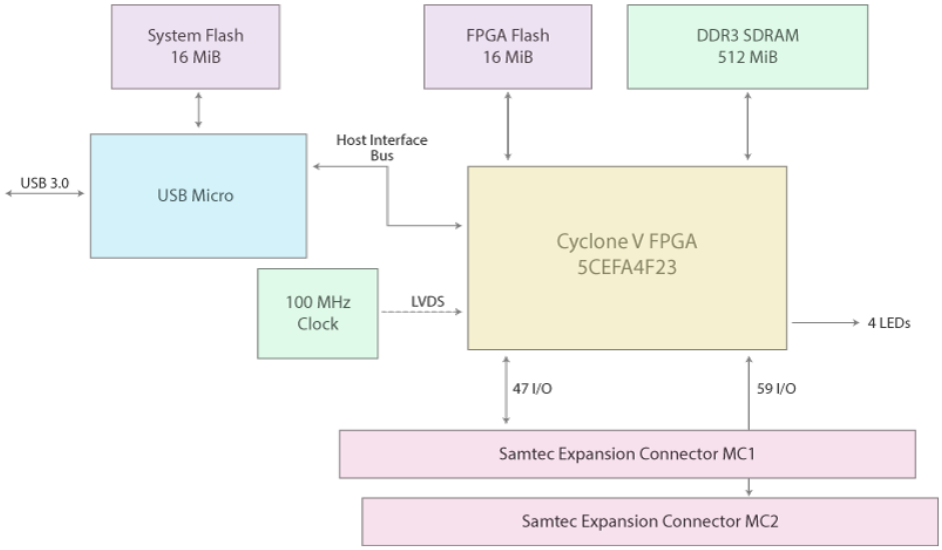


Figure 3. ZEM5310 FPGA evaluation board block diagram. *Note: Cyclone V is the name of the FPGA chip family.*

Table 2. Highlighted features of ZEM5310 FPGA evaluation board.

Type	Features and Specifications
FPGA core	Altera Cyclone V E (5CEFA4F23C7N)
Memory	2x 16-MiB serial flash (Numonyx N25Q128A)
	512-MiByte DDR3 (Micron MT41K256M16TW or equivalent)
Interface	**SuperSpeed USB 3.0 interface (Cypress FX3)**
I/O	106 user I/O including 2 CLKOUT and 4 CLK
API	Complete Application Programmer's Interface (API) in C, C++, C#, Ruby, Python, and Java

2. PARALLEL READOUT CIRCUIT

The parallel readout circuit is realized by combining two key hardware components: the ASIC and the FPGA evaluation board. All strict real-time requirement modules are self-contained on the FPGA. However, a graphical software interface on a personal computer (PC) enables users to have a deeper layer of analysis. Moreover, advanced software processing algorithms are usually available on high level programming language like Python. To take advantage of such features, we implemented an architecture of using USB interface to transfer data between the PC and the FPGA module. The demonstration of the data flow of the system is shown in Figure 3. The data acquisition operation is initialed by a Python script. It will read-out a text file that contains address/data/control-signal configuration for the ASIC. Sequentially, it will pass all the information to the FPGA board through a USB module. The FPGA works as a bridge to relay that information to the MCD-ASIC through the SPI protocol. After successfully programming the MCD-ASIC, the FPGA will capture the raw single bit data stream from the output of the ADCs on the ASIC and decimate it into useful data words. The reason to separate output bit streams of the ADCs from the SPI are (1) to allow continuous real-time fully parallel acquisition of the measured voltages and (2) allow SPI updates to happen while the ADC data is streaming out. Also, the decimator is left off the ASIC to allow flexibility in the filter type and order. In this paper, a Sinc filter is used as a study case, for other applications more sophisticated filters can be used to extract narrower bandwidth. To manage the data flow in and out to the FPGA, a finite state machine as the First-in-First-Out (FIFO) controller with FIFO buffer has been implemented. Finally, the Python script will retrieve data from the FIFO buffer via USB protocol when it is finished collecting samples and compute the Fourier transform spectrum of the signal.

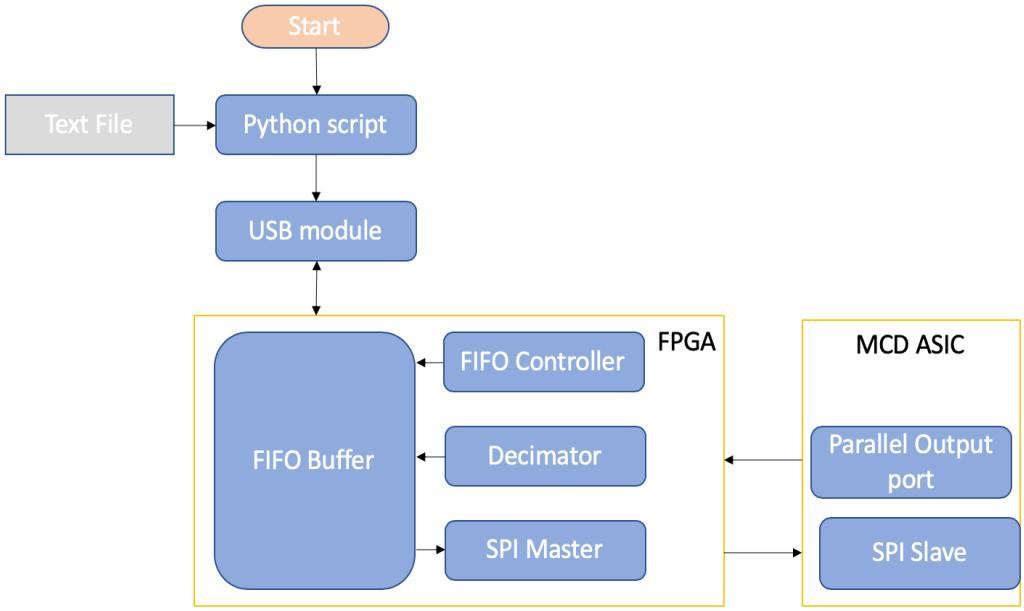


Figure 4. Data flow of the readout circuit.

2.1 Chopping Amplification

As mentioned in the previous section. $1/f$ noise is the most dominant in low-frequency measurement system. Beside from $1/f$ noise of the existing components, amplifier offset also contribute to degradation in performance of such systems [10-11]. To mitigate these noise effects, we utilized a Gated Correlated Double Sampling (CDS) technique to reduce offset, drift, and low-frequency noise. The topology of a single channel CDS is shown in Figure 4. The chopping circuit switches between analog input (AIN) and the common reference voltage (CM REF). It should be note that the detector is biased by a common reference voltage to position the voltage swing inside the dynamic range of the ADC. From a mathematical viewpoint, it can be shown as demonstrated below that the CDS behaves as a high-frequency filter for only the noise signal [12].

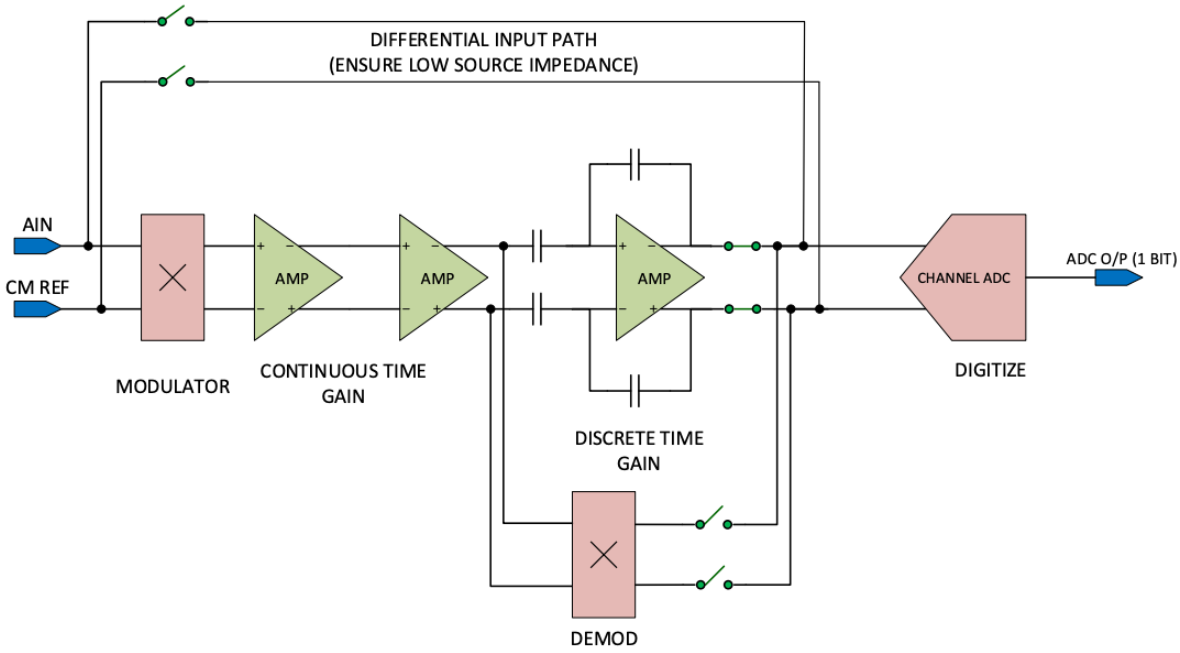


Figure 5. A typical channel topology that consists of a chopping circuit, a variable gain amplifier, and an ΣΔ ADC for each channel. The ADC's input is multiplexed between nodes within a channel and can be programmed.

The direct measurement is:

$$V_{ain} = V_{signal} + V_{noise} + V_{offset} + V_{cm\_ref} \tag{1}$$

The common reference voltage measurement is:

$$V_{cm\_ref\_meas} = V_{noise} + V_{offset} + V_{cm\_ref} \tag{2}$$

Subtracting the common reference voltage measurement from the direct measurement gives:

$$V = \left(V_{signal} + V_{noise} + V_{offset} + V_{cm\_ref}\right) - \left(V_{noise} + V_{offset} + V_{cm\_ref}\right) * Z^{-1} \tag{3}$$

with Z^{-1} as the delay operator. Since V_{offset} and V_{cm_ref} are static and do not change from sample to sample, Eq. (3) reduces to:

$$V = V_{signal} + V_{noise} * \left(1 - \frac{1}{Z}\right). \tag{4}$$

Using the bilinear transformation,

$$Z = \frac{1+\frac{sT}{2}}{1-\frac{sT}{2}} \tag{5}$$

and substituting Eq. (5) into Eq. (4), and replacing $T = 1/f$, give:

$$V = V_{signal} + V_{noise} * (\frac{2s}{s+2f_{sample}}). \tag{6}$$

The frequency response of the transfer function to V_{noise} exhibits a high-pass characteristic as shown in Figure 5. However, it affects only the $1/f$ noise portion of the signal, *i.e.,* the detector's output signal at higher frequencies remains unchanged. The CDS is still vulnerable to offset voltage of the non-ideal amplifier. In practice, if the offset voltage is too high, Eq. (4) approaches zero and the CDS becomes useless. To avoid this problem, an auto-zero differential amplifier is recommended to use as companion technique, especially for applications requiring high gain input [8].

2.2 ΣΔ ADC Modulator

Each ADC channel consists of a second order ΣΔ modulator to sample the ADC input at a rate f_{mod} which is many times faster than the output data rate f_{DR}. By oversampling the signal, with a discrete-time feedback system, it allows the sampled input signal to pass at unity gain, while quantization noise is shaped to have higher density at high frequency. However, the ΣΔ modulator only outputs a low-resolution single bit stream, so a digital filter such as a Sinc filter must be used to remove the high frequency noise and decimate the single bit stream to a high resolution data word. The combination of the oversampling ratio (OSR) defined as $f_{DR} = f_{mod}/OSR$ and the filter type determines the output bandwidth and the resulting overall frequency response.

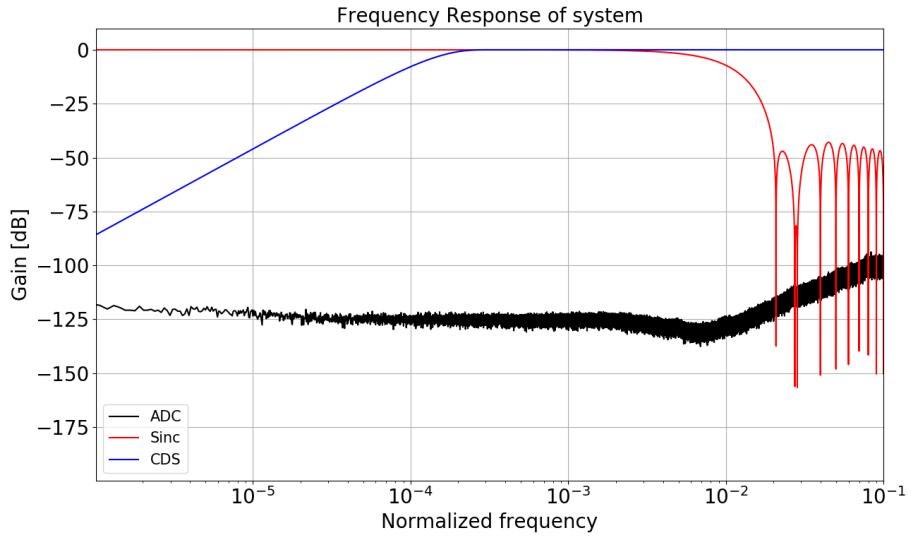


Figure 6. Frequency response of the system. Note that the CDS response only applied to noise signal.

It is interesting to note that the spectrum of the ADC is very flat in the low frequency region with no idle tones measured in the band of interest, *i.e.*, from 10^{-4} *to* 10^{-3} of the modulation frequency. Quantization noise of the ADC begins to ramp-up at 10^{-2} of the modulation frequency increasing by ~30 dB/decade which is removed by the Sinc filter.

3. EXPERIMENTAL RESULTS

In-house firmware for FPGA was developed to verify the operation of the ASIC. A 3rd order Sinc filter was employed on the FPGA to decimate the single bit stream into 24-bit data words with $f_{MOD} = 250\ kHz\ and\ OSR = 1024$. After successfully programming the MCD-ASIC, an oscilloscope was used to monitor the output data stream. Figure 6

shows the output data change of one channel versus the modulation clock. As expected, output single bit from an ADC changes at the falling edge of the modulation clock and is valid at the rising edge.

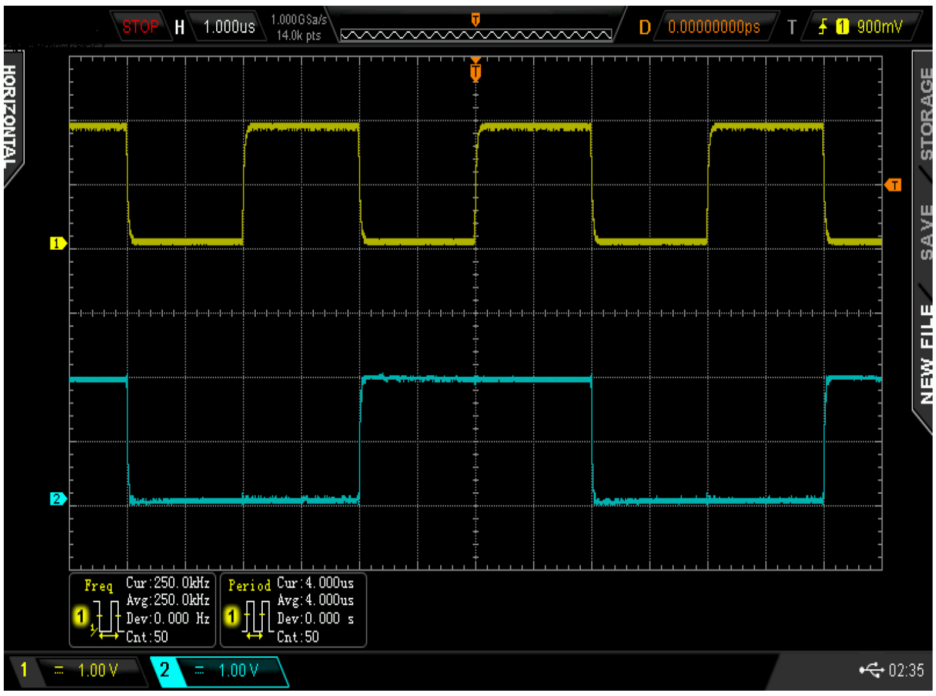
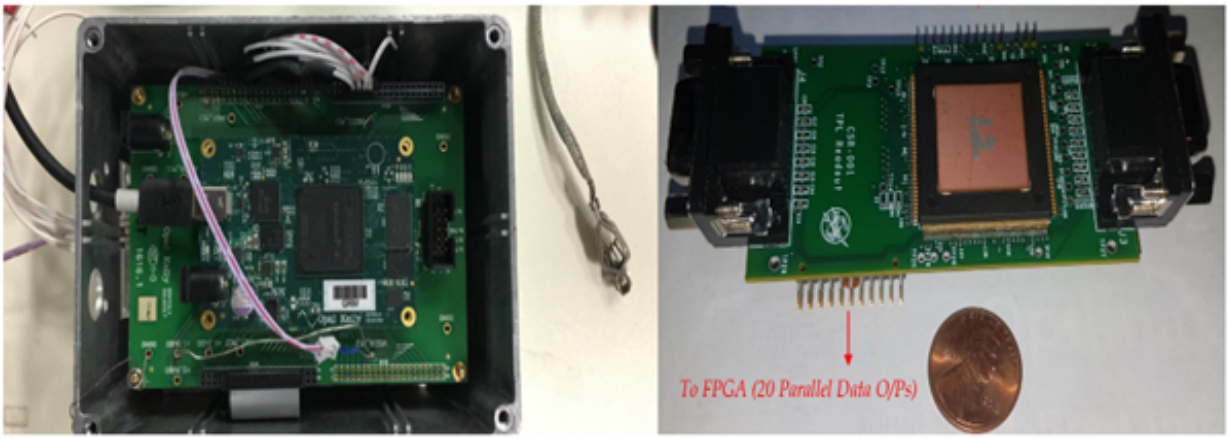


Figure 7. Output data vs modulation clock (yellow trace) at 250 kHz.

For noise measurement experiment, and in order to accurately measure the noise spectrum of a typical channel, the ADC's input was shorted to the common mode reference voltage to minimize interference from external noise sources. To further reduce the influence of ambient noise, both FPGA evaluation board and MCD-ASIC are integrated into a Faraday cage as shown in Figure 7. The number of samples that were collected to compute the noise spectrum was 65536. The result (Figure 8 bottom) shows a very low-noise performance ~12 $nV/\sqrt{Hz}$ in the low frequency region. The noise characteristic of the system is shown in Figure 8. The noise spectrum is similar to a band-pass response due to the convolution effect of the CDS and Sinc3 filter. However, there is no systematic noise detected, only random noise present during the experiment. As can be seen from the Figure 8 (top right), the underlying distribution of the data is approximated by a Gaussian distribution while sample density of the noise measurement remained constant over time.



(a) (b)

Figure 8. Boards are housed in a metal box Faraday cage; (a) shows the FPGA board and (b) MCD3G-ASIC board located underneath it.

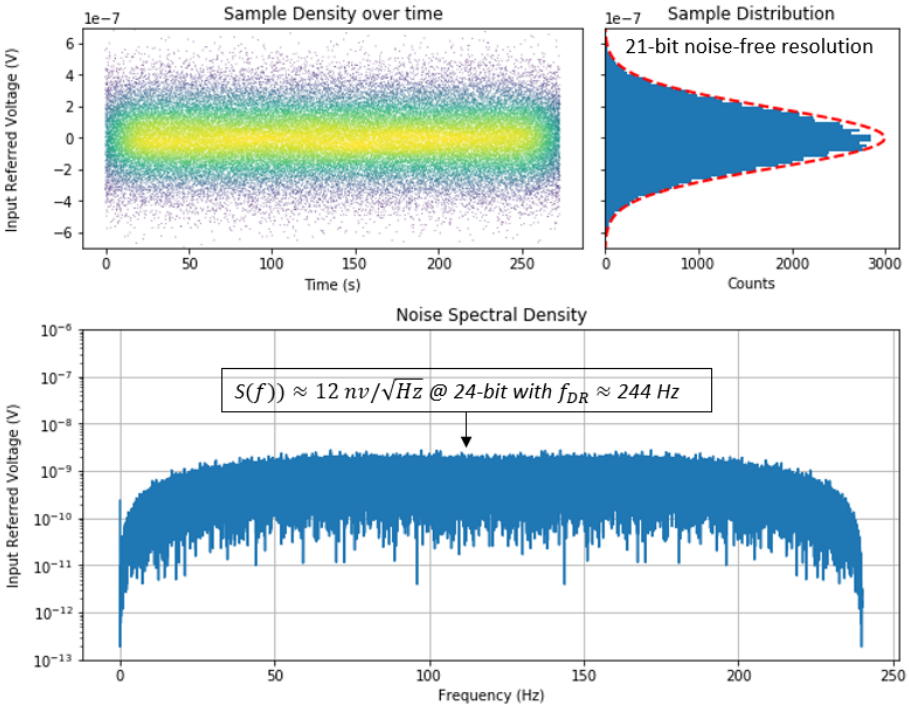


Figure 9. MCD-ASIC noise spectrum with an ADC sample rate of 240 Hz, channel gain of 250, and modulating frequency of 64 kHz.

After successfully characterizing each individual readout channel, to demonstrate integrity of the parallel readout circuit, the readout performance for thermopile channels on a Non-Dispersive Infra-Red Gas Analyzer (NDIRGA) was characterized. The NDIRGA is used for measuring the partial pressures of H_2O and CO_2 vapor sublimated from ice as a function of temperature, a proposed instrument subsystem for the Comet Astrobiology Exploration Sample Return (CAESAR) New Frontiers 4 mission and the tests were conducted in a thermal vacuum chamber during Phase A [14]. The test measurement set-up is shown in Figure 9 and includes a quad-channel thermopile and a broadband infrared source operated at 700°C and pulsed at 0.5 Hz. The source radiance is collimated and focused, using infrared lenses, on to the detector to maximize the optical throughput of the system. There is no phase mismatch detected across the channels. The voltage response, in ADC counts, of the 4 thermopile spectral channels, defined by infrared passband filters centered at 2.7 µm, 4.2µm, 3.95µm and 6.58 µm, are shown in Figure 10.

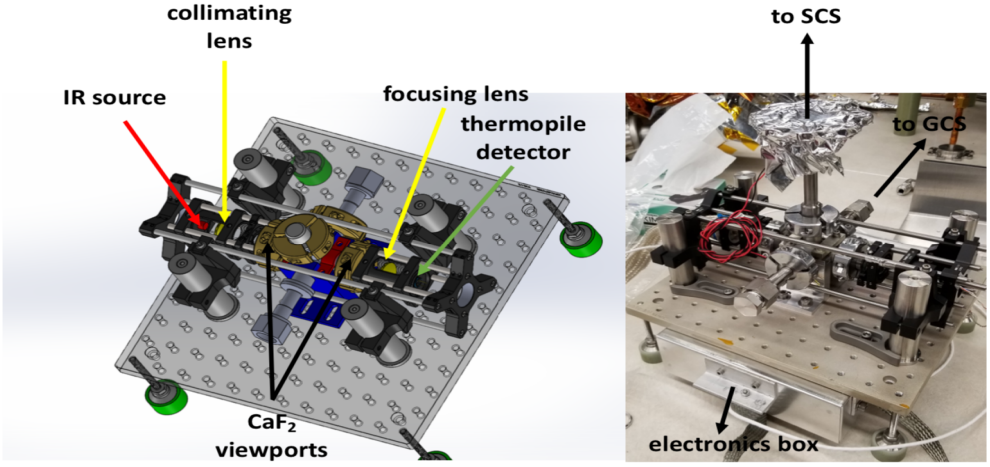


Figure 10. NDIRGA test system for evaluation of parallel readout circuit: (left) optical setup and (right) physical setup (SCS -Sample Containment System; GCS – Gas Containment System, see [14]).

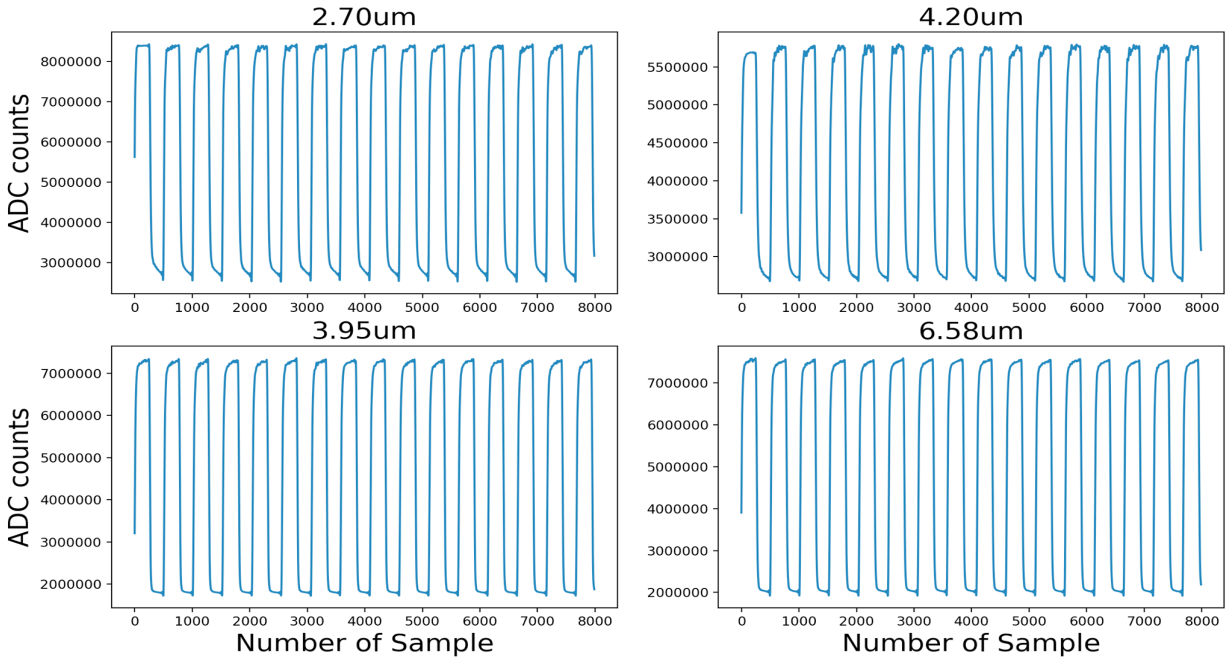


Figure 11. Response of four spectral channels of the quad-thermopile. The infrared source is pulsed at 0.5 Hz which takes 488 samples to finish a cycle at output data rate at 244 Hz.

4. CONCLUSION AND FUTURE WORK

In this paper, a parallel readout circuit, that integrates a custom ASIC with an FPGA, has been demonstrated. By using CDS and ΣΔ ADC to reduce the $1/f$ noise, the readout circuit is optimized for low-frequency measurement. The ASIC showed a very low-noise performance ~$12\,nV/\sqrt{Hz}$ in the low frequency region. This work can be replicated as an essential block for many instruments that use detectors that operate in the low-frequency region.

In future work, a plan is in place to transfer the firmware to a radiation hard FPGA chip to construct a fully radiation hard parallel readout circuit for space-based applications. The road map for this development is shown in Figure 11. The target platform is the SpaceCube v3.0 mini which is currently being developed by NASA GSFC [15]. The FPGA chip on that platform is the XQR Kintex UltraScale KU060 suitable for space applications [16]. The XEM8350-KU60 evaluation board from Opal Kelly Inc. has the commercial counter part of the SpaceCube FPGA on its module. However, the XEM8350 is nearly 9x more expensive than the ZEM5310 that was used in this work. To reduce the cost of development, the firmware was first prototyped on the ZEM5310 platform. Moving the firmware onto the XEM8350 platform is an intermediate step (see Figure 11) to ensure full compatibility with the final target platform. After verifying the results from the intermediate step the firmware will be finally implemented on the SpaceCube FPGA platform ensuring a cost-effective, radiation hard, parallel readout solution.

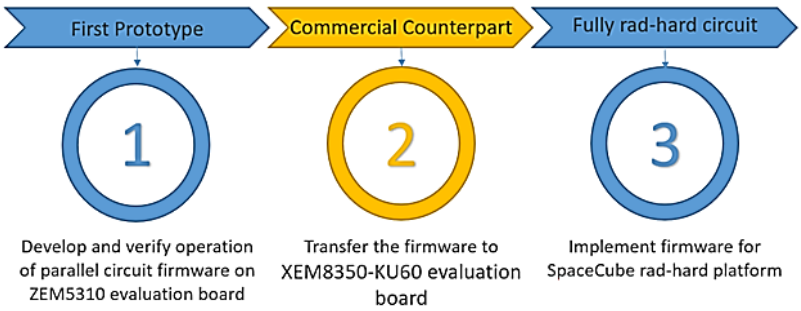


Figure 12. Roadmap for development of a fully radiation hard ASIC-FPGA parallel readout circuit.

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