Recent Radiation Test Results on a 22FDX Test Vehicle

Megan C. Casey[1], Scott Stansberry[2],
Christina Seidleck[2], and Jonathan A. Pellish[1]

[1]NASA Goddard Space Flight Center
[2]ASRC Federal Space and Defense, Inc. (SSAI)

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Acronyms

- DUT – Device Under Test
- pMOS – P-Channel Metal Oxide Semiconductor
- nMOS – N-Channel Metal Oxide Semiconductor
- TID – Total Ionizing Dose
- SOI – Silicon-on-Insulator
- FDSOI – Fully-Depleted Silicon-on-Insulator
- SRAM – Static Random Access Memory
- VPW – P-Well Bias Voltage
- VNW – N-Well Bias Voltage
- SEE – Single-Event Effects
- LBNL – Lawrence Berkeley National Laboratory
- REF – Radiation Effects Facility
- PDSOI – Partially-Depleted Silicon-on-Insulator
- RBB – Reverse Body Bias
- FBB – Forward Body Bias

Introduction

- GlobalFoundries' 22FDX process is a 22 nm fully-depleted SOI process
  - Previous generations were PDSOI (45 nm, 32 nm)
- It employs standard, planar transistors (rather than novel designs like finFETs used in other highly scaled processes)
  - Planar transistors are simpler and less expensive to design and manufacture than 3D
- FDSOI supports body biasing, which can significantly reduce energy consumption
- FDSOI has a built-in insulator layer to control leakage current and minimize capacitance and various types of noise

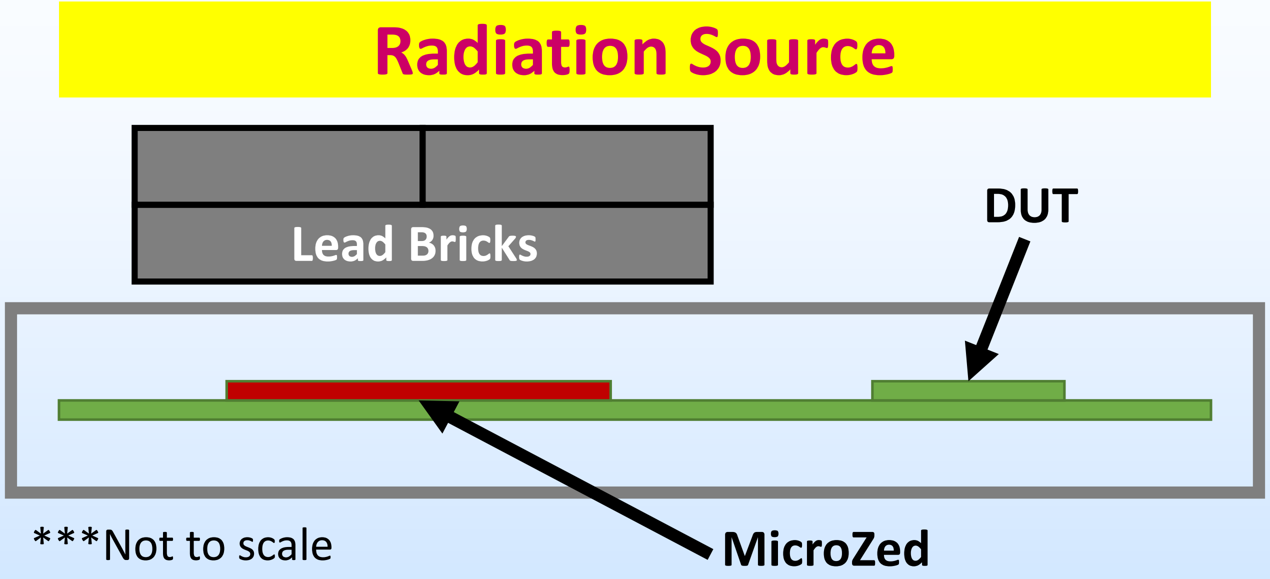
Body Biasing

- 22FDX offers two well configurations
  - Standard: NMOS are located in p-wells and PMOS are located in n-wells
    - Allows for reverse body biasing the transistors and reduces leakage currents
  - Flipped well: NMOS are located in n-wells and PMOS are located in p-wells
    - Allows for forward body biasing and higher performance operation

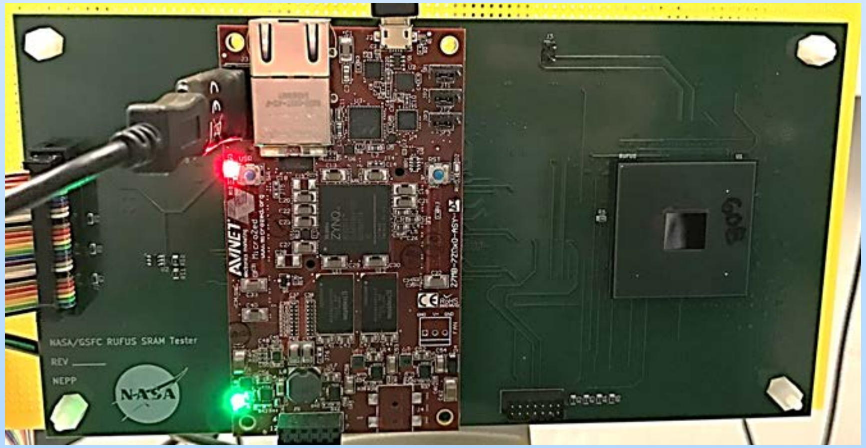
Test Vehicle

- DUTs are a 128-Mb SRAM line monitor circuit
- Nominal supply voltage is 0.8 V, but voltages as low as 0.4 V are supported by the technology
    - The SRAM is theoretically functional from 0.64 V to 1.08 V, but, in practice, normal operation at 0.7 V at the lowest
- The bit cell array is manufactured with all transistors in a p-well, while the n-well is implanted to isolate the SRAM bit cell array
    - NMOS are in the standard configuration (allows reverse body biasing)
    - PMOS are in the flipped well configuration (allows forward body biasing)
- As a result of the n-well only being used for isolation, n-well biasing was expected to have a limited effect on the radiation response of the SRAM

Setup



***Not to scale



- Previous testing indicated MicroZed survived to ~16 krad
- Lead bricks were stacked to reduce dose rate to MicroZeds
- MicroZeds were also replaced before overnight steps

Bias Conditions

During Irradiation

- DUT 609
  - Nominal array voltage (0.8 V)
  - Nominal p-well voltage (0 V)
  - Nominal n-well voltage (0 V)
- DUT 601
  - Nominal array voltage (0.8 V)
  - Extreme p-well voltage (-2 V)
  - Extreme n-well voltage (2 V)

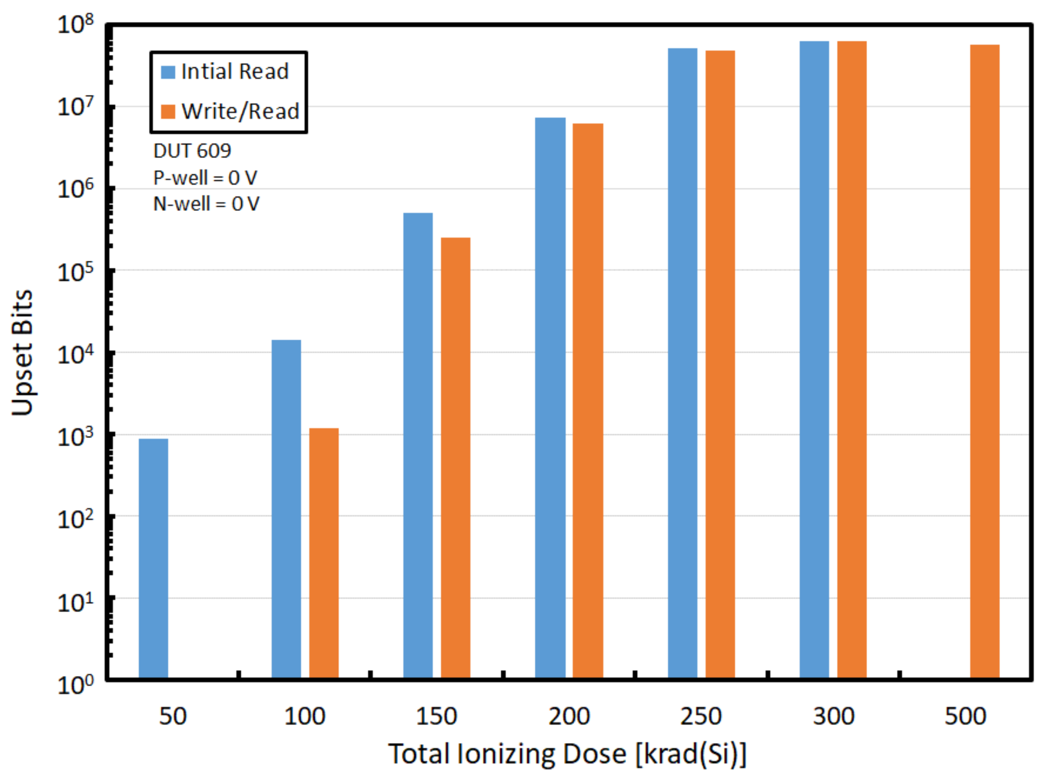
Post-Irradiation Measurements

- Sweep array voltage (0.7 V to 1.08 V), holding n- and p-well voltages constant (0 V)
- Sweep p-well voltage (0 V to -2 V), holding array (0.8 V) and n-well (0 V) voltages constant
- Sweep n-well voltage (0 V to 2 V), holding array (0.8 V) and p-well (0 V) voltages constant
- Sweep p- (0 V to -2 V) and n-well (0 V to 2 V) voltages, holding array (0.8 V) voltage constant
- Measure retention voltage at nominal well voltages

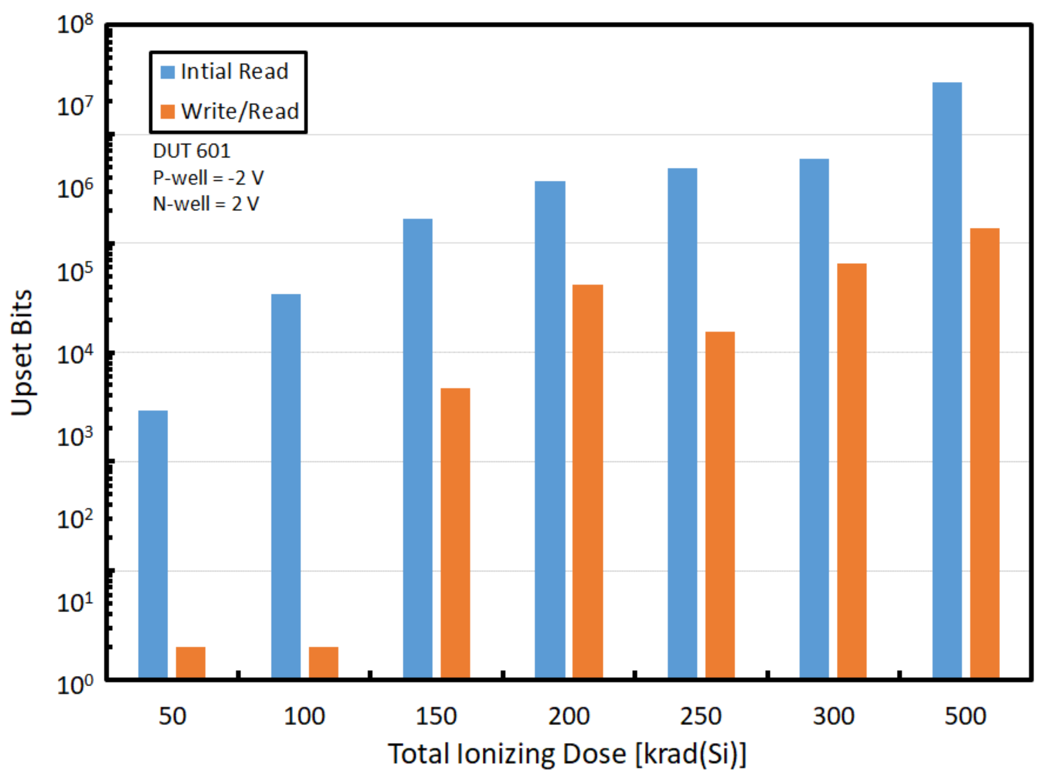
Total Ionizing Dose Test Results

Initial Read

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V

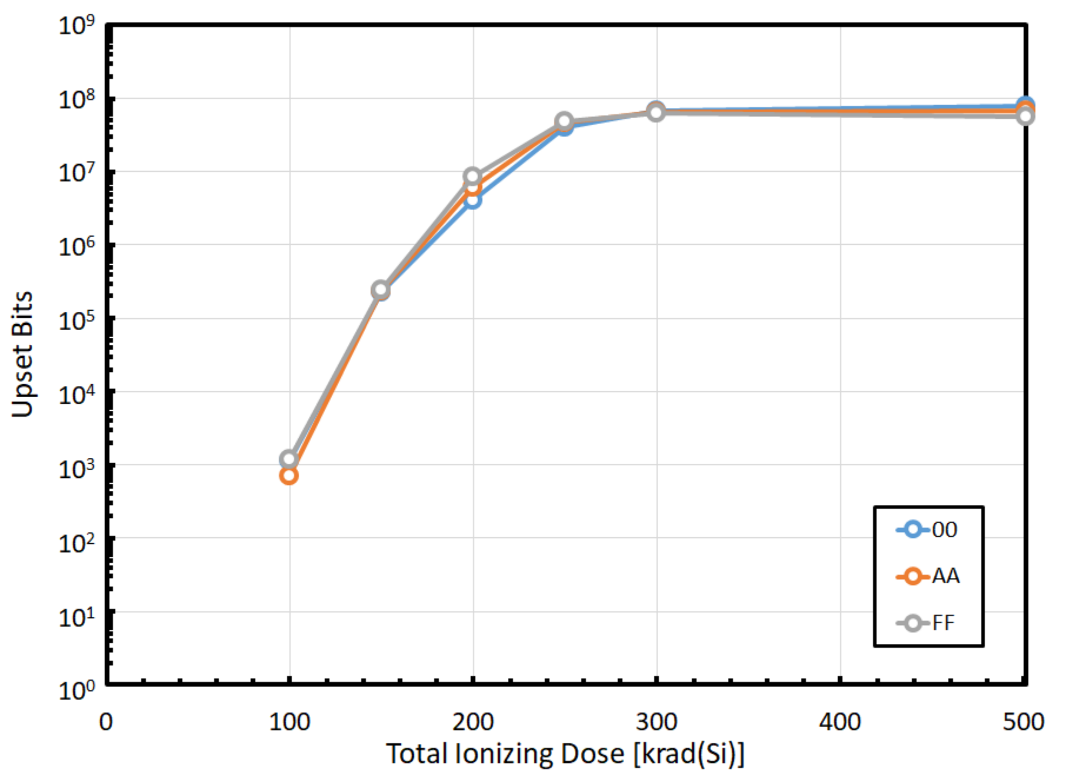


More upsets were observed in part biased with nominal voltage conditions during irradiation

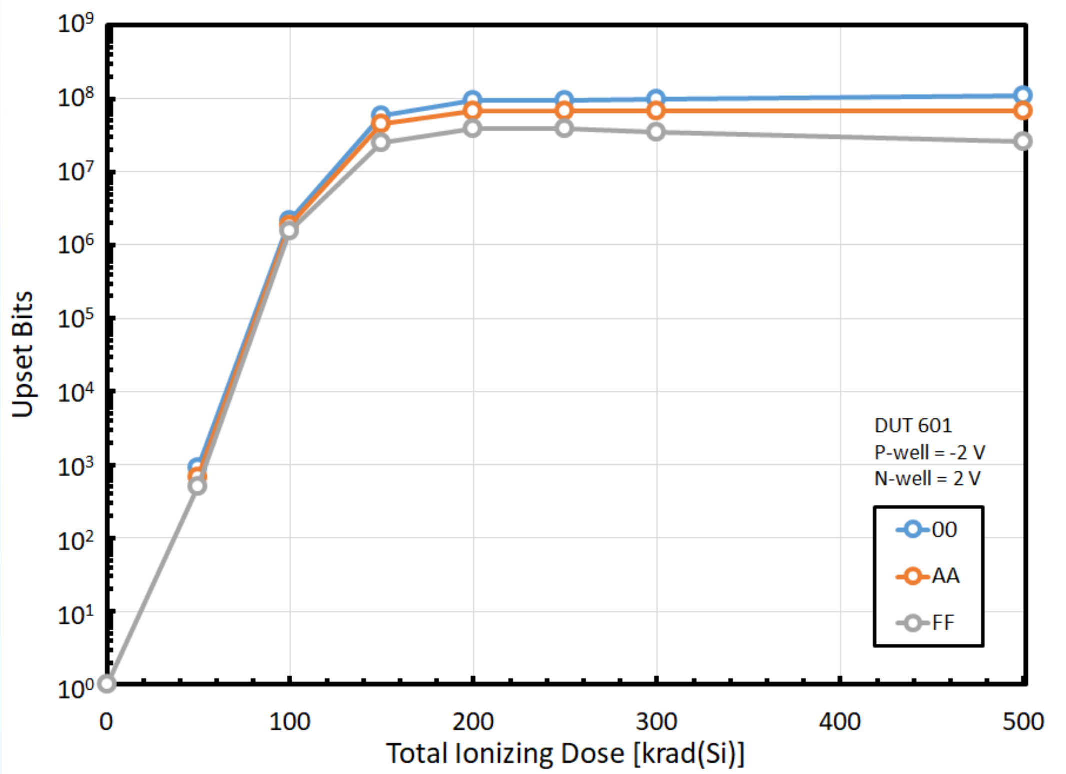
Total Ionizing Dose Test Results

Input Pattern

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V

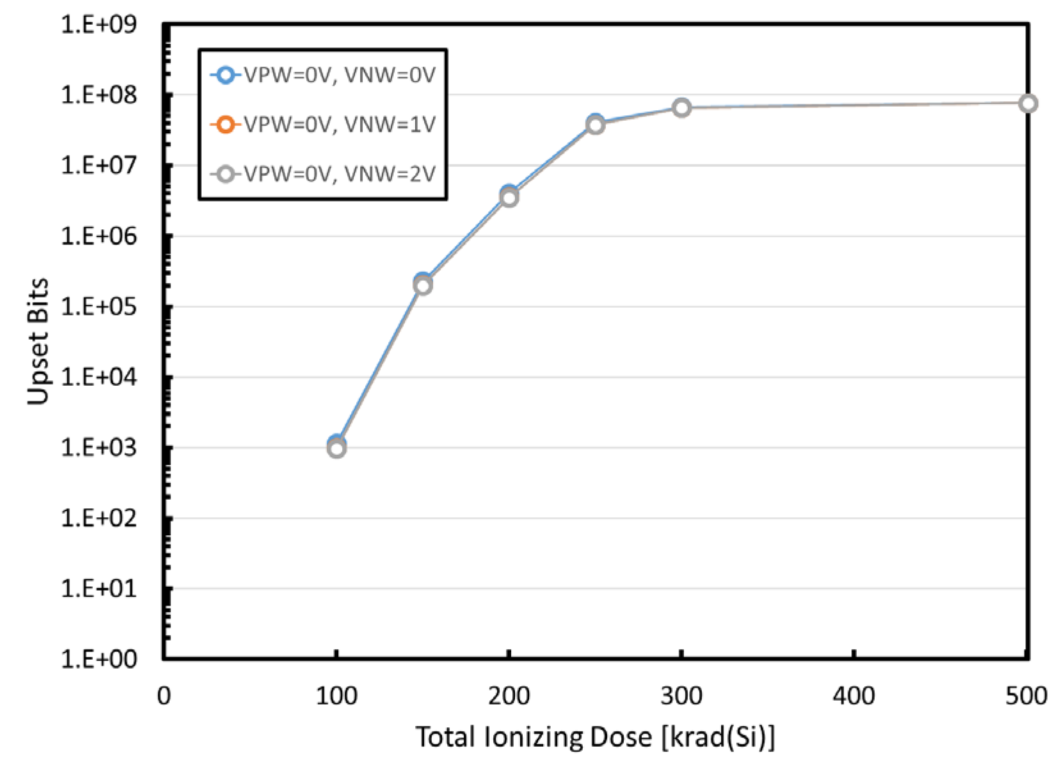


A pattern dependence emerges when biased in the "extreme" conditions during irradiation

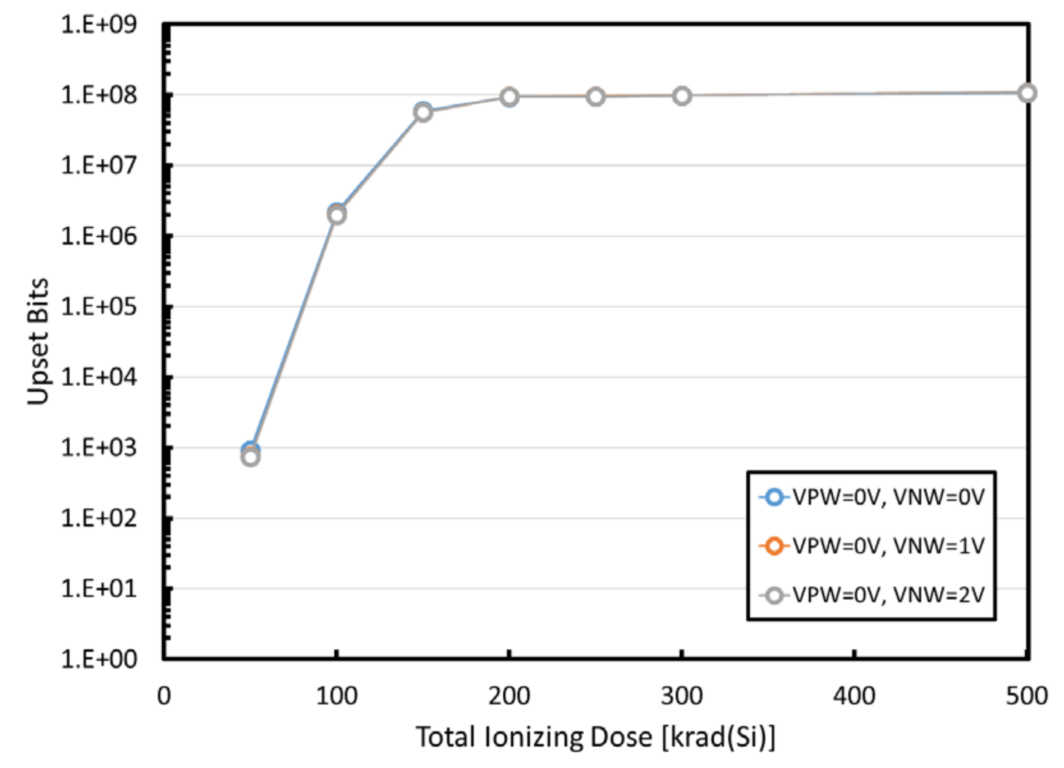
Total Ionizing Dose Test Results

N-Well Bias Voltage

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V

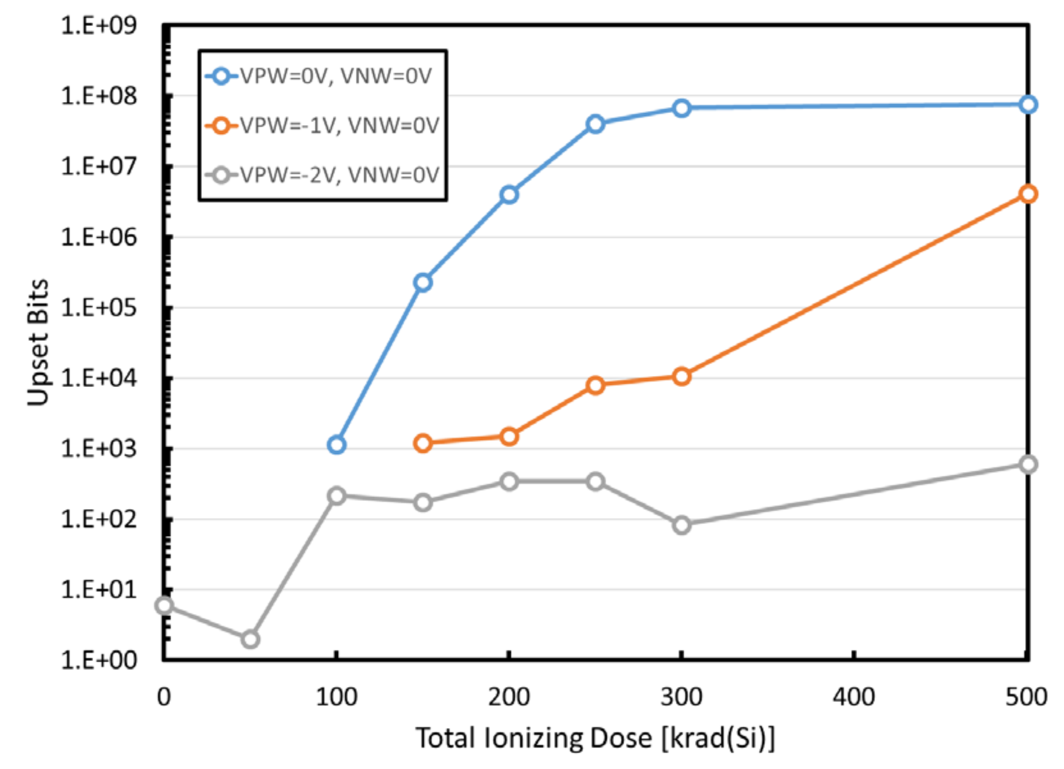


N-Well bias has no impact on the number of incorrect bits post-irradiation

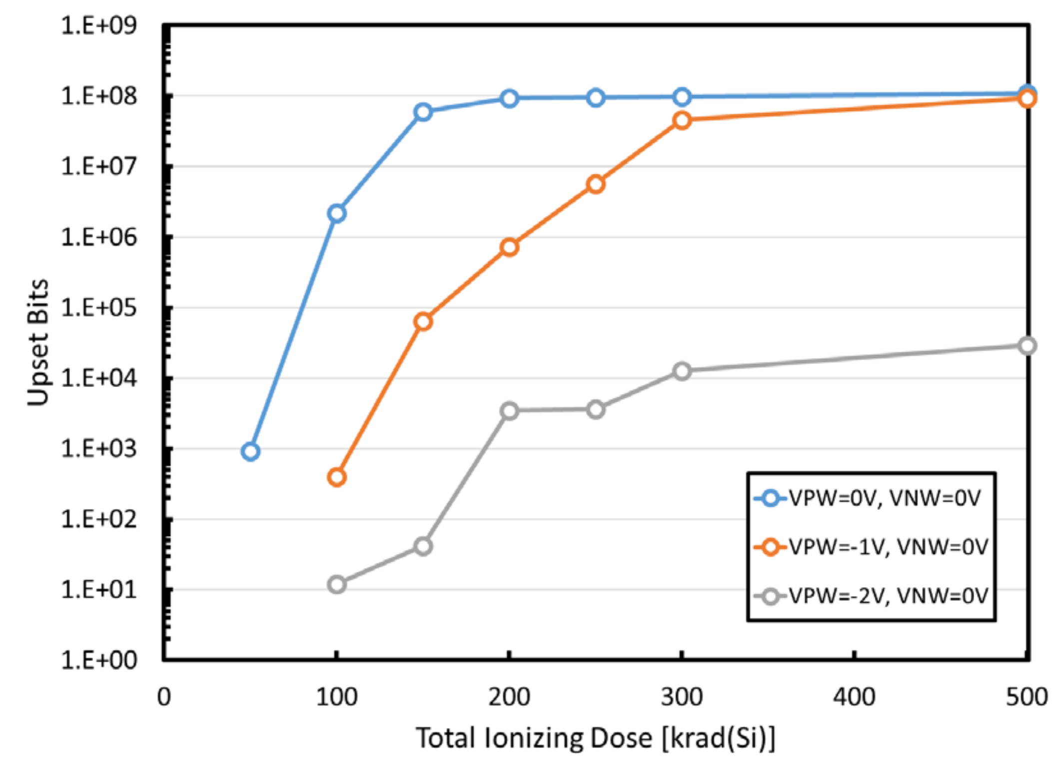
Total Ionizing Dose Test Results

P-Well Bias Voltage

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V

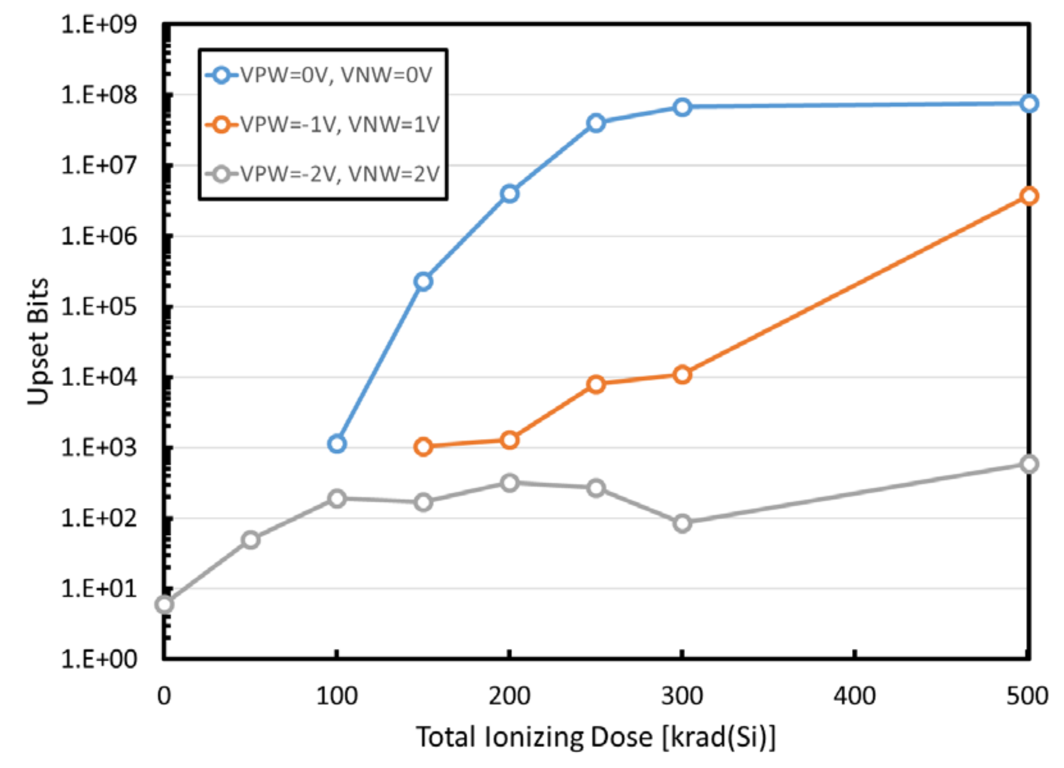


The more negative the p-well bias voltage is after irradiation, the fewer the number of bits are read incorrectly

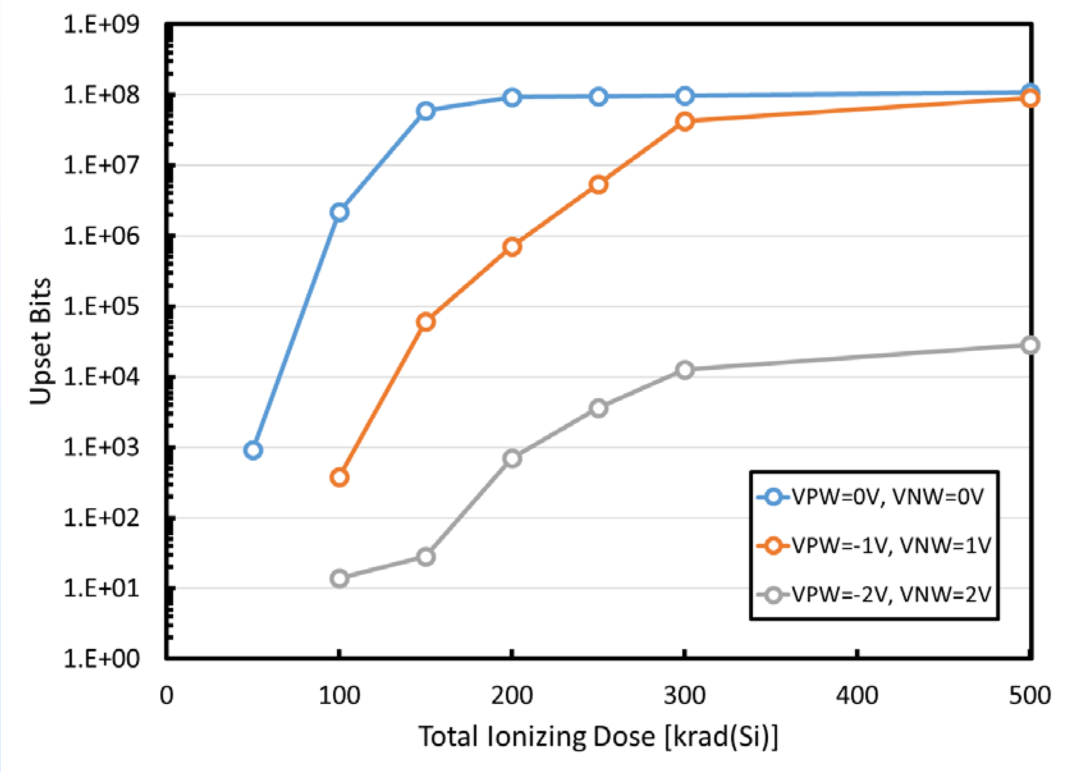
Total Ionizing Dose Test Results

P-Well and N-Well Bias Voltage

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V



Changing the p-well and n-well bias voltages simultaneously results in nearly identical results as when just changing the p-well bias voltage

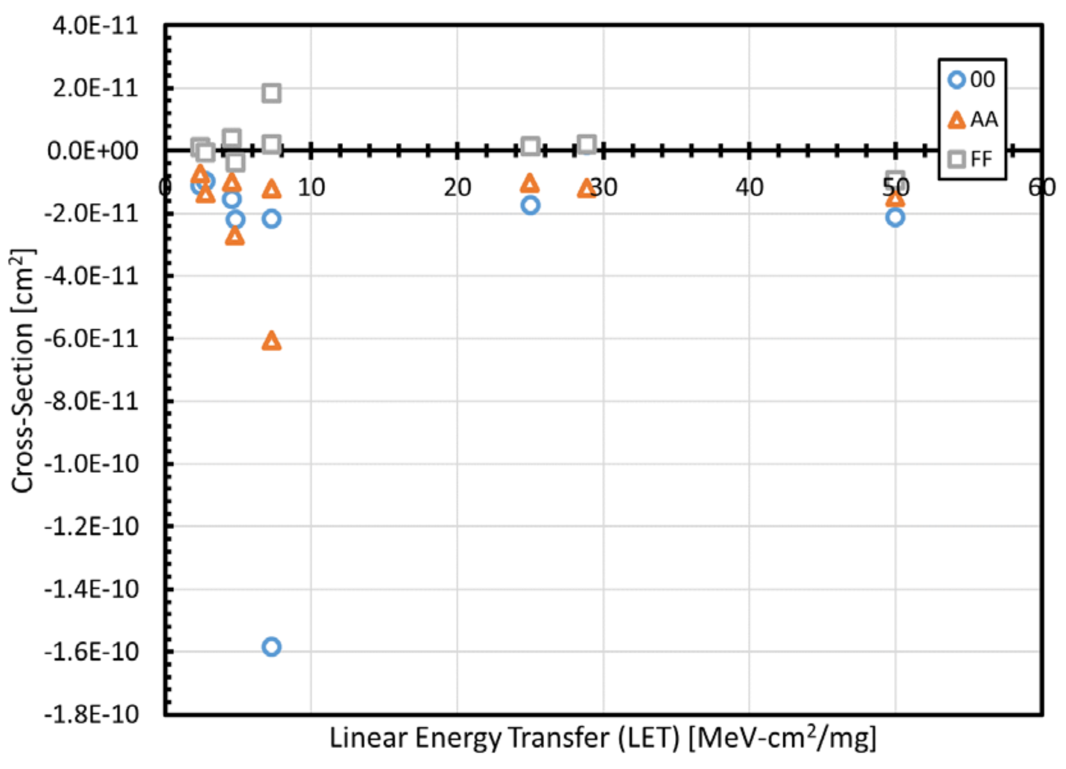
Combined Total Ionizing Dose and Single-Event Effects Testing

- After TID irradiations, DUTs were stored on dry ice to ensure no annealing and were then transported to LBNL and subjected to heavy ion irradiation
- Due to high levels of gamma dose, the number of pre-heavy-ion-irradiation bits that were upset was on average about half of all bits
  - Made measuring the single-event contribution to the number of upset bits difficult to obtain
  - Data are still useful for observing trends rather than considering absolute values

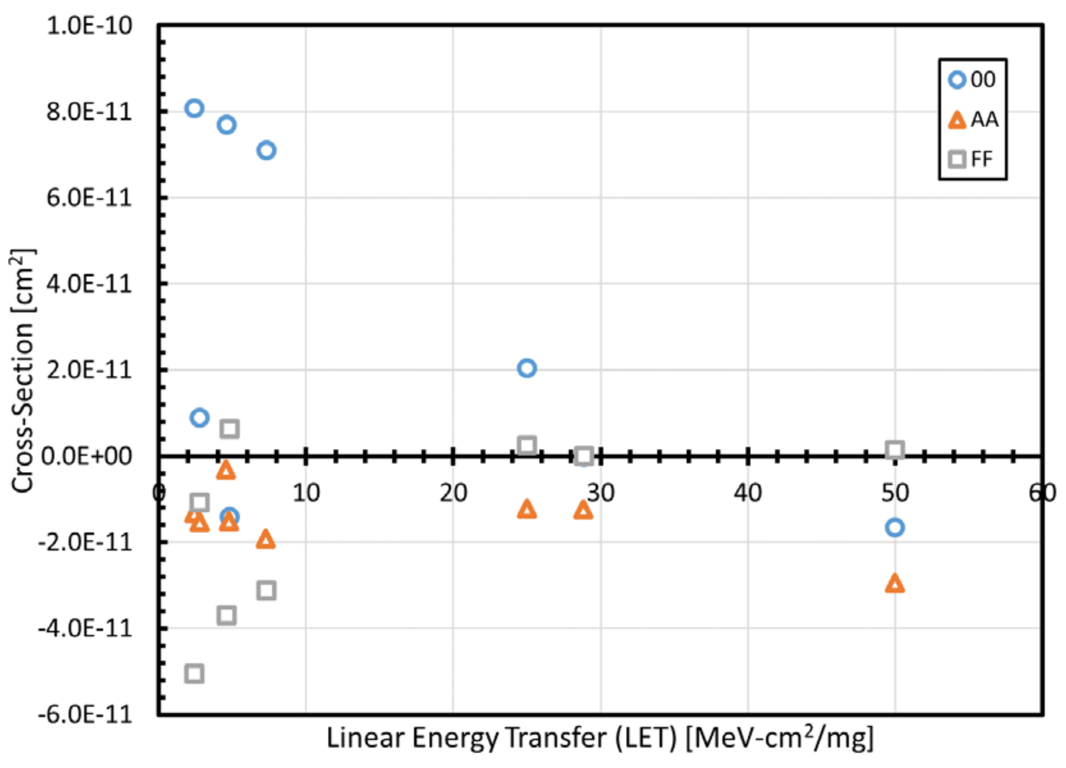
Combined Effects Test Results

Input Pattern

P-well = 0 V, N-well = 0 V



P-well = -2 V, N-well = 2 V



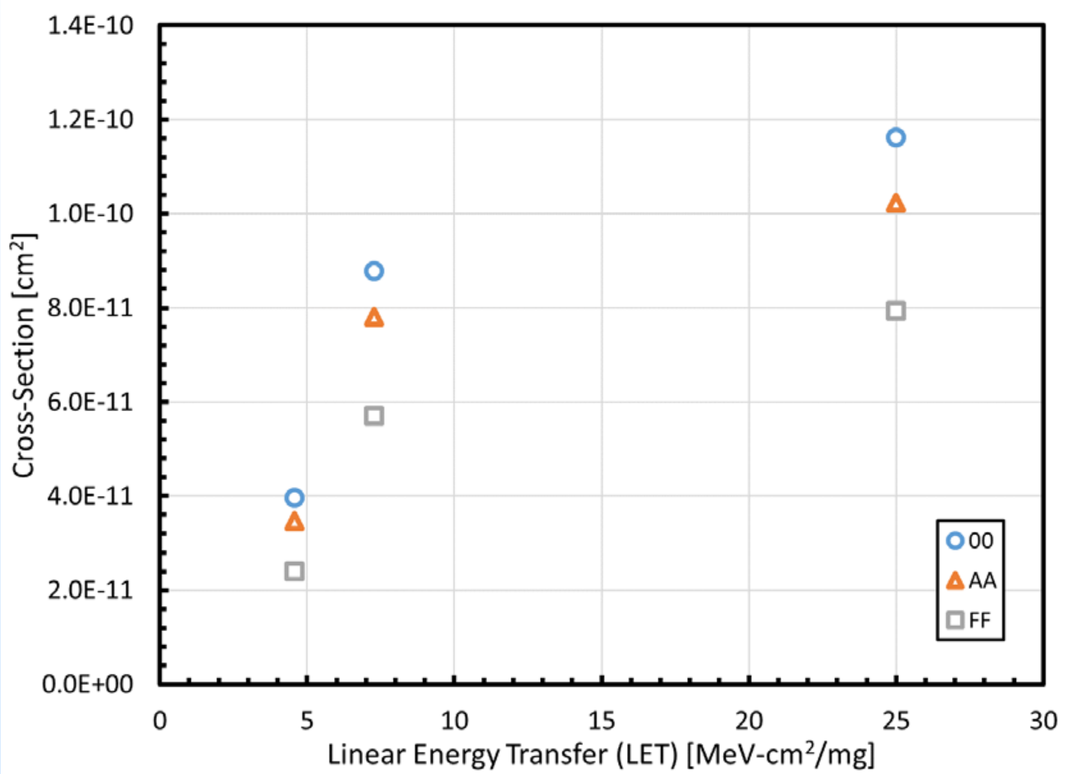
Pattern dependence observed in TID-only results is also apparent in combined effects results

Combined Effects Test Results

Pattern Input

- When the DUT biased with the extreme conditions during TID irradiation is heavy-ion irradiated under the same bias conditions, the SEE response looks like the standard Weibull curve
- The all zeroes pattern still results in the most upsets (like the TID-only results)

P-well = -2 V, N-well = 2 V



Conclusions

- Parts irradiated with “extreme” bias conditions (VPW = -2 V and VNW = 2 V) have fewer incorrect bits when TID-irradiated compared to parts irradiated with nominal bias voltages (VPW = 0 V and VNW = 0 V)
- An input pattern dependence emerges in “extreme” bias parts
    - More upsets are observed when all 0s are written and read back
- Varying the n-well bias voltage has no impact on the number of upset cells after irradiation
- P-well bias voltage greatly changes the number of upset cells in both irradiation bias conditions
    - The “extreme” condition results in a saturated response sooner than the nominal condition
    - The “extreme” condition also has a higher number of upset cells for all p-well voltages
- Combined effects testing also showed pattern dependence in the device irradiated with “extreme” voltage conditions