Recent Radiation Test Results on a 22FDX Test Vehicle

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Acronyms

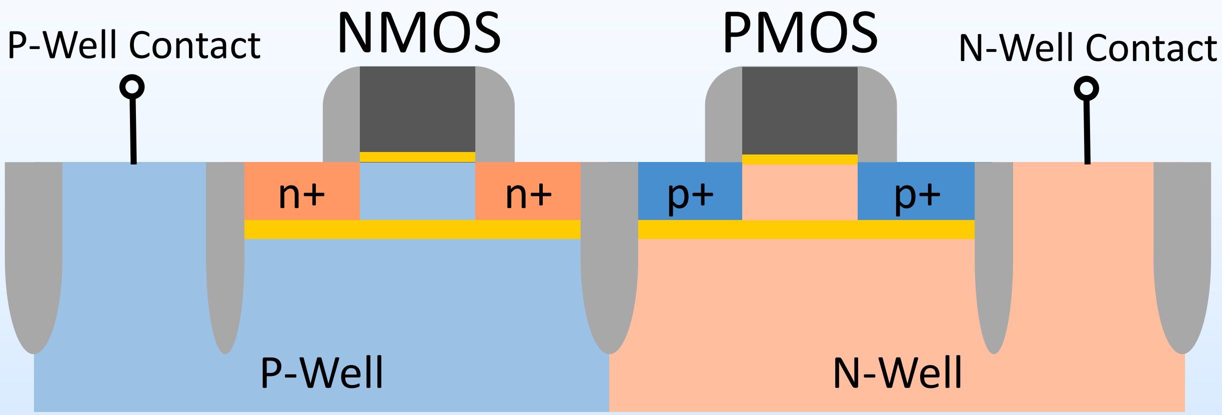
- DUT – Device Under Test
- FBB – Forward Body Bias
- FDSOI – Fully-Depleted Silicon-on-Insulator
- LBNL – Lawrence Berkeley National Laboratory
- nMOS – N-Channel Metal Oxide Semiconductor
- PDSOI – Partially-Depleted Silicon-on-Insulator
- pMOS – P-Channel Metal Oxide Semiconductor
- REF – Radiation Effects Facility
- RBB – Reverse Body Bias
- SEE – Single-Event Effects
- SOI – Silicon-on-Insulator
- SRAM – Static Random Access Memory
- TID – Total Ionizing Dose
- VNW – N-Well Bias Voltage
- VPW – P-Well Bias Voltage

Introduction

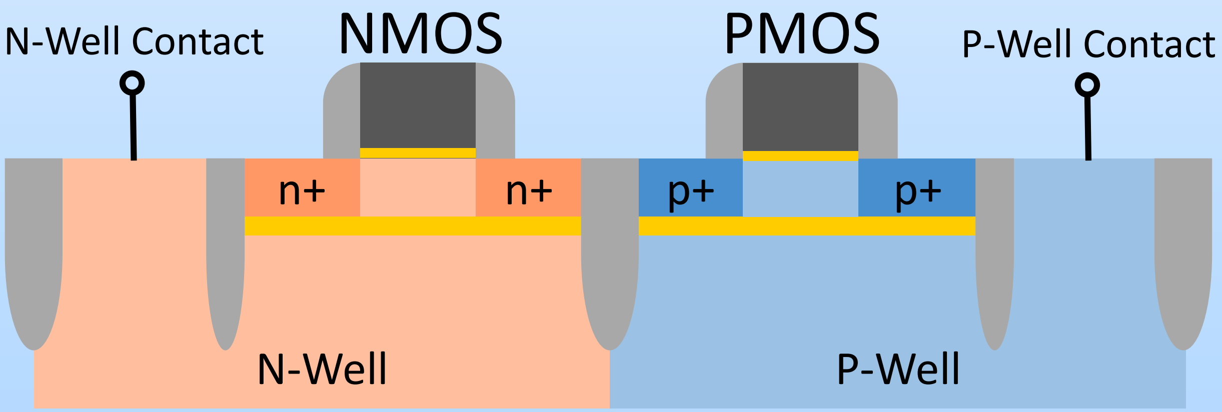
- GlobalFoundries’ 22FDX process is a 22 nm fully-depleted SOI process
  - Previous generations were PDSOI (45 nm, 32 nm)
- It employs standard, planar transistors (rather than novel designs like finFETs used in other highly scaled processes)
  - Planar transistors are simpler and less expensive to design and manufacture than 3D
- FDSOI supports body biasing, which can significantly reduce energy consumption

Body Biasing

Standard



Flipped Well

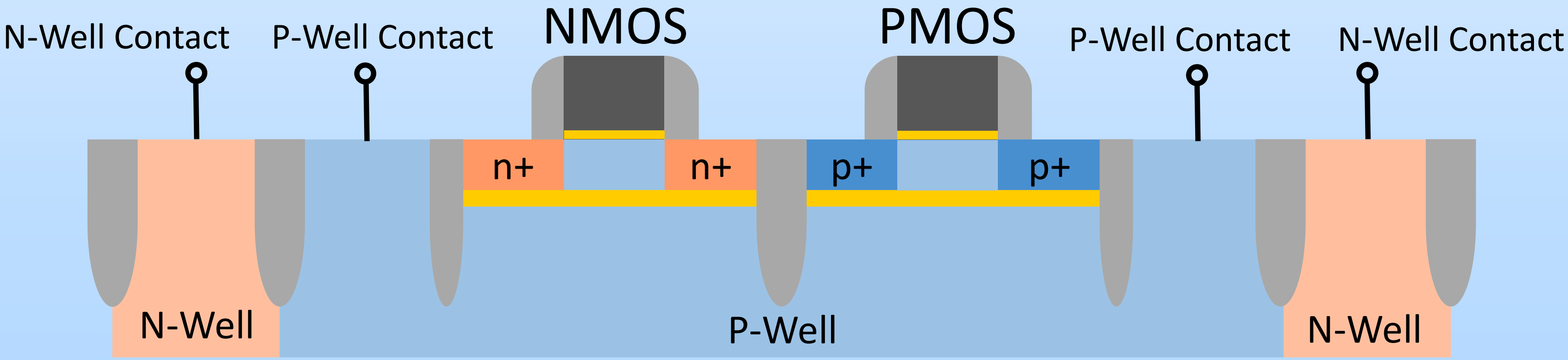


- 22FDX offers two well configurations
  - Standard: NMOS are located in p-wells and PMOS are located in n-wells
    - Allows for reverse body biasing the transistors and reduces leakage currents
  - Flipped well: NMOS are located in n-wells and PMOS are located in p-wells
    - Allows for forward body biasing and higher performance operation

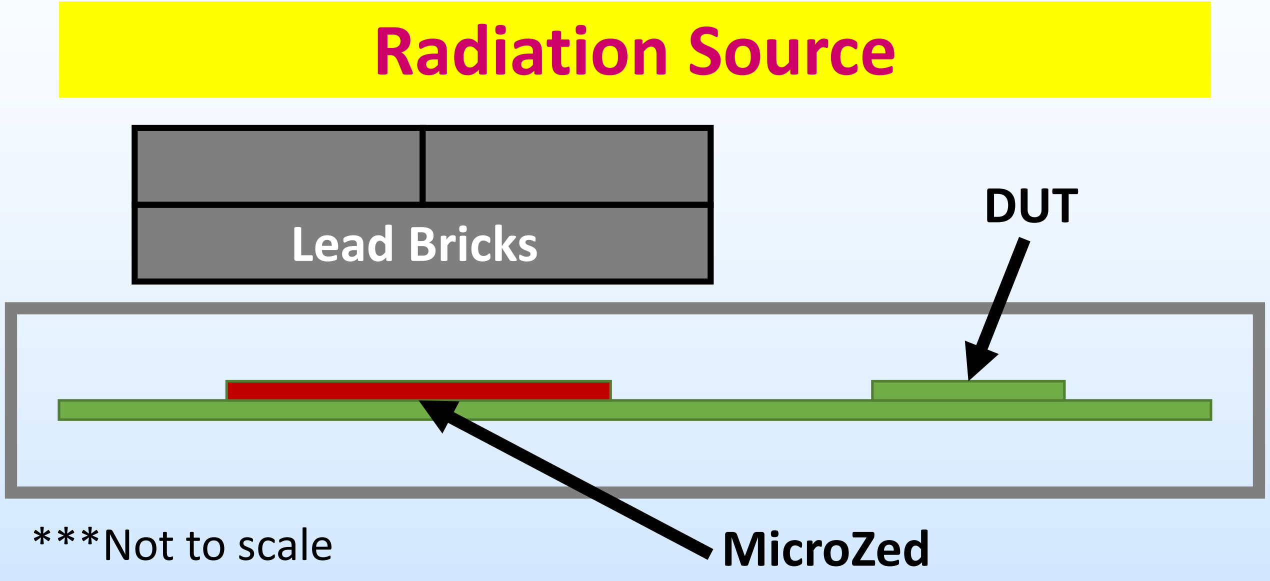
- P-well voltage can decrease from nominal 0 V to -2 V
- N-well voltage can increase from nominal 0 V to 2 V

Test Vehicle

- DUTs are a 128-Mb SRAM line monitor circuit
- Nominal supply voltage is 0.8 V, but voltages as low as 0.4 V and as high as 1.08 V are supported by the technology
- The bit cell array in this device is manufactured with all transistors in a p-well, while the n-well is implanted to isolate the SRAM bit cell array
  - NMOS are in the standard configuration (allows reverse body biasing)
  - PMOS are in the flipped well configuration (allows forward body biasing)
- As a result of the n-well only being used for isolation, n-well biasing was expected to have a limited effect on the radiation response of the SRAM



Setup



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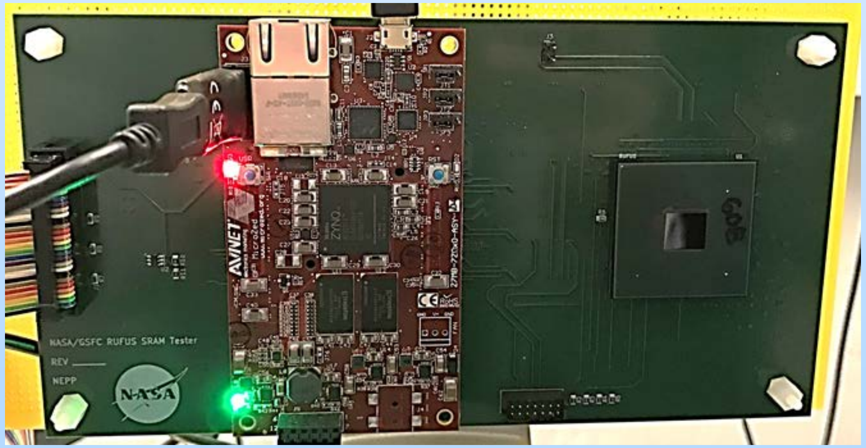


- Previous testing indicated MicroZed survived to ~17 krad
- Lead bricks were stacked to reduce dose rate to MicroZeds
- MicroZeds were also replaced before overnight steps
- Pattern was written before irradiation and read back and the number of upset bits was recorded
- After irradiation, cells were read back again and number of upsets were recorded
  - If any cells were incorrect, then the memory was rewritten and read back to see if the number of incorrect cells changed

Bias Conditions

During Irradiation

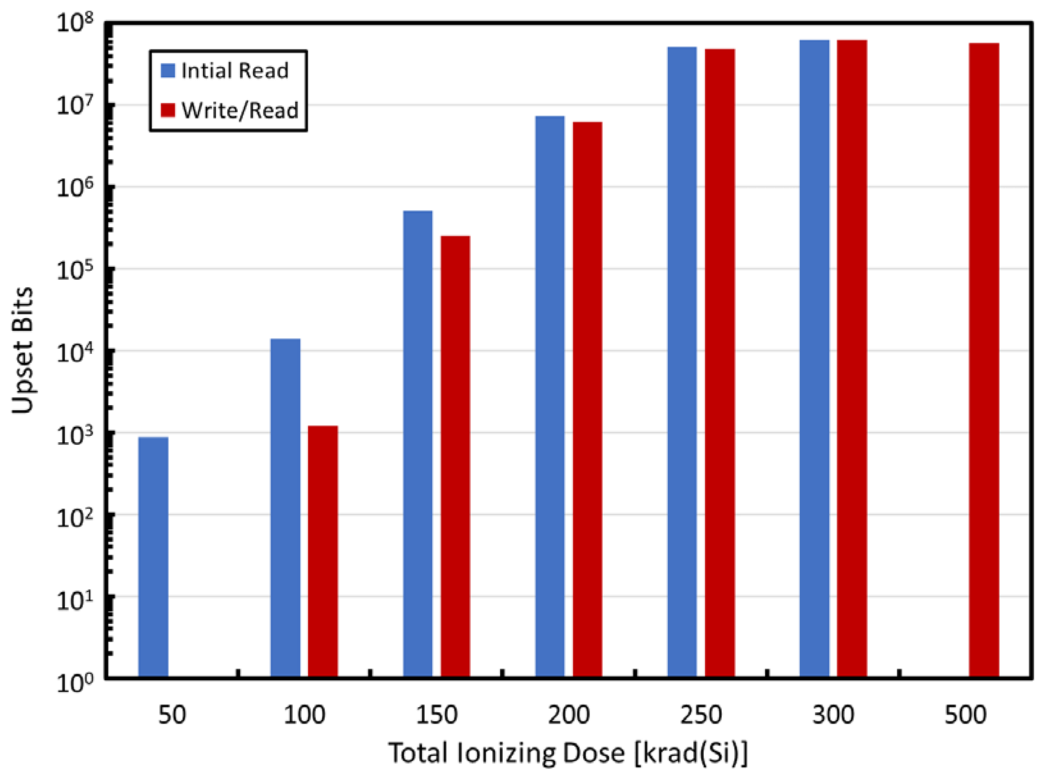
- DUT 609
  - Nominal array voltage (0.8 V)
  - Nominal p-well voltage (0 V)
  - Nominal n-well voltage (0 V)
- DUT 601
  - Nominal array voltage (0.8 V)
  - Extreme p-well voltage (-2 V)
  - Extreme n-well voltage (2 V)

Post-Irradiation Measurements

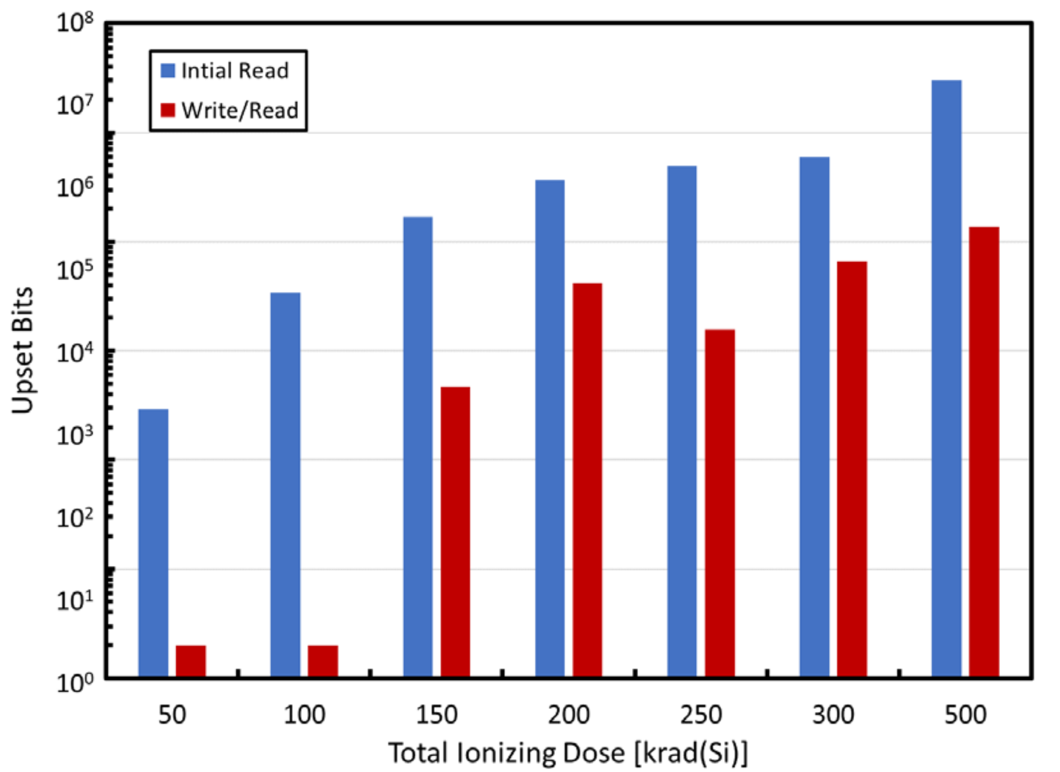
- Sweep array voltage (0.7 V to 1.08 V), holding n- and p-well voltages constant (0 V)
- Sweep p-well voltage (0 V to -2 V), holding array (0.8 V) and n-well (0 V) voltages constant
- Sweep n-well voltage (0 V to 2 V), holding array (0.8 V) and p-well (0 V) voltages constant
- Sweep p- (0 V to -2 V) and n-well (0 V to 2 V) voltages, holding array (0.8 V) voltage constant
- Measure retention voltage at nominal well voltages

Total Ionizing Dose Test Results

Bias: P-well = 0 V, N-well = 0 V, Pattern: FF



Bias: P-well = -2 V, N-well = 2 V, Pattern: FF

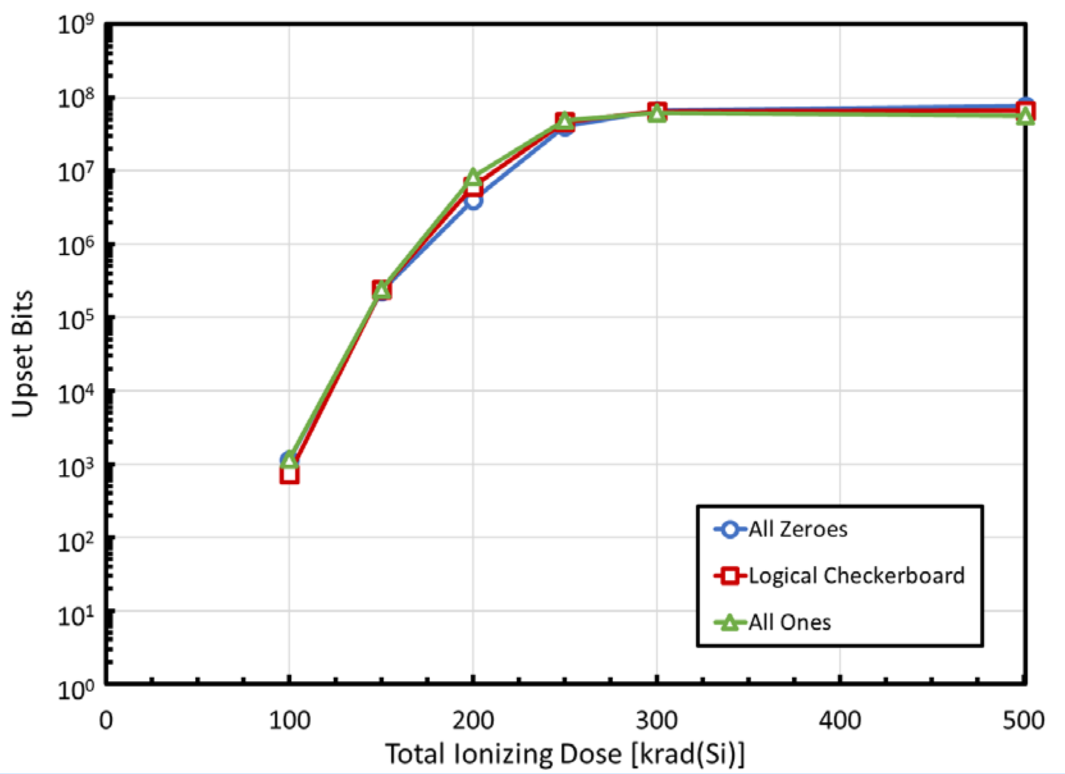


More upsets were observed in part biased with nominal voltage conditions during irradiation

Total Ionizing Dose Test Results

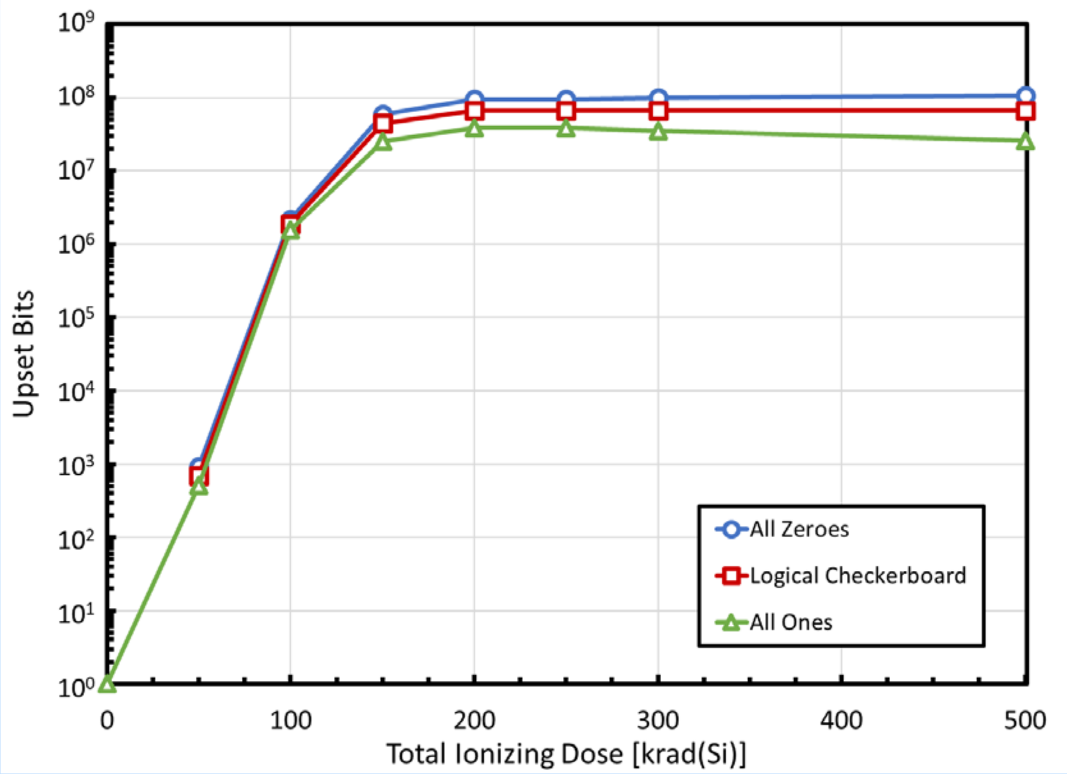
Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test: P-well = 0 V, N-well = 0 V



Bias: P-well = -2 V, N-well = 2 V, Pattern: FF

Test: P-well = 0 V, N-well = 0 V

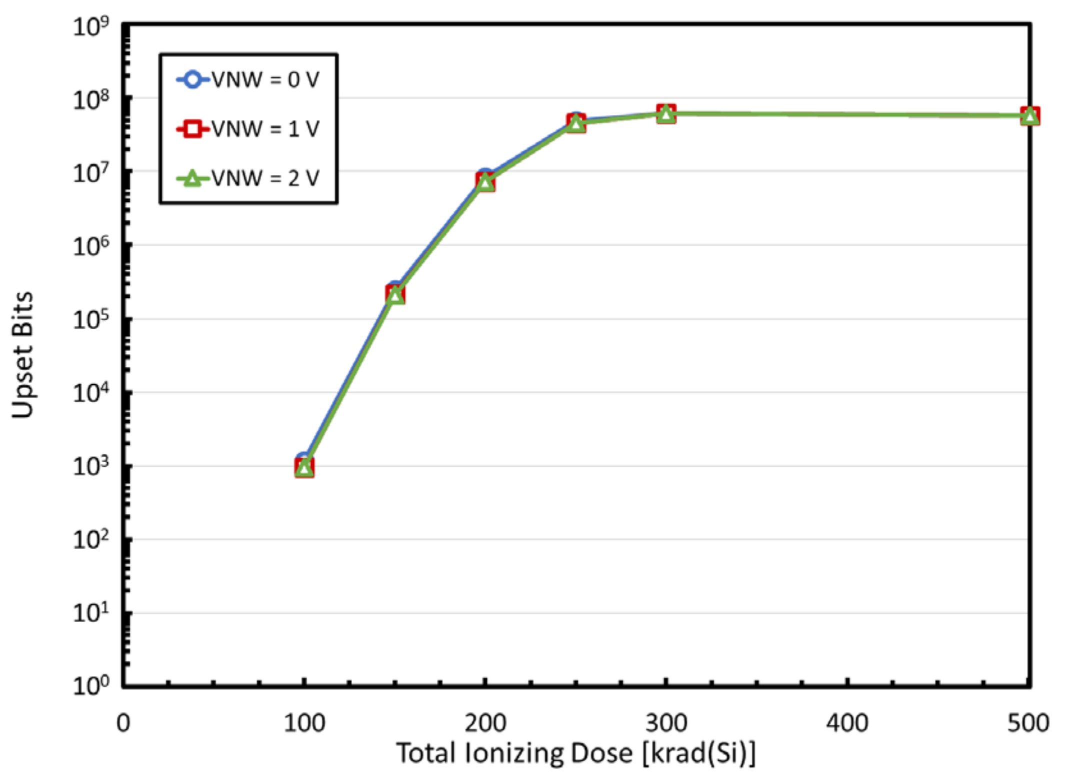


A pattern dependence emerges when biased in the “extreme” conditions during irradiation

Total Ionizing Dose Test Results

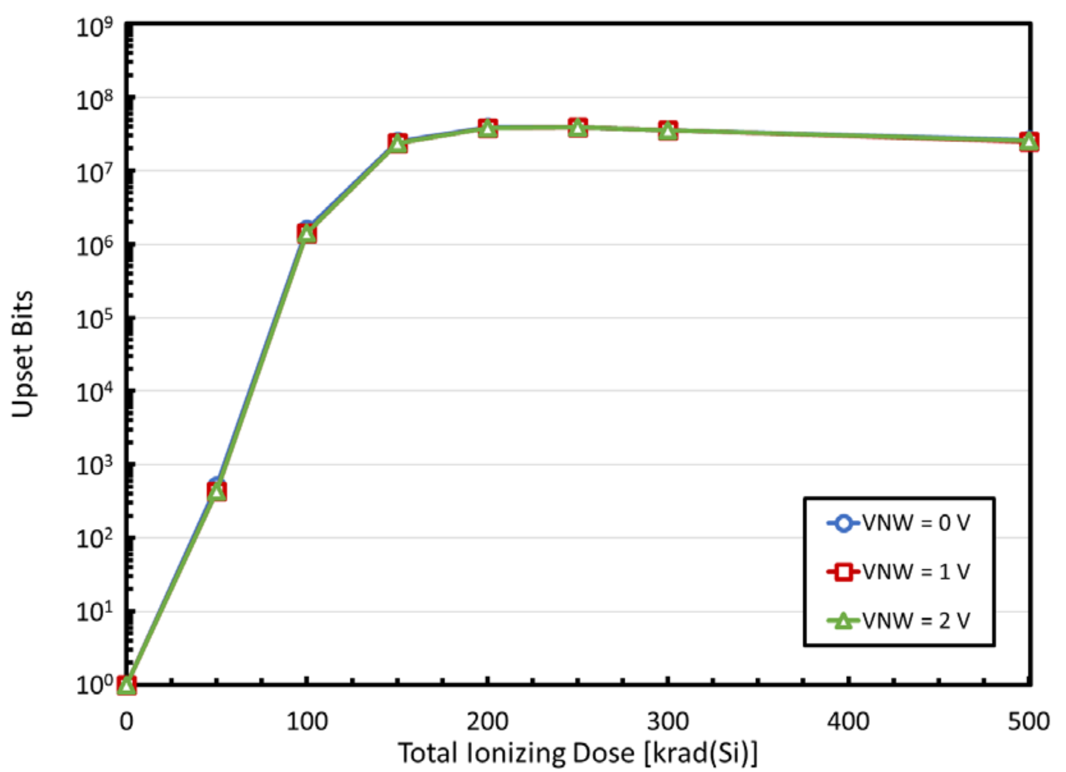
Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test: P-well = 0 V, Pattern: FF



Bias: P-well = -2 V, N-well = 2 V, Pattern: FF

Test: P-well = 0 V, Pattern: FF

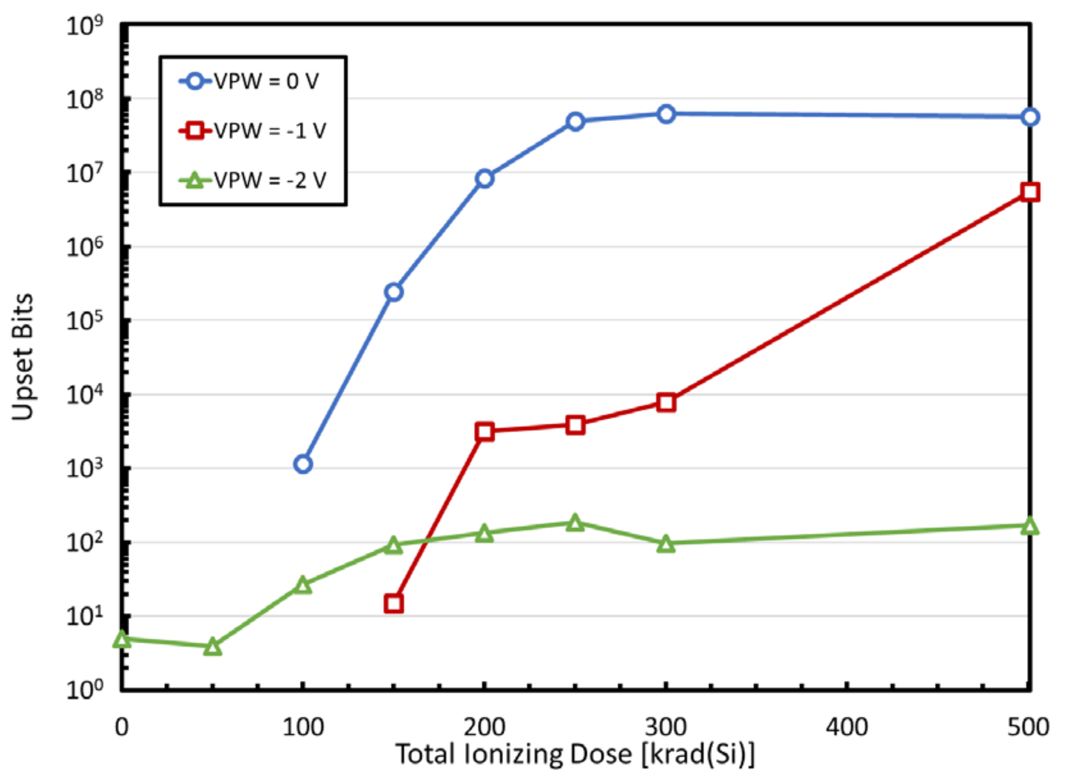


As expected, n-well bias has no impact on the number of incorrect bits post-irradiation

Total Ionizing Dose Test Results

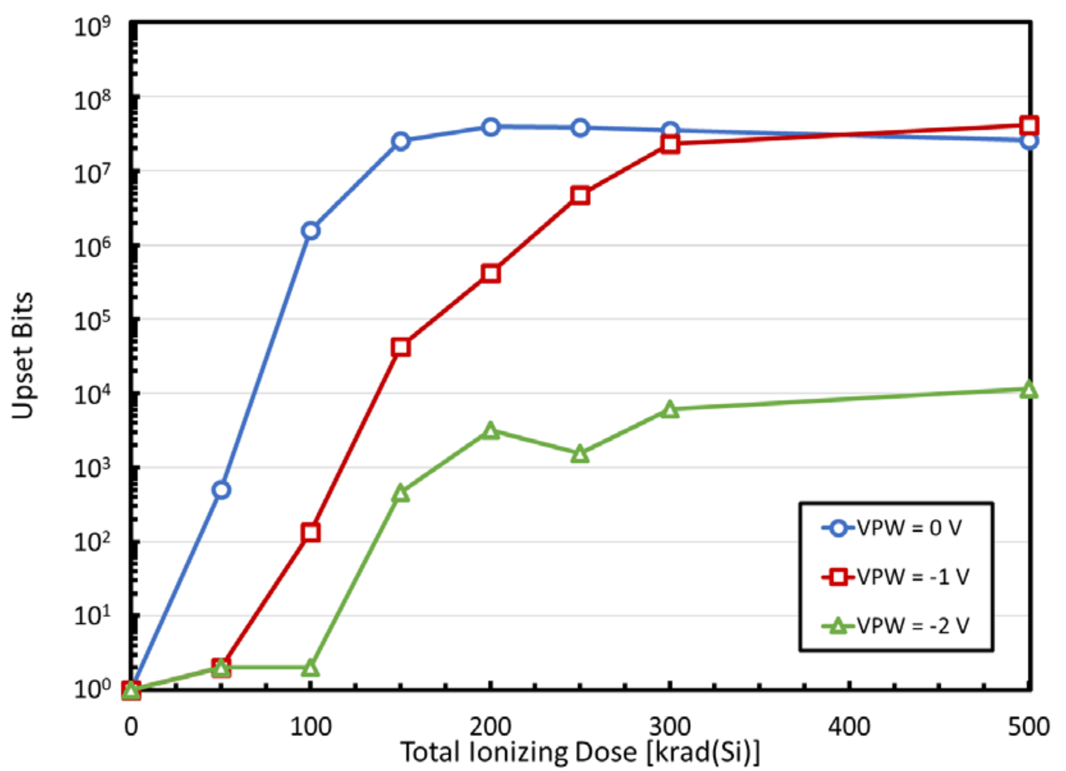
Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test: N-well = 0 V, Pattern: FF



Bias: P-well = -2 V, N-well = 2 V, Pattern: FF

Test: N-well = 0 V, Pattern: FF

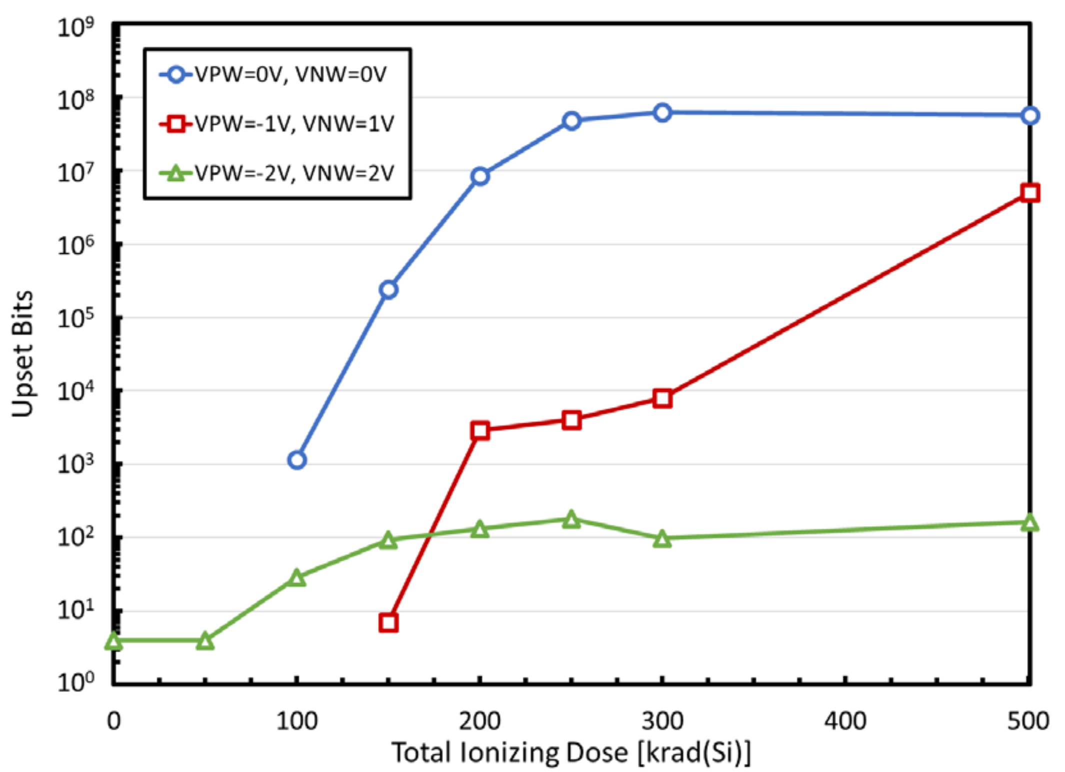


The more negative the p-well bias voltage is after irradiation, the fewer the number of bits are read incorrectly

Total Ionizing Dose Test Results

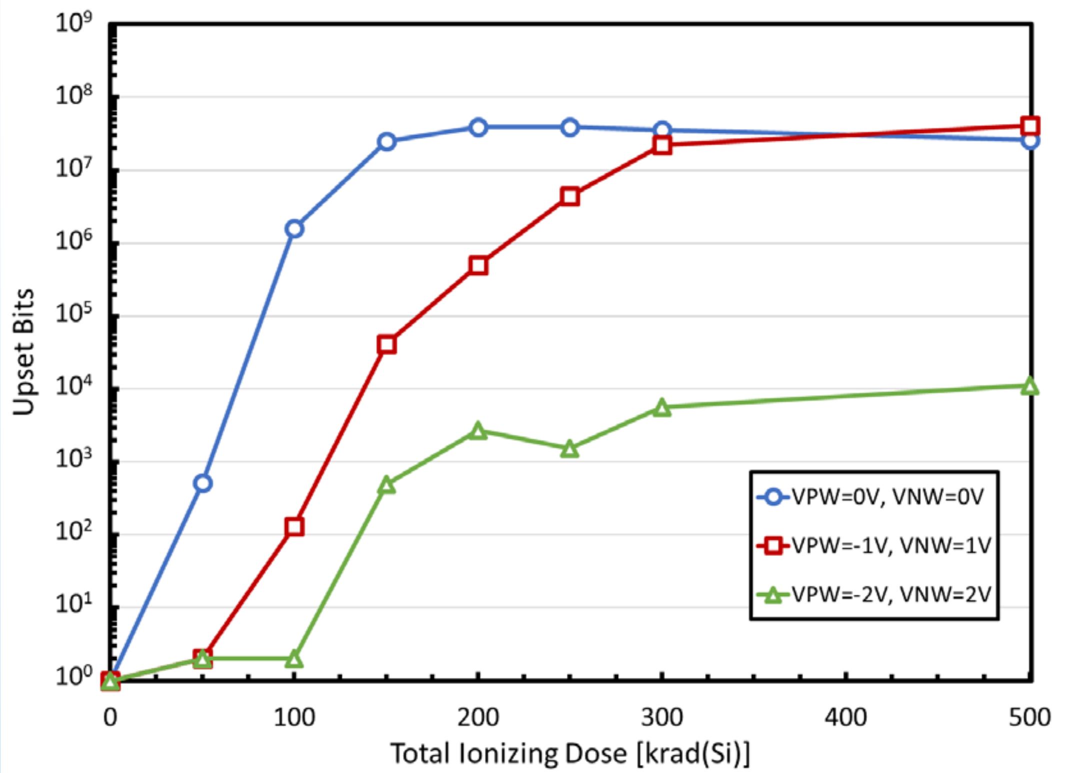
Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test Pattern: FF



Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test Pattern: FF

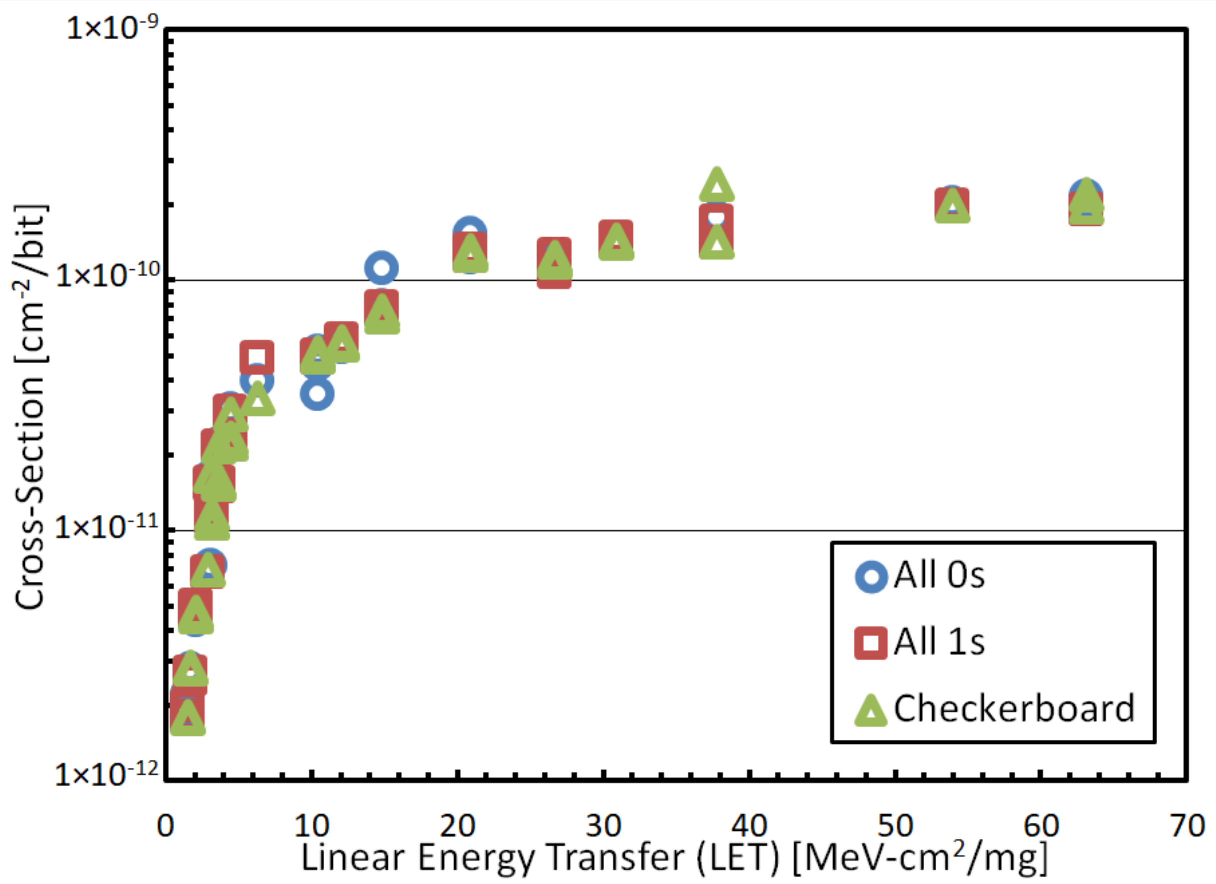


Changing the p-well and n-well bias voltages simultaneously results in nearly identical results as when just changing the p-well bias voltage

Combined Total Ionizing Dose and Single-Event Effects Testing

- After TID irradiations, DUTs were stored on dry ice to ensure no annealing and were then transported to LBNL and subjected to heavy ion irradiation
- Due to high levels of gamma dose, the number of pre-heavy-ion-irradiation bits that were upset was on average about half of all bits
  - Made measuring the single-event contribution to the number of upset bits difficult to obtain
  - Data are still useful for observing trends rather than considering absolute values

Previous SEE Testing

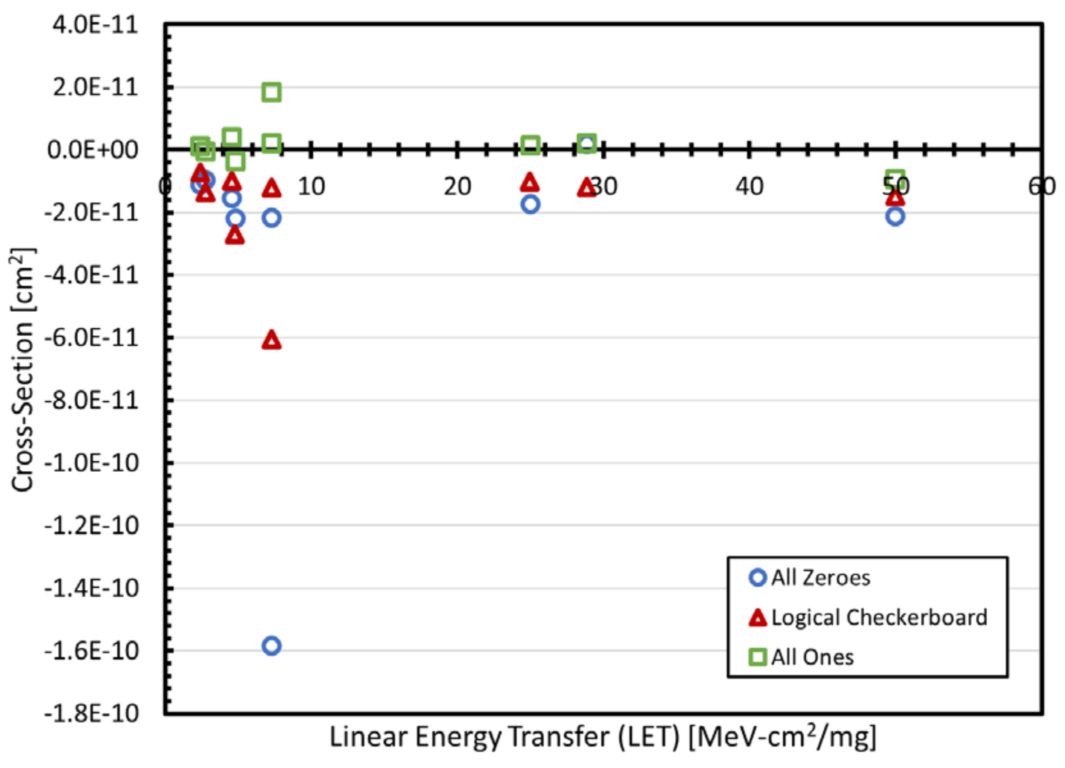


Previous SEE testing conducted on devices that were not TID-irradiated showed no pattern dependence

Combined Effects Test Results

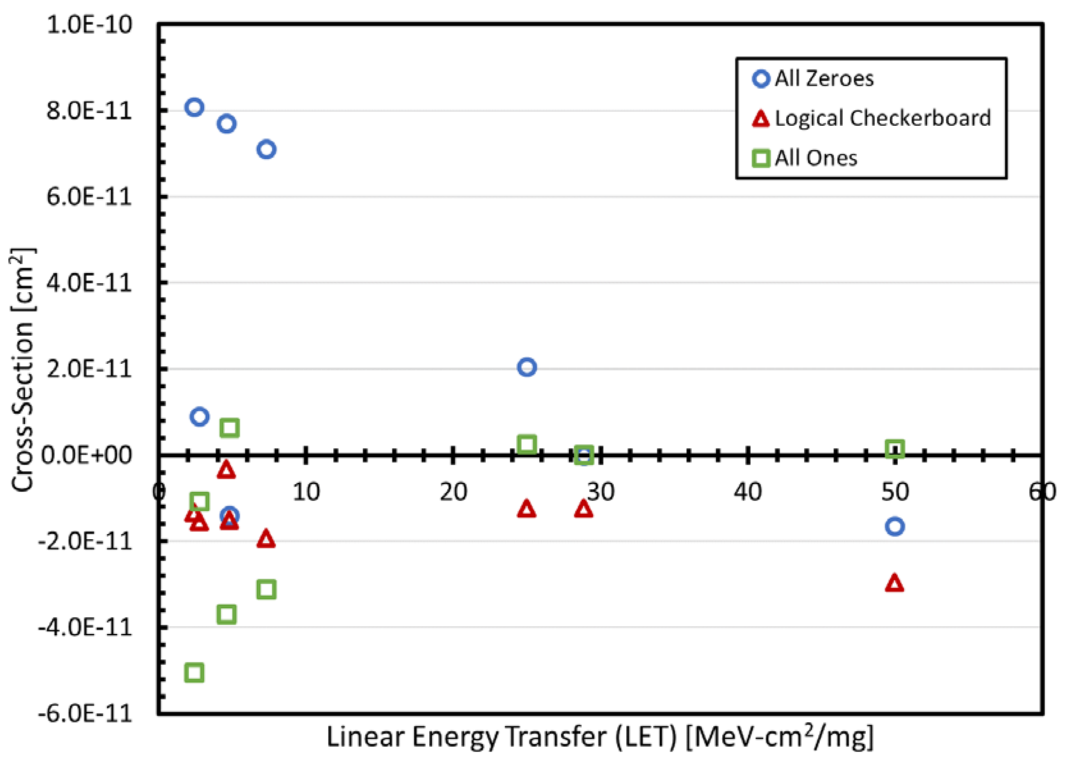
Bias: P-well = 0 V, N-well = 0 V

Test: P-well = 0 V, N-well = 0 V



Bias: P-well = -2 V, N-well = 2 V

Test: P-well = 0 V, N-well = 0 V

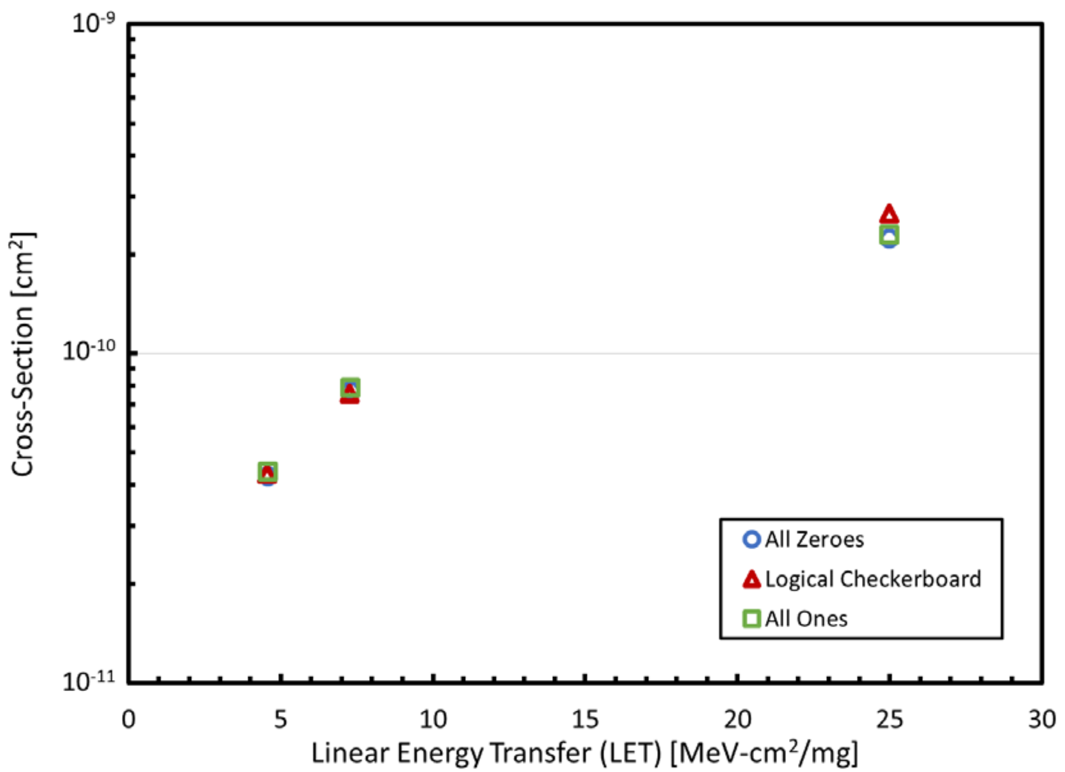


When tested at the “extreme” conditions, both bias conditions provide little information

Combined Effects Test Results

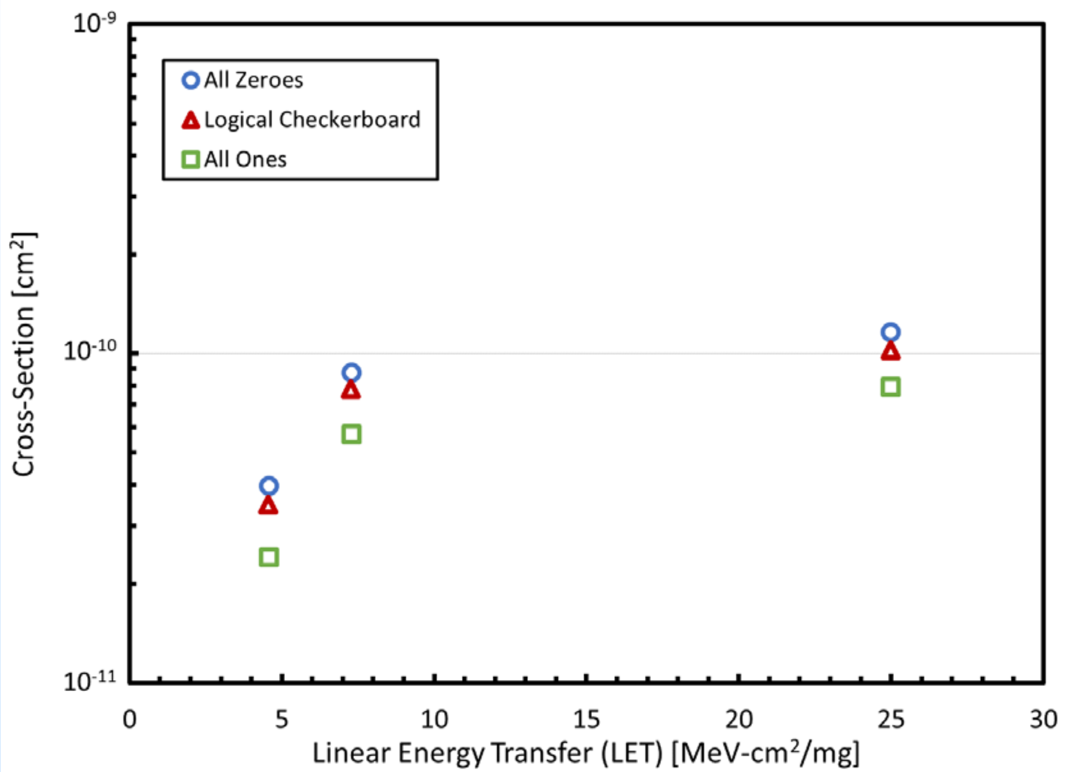
Bias: P-well = 0 V, N-well = 0 V, Pattern: FF

Test: P-well = -2 V, N-well = 2 V



Bias: P-well = -2 V, N-well = 2 V, Pattern: FF

Test: P-well = -2 V, N-well = 2 V



Pattern dependence observed in TID-only results is also apparent in combined effects results for part biased with "extreme" conditions

Implications of Pattern Dependence

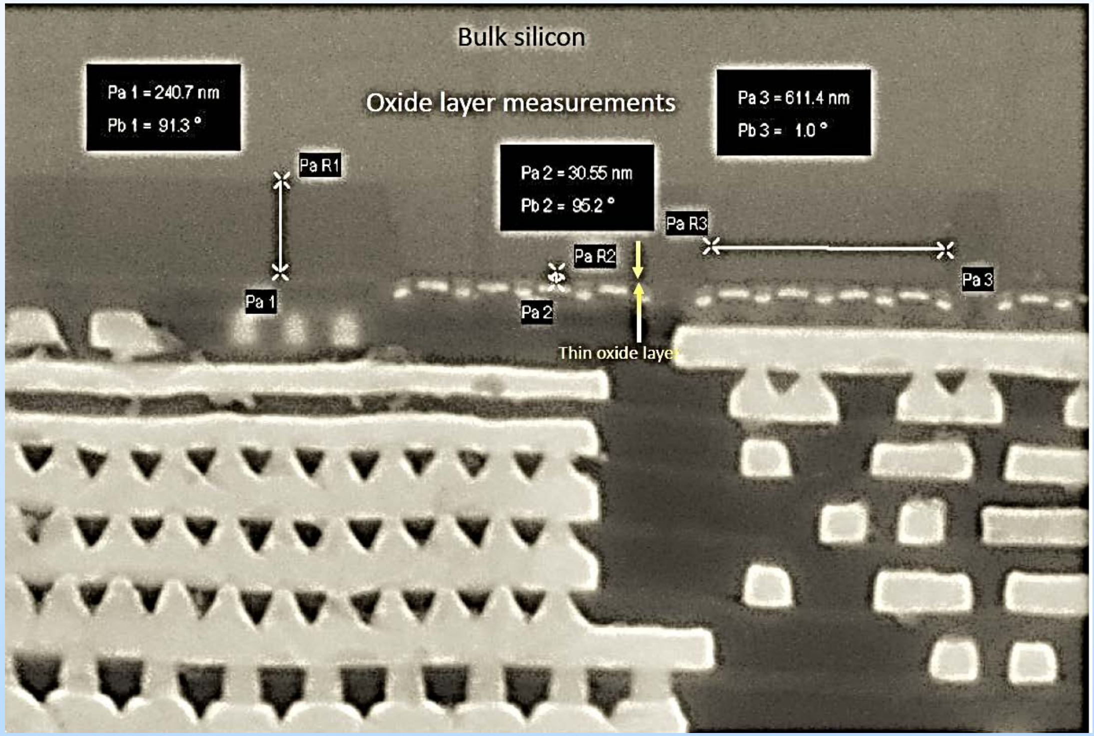
- In both the TID-only and combined effects testing, a pattern dependence has emerged where there are more incorrect bits when an all-zeroes pattern is written to the memory than when an all-ones pattern is written
  - This pattern was not observed in SEE testing of parts that had not been TID-irradiated
  - May indicate the NMOS transistors are experiencing greater degradation than the PMOS transitors
- We are still working to understand the mechanism for this response, but believe the flipped well (RBB – reduced leakage currents) configuration for the NMOS transistors contributes to the degraded response compared to the standard (FBB – enhanced performance) configuration for the PMOS transistors

Conclusions

- Parts irradiated with “extreme” bias conditions (VPW = -2 V and VNW = 2 V) have fewer incorrect bits when TID-irradiated compared to parts irradiated with nominal bias voltages (VPW = 0 V and VNW = 0 V)
- An input pattern dependence emerges in “extreme” bias parts
  - More upsets are observed when all 0s are written and read back
- Varying the n-well bias voltage has no impact on the number of upset cells after irradiation
- P-well bias voltage greatly changes the number of upset cells in both irradiation bias conditions
  - The “extreme” condition results in a saturated response sooner than the nominal condition
  - The “extreme” condition also has a higher number of upset cells for all p-well voltages
  - Dynamically adjusting well bias voltages may compensate for TID-induced degradation
- Combined effects testing also showed pattern dependence in the device irradiated with “extreme” voltage conditions

Backup Slides

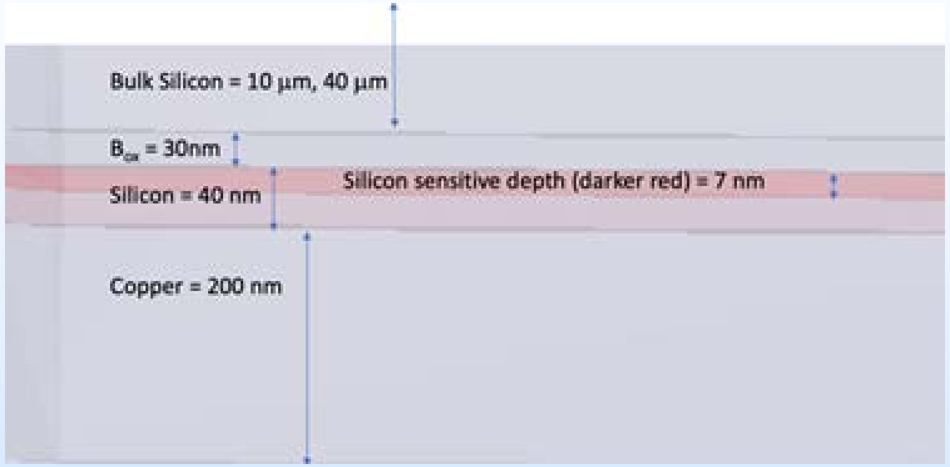
Background

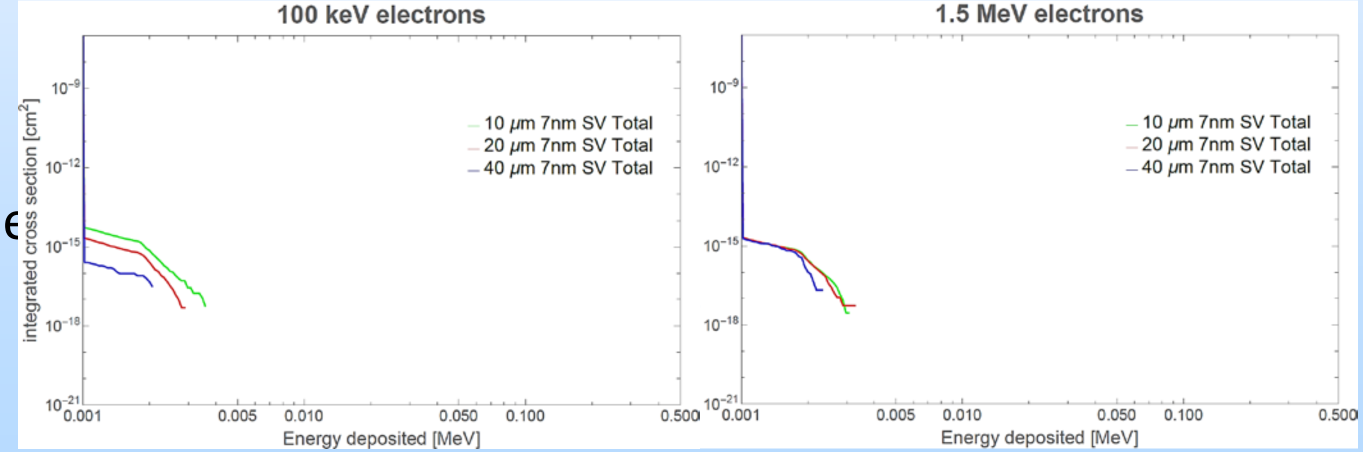


- The same 128-Mb SRAM line monitor test vehicles were used in this work as in the TID/combined effects testing
    - Previous heavy-ion SEE data was used to approximate the critical charge of the technology at 0.06 fC
- A single device was cross-sectioned and the thicknesses of the layers were measured
    - The substrate is at the top of the image and moving down is 30 nm of BOX, 40 nm of silicon, including 7-nm channel, and 200 nm of metal layers

Modeling and Simulation

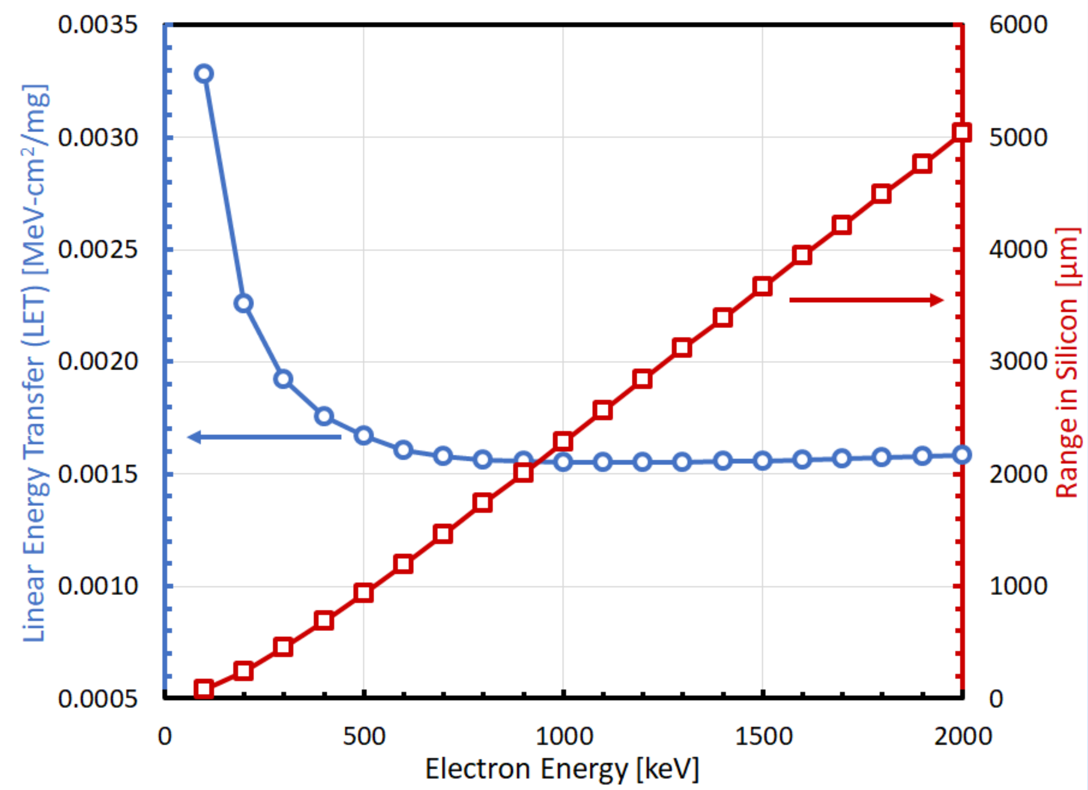
- Using the layer thicknesses measured in the cross-section, the device was modeled using the MRED code
- Various substrate thickness were simulated, as well as extreme ends of the electron energies (100 keV and 1.5 MeV)
- Assuming the critical charge of 0.06 fC and that holes do not contribute to the transient current, then the critical deposited energy is 1.35 keV
- As each simulation is for a single sensitive volume, the resulting cross-sections are per-bit, so multiplying by the number of bits in the SRAM gets us our per-device cross-section, and therefore our minimum test fluences



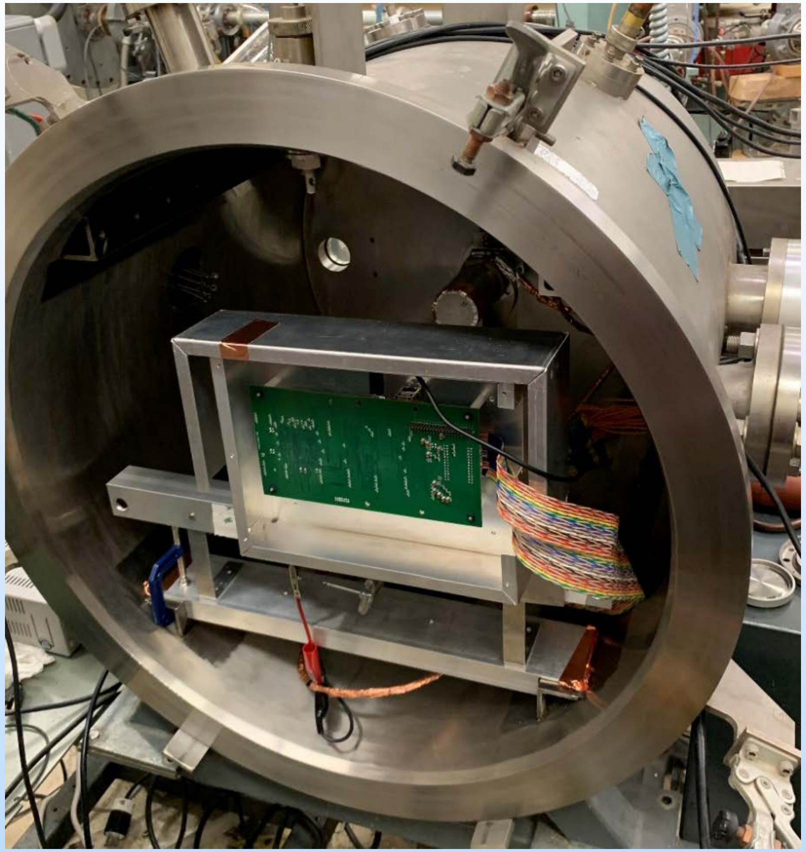


Test Facility

- All experiments were conducted at the NASA GSFC REF
- The 2-MeV Van de Graaff generator used is capable of supplying either protons or electrons with a mono-energetic beam ranging from approximately 100 keV to 2 MeV
- Each irradiation was run to a fluence of 1.05×10^{10} e$^-$/cm^2 at an average flux of 1×10^{9} e$^-$/cm^2/s
    - Results in a dose per run of 275 to 321 rad depending on electron energy



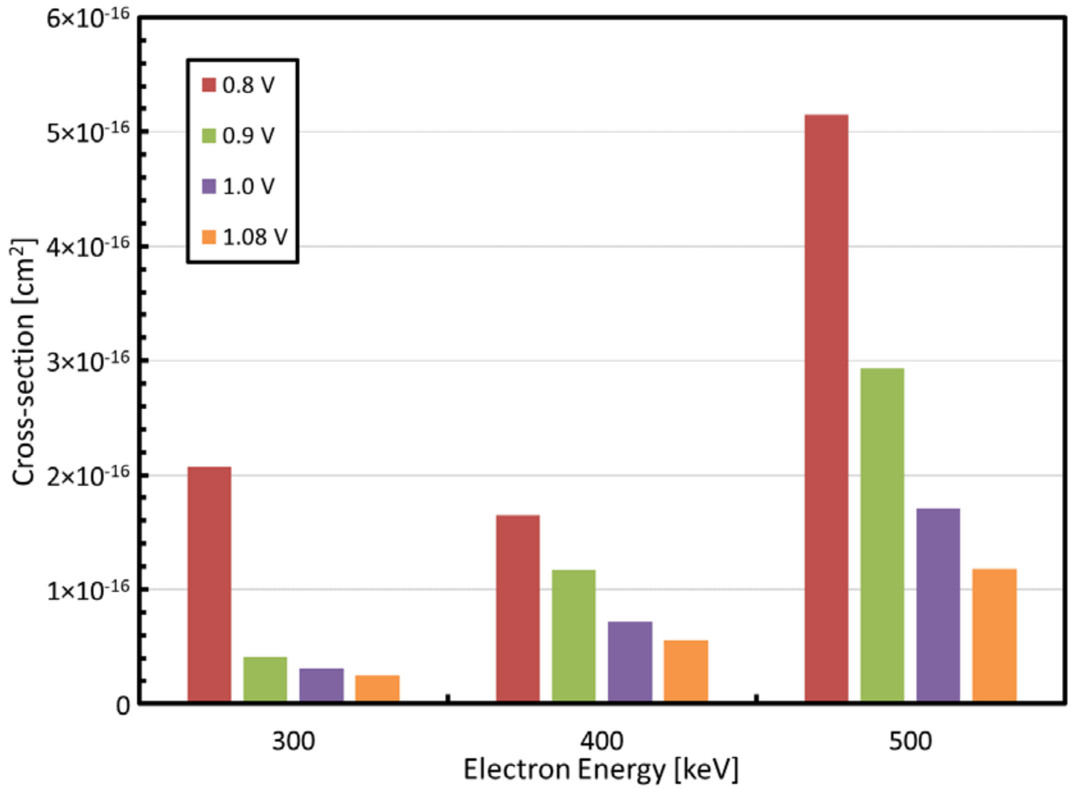
Test Set-up



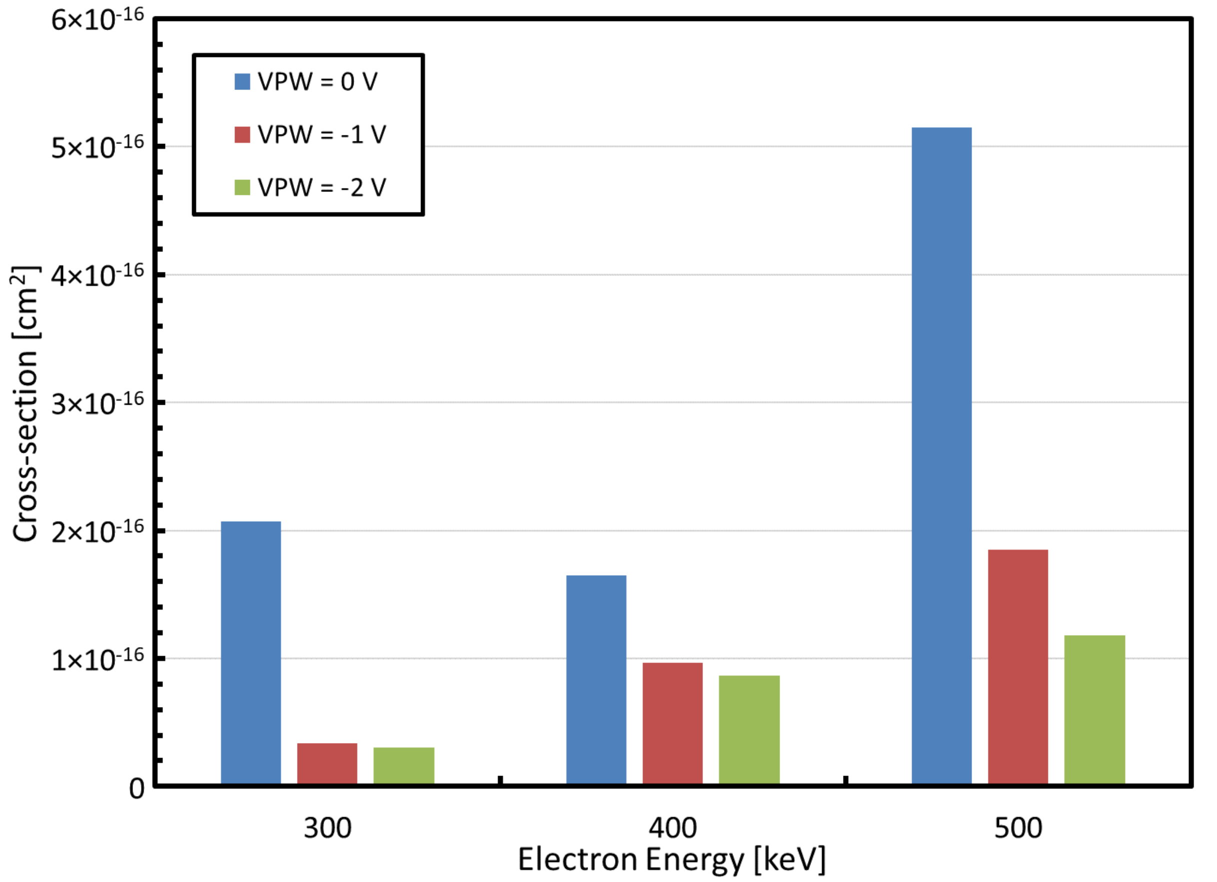
Custom shield was manufactured to limit irradiation to only DUT and reduce charging on the test board and cables, as well as the MicroZed

Low-Energy Electron Test Results

- Most previous low-energy electron SEE test data uses parts with lower than nominal supply voltages to increase device sensitivity
- We were able to irradiate at nominal and higher voltages and saw cross-sections decrease with increasing voltage
- Significant dose effects were observed at much lower doses than the TID results
  - Stuck bits were observed at ~6.2 krad
  - Consistent with dose enhancement effects observed by Gadlage et al., TNS 2017



Low-Energy Electron Test Results



Greater p-well bias voltage results in fewer upsets than nominal – consistent with heavy ion SEE test results and gamma TID results

Conclusions and Future Work

- We observed single-event upsets from low-energy electrons at nominal supply voltages
- Dose enhancement seriously complicates the ability to accumulate wide range of data on a single device
- Low-energy electron SEE trends are consistent with heavy-ion SEE
  - Decreased sensitivity with increased supply voltage
  - Decreased sensitivity with increased p-well bias voltage

- Additional testing is planned with fewer collected datapoints at each electron energy to reduce dose effects
  - Additional electron energies are also planned