Title of the White Paper: High Temperature Electronics for Venus Surface Applications: A Summary of Recent Technical Advances

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1.0 Summary

This white paper has a technical focus meant to provide background to those unfamiliar with the challenges of high temperature electronics, and an understanding of why new surface mission concepts are now viable for Venus and other applications. It describes that, for the first time, high temperature electronics have been developed to enable a paradigm change in extended duration Venus surface exploration. This white paper concentrates on the advances made in Silicon Carbide (SiC) integrated circuit (IC) electronics that have matured to a state where a simple long-life scientific probe is feasible for Venus surface operations. These electronics have been demonstrated for more than a year at 500˚C, 60 days in high-fidelity simulated Venus surface conditions chamber, and have been integrated and demonstrated with prototype long-lived scientific observation sensor technology. Continued maturation of these needed high temperature electronics and sensors is ongoing in the Long-Lived In-Situ Solar System Explorer (LLISSE) project to provide an operational system including sensor control and operation, signal processing, power management, and communications in the early part of the 2020's. A key focus of this work includes increasing the complexity and decreasing the power consumption of the ICs which will pave the way to enhanced capabilities, such as long-duration Venus seismic measurements. Other IC development efforts include high temperature memory, terrestrial based characterization of volcanic magma, and development of a simple microprocessor. This electronics has also shown to have exceptionally high radiation tolerance, and thus have relevance for a broad range of solar system exploration. **Although presently at the level of complexity of 1970-1980 silicon-based electronics, such electronics can enable breakthroughs in Venus planetary exploration akin to 1970s-launched planetary exploration successes (such as Viking and Voyager).**

2.0 High Temperature Electronics Maturation

2.1 State-of-the-Art Advancements Since the Last Decadal

Standard electronics for planetary instrumentation/operations are silicon (Si) based. However, Si-based electronics do not operate at Venus surface temperatures [1-3]. Venus surface conditions are extremely challenging and no landers based on conventional electronics have returned more than ~2 hours of data from the Venus surface. Thus, operation in Venus surface conditions implies a need to use a different type of electronics than standard Si, e.g., wide bandgap electronics, such as SiC, or other high temperature electronic systems [4]. The design choices available in a small package, operational capability for prolonged time periods in high pressure/temperature environments, and the ability to form complex integrated circuits (IC's) suggest SiC as the most viable technology for multiple high temperature applications. One of the major advances since the last Decadal survey has been the advancement of SiC IC electronics to the point where it can enable drastically lower mass and longer duration Venus surface missions.

In particular, SiC integrated circuits with unprecedented sustained lifetimes at/above Venus surface temperatures have been fabricated and demonstrated by NASA Glenn Research Center *(GRC)* [5]. Originally developed for jet engine applications, this work has notably expanded capabilities and produced the world's first microcircuits of moderate complexity (Medium Scale Integration) that have the potential for sustained operation at 500˚C [6-8]. These circuits contain

10's to 100's of SiC Junction Field Effect Transistors (JFETs) and two metal interconnect layers, orders of magnitude more complicated than previous long-term 500°C demonstrations. (This JFET configuration is in contrast to Metal Oxide Field Effect (MOSFET) transistors that are the standard for commercial Si electronics, and are not viable for extended durations at Venus temperatures even using SiC semiconductors [2-3].) This enables a wide range of on-board data processing, including signal amplification, local processing (e.g. digitization), and wireless transmission of data. Although presently at the level of complexity of 1970-1980 silicon-based electronics, such electronics can enable breakthroughs in Venus planetary exploration akin to 1970s-launched planetary exploration successes (such as Viking and Voyager).

A major distinguishing aspect of this work is the long duration operational testing of these circuits, including device packaging. Operational life at 500˚C of over a year has been shown for SiC JFET circuits as complex as 179 transistors. This is shown in Figure 2.1.1, where demonstration of where more than 1 year of operation in Earth air oven at 500 °C was achieved for a ring oscillator clock and a Random Access Memory (RAM) circuit [9]. Other work has shown operation of circuits up to 961˚C for shorter durations, and across a total temperature range from low (-190 °C) to high temperatures (961 °C), a span more than 1000˚C [10-11]. A broad range of circuits have already demonstrated to enable a broad range of basic and durable functionality for the Venus surface environment. This new capability is a foundation for realizing a range of specifically designed electronics to meet targeted mission needs.

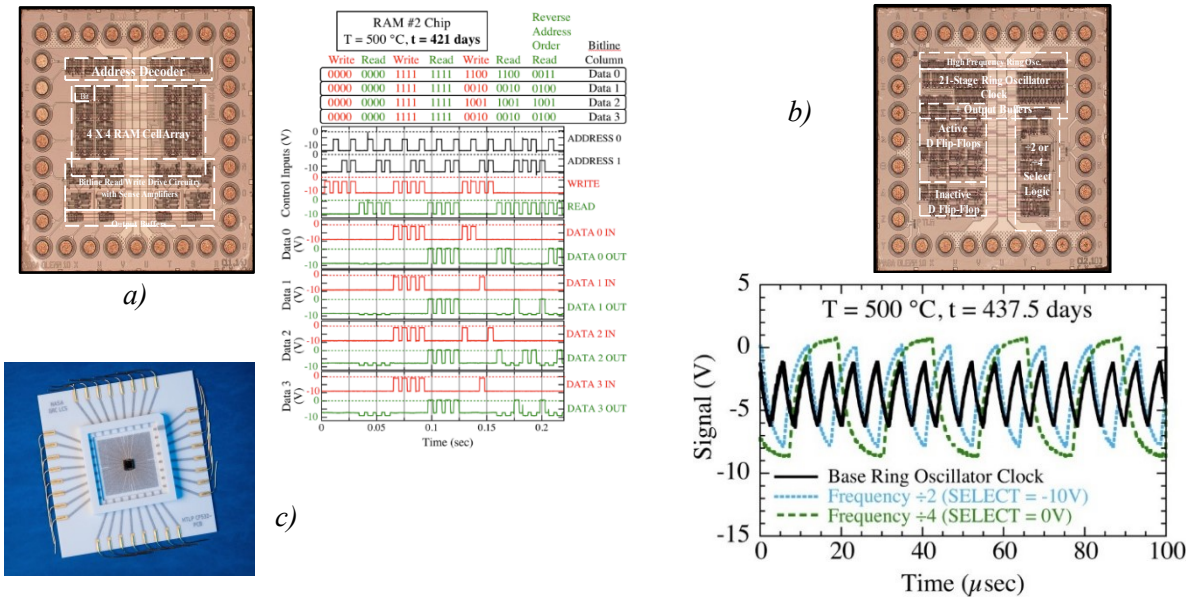

Figure 2.1.1. Long duration operation of over a year in an air oven of two electronics circuits a) RAM circuit data after 421 days at 500˚ C, and device picture; b) Ring oscillator clock (175 transistors) data after 437.5 days at 500˚ C, and device picture. c) High temperature packaging example (32 pins).

2.2 Demonstration in Simulated Venus Surface Environments

A paradigm shift for potential Venus exploration took place with the world-first demonstration of moderately complex electronics operating for extended periods in-situ in simulated Venus surface atmospheric conditions [12]. This demonstration took place in the Glenn Extreme Environment Rig (GEER). GEER is a 28 cubic ft. (800 L) chamber that simulates

the Venus atmosphere, temperature, pressure, and chemical species from the upper atmosphere to the surface. To very briefly summarize this first demonstration, Figure 2.2.1 shows the inside-chamber end of a probe assembly with a 3 mm x 3 mm SiC JFET ring oscillator chip with 12 transistors before and after testing in GEER. A mesh screen cap covered the probe allowing immersion of the packaged circuit during test in the simulated Venus surface atmosphere, while providing protection from physical damage during probe mounting. The GEER chamber was operated at Venus surface conditions for 21.7 days, which included temperature, pressure, and the first ten atmospheric species including corrosive sulfur and fluorine compounds, before ending the test for scheduling reasons. The SiC ring oscillator IC fully functioned at 1.26 ± 0.06 MHz over the entire 21.7 days it was exposed to Venus surface atmospheric conditions. This was the first demonstration of any electronics for such duration exposed to the environment and without any cooling or environmental protection.

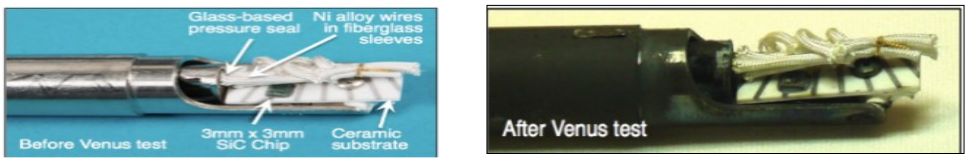

Figure 2.2.1. High temperature probe with SiC electronics before (left) and after (right) simulated Venus surface testing for 21.5 days.

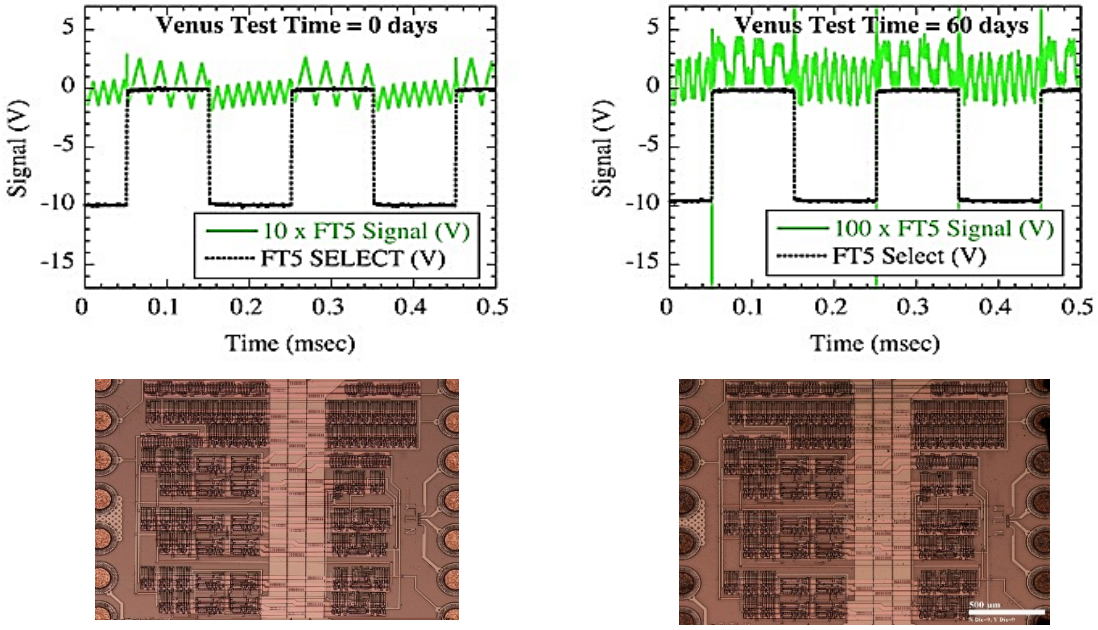

Figure 2.2.2. Testing of Clock Circuit for 60 days in Venus simulated environment. Clock operation and optical picture of an operational clock circuit before (left) and after (right) operation in simulated surface conditions for 60 days. Any wave form changes in the 60 day output data is due to the feedthroughs into the GEER chamber, not the core circuit operation.

This work has since been notably expanded on in both complexity and duration. A two-month (60-day) operational demonstration of two 175-transistor SiC JFET clock circuits directly exposed

in GEER in Venus simulated surface conditions was successfully completed. This is an almost threefold increase in operational time and with SiC JFET chips of more than sevenfold increased IC complexity [13]. Figure 2.2.2 shows both the device response and the micrographs of these clock circuits. The operation of the circuits was unaffected by the simulated Venus surface exposure (any apparent change in signal is due to noise introduction by the electrical feedthroughs into the chamber), and the devices themselves appear nearly unchanged. One feature of this electronics development has been a detailed characterization of the materials that are durable in the reactive Venus surface environment [14]; the most durable of these materials are core to the circuit and packaging construction and are also viable in jet engine applications. Thus the near identical device images before and after 60 days of GEER testing. These and other results have resulted in, e.g., Science Magazine to feature this work in an article with title: *Armed With Tough Computer Chips Scientists Are Ready To Return To The Hell Of Venus* [15].

2.3 Venus Lander (LLISSE) Electronics Development

Development has begun on a small probe system to enable long-lived surface missions based in part on this development of high temperature electronics. In particular, the Long-Lived In-Situ Solar System Explorer (LLISSE) is a small probe system to enable a long-lived Venus surface mission. Such a probe would operate on the 465°C, 92 atmosphere caustic environment of the Venus surface for 60 days or more while providing measurements and uniquely contributing to our understanding of key questions for Venus exploration [16]. As described in another white paper (see list below), LLISSE is also a platform for a variety other science missions through modifications of the associated sensors and operational approach. Core to any of these missions are the high electronics temperature electronics that operate the overall system.

Efforts have been on-going to produce integrated circuits to enable all aspects of LLISSE operational for months. Functionalities being developed as part of on-going development of the LLISSE lander system include:

- Amplification of the analog sensor signals
- Sequential sampling of data from multiple analog sensors
- Digitization of the analog inputs
- Processing of digitized data from each sensor for transmission to an orbiter.

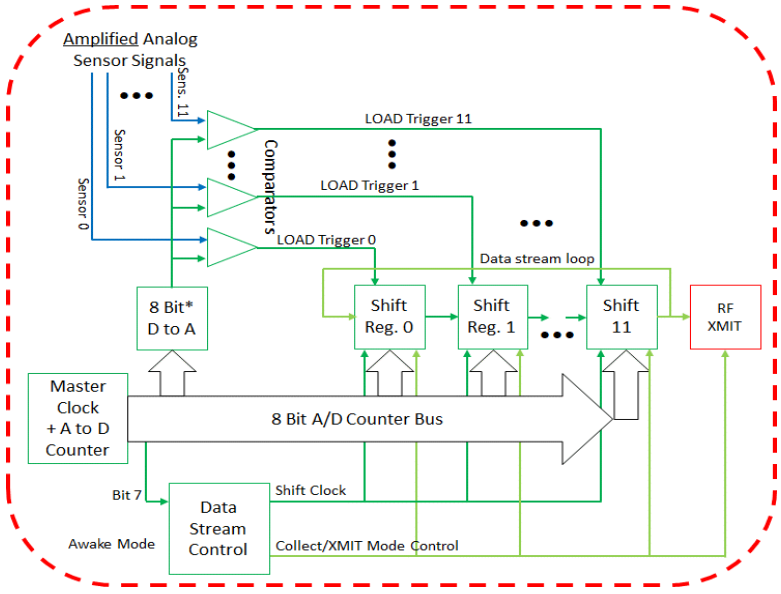

Figure 2.3.1. Baseline electronics processing approach for LLISSE.

The approach used to accomplish these basic functionalities are shown in Figure 2.3.1. Other components of the system not shown include a timer circuit that turns on the system at set periodic intervals. Figure 2.3.1 shows the need for a number of circuits including those for amplification, triggering, shift registers, an A/D counter, data stream control, and a master clock. Circuits with the capability to provide these basic sensor and data processing functionalities

for LLISSE have been designed and fabricated. Further work will be needed to increase circuit complexity, decrease the number of chip counts and power usage, and address thermal stress issues.

Further work will also be needed to address other aspects of LLISSE operations not described in Figure 2.3.1. This includes power control and timer circuitry, as well as communications at 100 MHz frequency. In parallel, major increases in circuit complexity are planned; it is estimated that the circuits will become at least 20-fold more complicated with 50% reduced power use versus presently demonstrated circuits over the next two years, with a corresponding increase in capability. This increase in functionality and complexity will be the foundation for realizing LLISSE as an operational system.

LLISSE sensors and electronics development have also been on-going in parallel. The core of this work is to couple the electronics with the sensors to assure that the electronics can provide the needed capabilities to amplify and process sensor data in order to meet science needs. The most notable example of this develop is in the area of chemical sensors with electronics (See HOTTech discussion below). Likewise, a temperature sensor integrated with electronics has been operated for 60 days in Venus simulated conditions, a wind sensor with electronics has tracked the controlled introduction of gases into the GEER chamber during operation, and multiple versions of a pressure sensor have been coupled with electronics in GEER.

In summary, as part of LLISSE development, high temperature electronics have been demonstrated in simulated Venus surface environmental conditions for up to 60 days, coupled with sensor technology, and the core circuits for LLISSE sensor and data processing functionality have been fabricated. Further work is needed to increase circuit complexity, decrease power usage, address thermal stress issues, and for power control and communications. Development and associated relevant environment demonstrations are planned to occur between in the early 2020's, and feed into the development of, e.g., a LLISSE Engineering Model or the LLISSE Technology Demonstrator (LLISSE-TD) in the next 2-3 years to follow.

2.4 Other Venus Relevant Electronics Development

Other NASA funded activities have also been underway related to developing high temperature technologies for Venus applications. A major effort has been the High Operating Temperature Technology (HOTTech) Project [17]. The primary science objective of the project is to develop and mature technologies that will enable, significantly enhance, or reduce technical risk for in situ missions to high-temperature environments with temperatures approaching 500°C or higher for the robotic exploration of high-temperature environments such as the Venus surface, Mercury, or the deep atmosphere of Gas Giants.

Two major activities related to SiC electronics are on-going in HOTTech. One is noted above: Demonstrate high temperature electronics integrated with an array of high temperature chemical sensors for use in extended duration Venus surface measurements. Notable progress has been made in this work with 4 sensors showing operation in Venus conditions for 60 days. One of those sensors, a hydrogen fluoride (HF) sensor, was later integrated with basic high temperature electronics, operated in GEER simulated Venus conditions, and the combined system showed response to a controlled introduction of HF into the GEER chamber ambient. This HOTTech activity directly feeds into the LLISSE project and is also planned to culminate with a demonstration of chemical sensors suspended from a UAV measuring emissions from volcanic magma.

A second SiC electronics activity in HOTTech is the development and demonstration high temperature memory circuits, RAM and Read Only Memory (ROM), operable for extended

periods in Venus environments. Both circuit types have been fabricated, RAM already demonstrated for extend periods at 500°C [9], and the planned culmination of this project is extended operation of memory at 500°C and in GEER simulated Venus surface environments. Such a capability can change the nature of extended Venus surface missions, but would require improved high power density sources.

Beyond HOTTech, other funded high temperature electronics developments includes that for a long-lived Venus surface imager (Venus In-Situ Surface Imager) funded under the Planetary Instrument Concepts for the Advancement of Solar System Observations (PICASSO) program [18]. This work processes signals from a photodiode array as part of a proof-of-concept Venus imager patterned after that of the Mars Viking lander. *Further, radiation testing has also shown that SiC JFET ICs can operate for years in the high-radiation environments of Jovian moons or nuclear reactors without the radiation shielding that is typically required for silicon-based electronics* [19]. Future work include the design and fabrication a simple SiC JFET based microprocessor and evaluate its radiation durability.

Relevant Decadal Whitepapers

- Long-Lived In-Situ Solar System Explorer (LLISSE), Potential Contributions to the next decade of Solar System Exploration, Lead: T. Kremic, NASA Glenn Research Center
- Venus Lander Surface Platform Study, Lead: T. Kremic, NASA Glenn Research Center
- The Venus Strategic Plan, Lead: N. R. Izenberg, Johns Hopkins University Applied Physics Lab
- The Importance of Venus Experimental Facilities, Lead: A. Santos, NASA Glenn Research Center

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