National Aeronautics and Space Administration

Micron MT29F1T08CMHBBJ4
1Tb NAND Flash Memory
Single Event Effect Characterization Test Report

Prepared by:

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Date

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1. Introduction

The purpose of this testing is to characterize the Single-Event Effect (SEE) response of the Micron MT29F1T08CMHBBJ4 3D NAND Flash memory. The MT29F1T08CMHBBJ4 is a 1Tb NAND Flash memory, consisting of a four-die stack of 256Gb MLC dice packaged in a 132-ball VBGA package. All data presented is the result of testing only the top die (256Gb) of the package. Testing was performed at two heavy-ion cyclotron facilities with an identical test setup, over the course of four test trips from 2017-2019.

Total ionizing dose (TID) testing was not performed as part of this work.

2. Devices Under Test

Thirty (30) parts from a commercial lot of MT29F1T08CMHBBJ4 were provided to Code 561 for testing. A total of seven (7) devices were exposed to the heavy ion beams while testing. All of these devices were deemed functional after acid-etching necessary to expose the top die, and performed in accordance with specifications and descriptions from the Micron MT29F1T08CMHBBJ4 datasheet. Part identification information can be found in Table I, while the memory organization of the device is shown in Figure 1. Pinouts and extra information can be found in the datasheet.

Table I: Part Identification Information

Qty	Part Number	LDC	REAG-ID	Package
7	MT29F1T08CMHBBJ4	-	17-049	132-Ball VBGA – 12mm x 18mm (Package Code: J4)

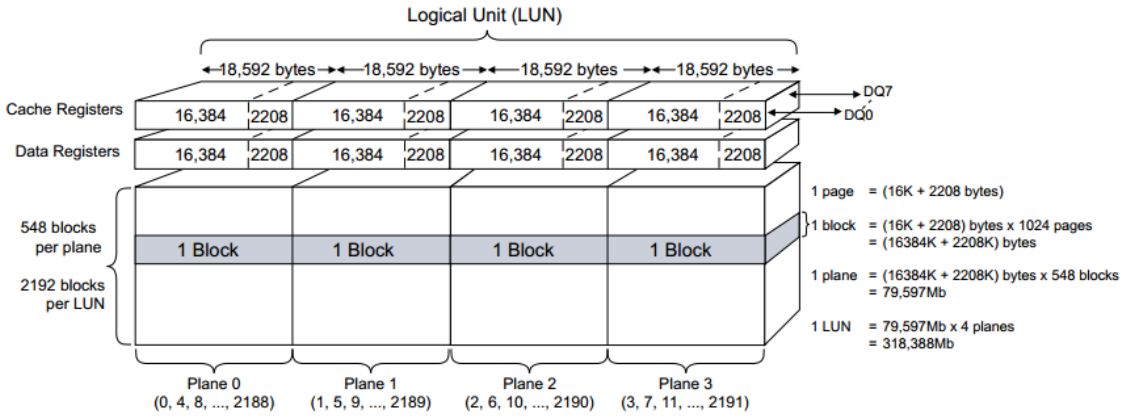

Figure 1: Memory organization for MT29F1T08CMHBBJ4

3. Test Setup

a. Hardware

A custom PCB was developed for the MT29F1T08CMHBBJ4 (Fig. 2, below). The board provides a BGA footprint for the flash memory to be soldered in place, and a socket for a microcontroller board to be attached for test operation. The microcontroller board is the commercially-available Teensy 3.6 (PJRC, Inc.) which has an ARM Cortex-M4 MCU overclocked to operate at 240 MHz. The microcontroller I/O for control and data pins is routed through a set of high-speed level shifters to interface with the flash memory's 1.8-V I/O level.

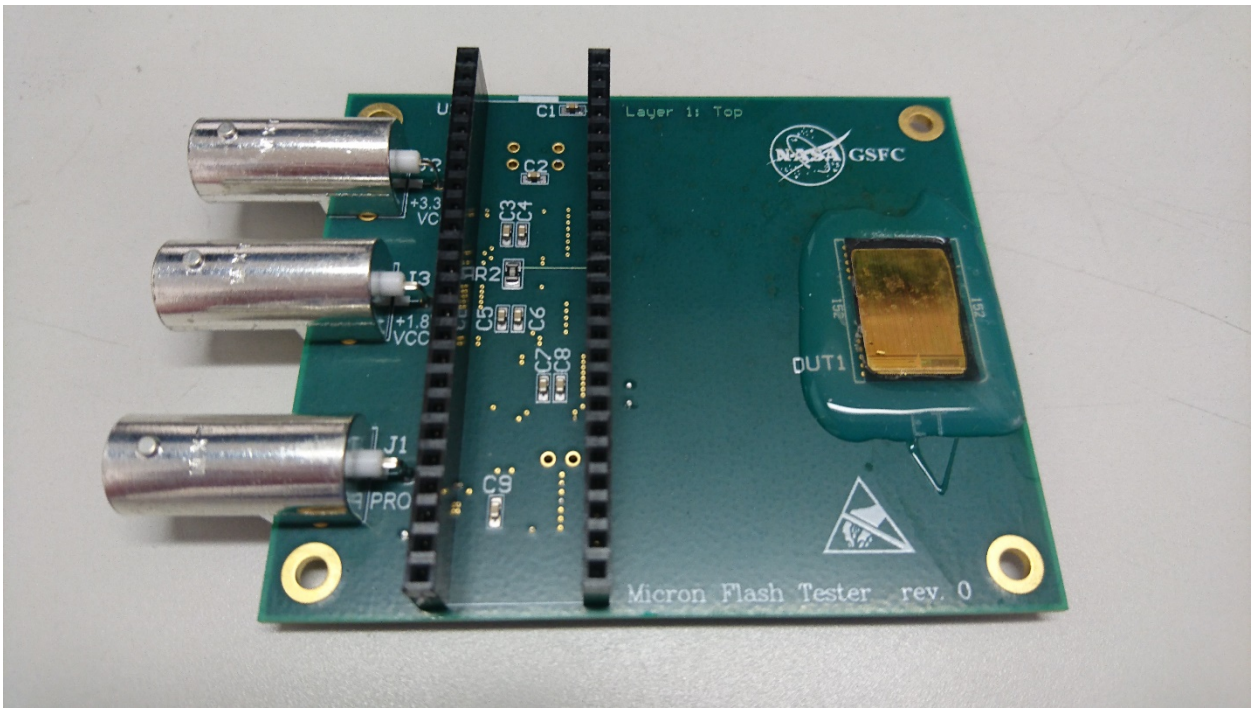

Figure 2. A single testing circuit board

b. Software

Software written for the microcontroller allowed a set of basic operations to be performed. Those operations included erasing, programming, and reading a specified area of memory. Those low-level operations were combined into larger test modes that defined a single irradiation run. Control of the test modes, and logging of operational and error data, came from a host computer over a USB link. The die temperature was monitored using the internal temperature sensing feature of this device, and was logged with the other test data on the host PC.

The test modes available in the microcontroller software included **static testing**, where the memory was erased, programmed, and verified before irradiation. After irradiation (either with the power off or with power on in a standby mode) the device was re-read to check for memory errors. **Dynamic read-only** testing added continuous reading of the memory array during irradiation.

Dynamic read-write testing included a loop of erasing, programming, and reading repeated throughout the irradiation.

c. Test Equipment

A three-channel Keithley 2230-30-1 DC power supply provided power to the DUT. The VCC was set to a nominal 3.3 V, while VCCQ was set to 1.8 V. The microcontroller used to control the flash memory was powered separately via its USB link. Command and data messages were communicated between the host PC and microcontroller via a 10Mbps serial link over USB. The power supply currents were logged with a LabView program that communicated over USB with the power supply.

4. Test Performance

a. DUT Preparation

This SEE test required decapsulation of the plastic package to expose the device to the heavy-ion beam and ensure sufficient penetration of the individual ions into the active regions of the die. The devices were decapsulated with a mixture of nitric and sulfuric acid, and functionality was confirmed post-decapsulation.

The memory was configured to operate in both single level cell (SLC) and multi-level cell (MLC) modes to characterize the radiation response in each. The memory was exercised in both static and dynamic mode, with varying data patterns, to fully explore different sensitivities and error response signatures.

b. Test Facility

Initial heavy-ion testing was performed at the Texas A&M University Cyclotron Facility (TAMU) in 2017, using their K500 cyclotron at the 15 MeV/amu tune. Follow on testing was performed at the Lawrence Berkeley National Lab (LBNL) 88” Cyclotron at the 10 MeV/amu tune in 2017, TAMU in 2018, and LBNL in 2019.

The Linear Energy Transfer (LET) of the heavy ions, essentially a measure of energy deposited per unit length, was varied to record the radiation response of the device to particles encountered in a typical space environment. Several different ion species were tested, and the SEE cross section of the device (errors divided by total particle fluence) at each LET was recorded in order to characterize the device’s SEE sensitivity. The following ions in Tables II and III were used for this test at the listed LET and range:

Table II: TAMU Ions Used

Ion	LET (MeV*cm^2/mg) After 1mil Aramica and 50mm air	Range in Si (µm)
Ne	2.8	267.5
Ar	8.6	180.1
Kr	28.8	122

Table III: LBNL Ions Used

Ion	LET (MeV*cm^2/mg) In vacuum	Range in Si (µm)	Beam Tune (MeV/amu)
B	0.89	305.7	10
Ne	3.49	174.6	10
Ar	9.74	130.1	10
Cu	21.17	108.0	10
Kr	30.86	109.9	10
Ag	48.15	90.0	10
Xe	58.78	90.0	10
Au	85.76	105.9	10

In addition to the LET from Tables II and III, the devices were rotated in the beam line after being tested at normal incidence to get a higher effective LET for each ion. Rotating the device does reduce the range of the particles in the material but was sufficient to traverse the top device die. The angles that were used: 0˚, 30˚, and 40˚ where the LET and range fall off as 1/cosϴ.

The MT29F1T08CMHBBJ4 test setup consisted of a host PC in the control room, and a power supply test board in the irradiation room. A USB cable connected the host PC to the equipment in the irradiation room. The DUT was aligned with the center of the beam, as shown in Figure 3, for all angles with saved positioning. Figure 4 is the board on the end of the beam-line at TAMU. Figure 5 shows the board in the chamber at LBNL.

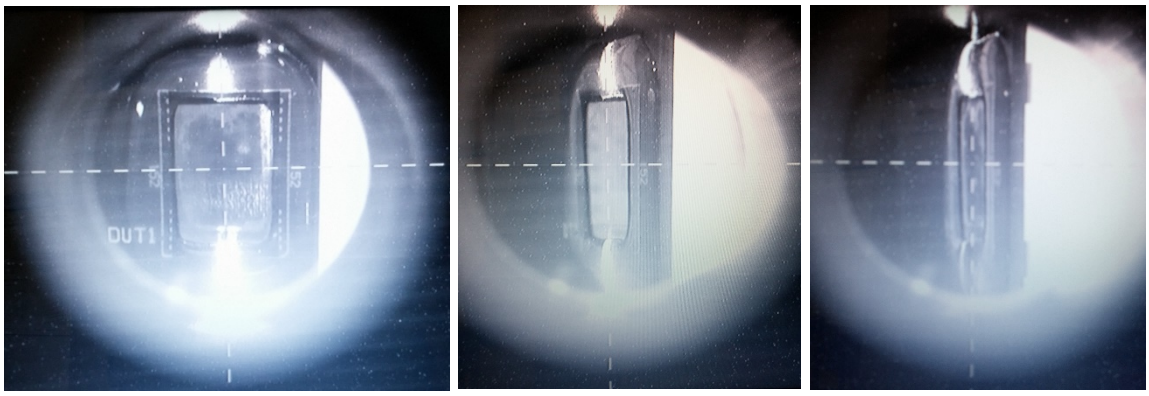

Figure 3: Opened device centered in beamline camera at all angles tested 0, 45, and 60.

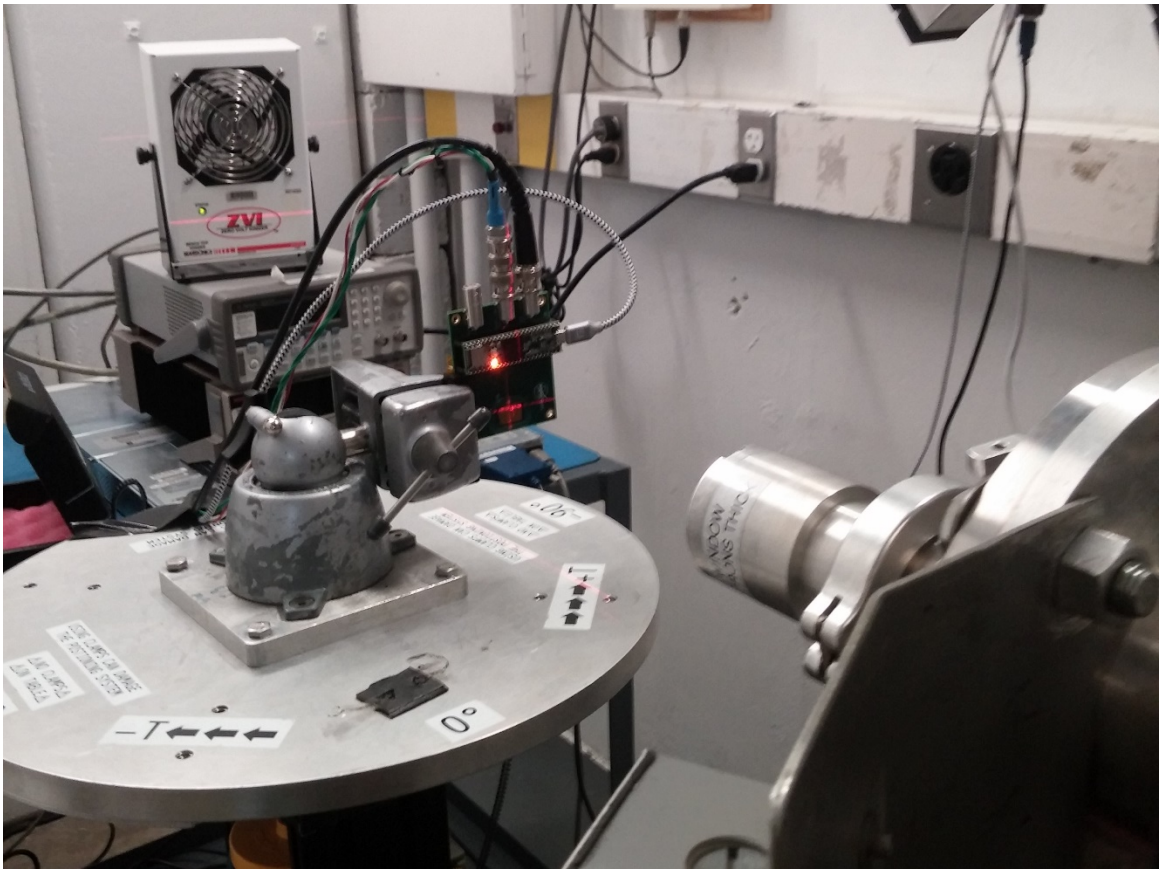

Figure 4: The MT29F1T08CMHBBJ4 setup aligning in the beam-line at TAMU.

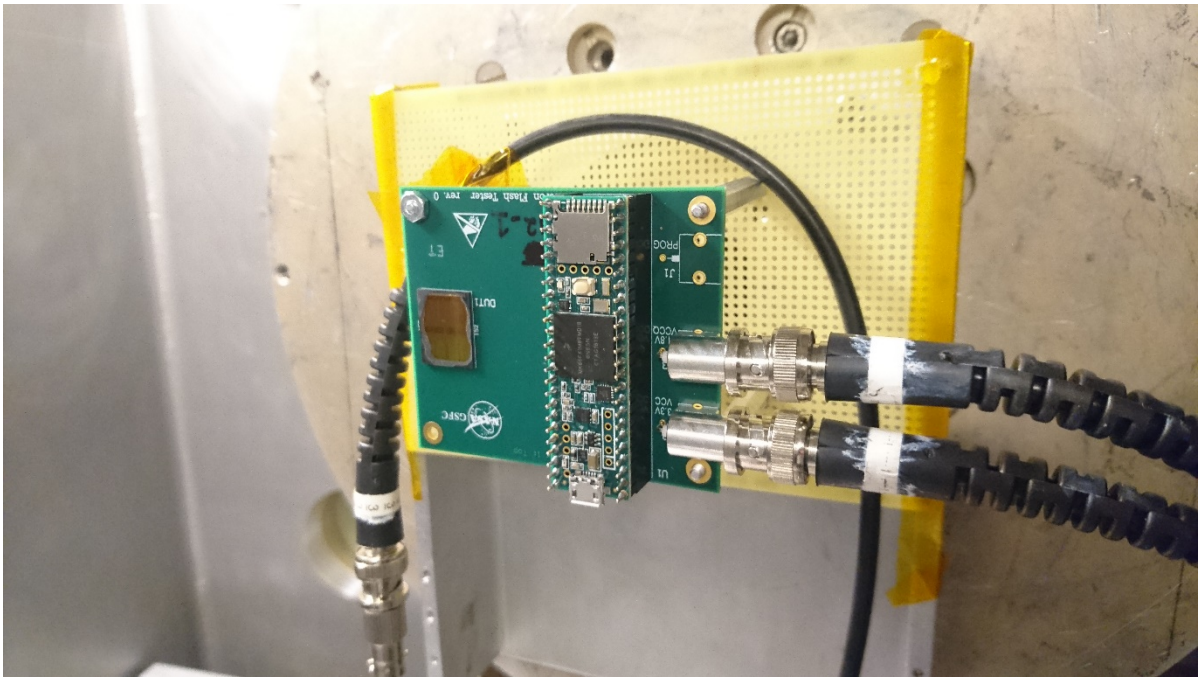

Figure 5: The MT29F1T08CMHBBJ4 setup in the vacuum chamber before closure at LBNL.

c. Test Run Configurations & Memory Organization

Each test run started with a complete power cycle to the test setup. The microcontroller tester was configured to operate the device in the manner required (data pattern, operational mode, SLC vs. MLC, memory test size), and then a pre-irradiation erase/program/readback cycle was performed to characterize the device's performance prior to each run. Each pre-rad readback cycle counted the intrinsic errors of the device, which would normally be corrected by ECC handled at the controller level. The number of intrinsic errors depends on the mode of operation; SLC operation has lower numbers of intrinsic errors because it has higher margins in each flash cell. No ECC was used during this testing.

Static test runs typically used 10 entire, contiguous blocks of memory free of any pre-marked bad blocks. Dynamic runs typically used 100 blocks (excluding any pre-marked bad blocks) but only tested the first 8 pages in each block in an effort to test a larger number of blocks in a fast time. Details on the memory sizes tested and typical pre-rad errors are shown below in Table IV.

Table IV: Memory Configuration and Pre-Rad Error Counts

Test Type	Cell Config	Blocks	Pages Per Block	Range of Pre-Rad Errors
Static	SLC	10	512	20 - 400
Dynamic	SLC	100	8	0 - 200
Static	MLC	10	1024	2700 - 7800

After pre-rad characterization, the power supply logging was initiated and the heavy-ion beam activated. For a static run, the beam remained on until a pre-set fluence limit was reached. For a dynamic run (read-only or read-write) the run ended when either the pre-set limit was reached, or a SEFI was observed.

5. Test Results

a. Single-Event Latchup

No destructive SEE, including single-event latchup (SEL) were observed throughout the testing, up to the highest LET tested (58.78 MeV*cm^2/mg). Testing was performed at nominal voltage (V_{cc} = 3.3 V, V_{CCQ} = 1.8 V). One device was exposed to a cumulative fluence greater than 1x10^{7}cm^{-2} at this LET. The device temperature was maintained at approximately 60°C for this test.

b. Single-Event Upsets

The memory is susceptible to single event upsets (SEU) induced by a heavy ion strike. Both single- and multiple-bit upsets within a single byte were observed in testing. Due to the 3D structure of the device, a single particle can cause multiple single-bit upsets (SBUs) in different words as it traverses the layered memory. A cross-section vs. LET plot is shown below. The LET threshold for SEU in SLC mode is less than the lowest LET tested (0.89 MeV*cm^2/mg).

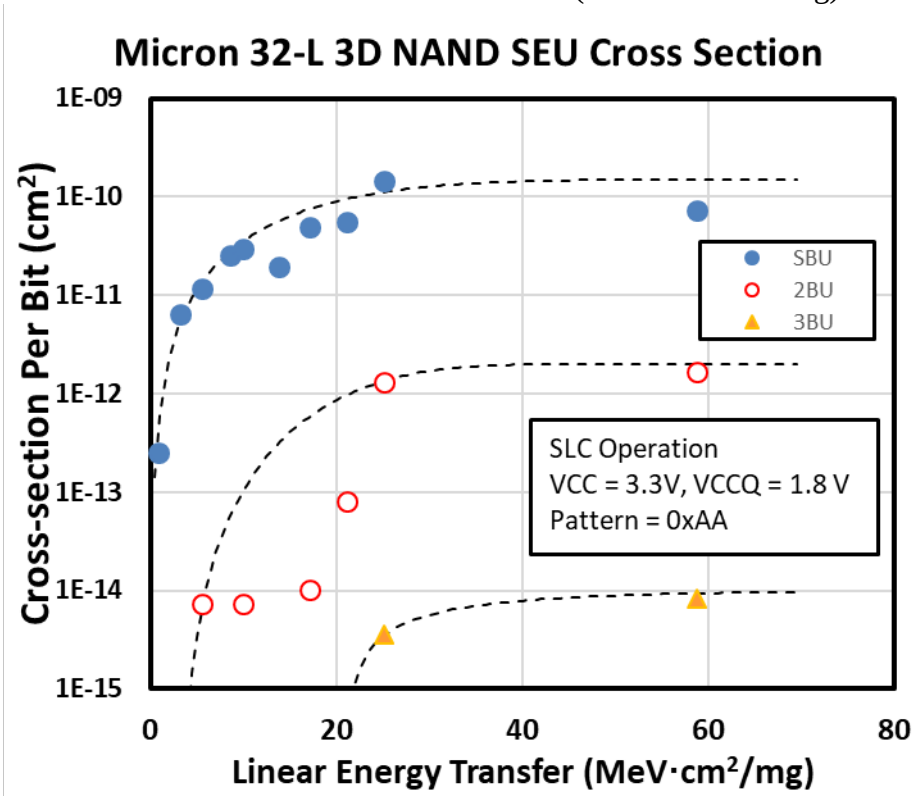

Figure 6: MT29F1T08CMHBBJ4 error cross section, comparing bit error cross sections for single-bit, 2-bit, and 3+-bit errors. This data was obtained in SLC mode.

c. Single-Event Functional Interrupts (SEFI)

Single-event functional interrupts (SEFI) are those errors that interrupt normal device functionality. With these NAND flash devices, SEFIs commonly resulted in large numbers of apparent errors (potentially affecting entire pages/blocks) when reading back the memory. They can be detected either by a suddenly-large increase in memory errors, a failure to properly respond to queries (for example, incorrect device ID or features), or a total lack of communication. A software reset was generally ineffective in restoring normal operation, but a power cycle was always effective. After reset, the large blocks of errors were cleared and only the radiation-induced SEUs remained, along with any pre-irradiation bit errors.

d. High Current SEFIs

During the 2017 and 2018 tests, SEFI modes were identified with elevated current states. It was not believed that these are due to a physical latchup mechanism. The 2019 test attempted to further characterize these events, understand their effect on the device under test, and their impact on the other die in the stacked package.

The cleanest data set for evaluating SEFIs comes from the 2019 test. Elevated currents were only observed in the 2019 test when operated at a flux greater than $1x10^3/cm^2/s$. It is not known whether the flux directly impacts the sensitivity (i.e. multiple strikes in quick succession causing a SEFI) or whether it is simply due to the larger statistical sample that a higher flux allows. In either case, the sensitivity to these high-current states is quite low.

At the highest LET tested (**85.8 MeV·cm^2/mg**, an exceptionally high value) the first run to a total fluence of $1x10^7/cm^2$ with an average flux of $2.4x10^4/cm^2/s$ resulted in several changes to the steady-state current while continuously reading the device ID under beam. The peak value appeared to be 101mA while operating with a 250mA current limit. It cannot be determined exactly how many independent events occurred, as the run was allowed to continue to look for destructive events (none were observed). The device temperature was maintained at approximately **78°C**. Based on this data, it is concluded that there is no susceptibility to destructive single-event effects.

Following that run, nine runs were conducted with the same beam, but a much slower flux ($3x10^2/cm^2/s$ to $3x10^3/cm^2/s$). All runs continuously polled the memory for the device ID; none experienced a change in supply current. Two of the nine runs experienced a SEFI in which the device ID was no longer accurate. The total fluence of these runs was $1.11x10^6/cm^2$. It is concluded that the sensitive cross-section to high-current SEFIs is less than $1/(1.11x10^6/cm^2)$.

Similar results were observed with silver and copper beams having respective LETs of 48.15 and 21.17 MeV·cm^2/mg. No high-current events occurred with lower LETs, though their data are presented as a limiting cross-section. A threshold appears to be approximately 9.74 MeV·cm2/mg, the highest LET for which no events were observed under any condition.

e. Block SEFIs

The vast majority of SEFIs did not result in a high current level and resulted in at least one block that was unresponsive to commands, failed to write data, or returned garbage (though without disrupting the actual stored data). Many events resulted in a single block that was affected, though a number of runs had multiple blocks were affected during a single event. The rate of block SEFI, then, is slightly higher than the rate of all SEFI events because multiple blocks can be SEFI'd during a single event. The cross-sectional data for block SEFIs is shown in Fig. 7.

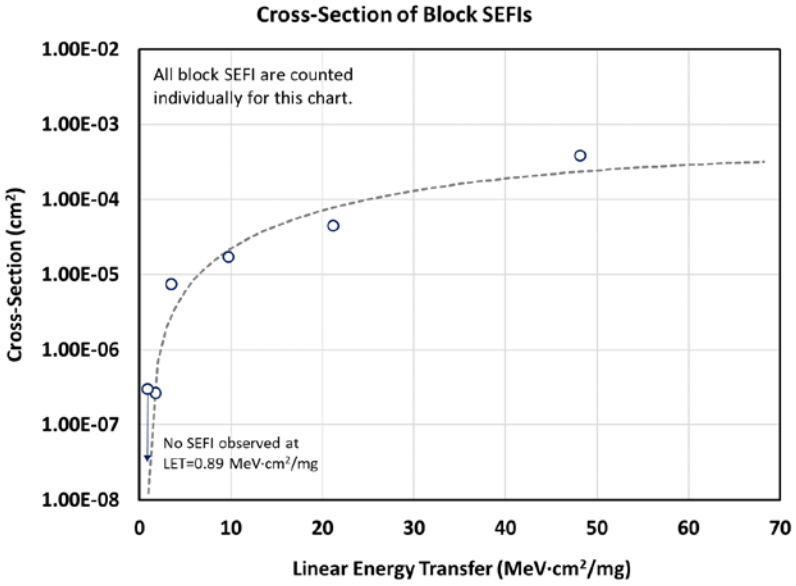

Fig. 7. Block SEFI cross-section vs. LET curve

f. All SEFI Events

All SEFIs observed, including those that resulted in a current increase or at least one block SEFI, are shown below. These are predominantly block errors (from 1-3 blocks at a time that fail to erase, program, or readback correctly) and were captured with dynamic read/write testing. Those data are plotted for two operating voltages, 3.3 V (nominal) and 2.7 V (the lower limit for this part). No substantial difference was noted between the two voltages. The red circles represent SEFIs observed during "READ ID" testing during which the memory was kept in a static configuration and only the device ID was queried periodically to validate communication with the part.

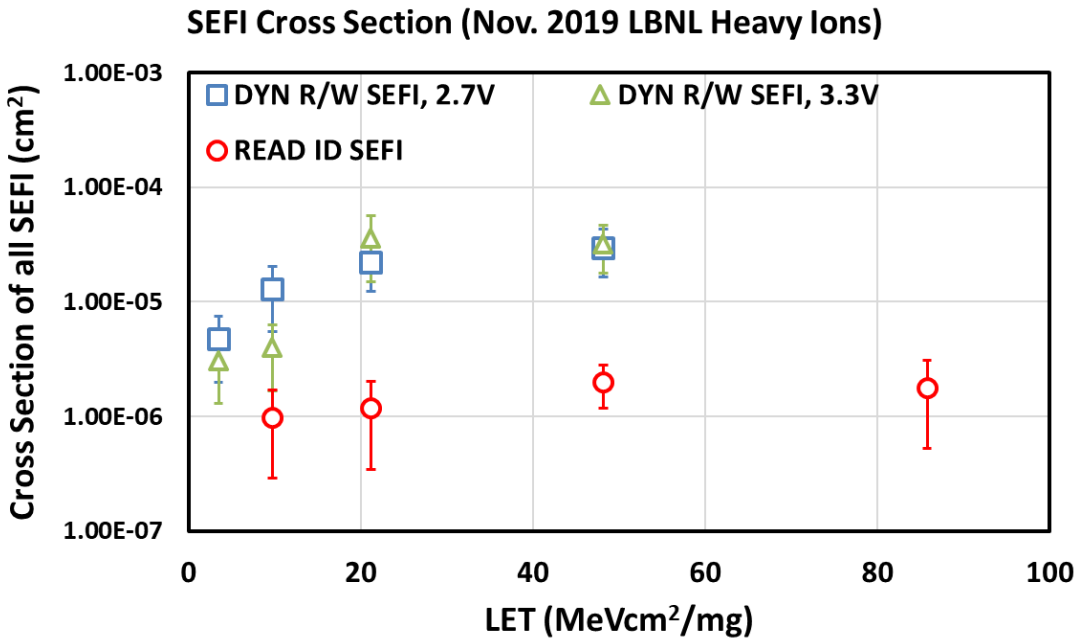

Fig. 8. Cross section vs. LET data for all SEFI observed during different testing modes.

6. Conclusions

The MT29F1T08CMHBBJ4 does not exhibit any destructive SEE up to and including the highest tested LET. Functional interruptions requiring a reset and/or power cycle (SEFIs) will likely occur during a typical mission, but at a rate of less than once per year per die during background radiation conditions outside of Earth's magnetosphere. Bit errors (predominantly single-bit errors) will occur in the memory array and must be handled with an appropriate EDAC scheme in accordance with any other mission- or manufacturer-required ECC levels. To provide some context, one rate estimation of single-bit errors computed ~8E-11/bit/day in near-Earth interplanetary space, or ~30,000 per Tb per year during solar minimum, though mission-specific calculations must be determined by the user. Solar flare activity may briefly increase these rates by several orders of magnitude.

Some single-event functional interrupts (SEFI) are accompanied by elevated current levels, possibly due to uncommanded operations, electrical bus contention, or other mis-configured operational modes. These levels remain within the extreme maximums on the datasheet and commonly require a power-cycle to the device to clear. It is unclear what effect extended operation at these current levels could have on device reliability.

7. References

[1] Micron MT29F1T08CMHBBJ4 datasheet marked Rev. M 12/29/2016