National Aeronautics and Space Administration

Vorago RH-OBC-1
Single Event Effect Characterization Test Report

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1 Introduction

The Vorago Technologies RH-OBC-1 is a CubeSat Kit Bus compatible single board computer with a Vorago VA10820 ARM Cortex-M0 microcontroller at its core. The board also includes a set of common peripheral integrated circuits, like voltage regulators, non-volatile memories (NVM), an analog-to-digital converter (ADC), a watchdog/supervisor, and a Controller Area Network (CAN) bus transceiver. Many of these components are either radiation hardened or available as rad hard versions. A universal serial bus (USB) controller is also provided for ground programming/debugging, but is not powered in flight. CubeSat-specific components like a PC104 header and remove-before-flight switch are provided for standard CubeSat applications.

A power supply gating circuit implemented by Vorago can cycle power to isolated 3.3V and 5V rails which power the commercial CAN transceiver, such that it can be rebooted in the event of an on-orbit single-event latchup without affecting the rest of the system. The system can be triggered by the MCU or by the ISL706 supervisor/watchdog device. No provision exists to power cycle the other components on the standard board, which are directly tied to the primary power rails.

High-energy proton (200 MeV) testing was conducted at both board and component levels to investigate single-event effects. Several of the individual components also have piece-part radiation data available from various sources, and one of the primary objectives of this test was to evaluate the performance of the board overall and identify any issues that arise from board-level testing. Limited total ionizing dose data was also obtained as a byproduct of this proton test.

The VA10820 microcontroller (MCU) has previously been characterized for single-event effects by Vorago using heavy ions at Lawrence Berkeley National Lab. Contact Vorago directly for details.

2 Devices Under Test

One single-board computer (SBC) was provided to NASA GSFC Code 561 for testing. The board was modified to allow for additional instrumentation during testing by inserting voltage probes and current-monitoring resistors to each component on the board. No decapsulation was required or performed for this proton test.

Table I: Part Identification Information

Qty	Part Number	LDC	REAG-ID	Package
1	RH-OBC-1	-	18-035	CubeSat compatible board

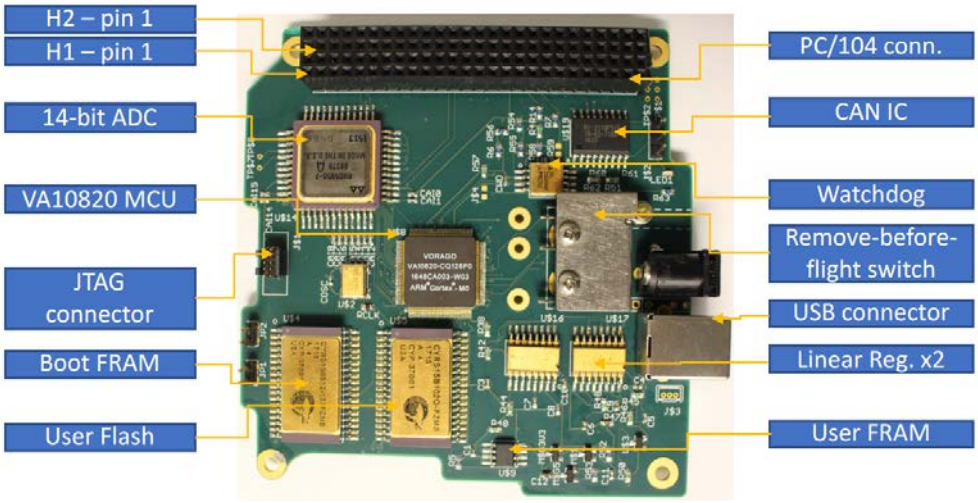

Figure 1: RH-OBC-1 components

3 Test Setup

3.1 Hardware

The RH-OBC-1 printed circuit board (PCB) was modified by the addition of a number of voltage monitoring test points and current-monitoring resistors such that voltage and current at each component could be monitored in real-time during board-level testing. Modifications were implemented by manually lifting the power pins for each component and inserting a surface mount resistor in series, then adding wires to a motherboard that was attached to the SBC's 104-pin header (where it monitored additional signals present on the header). All monitored signals were routed to an Agilent data acquisition instrument (DAQ) where the internal DMM rapidly read each value. By this means, a single-event latchup or SEFI event that blocked communication with the SBC could be traced back to an individual component.

In addition, the resistors which program the output values of the two low dropout voltage regulators (LDOs) were modified; the existing resistors were left installed to keep the SBC in a usable condition, but additional resistors were installed in parallel on the motherboard with switches to include them in the voltage divider circuit. Ultimately, the programmed output voltages of the 3.3

V and 1.5 V regulators could be adjusted up to a 3.6 V / 1.65 V setting or down to a 3.15 V / 1.425 V setting. The main 5 V rail could also be adjusted from the external power supply. Together, these combinations allow some exploration of corner cases of board performance, regulator degradation/damage, and process variation.

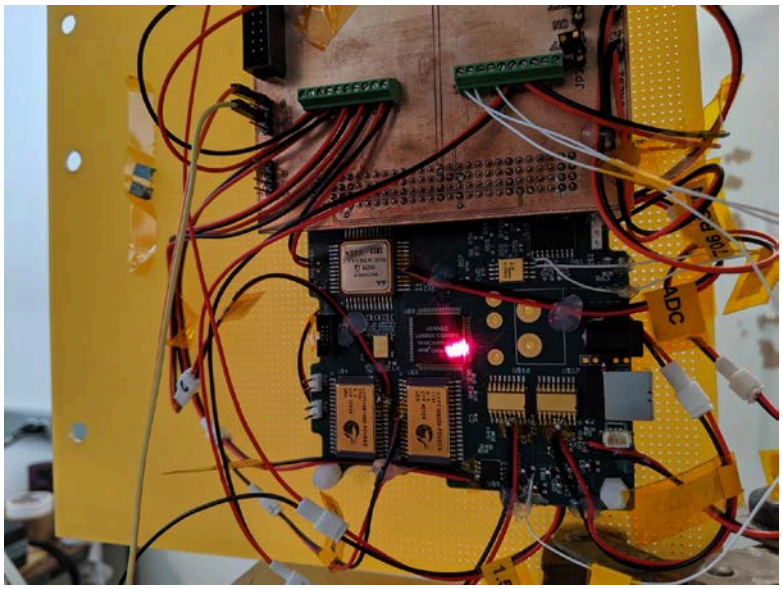

Figure 2. The SBC as modified for proton testing

3.2 Software

The Vorago board support package demo software was modified to add a series of “self-test” routines on the hardware during irradiation. A serial link provided status and results of each test routine to a remote PC. The following tests were implemented:

Table II: Software self-test routines

Test	Description
Periodic Timer Interrupt	Provides periodic “heartbeat” to confirm core functionality
RAM/ROM single-bit error (SBE)	SBE are counted by the internal error detection and correction (EDAC) system and sorted by memory type and address.
RAM/ROM multi-bit error (MBE)	Uncorrectable MBE result in an automatic reset with traceability from a MERESET vector at boot.
I2C Loopback	Loopback configured on SBC; returns count of incorrect bytes from each transmission.
SPI Loopback	Loopback configured on SBC; returns count of incorrect bytes from each transmission.
CAN Test	Loopback configured on SBC; returns count of incorrect bytes from each transmission. In case of miscompare, power to CAN transceiver is cycled by using SBC’s power supply gating feature
User Flash Test	Flash memory is periodically verified for correct data. Errors are reported. Every four loops the memory is erased, programmed, and verified.
User FRAM Test	Reads and writes 64 bytes each iteration and reports the number of errors. More than one errors results in a reset attempt of the interface.
Boot FRAM Test	Reads and writes 64 bytes each iteration and reports the number of errors. More than one errors results in a reset attempt of the interface.
ADC Test	Reads and averages eight samples each from channels 9 and 10. Averages outside of a pre-programmed bounding window indicate a significant error and result in a reset of the GPIO port and command to reinitialize the ADC.

3.3 Test Equipment

An Agilent 34970A Data Acquisition (DAQ) instrument monitored voltages in real-time, with logging done on an external PC running Agilent Benchlink software. The voltages measured were a combination of direct voltage measurements and current-shunt resistor voltage drops.

4 Test Performance

4.1 Test Facility

The proton irradiation was performed at the Massachusetts General Hospital's Francis Burr Proton Therapy Center in June 2019. The cyclotron was tuned to deliver 200 MeV protons in a scattered pattern through two collimators sizes; a 2.8cm collimator was used to irradiation individual components, while a 16cm collimator was used to irradiate the entire board. The facility provides a separate test cave for scientific users, with substantial cable run (~75ft) to the outside data monitoring tables.

Table III: MGH Beam Configuration

Ion	Initial Energy (MeV)	Flux	Delivery	Spot Size
P+	200	$4x10^7$ - $8x10^7/cm^2/s$	Scatter	2.8 cm
P+	200	~$1x10^8/cm^2/s$	Scatter	16 cm

Figure 3: Test board in direct beam line (see laser dot) inside the irradiation cave

5 Test Results

The large variety of test combinations possible could not be fully explored in the time available. However, a number of tests were run on the full board and on individual components. The results are best presented sorted by the component(s) being irradiated, and are summarized as such in the following sections.

5.1 Single-Component Collimated Beam Tests

Four of the on-board components were individually irradiated by using a 2.8 cm collimator on the beam line. These tests exposed the processor (MCU), CAN transceiver, user FRAM, and boot FRAM individually while monitoring the overall system response. The remaining components were only tested at board-level and showed no errors. For some runs, the voltages generated by the on-board voltage regulators were adjusted to explore their effect on system response to SEE.

5.1.1 VA10820 MCU Irradiations

Focused Irradiations - VA10820 MCU							
Run	**Voltage Regulators (V)**	**Energy (MeV)**	**Flux p+/cm2/s**	**Fluence p+/cm2**	**ROM SBE**	**RAM SBE**	**Other Events**
1	3.3/1.5	200	5.10E+07	1.00E+10	1136	286	None
2	3.6/1.65	200	4.75E+07	1.00E+10	1025	250	None
3	3.15/1.425	200	5.63E+07	1.00E+10	1265	301	None
19	3.3/1.5	200	7.77E+07	1.00E+11	3285	847	None

5.1.2 HI-3110 CAN Transceiver Irradiations

Focused Irradiations - HI-3110 CAN Transceiver					
Run	**Voltage Regulators (V)**	**Energy (MeV)**	**Flux p+/cm2/s**	**Fluence p+/cm2**	**Errors Noted**
4	3.6/1.65	200	6.61E+07	1.00E+10	No errors observed.

5.1.3 FM25V20A User FRAM

Focused Irradiations - FM25V20A User FRAM					
Run	**Voltage Regulators (V)**	**Energy (MeV)**	**Flux p+/cm2/s**	**Fluence p+/cm2**	**Errors Noted**
5	3.6/1.65	200	5.59E+07	1.84E+09	SEFI with continuous 0xFF data from FRAM; power cycle required
6	3.6/1.65	200	5.62E+07	2.00E+10	No errors observed.
7	3.3/1.5	200	5.97E+07	1.11E+10	SEFI with continuous 0xFF data from FRAM; power cycle required

5.1.4 CYPT15B102 Boot FRAM

Focused Irradiations - CYPT15B102 Boot FRAM					
Run	**Voltage Regulators (V)**	**Energy (MeV)**	**Flux p+/cm2/s**	**Fluence p+/cm2**	**Errors Noted**
18	3.3/1.5	200	6.87E+07	1.95E+10	Run aborted when SEFI detected; all readbacks 0xFF; power cycle required

5.2 Full Board Irradiations

Run	Main Board Power (V)	Voltage Reg. Setting (V)	Energy (MeV)	Flux p+/cm2/s	Fluence p+/cm2	ROM SBE	RAM SBE	Other Errors	Notes
8	5.0	3.3/1.5	200	1.10E+08	1.19E+09	not available	not available		
9	5.0	3.3/1.5	200	1.08E+08	1.00E+10	369	108		
10	5.0	3.3/1.5	200	1.01E+08	2.50E+09			MCU Reset	Mysterious device reset generated within MCU; device did not report a valid reset source upon boot as it would from a multi-bit error, external reset, power on reset, etc.
11	5.0	3.3/1.5	200	9.99E+07	9.17E+09	358	107		
12	5.0	3.3/1.5	200	1.10E+08	1.01E+10	not available	not available	Boot FRAM SEFI	Boot FRAM errors indicated SEFI; Reset signal was sent to MCU which correctly rebooted; however, MCU was then unable to load its boot code from the locked-up Boot FRAM. Watchdog detected this condition and continuously tried to restart system without success, as it could not power cycle the Boot FRAM. Board required full power cycle to restore functionality.
13	5.0	3.3/1.5	200	1.16E+08	1.00E+11	4071	931		
14	5.0	3.3/1.5	200	1.03E+08	4.98E+10	1937	495	User FRAM SEFI	User FRAM errors indicated SEFI. The rest of the system remained functional, and MCU could be rebooted successfully (from the Boot FRAM). A power cycle was necessary to restore functionality to the User FRAM.
15	5.5	3.6/1.65	200	9.82E+07	3.39E+10	not available	not available	Boot FRAM SEFI	Higher voltage conditions, same result as run #12
16	4.5	3.15/ 1.425	200	1.16E+08	6.03E+10	2609	611	User FRAM SEFI	Lower voltage conditions, same result as run #14.

6 Conclusions

The RH-OBC-1 board did not suffer any destructive effects under 200 MeV proton exposure. The entire board was subject to at least $3x10^{11}$ protons/cm^2 from the board-level irradiations alone, which also contributed approximately 12.2 krad(Si) of total dose without noticeable degradation. Single-bit errors were detected in the MCU core as expected, but were automatically handled by the device's EDAC system. No multi-bit errors were detected. One unknown reset was created inside the MCU core, and is believed to be the only MCU fault during this test. It appears to be an internal fault and did not cause a Power-On Reset (POR) to be commanded by the ISL706 watchdog/supervisor IC.

The peripherals on board had mixed results. The rad-hard Cobham ADC performed flawlessly as expected, as did rad-hard regulators and supervisor/watchdog device. The commercial CAN transceiver functioned without error. However, the two Cypress FRAM memories were both susceptible to functional interrupts (SEFI), and the board as tested lacked any means to gate power to these devices to automatically recover. Most critically, without means to cycle power to the Boot FRAM, any subsequent condition causing a commanded or uncommanded MCU reset could leave the MCU unable to reload its own boot code until an external board-level power cycle is commanded. It is possible that such a combination of faults and its consequence (requiring external intervention) would not have been detected by piece-part testing alone. Vorago now provides a mitigation strategy which includes in part powering down the Boot FRAM when not in use to avoid an unknown SEFI state at system boot.

7 References

Manufacturer's website: https://www.voragotech.com/products/rh-obc-1