Progressing -190 °C to +500 °C Durable SiC JFET ICs From MSI to LSI

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***Abstract*—** This invited paper describes prototype SiC JFET integrated circuit (IC) and packaging technology that has produced arguably the most harsh-environment durable electronics ever demonstrated. Prototype medium-scale integration (MSI) ICs fabricated by NASA Glenn Research Center have successfully operated for over 1 year in 500 °C air-ambient, over 60 days in 460 °C and 9.3 MPa pressure caustic Venus surface environment test chamber, from -190 °C to +812 °C, and radiation exposure through 7 MRad(Si) total ionizing dose and 86 MeV-cm^2/mg heavy ion strikes. Recent on-going work focused on upscaling this "go anywhere" IC capability from MSI to large-scale integration (LSI) prototype via benchmark memory ICs is described.

I. Introduction

Expansion of integrated circuit (IC) temperature limits offers important performance benefits to a variety of automotive, aerospace, deep-well drilling, and manufacturing applications [1]. The majority of these applications will demand electronics capable of *years of stable operation in the harsh environment* in physically small form without cooling overhead. Towards this end, NASA Glenn Research Center has been developing and demonstrating successive generations of increasingly capable silicon carbide (SiC) junction field effect transistor-resistor (JFET-R) ICs and packaging for extreme environments.

II. Durability Foundations

A chain of robust technologies that extends beyond the semiconductor chip itself is necessary to reach useful deployment of harsh-environment analog and digital ICs. Since failure can occur at a single weakest link, long-term 500 °C durability was prioritized as the overriding development goal. Also, the ability to conduct "cold-start" at low temperature and function through "warm-up" to high temperature was also prioritized as application-relevant. This "design for durability" approach resulted in the following IC technology foundations illustrated in Fig. 1:

- 4H-SiC: Among the most chemically inert of the wide band gap semiconductors, enabling dopants and interfaces to remain fixed/stable over long 500 °C operating times. Established 4H-SiC wafer and power diode/transistor mass-manufacturing infrastructure.
- N-channel JFETs: Inherently robust all pn-junction transistor that avoids gate oxide high-T degradation mechanisms that preclude SiC MOSFET long-term 500 °C durability. Compared to SiC BJT, SiC n-JFET is far less sensitive to p-type ohmic contact resistance. Epitaxial pn junctions minimize high-T leakage currents along with negative signal voltages that avoid forward-biasing pn-junctions.
- Layout ratio circuit design (Fig. 2): JFET and resistor conductance is governed by the same 4H-SiC n-channel, so temperature compensation of circuits is effectively built-in [2,3]. Circuit design is based upon component dimensional layout ratios instead of T-dependent current/resistance values. The circuit topology requires +V_{DD} and -V_{SS} power supplies and the signal voltages are negative with respect to GND.
- Two-level interconnect (Fig. 3): $TaSi_2$ interconnect metals are deposited via close-proximity sputtering and dry-etch patterned [3,4]. Multiple layers of TEOS-precursor SiO_2 and stoichiometric Si_3N_4 dielectric passivation deposited by LPCVD at 720 °C nominally keeps atmospheric oxygen from reacting with the underlying $TaSi_2$ [4].
- Bond pads: Specialized "IrIS" metal stack (Fig. 4) anchored directly to SiC around the chip periphery to support gold ball wire bonds [5].
- Ceramic packaging and circuit boards (Fig. 5): HTCC alumina material co-fired platinum conductive traces and gold die attach [6]. The chip packages are non-hermetic.

The processes and materials employed in IC fabrication are compatible with large-scale semiconductor mass-production based upon somewhat modified tools.

III. Extreme Environment Results

Both analog and digital circuits have been implemented. Figures 6-11 summarize NASA Glenn "Generation 10" prototype IC harsh-environment testing accomplishments.

- -190 °C to +812 °C operation: 1022 °C temperature span demonstrated for simple logic gates (Fig. 6) and ring oscillators without adjustments to input voltages [7]. 11-stage ring oscillator achieved +961 °C operation (Fig. 7) [8].
- 1 year of 500 °C operation: ICs approaching 200 transistors/chip were electrically for operated over 1 year in 500 °C air-ambient ovens with negligible change in circuit characteristics (Figs. 8,9) [3].

- Radiation: Gen. 10 JFET-R ICs successfully withstood 7 MRad(Si) total ionizing dose (Fig. 10) and single-event heavy ion strike testing through 86 MeV-cm^2/mg at 25 °C under electrical bias [9].
- Venus environment: 60 days Gen. 10 JFET-R IC operation in test chamber unprotected from 9.3 MPa 460 °C chemically caustic Venus surface environment (Fig. 11) [10].

It is worth noting that no Gen. 10 JFET-R ICs failed during 60-day Venus surface conditions and radiation testing, and that 500 °C oven-testing was ended prior to all ICs failing. However, the number of chips subjected to each test was less than 10. Laboratory upgrades are presently underway towards achieving greatly improved testing statistics for $T \geq 500$ °C and additionally facilitate more rapid repetitive thermal cycling. Even under limited statistics, dielectric cracking (Fig. 12) has been elucidated as the clearly dominant mechanism limiting long-term high-temperature IC durability [11].

IV. Development Update

Given that accessibility and commercialization are crucial to new technology infusion, mask layout rules and SPICE models were made publicly available during the design phase of Gen. 12 (based on 3 µm gate length, presently in fabrication) [12]. Via funded Space Act Agreements, IC layouts and circuits submitted by 3rd parties are being prototyped on the same Gen. 12 wafers as NASA-designed ICs. Design services for SiC JFET-R ICs have also become commercially available [13].

In addition to reducing/retiring dielectric cracking, it is vital to upscale chip complexity so as to make correspondingly increased capability available to harsh environments. Table 1 comparatively benchmarks major chip metrics for Gen. 10, 11, and 12 prototype ICs.

As seen in Table 1 and Fig. 13, Gen. 11 ICs implemented roughly 5-fold more complex ICs than Gen. 10. However, the Gen. 11 interconnect process, which was altered from Gen. 10 in effort to mitigate dielectric cracking as well as enable larger die size, resulted in metal peeling near the wafer periphery, degraded dielectric cracking properties, and subsequently inferior circuit yields [14]. In contrast to yearlong 500 °C durability achieved in Gen. 10, no Gen. 11 chips oven-tested to date have reached 1000 hours of 500 °C operation without malfunction. Therefore, presently on-going development of improved interconnect/dielectric is paramount to successful realization of 500 °C durable Gen. 12 prototype ICs.

Despite the interconnect/dielectric issues, important progress was nevertheless demonstrated in Gen. 11. The first LSI SiC JFET-R ICs were implemented in Gen. 11 in the form of benchmark RAM and ROM chips. In addition to improved bit density, these memory chips successfully implemented 25 °C to 500 °C, 0V to +23V shared data bus architecture with tri-state buffers. Fig. 14 shows completely functional 992-bit ROM chip test waveforms collected at 25 °C and 500 °C. All functional address/read/write aspects of the RAM circuit design were experimentally verified in oven-testing from 25 °C to 500 °C (Fig. 15). However, no Gen. 11 RAM ICs yielded completely error-free functionality for all 120 storage bits. Post-test analysis of oven-failed Gen. 11 RAM and ROM chips has been delayed by NASA response to COVID-19, but dielectric cracking is the primary suspect consistent with unbiased oven testing behavior reported in Ref. [14].

V. Conclusion

Prototype MSI SiC JFET-R chips have greatly expanded the demonstrated environmental envelope for long-term stable IC operation. Further development of this unique capability is focused on upscaling these “go anywhere” SiC ICs which should also advance both commercialization and beneficial infusion into applications.

Acknowledgment

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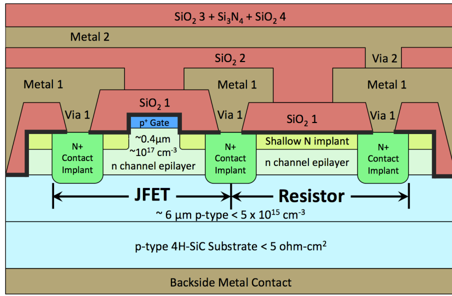
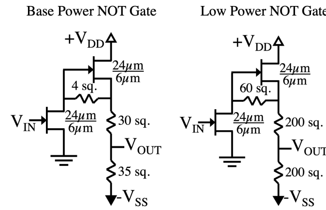


Fig. 1. Simplified cross-sectional illustrations of NASA Glenn 4H-SiC JFET-R integrated device approach with two levels of interconnect [2].



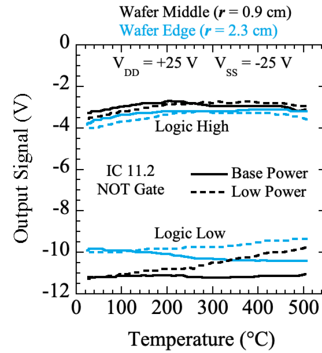


Fig. 2. SiC JFET-R logic based on shared FET/resistor n-channel and dimensional ratio design (top, schematics) enables in built-in temperature compensation (bottom, measured Gen. 11 results).

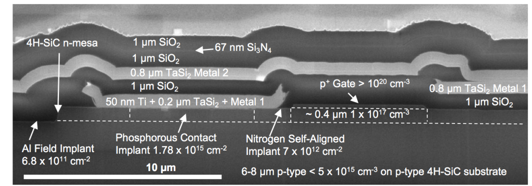


Fig. 3. Annotated scanning electron microscopic cross-section of Gen. 10 JFET source and gate region with two levels of $TaSi_2$ interconnect and TEOS SiO_2 and Si_3N_4 dielectric/passivation [3].

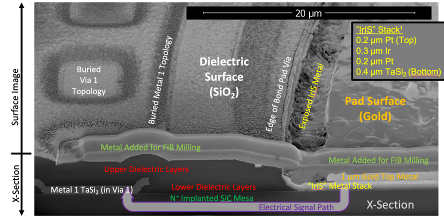


Fig. 4. Annotated scanning electron microscope cross-section of edge of Gen. 10 bond pad featuring "IrIS" metal stack [5] anchored directly on conductive SiC.

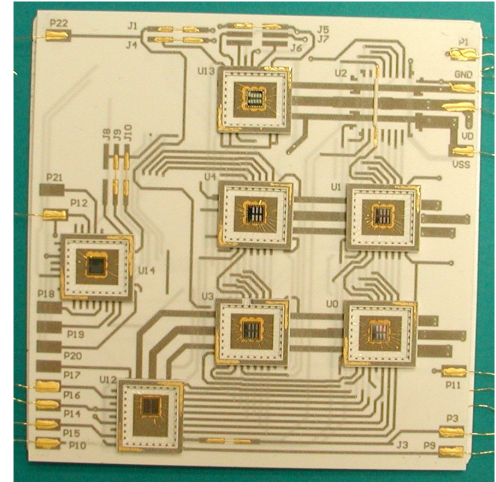


Fig. 5. Photo of 11 cm x 11 cm prototype ceramic circuit board with packaged Gen. 11 SiC JFET-R chips (prior to attaching lids) in preparation for upcoming 460 °C Venus chamber testing.

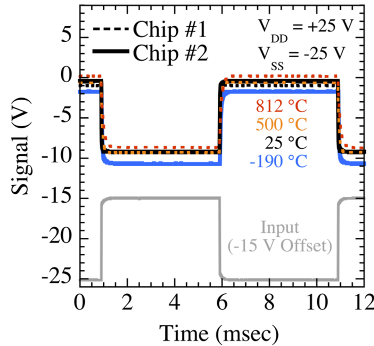


Fig. 6. Waveforms demonstrating Gen. 10 NOT gate operation from -190 °C to +812 °C without any changes to input voltages [7].

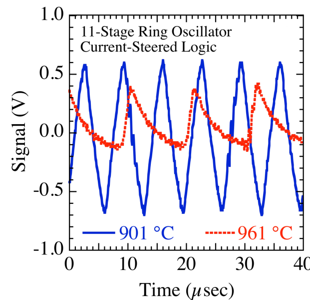


Fig. 7. Waveforms from 901 °C and 961 °C operation of an 11-stage Gen. 10 SiC JFET-R ring oscillator IC [8].

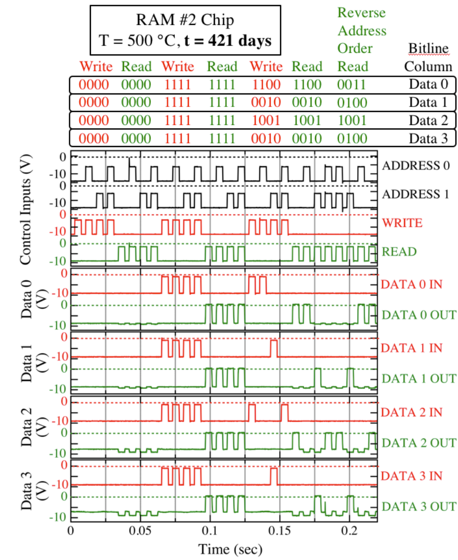


Fig. 8. Waveforms demonstrating 195-JFET Gen. 10 RAM chip remains fully functional on day 421 of 500 °C electrical testing in air-ambient oven [3].

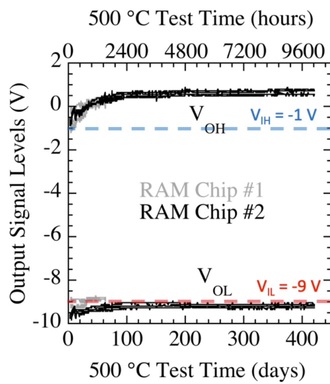


Fig. 9. Gen. 10 RAM chip output voltage levels logged during 421 days of 500 °C electrical testing in air-ambient oven. [3]

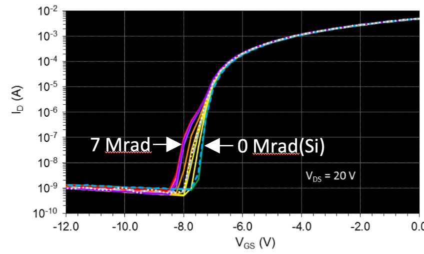


Fig. 10. Typical Gen. 10 JFET drain current vs. gate voltage turn-off characteristics measured after 0 Mrad(Si) through 7 Mrad(Si) total ionizing dose radiation exposures at 25 °C. Degradation was confined in the sub-threshold region and no failures were observed [9].

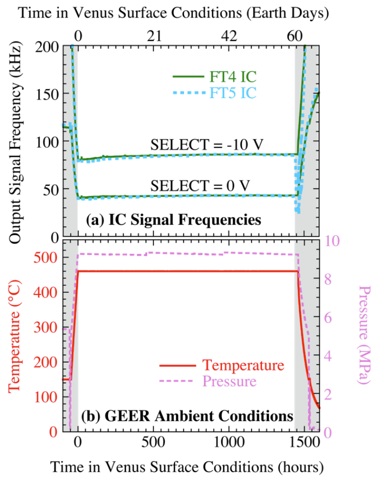


Fig. 11. Gen. 10 ÷2/÷4 clock IC (a) signal frequencies plotted with corresponding (b) T and P of the GEER Venus environment chamber. Chips operated for 60 days in the 9.3 MPa 460 °C reactive Venus surface gas chemistry without cooling [10].

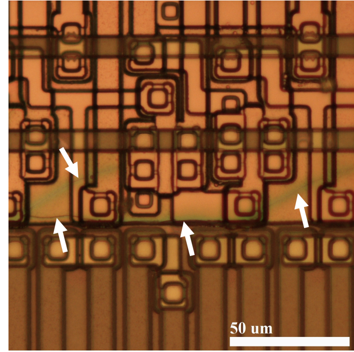
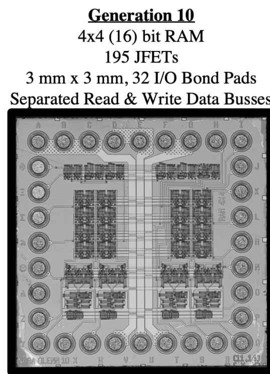


Fig. 12. White arrows denote examples of dielectric cracks and metal discoloration (oxidation) observed following a Gen. 10 ÷2/÷4 clock IC failure experienced during prolonged 500 °C air-ambient oven testing [3].

	Generation 10	Generation 11	Generation 12
Gate Length	6 µm	6 µm	3 µm
Resistor Width	6 µm	3 µm	2 µm
Contact Via	6 µm	6 µm	3 µm
JFET Count	~ 200 /chip	~ 1000/chip	~ 3000/chip
Die Size	3 mm x 3 mm	4.65 mm x 4.65 mm	5 mm x 5 mm
Bond Pads	32	32	56, 62, 72

Table 1. Major design metrics for recent generations of prototype NASA Glenn SiC JFET-R IC chips. Note that Gen. 12 is presently in fabrication, but has been delayed by NASA response to COVID-19.



Generation 11
15x8 (120) bit RAM
~ 1000 JFETs
4.65 mm x 4.65 mm, 32 I/O Bond Pads
Shared (Tri-State) Read & Write Data Bus

Generation 12
31x8 (248) bit RAM
~ 2000 JFETs
5 mm x 5 mm, 62 I/O Bond Pads
Shared (Tri-State) Read & Write Data Bus

Fig. 13. Comparison of Gen. 10, 11, and 12 prototype SiC JFET-R RAM chip designs.

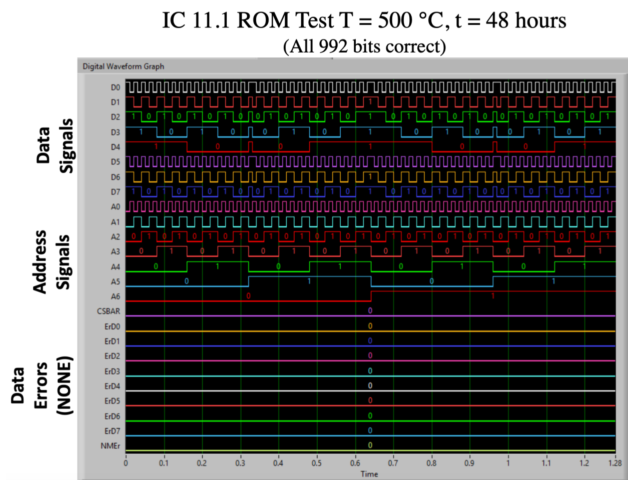


Fig. 14. Gen. 11 ROM chip 500 °C test waveforms demonstrating functionality of the entire 992-bit mask-programmed data pattern without any errors. Just after 200 hours testing at 500 °C, systematic data pattern errors were observed. While dielctric cracking failure is suspected, failure analysis of this chip has been delayed by COVID-19.

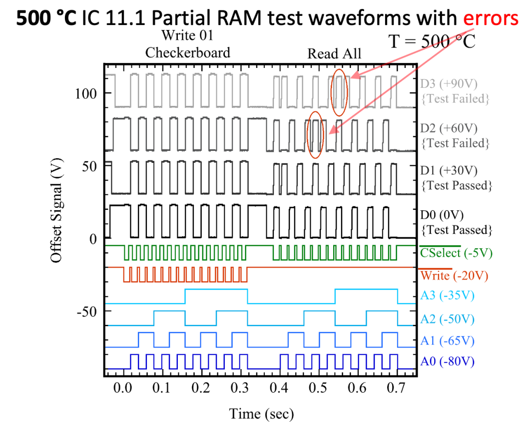


Fig. 15. Measured 500 °C waveforms (right) detail part of a "checkerboard" test pattern that verifies Gen. 11 RAM chip read and write operations using the shared data bus. Except for the two read errors denoted, the 4 (of 8 possible) data columns plotted show desired RAM functionality.