NASA Goddard Space Flight Center's Compendium of Radiation Effects Test Results

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Abstract-- Total ionizing dose, displacement damage dose, and single event effects testing were performed to characterize and determine the suitability of candidate electronics for NASA space utilization. Devices tested include FETs, flash memory, FPGAs, optoelectronics, digital, analog, and bipolar devices.

I. INTRODUCTION

NASA spacecraft are subjected to a harsh space environment that includes exposure to various types of radiation. The performance of electronic devices in a space radiation environment is often limited by its susceptibility to single event effects (SEE), total ionizing dose (TID), and displacement damage dose (DDD). Ground-based testing is used to evaluate candidate spacecraft electronics to determine risk to spaceflight applications. Interpreting the result of radiation testing of complex devices is quite difficult. Given the rapidly changing nature of technology, radiation test data are most often application-specific and adequate understanding of the test conditions is critical [1].

These test results show sensitivities of candidate spacecraft and electronic devices to SEE including single-event upset (SEU), single-event functional interrupt (SEFI), single-event latchup (SEL), single-event burnout (SEB), single-event gate rupture (SEGR), single-event transient (SET), TID, and DDD effects. All tests were performed between February 2019 and February 2020.

II. TEST TECHNIQUES AND SETUP

A. Test Method

TID testing was performed using MIL-STD-883, Test Method 1019.9 [7] unless otherwise noted as research. All tests were performed at room temperature and with nominal power supply voltages, unless otherwise noted. Based on the application, samples would be tested in a biased and/or unbiased configuration. Functionality and parametric changes were measured after step irradiations (for example: every 10 krad(Si)).

Proton damage tests were performed on biased or unbiased devices. Functionality and parametric changes were measured either continually during irradiation (in-situ) or after step irradiations (for example: every 10 krad(Si), or every $1\text{x}10^{10}$ protons/cm^2).

Unless otherwise noted, SEE testing was performed in accordance with JESD57A test procedures [8]. Depending on the DUT and the test objectives, one or two SEE test methods were typically used:

a) *Dynamic* – The DUT was exercised and monitored continuously while being irradiated. The type of input stimulus and output data capture methods are highly device- and application-dependent. In all cases the power supply levels were actively monitored during irradiation. These results are highly application-dependent and may only represent the specific operational mode tested.

b) *Static/Biased* – The DUT was provided basic power and configuration information (where applicable), but not actively operated during irradiation. The device output may or may not have been actively monitored during irradiation, while the power supply current was actively monitored for changes.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs, and for hard errors, such as SEGR. Detailed descriptions of the types of errors observed are noted in the individual test reports.

SET testing was performed using high-speed oscilloscopes controlled via NI LabVIEW® [9]. Individual criteria for SETs are specific to the device and application being tested. Please see the individual test reports for details.

Heavy ion SEE sensitivity experiments include measurement of the linear energy transfer threshold (LET$_{th}$) and cross section at the maximum measured LET. The LET$_{th}$ is defined as the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/cm^2. In the case where events are observed at the smallest LET tested, LET$_{th}$ will either be reported as less than the lowest measured LET or determined approximately as the LET$_{th}$ parameter from a Weibull fit. In the case of SEGR and SEB experiments, measurements are made of the SEGR or SEB threshold V_{DS} (drain-to-source voltage) as a function of LET and ion energy at a fixed V_{GS} (gate-to-source voltage).

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Proton SEE tests were performed in a manner similar to heavy ion exposures; however, because protons usually cause SEE via indirect ionization of recoil particles, results are parameterized in terms of proton energy rather than LET. Because such proton-induced nuclear interactions are rare, proton tests also feature higher cumulative fluences and particle flux rates than heavy-ion experiments.

For pulsed laser SEE testing, DUTs are mounted on an X-Y-Z stage that can move in steps of 0.1 microns for accurate determination of the volumes sensitive to single-event effects. The light is incident from the front side and is focused using a 100x lens that produces a spot diameter of approximately 1 μm at full-width half-maximum (FWHM). An illuminator, together with an infrared camera and monitor, were used to image the area of interest thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

B. Test Facilities – TID

TID testing was performed using a gamma source. Dose rates used for testing were between 10 mrad(Si)/s and 2.6 krad(Si)/s.

C. Test Facilities – DDD

Proton DDD tests were performed at the University of California at Davis Crocker Nuclear Laboratory (UCD - CNL) [5] using a 76” cyclotron and energy of 63 MeV.

Neutron DDD tests were performed at Ohio State University Nuclear Reactor Laboratory [4] using the following energies: 500, 5k, 10k and 20k watts. In-situ measurements were taken.

D. Test Facilities – Laser

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) using single-photon absorption.

E. Test Facilities – SEE

Proton SEE tests were performed at Massachusetts General Francis H. Burr Proton Therapy (MGH) [3]. Low energy proton and electron (500 keV to 1.5 MeV) SEE tests were performed at Goddard Space Flight Center.

Heavy ion experiments were conducted at Lawrence Berkeley National Laboratory (LBNL) 88-inch cyclotron [8], and at the Texas A&M University Cyclotron (TAMU) [9]. Energies and LETs available varied slightly from one test date to another.

III. TEST RESULTS OVERVIEW

Abbreviations for principal investigators (PIs) are listed in Table I. Abbreviations and conventions are listed in Table II. Summary of TID, DDD, and SEE test results from February 2019 through February 2020 are listed in Table III. Please note that these test results can depend on operational conditions.

TABLE I
LIST OF PRINCIPAL INVESTIGATORS

Principal Investigator (PI)	Abbreviation
Melanie D. Berg	MB
Michael J. Campola	MJC
Megan C. Casey	MCC
Jean-Marie Lauenstein	JML
Kaitlyn Ryder	KR
Edward (Ted) Wilcox	TW
Edward J. Wyrwas	EW

TABLE II
ACRONYMS

Acronym	Definition
σ	cross section (cm^2/device, unless specified as cm^2/bit)
A	Amperes
ADC	Analog to Digital Converter
BiCMOS	Bipolar – Complementary Metal Oxide Semiconductor
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Semiconductor
CNL	Crocker Nuclear Laboratory
CTR	Current Transfer Ratio
DDD	Displacement Damage Dose
DUT	Device Under Test
EDAC	Error Detection and Correction
FPGA	Field Programmable Gate Array
FRAM	Ferroelectric Random-Access Memory
FWHM	Full-Width Half-Maximum
HEMT	High Electron Mobility Transistor
GSFC	Goddard Space Flight Center
HDR	High Dose Rate
IC	Integrated Circuit
I_{DSS}	Zero Gate Voltage Drain Current
I_{GSS}	Gate-Source Leakage Current
JFET	Junction Field Effect Transistor
LBNL	Lawrence Berkeley National Laboratory
LDC	Lot Date Code
LDO	Low Dropout Regulator
LDR	Low Dose Rate
LET	Linear Energy Transfer
MCU	Microcontroller Unit
MEMS	Microelectro-mechanical Systems
MGH	Massachusetts General Francis H. Burr Proton Therapy
MGH	Massachusetts General Francis H. Burr Proton Therapy
MLC	Multi-Level Cell
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NEPP	NASA Electronics Parts and Packaging
PI	Principal Investigator
REAG	Radiation Effects & Analysis Group
$R_{DS\ ON}$	Drain-Source On-state Resistance
R/W	Read-Write
SEB	Single-Event Burnout
SECDED	Single Error Correct Double Error Detect
SEE	Single-Event Effect
SEFI	Single-Event Functional Interrupt
SEGR	Single-Event Gate Rupture
SEL	Single-Event Latchup
SEU	Single-Event Upset
SLC	Single-Level Cell
SRAM	Static Random-Access Memory
SMD	Standard Microcircuit Drawings
STMD	Space Technology Mission Directorate
TAMU	Texas A&M University
TID	Total Ionizing Dose
UCD	University of California at Davis
VDMOS	Vertical Double-diffused Metal Oxide Semiconductor
$V_{GS\ OFF}$	Gate Source Cutoff Voltage
V_{DS}	Drain-Source Voltage
WSR	Windowed Shift Register

TABLE III

SUMMARY OF RADIATION TEST RESULTS

Part Number	Manufacturer	LDC; (REAG ID#)	Device Function	Technology	PI	Sample Size	Test Env.	Test Facility (Test Date)	Test Results (Effect, Dose Level/Energy, Results)
FETs									
U309	InterFET Corp.	1526; (19-009)	JFET	Bipolar	MCC	5	Heavy Ions	LBNL (Apr 2019)	No SEEs were observed up to an LET of 58.8 MeV-cm^2/mg at V_{DS} = 20 V, V_{GS} = -2.1 V and -15 V.
						14	Gamma	GSFC (Aug 2019)	TID, HDR, I_{GSS}, $V_{GS\ OFF}$, and I_{DSS} stayed within specifications to 50 krad(Si). [10]
EPC2019	EPC	6C19/C701; (19-017)	JFET	eGaN	JML	Set 1: 4 Set 2: 4	Neutrons	OSU (Apr 2019)	DDD and TID. ID_{SS}, I_{GSS}, and Gate V_{TH} stayed within specifications up to 4.3 x 10^{14} cm^{-2} (1 MeV eq) + 1.2 Mrad(Si) (Set 1) and 1.9x10^{14} cm^{-2} (1 MeV eq) + 0.535 Mrad(Si) (Set 2). R_{DS_ON} increase < 10 mΩ
SGF15E100	SSDI	n/a; (19-034)	FET	GaN FET	JML	10	Heavy Ions	TAMU (Jul 2019)	SEB. Last pass/first fail V_{DS} (at 0 V_{GS}): 300 V/350 V with Ag, LET(Si)= 42 MeV-cm^2/mg; fail 400 V with Cu, LET(Si)= 12 MeV-cm^2/mg; 600 V/650 V with Ar, LET(Si)= 13 MeV-cm^2/mg.
MEMORY									
MT29F4T08CTHBBM5	Micron	201816; (19-020)	3D NAND Flash	CMOS	TW	13	Gamma	GSFC (Apr 2019)	TID, HDR, Erase circuitry failed at 39 krad(Si). MLC mode showed a faster increase in error rate. [11]
22FDX SRAM-based Line-Monitor Test Vehicle	GlobalFoundries	n/a; (18-007)	22 nm SRAM	CMOS	MCC	3	Gamma	GSFC (Aug 2019)	Investigated effect of well bias during irradiation. One DUT was irradiated to 300 krad(Si), while the other two were irradiated to 500 krad(Si). DUTs remained functional, but over half of the bits were stuck.
						3	Heavy Ions	LBNL (Aug 2019)	Combined SEE and TID. Statistics were hard to obtain for SEE due to so many stuck bits after TID testing. There was a strong pattern dependence however, that did not previously exist. That indicates the PMOS were exhibiting greater degradation than the NMOS.
AS216MA1G2B-ASC	Avalanche	4518; (19-028)	40 nm MRAM	CMOS	TW	1	Heavy Ions	LBNL (May 2019)	SEL observed with 21.1 < LET_{th} < 58.8 cm^2/mg.
						1	Laser	NRL (Jun 2019)	SEL observed; laser energy ~ 40 pJ.
ASV016204	Avalanche	1819; (20-006)	40 nm MRAM	CMOS	TW	1	Laser	NRL (Jan 2020)	No SEEs observed at 80°C with a laser energy 21.6 pJ.
						6	Gamma	GSFC (Feb 2020)	No degradation at 1 Mrad(Si). [12]
MT29F1T08CMHBBJ4	Micron	n/a; (17-049)	3D NAND Flash	CMOS	TW	1	Heavy Ions	LBNL (Nov 2019)	SEFIs observed, SEL LET_{th} > 85 MeV-cm^2/mg at 78°C. [13]

Part Number	**Manufacturer**	**LDC; (REAG ID#)**	**Device Function**	**Technology**	**PI**	**Sample Size**	**Test Env.**	**Test Facility (Test Date)**	**Test Results (Effect, Dose Level/Energy, Results)**
MEMORY (Cont.)									
H25QFT8F4A9R-BDF	Hynix	936A; (19-043)	3D NAND Flash	CMOS	TW	2	Heavy Ions	LBNL (Nov 2019)	SEU $LET_{th} < 1.16$ MeV-cm^2/mg in SLC mode SEU $LET_{th} < 3.08$ MeV-cm^2/mg in TLC mode SEFI $1.54 < LET_{th} < 7.27$ MeV-cm^2/mg Two parts showed destructive SEE at LET = 58.8 MeV-cm^2/mg at 80°C
						1	Protons	GSFC (Jan 2020)	SEU observed; proton energies 500 keV – 1.2 MeV; $\sigma_{SAT} < 1\text{x}10^{-12}$cm^2/byte [14]
FPGAs\COMPLEX LOGIC									
RH-OBC-1	Vorago	n/a; (18-035)	Single Board Computer	CMOS	TW	1	Protons	MGH (Jun 2019)	200 MeV: SRAM SBU $\sigma = 3\text{x}10^{-8}$cm^2/device, ROM SBU $\sigma = 1.3\text{x}10^{-7}$cm^2/device, SRAM MBU $\sigma < 1\text{x}10^{-12}$cm^2/device (none observed); SEFI observed at 200 MeV with boot FRAM and user FRAM components (no σ available) [15]
Ryzen 7 1700 Summit Ridge (YD1700BBM88AE)	AMD	n/a; (17-038)	Processor	CMOS	EW	1	Protons	MGH (Jun 2019)	SEFIs and SEUs, 200 MeV, No failures up to 1.55 x 10^{11} p/cm^2, power cycle mitigated all SEE events. [16]
Ryzen 3 1200 Summit Ridge (YD1200BBAEBOX)	AMD	n/a; (19-023)	Processor	CMOS	EW	1	Protons	MGH (Jun 2019)	SEFIs and SEUs, 200 MeV, No failures up to 8.92 x 10^{10} p/cm^2, power cycle mitigated all SEE events. [17]
Ryzen 3 2200G Raven Ridge (YD2200C5FBBOX)	AMD	n/a; (19-024)	Processor	CMOS	EW	1	Protons	MGH (Jun 2019)	SEFIs and SEUs, 200 MeV, No failures up to 4.66 x 10^{10} p/cm^2, power cycle mitigated all SEE events. [18]
Radeon e9173 (Polaris)	AMD	n/a; (19-022)	GPU	CMOS	EW	1	Protons	MGH (Jun 2019)	SEFIs and SEUs, 200 MeV, Functional after 6.24 x 10^9 p/cm^2, non-destructive SEL observed during final run at 6.24 x 10^9 p/cm^2, power cycle mitigated all SEE events. [19]
Jetson TX2	nVidia	n/a; (19-021)	Single Board Computer	CMOS	EW	2	Protons	MGH (Jun 2019)	SEFIs and SEUs, 200 MeV, one device saw no failures up to 1.89 x 10^9 p/cm^2, second device failed at 1.61 x 10^9 p/cm^2, power cycle mitigated all non-destructive events. [20]
XCKU040-2FFVA1156E (UltraScale)	Xilinx	1509; (15-061)	FPGA	CMOS	MB	1	Heavy Ions	LBNL (Nov 2019)	Configuration, BRAM, and dynamic Fluence-to-Failure (FTF) testing were performed. $LET_{th} < 7.0 \times 10^{-2}$ MeV·cm^2/mg. SEU-cross-sections are design dependent. Configuration device threshold SEU cross-section (σ_{SEU} at LET_{th}) ≈ 1.0 × 10-6 (cm^2/device). Configuration scrubbing was not performed. [21]
MPF300T-FCG1152 (PolarFire)	Microsemi	1838; (19-045)	FPGA	CMOS	MB	1	Heavy Ions	LBNL (Nov 2019)	SEFI observed at 1.16 MeV·cm^2/mg and higher: core-current drops below 100 mA (lasting 1.7 ms) requiring a system reset. SEFI is being investigated because it could be due to a mode setting in the FPGA. SEU $LET_{th} < 1.16$ MeV·cm^2/mg with $\sigma_{SEU} \approx 3.0 \times 10^{-7}$ cm^2/design. [22]

Part Number	Manufacturer	LDC; (REAG ID#)	Device Function	Technology	PI	Sample Size	Test Env.	Test Facility (Test Date)	Test Results (Effect, Dose Level/Energy, Results)
HYBRIDS									
OLS500SB	Skyworks	1727; (18-028)	Optocoupler	Hybrid	MCC	10	Protons	UC Davis (Apr 2019)	DDD, 64 MeV, All parameters measured remained within specification up to a fluence of 2 x 10^{11} p+/cm^2.
HCPL-673K	Broadcom	1816; (19-002)	Optocoupler	Hybrid	MCC	6	Protons	UC Davis (Apr 2019)	DDD, 64 MeV, All parameters measured remained within specification up to a fluence of 2x10^{11} p+/cm^2.
PE99155	Teledyne	1247, 1706, 1729, 1805; (19-001)	DC-DC Converter	Hybrid	TW	4	Gamma	GSFC (Apr 2019)	Investigating effect of TID on start-up transients. No change in behavior observed after 25 krad (Si).
OMH3075S	Optek	n/a; (19-026)	Hall-effect Sensor	Hybrid	MJC	10	Gamma	GSFC (Aug 2019)	TID, LDR, All parameters tested remained within specification up to 40 krad(Si). [23]
LINEARS									
HSYE-117RH	Intersil	1830; (19-007)	Voltage Regulator	Bipolar	MCC	10	Gamma	GSFC (Mar 2019)	TID, LDR, Line and Load Regulation parameters increased above the maximum specification after 75 krad(Si). [24] [25]
RH1014MW	Analog Devices	1803A; (19-003)	Operational Amplifier	Bipolar	MCC	12	Gamma	GSFC (Apr 2019)	TID, LDR, The power supply currents exceeded the specification at 25 krad(Si) for the biased parts, but returned to normal at the next dose point and remained within spec for the remainder of the testing. All other parameters remained within specification up to 125 krad(Si). [26]
RH1021BMH-10	Analog Devices	1430A; (19-008)	Voltage Reference	Bipolar	MCC	22	Gamma	GSFC (Jul 2019)	TID, LDR, All parameters remained within specification to 128.6 krad(Si). [27]
MSK106	MSK	1840; (19-035)	Operational Amplifier	BiCMOS	MCC	2	Heavy Ions	LBNL (Aug 2019)	SETs; LET_{th} = 0.1 MeV-cm^2/mg, s = 5 x 10^{-3} cm^{-2}; Worst case transients with Xe were 13 Vp-p with 10 µs pulsewidth and 6 Vp-p with 35 µs pulsewidth.
RH1814	Linear Technologies	n/a; (19-036)	Operational Amplifier	BiCMOS	MCC	2	Heavy Ions	LBNL (Aug 2019)	SETs; LET_{th} = 0.1 MeV-cm^2/mg, s = 1.32 x 10^{-4} cm^{-2}; Worst case transients with Xe were 1.8 Vp-p with 10 ns pulsewidth and 0.1 Vp-p with 170 ns pulsewidth.
OP484FSZ	Analog Devices	1804; (19-038)	Operational Amplifier	Bipolar	JML	10	Neutrons	OSU (Aug 2019)	Parts were irradiated in 3 total dose groups. Input offset current and offset voltage experienced drift while the CMRR stayed within specifications as high as 1185 krad(Si) and 4.5 x 10^{14} 1-MeV n eq cm^{-2}. See report for details
AD8065	Analog Devices	1838; (19-031) 1128; (19-048)	Operational Amplifier	Bipolar	MCC	20 (10 from each LDC)	Gamma	GSFC (Jan 2020)	TID, LDR, With +/- 5 V supplies input bias current was out of specification at pre-irradiation measurements but changed little during the full dose. All other parameters remained within specification up to 30 krad(Si).

Part Number	Manufacturer	LDC; (REAG ID#)	Device Function	Technology	PI	Sample Size	Test Env.	Test Facility (Test Date)	Test Results (Effect, Dose Level/Energy, Results)
MISCELLANEOUS									
2N2222	Semicoa	1541; (19-040)	Transistor	Bipolar	MJC	5	Gamma	GSFC (Nov 2019)	TID, LDR, All parameters remained within specification to 30 krad(Si). [28]
HFB16HY20CC	Infineon	1729; (19-010), 1832; (19-033)	Diode	Bipolar	MJC	6	Heavy Ions	LBNL (Apr 2019)	All parts passed at maximum voltage of 200 V at Ag and Xe.
SNJ54LVC00AW	Texas Instruments	1432A; (19-044)	NAND Gate	CMOS	MJC	2	Heavy Ions	LBNL (Nov 2019)	No SELs observed with Xe at 0° and 45° to an LET of 87.9 MeV-cm^2/mg, temperature at 99°C, supply voltage at 3.6 V. [29]
AD7226	Analog Devices	n/a; (17-055)	A/D Converter	BiCMOS	MJC/TW	4	Heavy Ions	LBNL (Nov 2019)	No SELs observed with Ar at 60° and 85°C LET = 117.6 MeV-cm^2/mg. V$_{DD}$ 12 V. SETs observed with Xe.
						6	Gamma	GSFC (Oct 2019)	TID, HDR, 3 biased parts showed no change in output at 10 krad(Si). All 3 failed functionally between 10 krad(Si) and 20 krad(Si). 3 unbiased parts had 1 LSB of output degradation at 1 krad(Si) and 3 LSB of degradation at 20 krad(Si), but no functional failures observed.
MAX4595	Texas Instruments	n/a; (19-052)	Analog Switch	CMOS	TW	10	Gamma	GSFC (Dec 2019)	TID, HDR, No functional failures to 100 krad(Si), Off-state leakage (NC and COM pins) out of spec between 30 krad(Si) and 50 krad(Si).
MAX4651	Maxim Integrated	n/a; (19-053)	Analog Switch	CMOS	TW	12	Gamma	GSFC (Dec 2019)	TID, HDR, All parameters tested remained within specification up to 100 krad(Si).
						2	Laser	NRL (Jan 2020)	No SEL observed at 80°C with 26.8 pJ. 5.5 supply voltage.
DG409	Maxim Integrated	n/a; (19-054)	Multiplexor	CMOS	TW	15	Gamma	GSFC (Dec 2019)	TID, HDR, Degradation seen at less than 1 krad(Si). Functional failures between 1 and 2 krad(Si).
MIC4427	Microchip	4A1436; (19-030)	MOSFET Gate Driver	BiCMOS/ DMOS	MCC	8	Gamma	GSFC (Jan 2020)	TID, LDR, One DUT experienced functional failure at 20 krad(Si). Rise time (B) exceeded specification at 20 krad(Si). All other parameters remained within specification up to 30 krad(Si). [30]

IV. TEST RESULTS AND DISCUSSION

As in our past workshop compendia of GSFC test results, each device under test has a detailed test report available online at http://radhome.gsfc.nasa.gov [14] and at http://nepp.nasa.gov [15] describing in further detail the test method, conditions and monitored parameters, and test results. This section contains a summary of testing performed on a selection of featured parts.

A. SGF15E100, SSDI, GaN HEMT

Solid State Devices, Inc's 3rd generation GaN HEMT is rated up to 15 A and 1000 V, and maximum R_{DS_ON} of 190 mΩ. This commercial device combines a normally-on GaN HEMT with a low-voltage Si MOSFET to enable normally-off behavior (Fig. 1, bottom). Parts were specially procured from SSDI delidded without conformal coating. A controlled, 1-mil parylene-C coating was applied prior to testing to prevent arcing at high voltages. Heavy-ion tests were performed in-air at Texas A&M University's Cyclotron Institute using the 15 MeV/u tune. The test board consisted of socketed daughter cards plugged into a mother test board that enabled communication with individual devices. The MIL-STD750 TM1080 test circuit was used; to reduce parasitic inductance and capacitance, the stiffening capacitor and gate filter were placed at the daughter card socket leads (Fig. 1, top).

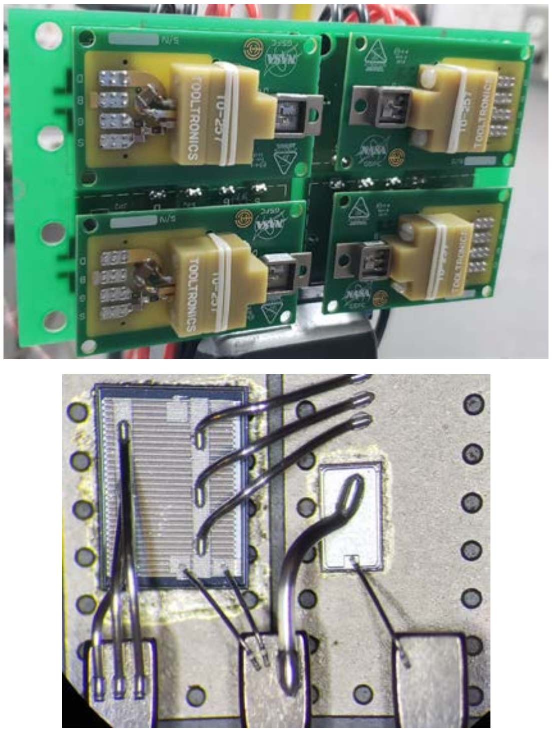

Fig. 1. (Top): Four (4) SGF15E100 devices mounted for heavy ion testing at TAMU. (Bottom): A photograph of a delidded, parylene-C coated device showing GaN HEMT on left and Si MOSFET on right.

Ten devices were tested at 0 V_{GS} and found to be susceptible to both heavy-ion induced degradation of drain-source leakage current and catastrophic SEB. At normal incidence, the last pass/first fail V_{DS} for SEB was 300 V/350 V with Ag at surface-incident LET(Si) of 42 MeV-cm^2/mg. Fig. 2 plots the VDS at which no SEB occurred and at which samples catastrophically failed, as a function of LET(Si). Additional tests with Cu (20 MeV-cm^2/mg in Si) were performed at 45° tilt and either 0° or 90° rotation (perpendicular or parallel to the HEMT electron 2-dimensional channel). Samples did not catastrophically fail at 500 V_{DS} with the ion beam aligned perpendicular to the channel, but failed (SEB) at 500 V_{DS} when aligned parallel to the channel; at normal incidence, samples also burned out at 500 V_{DS}. Finally, Fig. 2 (right side) shows the drain current degradation and SEB as a function of elapsed time during irradiation at normal incidence with Cu ions at 400 V_{DS}. Current was limited to 21 mA by the source-measure unit.

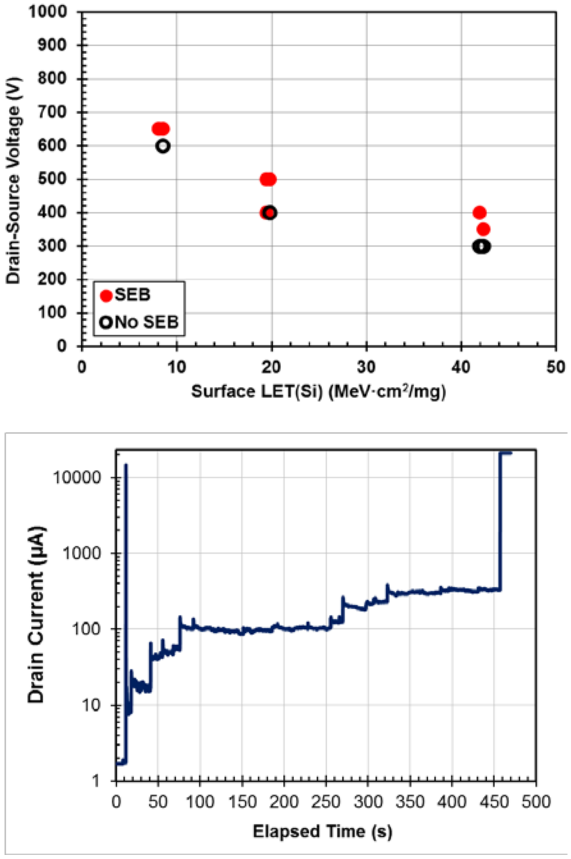

Fig. 2. (Top): SGF15E100 drain-source voltage at which SEB did not occur (open symbols) and at which SEB occurred (solid symbols) with normal-incidence ions, as a function of surface LET(Si). Overlapping symbols' LETs are offset slightly for visibility. (Bottom): Degradation of drain-source current and eventual SEB during irradiation with Cu (LET(Si) = 20 MeV-cm2/mg) at 400 V_{DS} and average flux = 628 cm^{-2}s^{-1} (supply current limit = 21 mA).

B. RH-OBC-1, Vorago, Single Board Computer

The Vorago Technologies RH-OBC-1 is a CubeSat Kit Bus compatible single board computer with a Vorago VA10820 ARM Cortex-M0 microcontroller at its core. The board also includes a set of common peripherals, like voltage regulators, non-volatile memories, an analog-to-digital converter, a watchdog, and a CAN bus controller. Fig. 3 shows a picture of the RH-OBC-1 board with each component labeled.

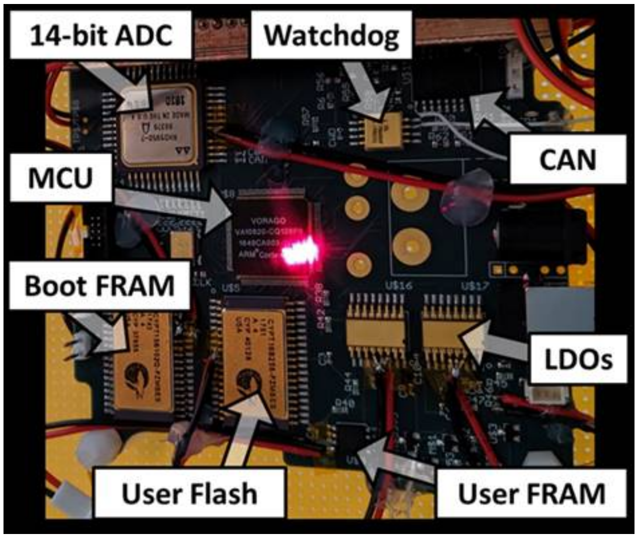

Fig. 3. RH-OBC-1 components.

High-energy proton (200 MeV) testing was conducted at the Massachusetts General Hospital’s Francis Burr Proton Therapy Center at both board and component levels to investigate single-event effects. Several of the individual components also have piece-part radiation data available from various sources, and one of the primary objectives of this test was to evaluate the performance of the board overall and identify any issues that arise from board-level testing. Limited total ionizing dose data was also obtained as a byproduct of this proton test.

Four of the on-board components were individually irradiated by using a 2.8 cm collimator on the beam line. These tests exposed the processor (MCU), CAN transceiver, user FRAM, and boot FRAM individually while monitoring the overall system response. The remaining components were only tested at board-level and showed no errors. For some runs, the voltages generated by the on-board voltage regulators were adjusted to explore their effect on system response to SEE.

The RH-OBC-1 board did not suffer any destructive effects under 200 MeV proton exposure. The entire board was subject to at least $3x10^{11}$ protons/cm^2 from the board-level irradiations alone, which also contributed approximately 12.2 krad(Si) of total dose without noticeable degradation. Single-bit errors were detected in the MCU core as expected, but were automatically handled by the device’s EDAC system. No multi-bit errors were detected. One unknown reset was created inside the MCU core, and is believed to be the only MCU fault during this test. It appears to be an internal fault and did not cause a Power-On Reset (POR) to be commanded by the ISL706 watchdog/supervisor IC.

The peripherals on board had mixed results. The rad-hard Cobham ADC performed flawlessly as expected, as did rad-hard regulators and supervisor/watchdog device. The commercial CAN transceiver functioned without error. However, the two Cypress FRAM memories were both susceptible to functional interrupts (SEFI), and the board as tested lacked any means to gate power to these devices to automatically recover. Most critically, without means to cycle power to the Boot FRAM, any subsequent condition causing a commanded or uncommanded MCU reset could leave the MCU unable to reload its own boot code until an external board-level power cycle is commanded. It is possible that such a combination of faults and its consequence (requiring external intervention) would not have been detected by piece-part testing alone. Vorago now provides a mitigation strategy which includes in part powering down the Boot FRAM when not in use to avoid an unknown SEFI state at system boot [18].

C. MPF300T-FCG1152 PolarFire®, Microsemi, FPGA

The PolarFire® FPGA is fabricated with 28 nm technology. Its configuration is built using SONOS flash memory. MPF300-EVAL-KIT PolarFire® Evaluation boards were provided by Microsemi for NEPP SEE testing. The first-look DUT was thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system. The part was successfully thinned to 100 um–120um.

NEPP created a new test system motherboard using the Xilinx KCU105 Evaluation board for this test. The central component of the motherboard is the Kintex-UltraScale (XCKU040-2FFVA1156E) FPGA. The motherboard also includes two FPGA Mezzanine Card (FMC) high-speed connectors. It was the primary interface between the motherboard and the target DUT-daughterboard. Because the motherboard FPGA is reprogrammable, it is possible to customize control/monitors (test system designs) and download them to the motherboard FPGA per experiment type. This enables specialized control and monitoring of hundreds of DUT I/O at speeds of MHz-GHz. Subsequently, the NEPP test harness is significantly more powerful than a processor or microcontroller. The motherboard contains mapped designs that are responsible for controlling and monitoring DUT activity, receiving commands from a host computer, processing data, and packetizing/reporting DUT behavior to a host computer and logic analyzer. The test designs (firmware) were mapped into the daughter board DUT for SEE evaluation.

Heavy-ion testing was performed at Lawrence Berkeley National Laboratories 88inch Cyclotron (LBNL). The vacuum chamber setup is shown in Fig.4. Because this test campaign was a first-look at the PolarFire FPGA device, only basic mechanisms were investigated. Accordingly, DUT test structures were shift-registers, counters, and embedded RAM (LSRAM). Due to repercussions from the wild fires, beam time was limited. Consequently, only

N, O, and Ne (at 16 MeV) were able to be used for the first-look experiments.

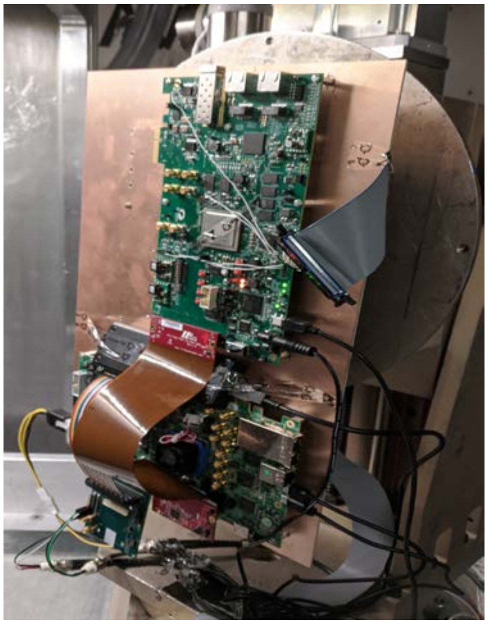

Fig. 4. Motherboard (KCU105) and daughterboard (PolarFire®) connection at the Lawrence Berkeley National Laboratory (LBNL) SEE vacuum chamber.

One significant anomaly (SEFI) was observed during heavy-ion testing. The core-current dropped below 100 mA when normal operational current was marked at approximately 2.75 A. This event was always recoverable. The current drop lasted for approximately 1.7 ms except for one instance, when it lasted for 177 s. All SEFI current drops were significant enough to stop operation and require a reset. No configuration was lost. The current drop occurred for every test at every LET during this first-look study. Microsemi is aware of the anomaly and suggests that it is due to a mode setting in the PolarFire device. This will be investigated and tested in the next PolarFire campaign.

Fig. 5 and Fig. 6 show the SEU cross-sections per DFF bit and per burst accordingly. Regarding Fig. 5, DFF upsets were single bit SEUs that were flushed out by the following shift register cycle DFF write; i.e., no SEUs lasted for more than one clock cycle and no data-paths were broken unless a SEFI (current-drop) occurred. Fig. 6 illustrates SEFI cross-sections for the LET tested. The SEFIs were not design-dependent. SEFI LET threshold has not been found and is expected to be investigated in an upcoming test campaign (including the impact of FPGA internal mode settings).

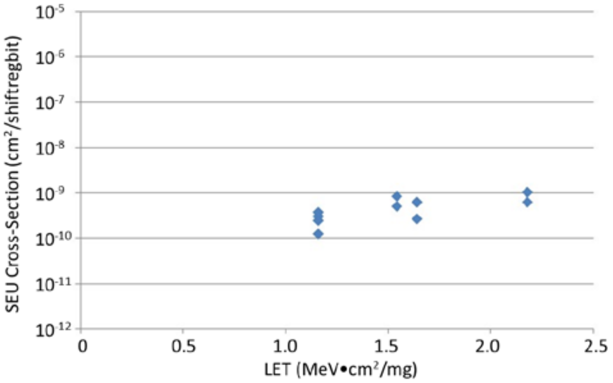

Fig. 5. Shift Register SEU Cross Sections Normalized per Shift Register Bit versus LET.

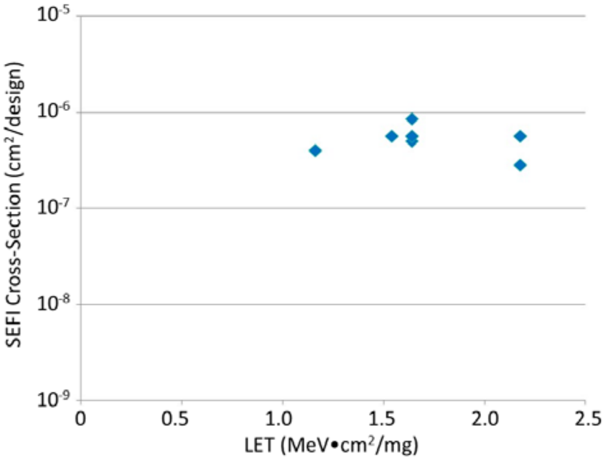

Fig. 6. Burst SEU Cross-Sections per Shift Register versus LET.

It is interesting to note that the counter array SEU cross sections per DFF are statistically equal to the WSR SEU cross-sections (both operating at the same frequency). This should be noted because the WSR does not have any combinatorial logic. This suggests that the DFF nodes will be the dominant mechanisms of failures. Additional testing is required.

All LSRAM SEUs were single bit with exception to SEFIs. This suggests that they will be correctable when implementing error correction (SECDED). SEFIs were due to the current drops; and have been verified by duration of SEFI responses during beam exposure. In all SEFI cases, LSRAM cells could be restored by an overwrite. However, SECDED would not be able to be applied (SEFIs are not single bit errors).

V. SUMMARY

We have presented data from recent TID, DDD, and SEE tests on a variety of primarily commercial devices. It is the authors' recommendation that this data be used with caution due to many application- or lot-specific test conditions. We also highly recommend that lot-specific testing be performed on any commercial devices, or any devices that are suspected to be sensitive. As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online describing in further detail, test method, test conditions/parameters, test results, and graphs of data [31][32].

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