



An Overview of Printed Circuit Board Risks and Supplier Capability

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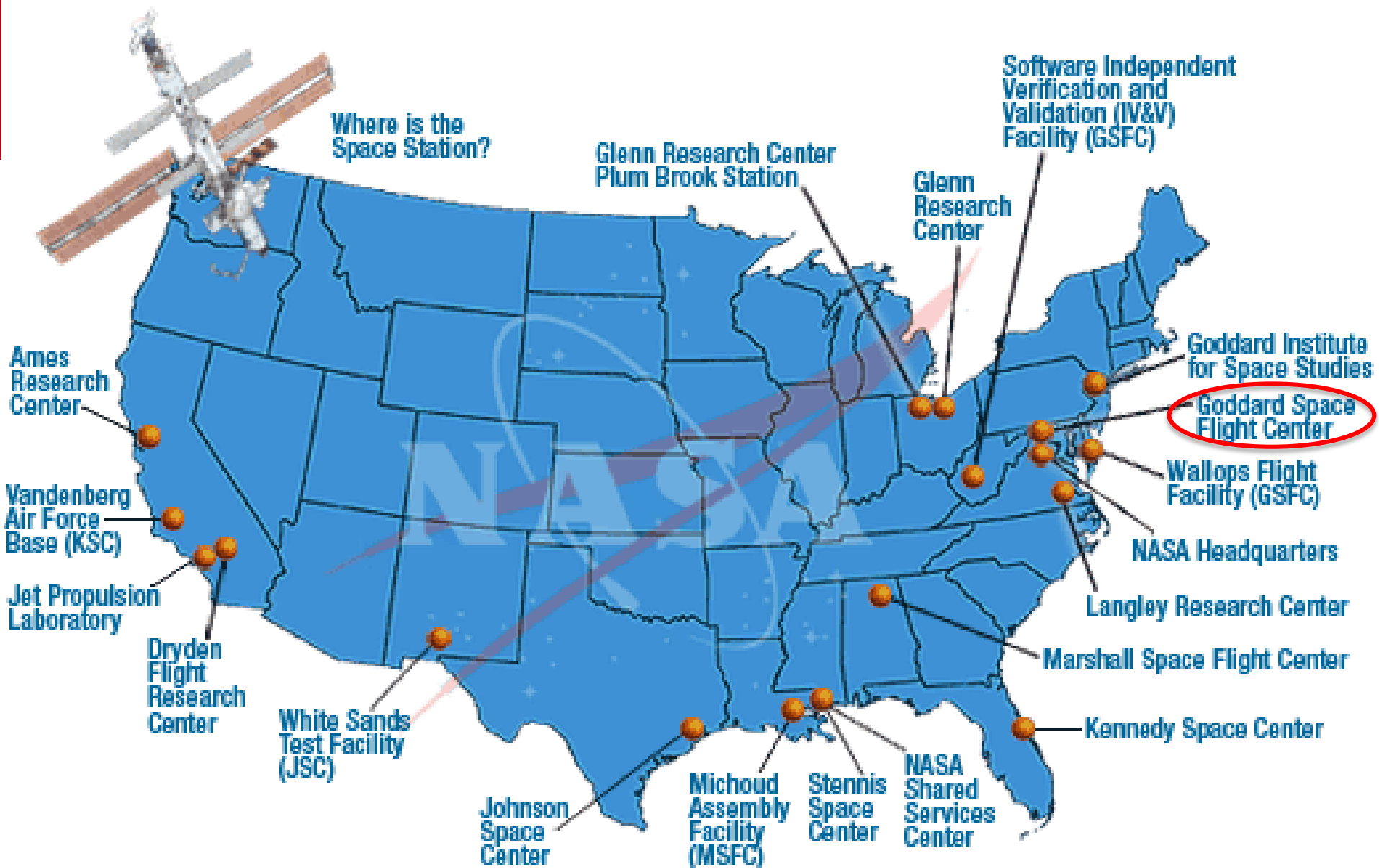
NASA Goddard Space Flight Center

Aerospace Webinar

Organizer: HDP User Group International Inc.

Outline

- **Introduction**
- **Printed Circuit Board Technology**
- **PCB Quality Assurance**
- **Supplier Capability Study**
- **Risk based Safety and Mission Assurance**
- **Closure**



One World-Class Organization

What makes Goddard one-of-a-kind?



GSFC: A Diverse Mission Portfolio

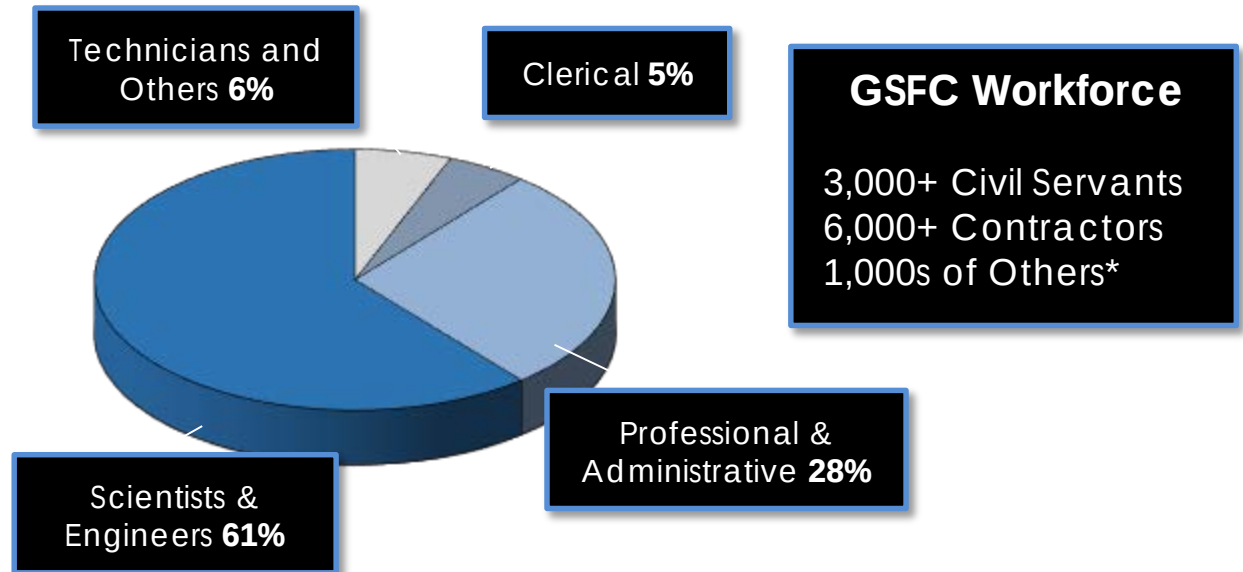


Who We Are



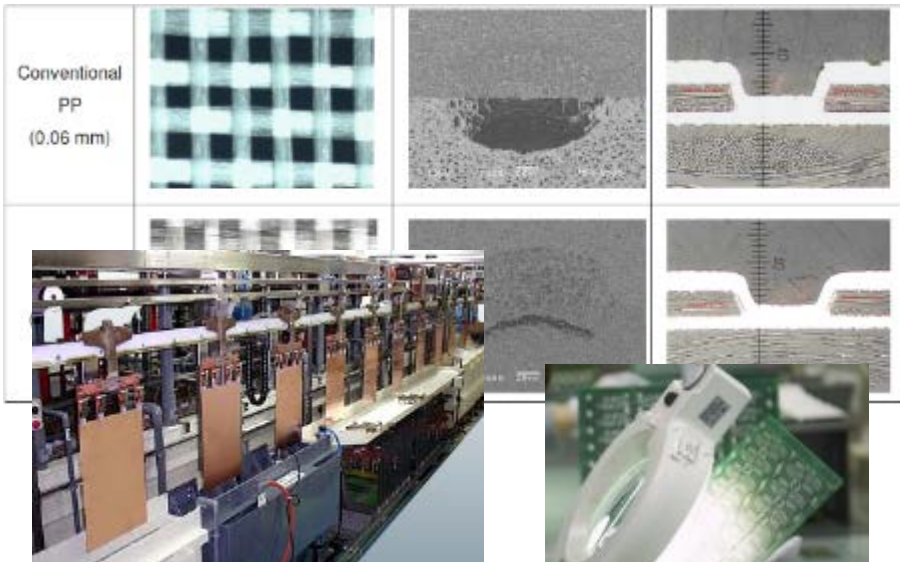
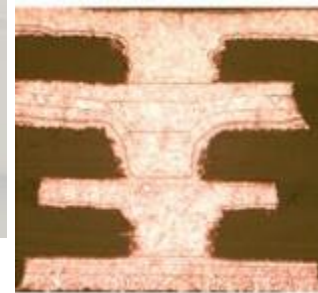
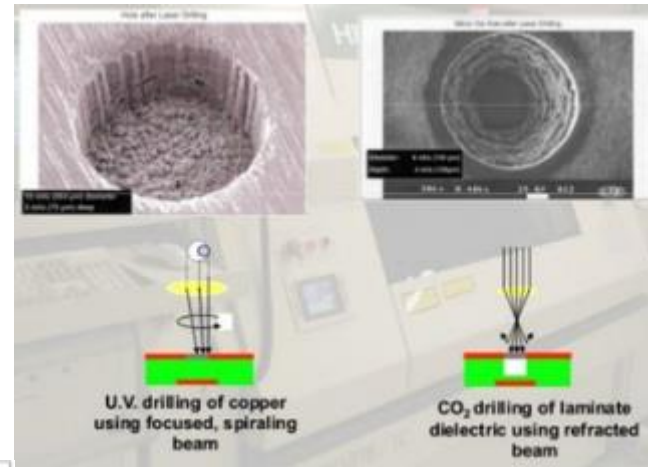
THE GODDARD COMMUNITY

More than 10,000 People



PCB Technology

In today's compressed development cycles where rapid and cost-effective testing and analysis are key, a properly designed and executed quality assurance function (with appropriate reliability analysis) can enable products with robust design margins.



If mission conditions are not well understood or the reliability analysis and accelerated testing are not conducted right, cost and schedule impacts, along with unexpected failures will add risk to a Project development cycle.

SOURCE: Industrial Laser Solutions. PCBShop.org

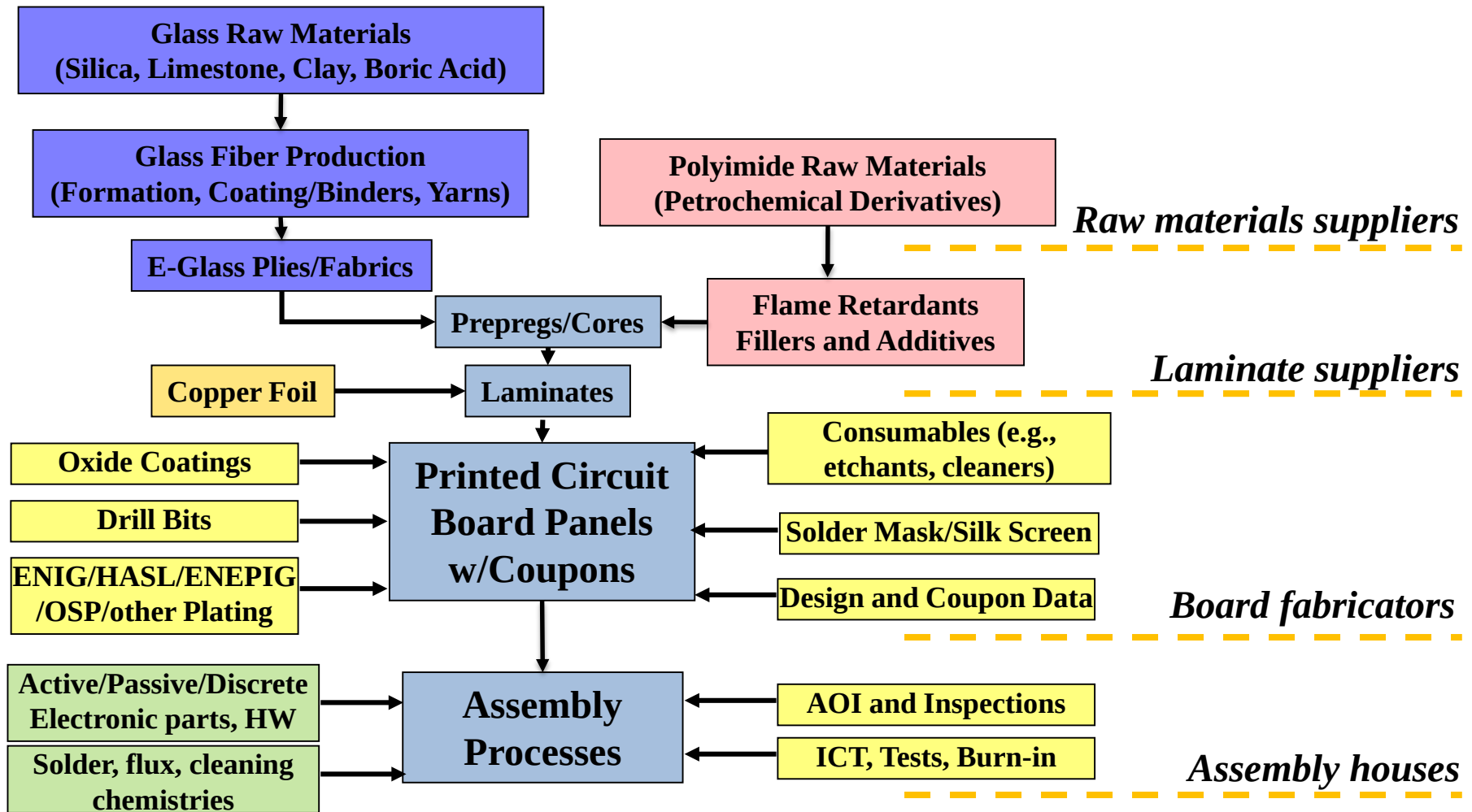
Printed Circuit Board – Classification and Design Process

PCB Design Process ^{1,2}

- Printed circuit boards are the baseline in electronic packaging – they are the interconnection medium upon which electronic components are formed into electronic systems.
 - PCB materials are generally glass reinforced organic polyimide (epoxy, BT, ceramic are also used).
 - Classified on the basis of
 - Dielectrics used
 - Reinforcement
 - Circuit type
 - Component types
 - Board construction
 - Design complexity
- ↓ An idea or Concept
 - ↓ Fundamental Design Strategy Electrical Architect
 - ↓ Parts Selection
 - ↓ Develop a Schematic
 - ↓ Generate a Bill of Materials
 - ↓ PCB Library Component Development
 - ↓ Netlist of the PCB Design
 - ↓ Netlist Verification
 - ↓ Mechanical Inputs
 - ↓ Design Requirements
 - ↓ PCB Design
 - ↓ PCB Design Verification
 - ↓ Gerber File Generation
 - ↓ PCB DFT / DFM
 - ↓ Design Review
 - ↓ Incorporate Design Review and DFT/ DFM Feedback
 - ↓ Overlay Output
 - ↓ Gerber Analysis and Plotfile Verification
 - ↓ Panelize PCB
 - ↓ Finalize Gerber Fabrication Package
 - ✓ PCB Fabrication

1. Coombs, Clyde F. *Printed circuits handbook*. Ed. Happy T. Holden. Vol. 1. New York: McGraw-Hill, 2001.
2. Steve Rose

Typical Polyimide PCBA Supply Chain¹

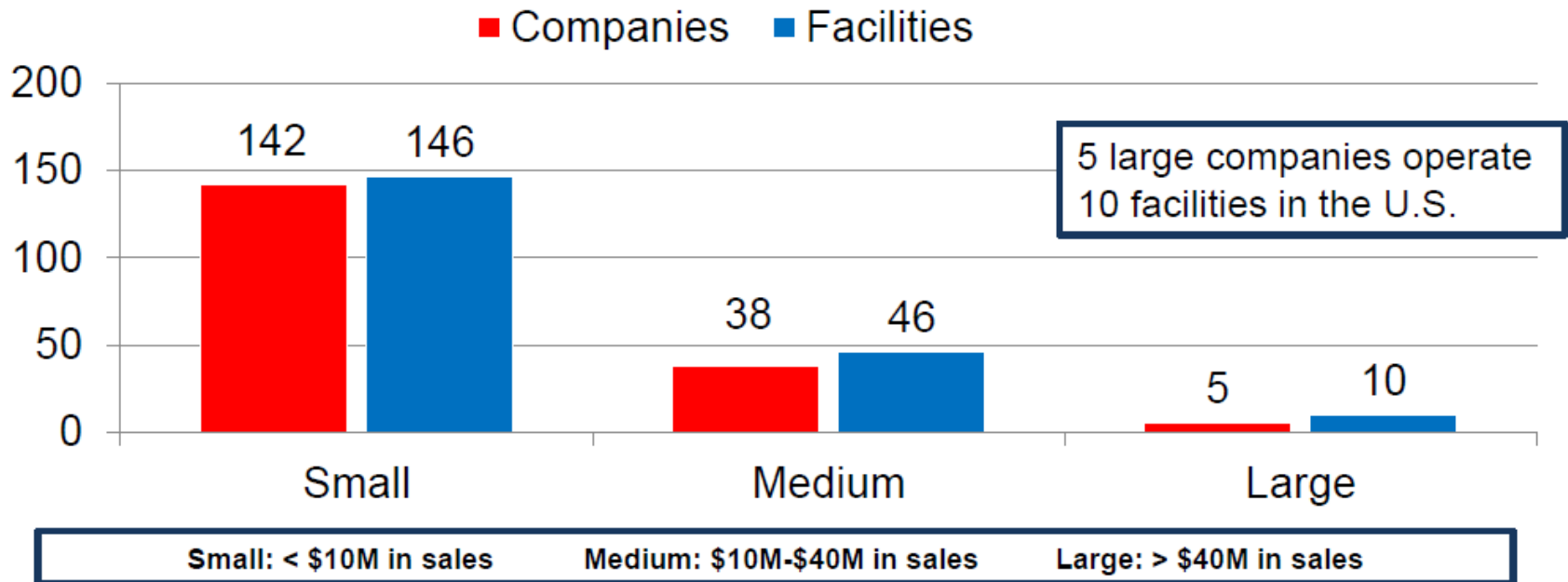


1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).

Bare PCB Suppliers¹

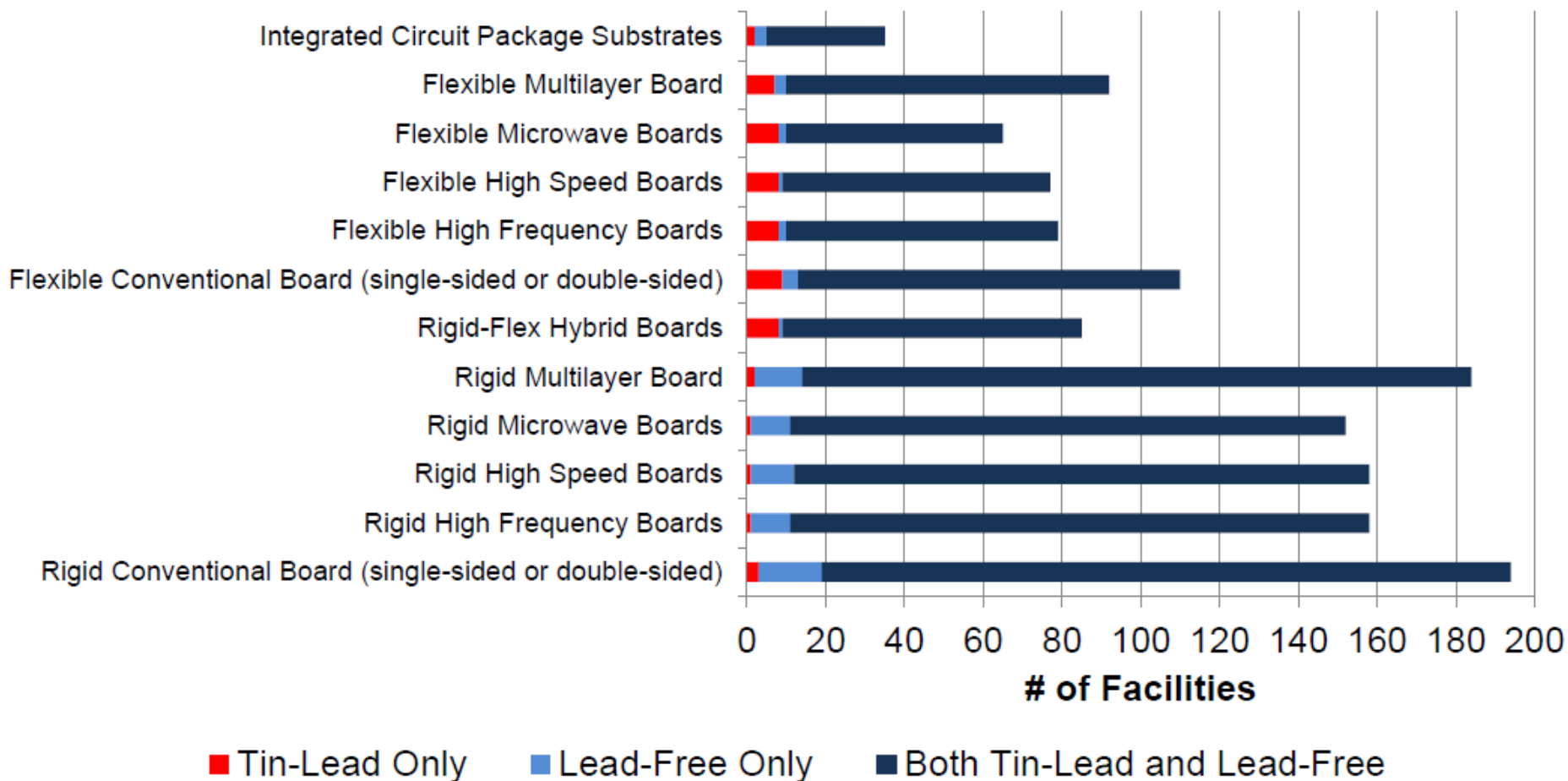
185 companies operate 202 bare printed circuit board manufacturing facilities in the U.S. - 2015

Number of Companies/Facilities by Bare PCB Sales



1. "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.

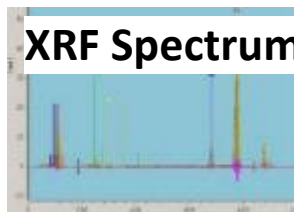
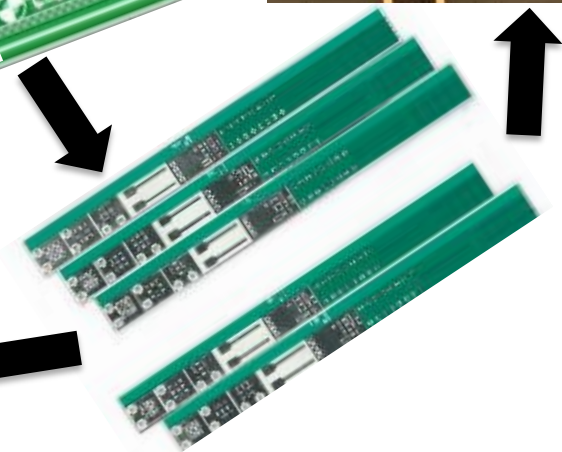
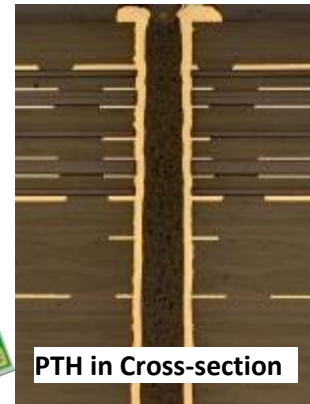
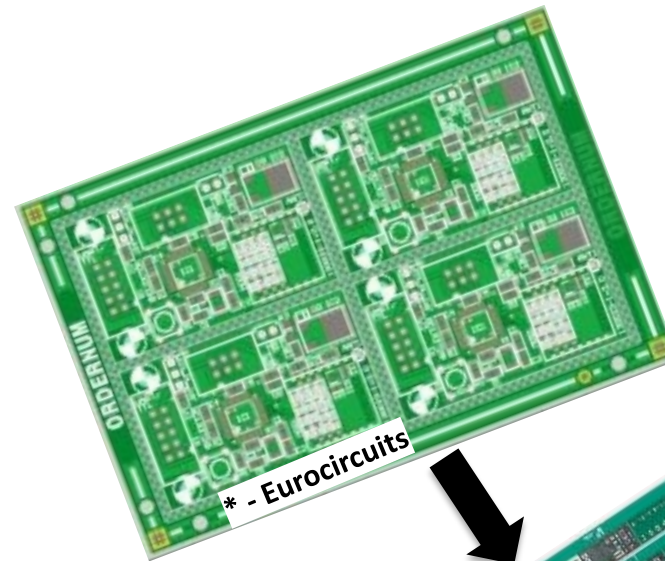
Bare PCB Supplier Capabilities¹



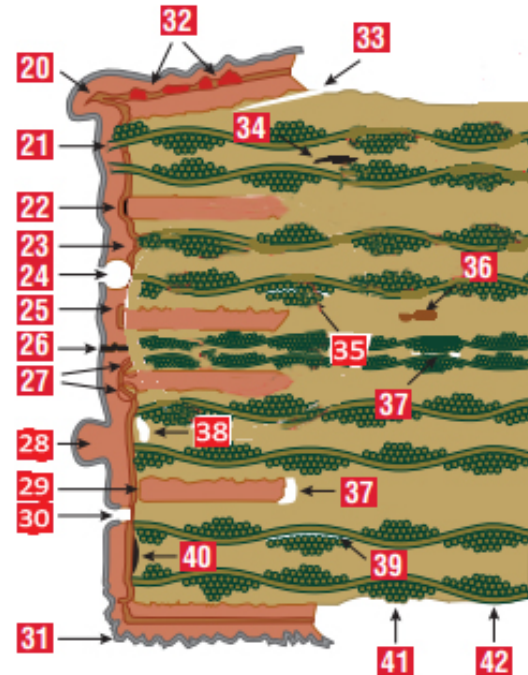
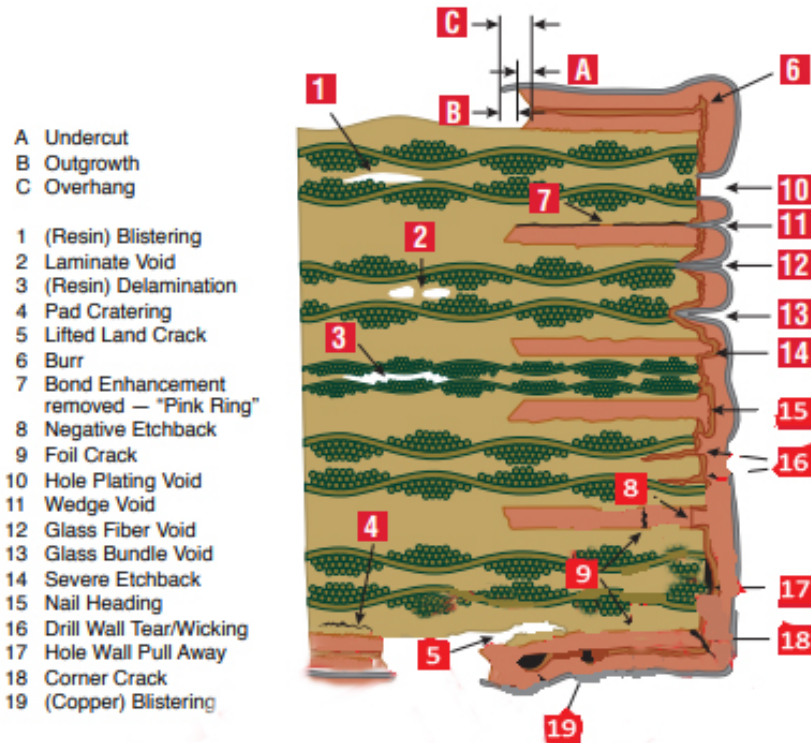
1. "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.

PCB Quality at NASA

- In a vast majority of cases, NASA uses IPC standards (e.g., IPC-6012, 6013, 6018)
 - IPC-6012 for rigid, IPC-6013 flex, IPC-6018 high speed etc..
- Inspection include:
 - Microsection evaluation (coupons)
 - Surface finish evaluation (coupons)
- Test include:
 - External visual examination
 - Electrical continuity and isolation
 - Solderability (not 100% cases)
 - Cleanliness
- In some cases MIL, ESA or “in-house” standards are applied.



Phenomenon in Cross-section of PCB PTHs



Originally Designed by
Viasystems Mommsers BV, Netherlands

Reviewed by BTI-PTH
Atotech Deutschland GmbH, Berlin

Updated to Industry Standard Terminology

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Image credit: ipc.org

Significance of Board Quality Requirements

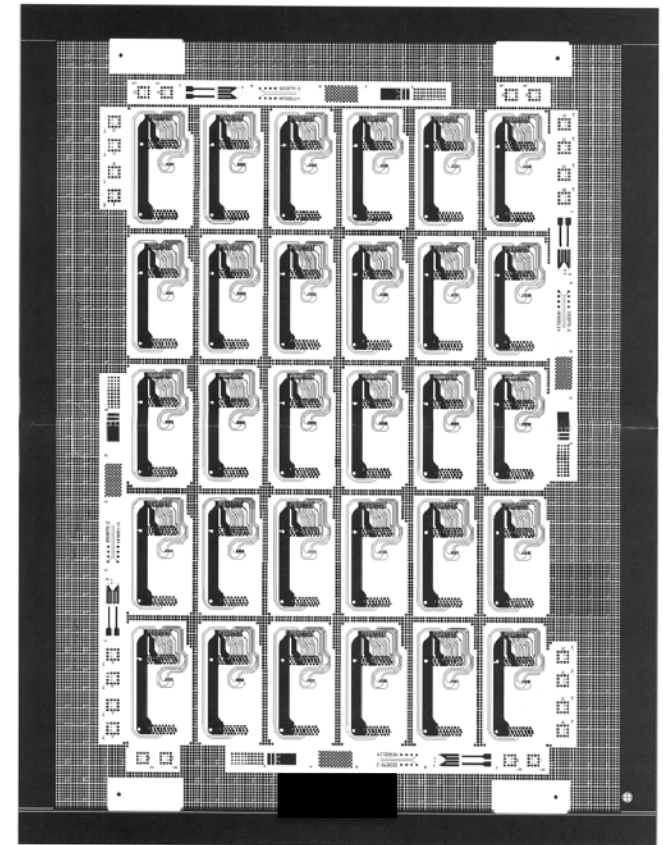
- Quality requirements and PCB coupons are a “front door”.
- Examples:
 - Internal Annular Ring:
 - Egregious violations indicate there may have been a serious problem in development of the board (layup, registration or lamination).
 - Other NCs don't indicate any risk at all (example: application of IPC-6012 Rev B. v/s IPC-6012 Rev. D)
 - Negative etchback v/s positive etchback:
 - Modern cleaning processes and flight experience result in equal reliability with both etchback conditions or no etchback, provided that there are no residues or contamination at the foil and e-less interface.
 - Wicking of copper:
 - Requirements are conservative based on broad statistics.
 - A basic analysis of the board layout can indicate directly if there is risk or not, regardless of requirements violations.

PCB Non-Conformance Rate Study – Objective

- In 2017 we started to evaluate a subset of GSFC PCB suppliers (direct or indirect) and corresponding PCB coupon microsection testing data.
- We developed a methodology for data generation and collection to provide trend analysis
 - Identify/predict violation of a process limit criteria (in case of an egregious NC).
- Provide analysis for severity categories of the non-conformance (NC).
- Provide recommendations to the suppliers (i.e. supplier quality engineering, continuous process monitoring, quality metrics definition).

Gap Between PCB Supplier's Internal Microsection Evaluation and Goddard's Results

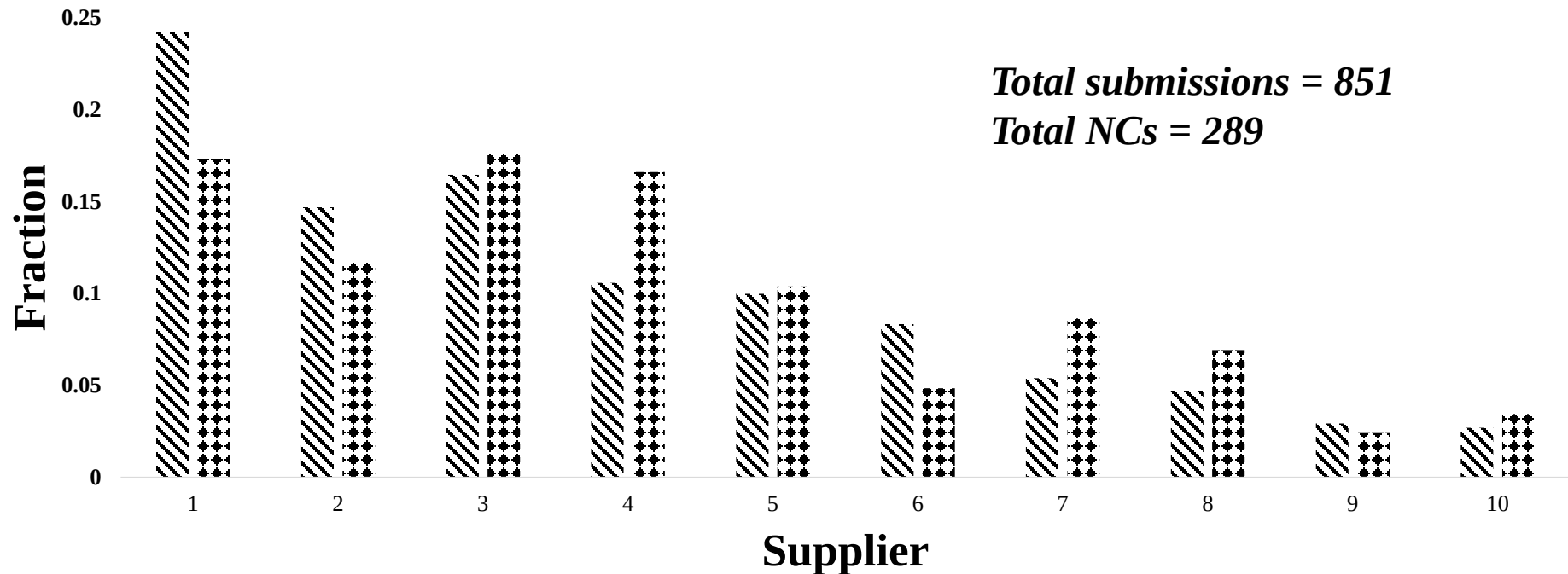
- Suppliers perform own microsectioning and inspect per specifications.
- Secondary GSFC independent microsection analysis yielded approx. 30% inspection NC.
- Some Possible Causes:
 - Screening escapes:
 - Test sample quality not consistent
 - Supplier microsection process
 - Inadequate coupons available to supplier
 - Requirement interpretations
 - Requirements flow-down issues
 - Alternative specifications (MIL, ECSS)
 - Buying heritage and off-the-shelf designs



Study Methodology – Data Generation

- Present study evaluates jobs performed by GSFC (lately the contribution of 3rd party labs has increased).
 - PCB coupon microsection evaluation in accordance to applicable IPC standards
 - Identified NCs
- Results from all GSFC suppliers were recorded from 2015 – 2020
 - Data includes NC and acceptable conditions in accordance with IPC Standards.
 - Total number of data points: 1224
 - Each job may have a number of NC with different severity levels
- Top ten (submission rate) suppliers represent 851 submissions (~70%)
- Total nonconformance observed for these top 10 suppliers: 289
- For each supplier, analyzed nonconformance(s)
 - Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
 - Classifying and analyzing top 5 severity categories.

Submission Rate & NC Spread



▨ Supplier's submission rate ▩ Nonconformance spread

$$\text{Supplier submission rate} = \frac{\text{total submission by individual supplier}}{\text{total submission by all suppliers}}$$

$$\text{Nonconformance spread} = \frac{\text{total nonconformance by individual supplier}}{\text{total nonconformance by all suppliers}}$$

Classification and Analysis - Top 5 Nonconformances

Twenty one distinct NC observed among the ten suppliers

NC from suppliers

Top ten PCB Suppliers at NASA Goddard									
1	2	3	4	5	6	7	8	9	10
A	F	E	A	N	K	E	E	T	A
B	A	D	F	O	F	P	A	K	F
C	D	B	D	F	L	C	D	U	S
D	E	Y	J	A	J	D	F	X	D
E	R	J	M	W	A	Q	R		P

	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note 6)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-inches (Au)	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greater than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	Exelis 8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminare cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil.	IPC 6012B Class 3/A
T	plating carcks	IPC 6012B Class 3/A
U	external annular ring < min. req'd. by drawing	ECSS-Q-ST-70-10C & 11C
W	Copper plating thickness greater than 2.0 mil	IPC-6013C Class 3
X	inclusions found between the plating layers	CSS-Q-ST-70-60C
Y	Foreign material plugging the via preventing HASL from completely covering the barrel	IPC-6012DS

Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to these NC.
- Implement techniques which may help to identify root cause(s).

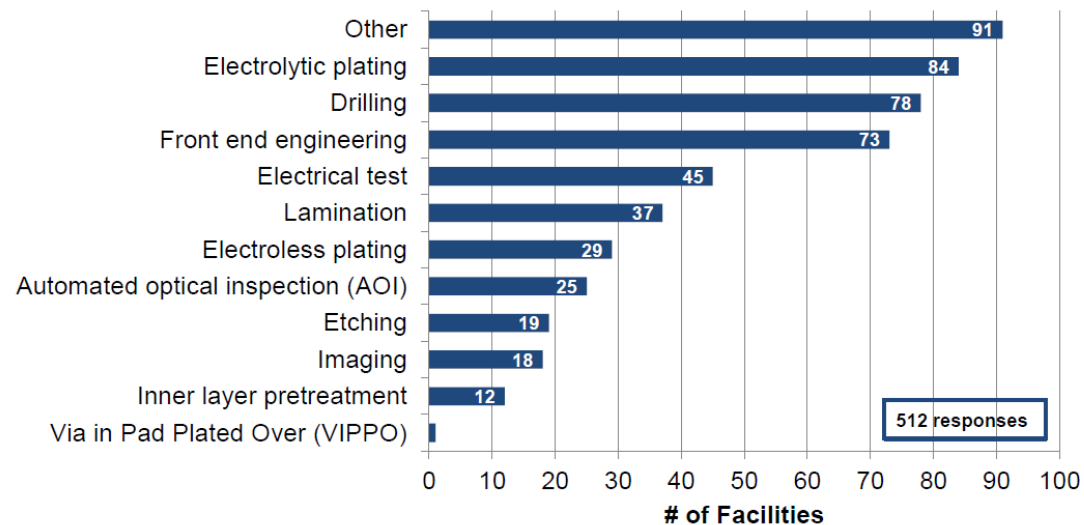
(A) Inner layer separations/inclusions

(D) Separation/inclusions between plating layers

(E) Copper wicking in excess of 2.0 mil

(F) Internal annular ring less than 2.0 mil

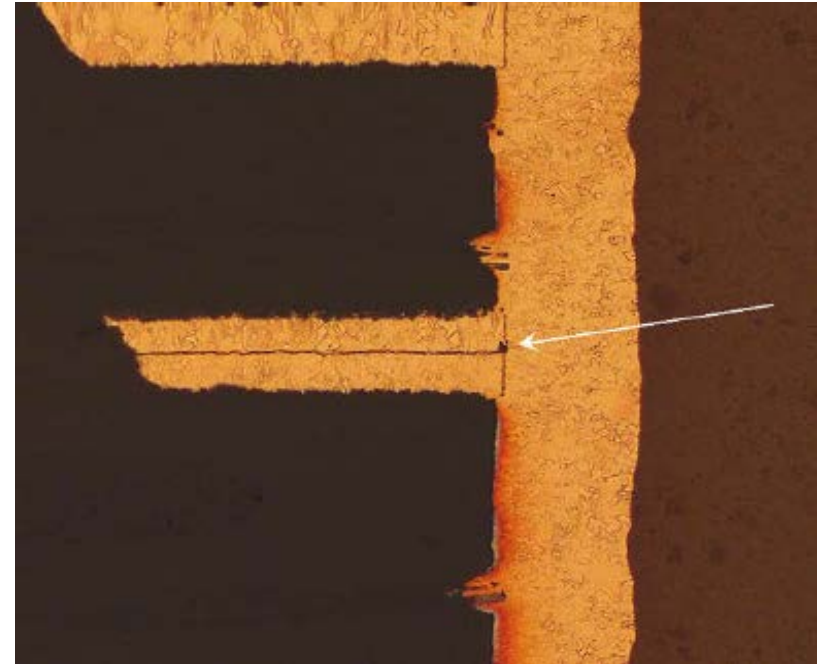
(J) ENIG is less than the minimum requirements



Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in an area where it is not expected.

Concern: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)



1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

Inner Layer Separations or Inclusions

Contributors

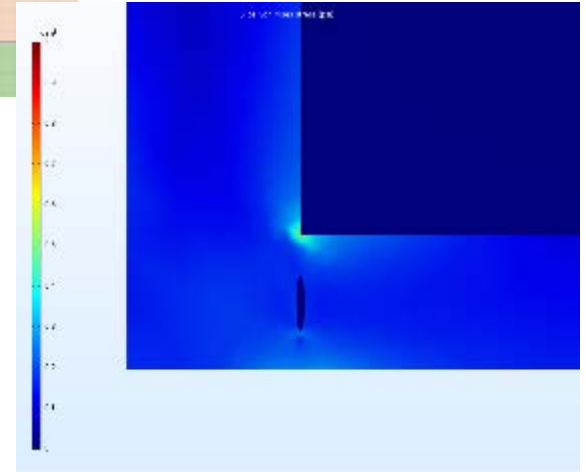
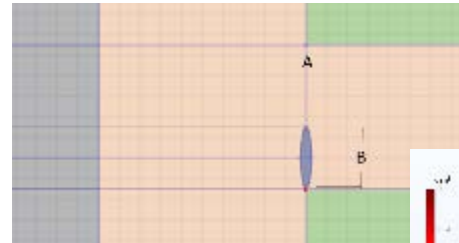
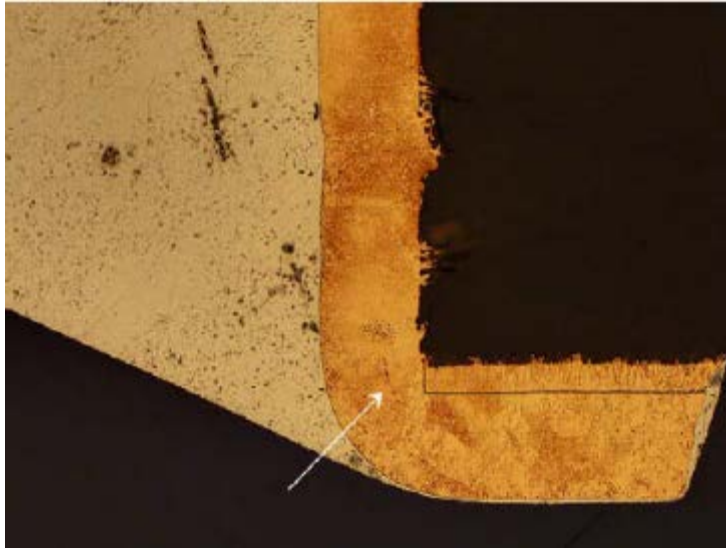
- Improper lamination press or cure cycles whether it be pressure, time, temperature.
- Others include inadequate coverage of inner layer oxide, moisture not completely removed in pre-lamination bake cycle.
- Poor quality prepreg and or laminate.
- Post-electroless copper cleaning residues, contaminated pretreatment prior to electrolytic plating, or an out-of-control electrolytic copper process.

Resolution

- Consistency in drilling processes.
- Reduce the resin content in the stack up.
- Good desmear, with adequate texture.
- Provide adequate copper border for support and resin venting

Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating layer and foil.



Concern: intermittent electrical open or complete opens due to mechanical or thermal stresses.

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

Separation or Inclusions Between Plating Layers

Contributors

- Incomplete wrap plating
- Overly-aggressive cleaning process
- Insufficient cleaning

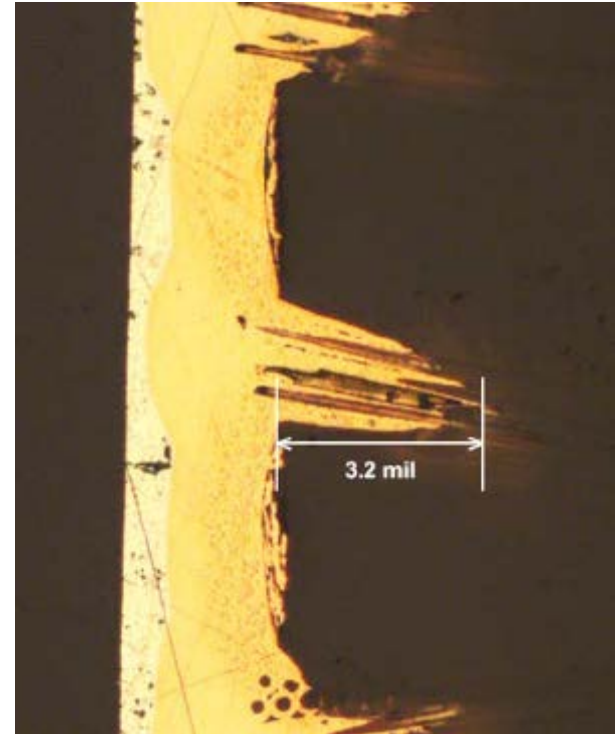
Resolution

- Adjust plating parameters
- Optimize cleaning processes

Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.

Concern: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.



1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Copper Wicking in Excess of 2.0 mil

Contributors

- Dull drill bits that causes a crack in the laminate.
- Incompatible laminate material.
- Insufficient glass etch.
- Poor glass to organic adhesion.

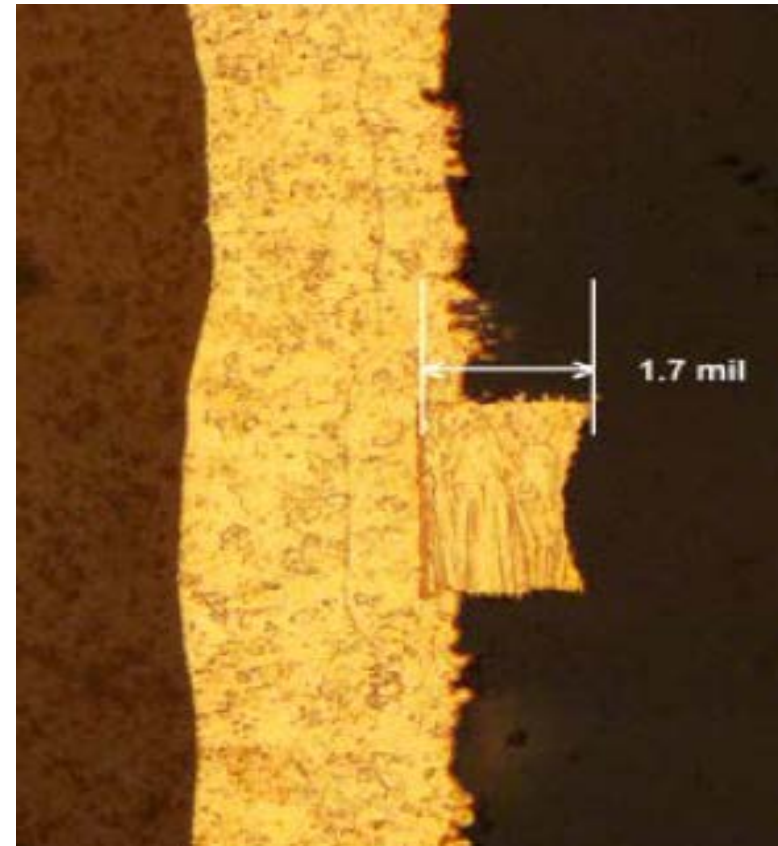
Resolution

- Optimize desmear parameters
- Improve drilling operation (feed and speed).
- Ensure sufficient resin wet-out of glass fibers (siloxane treatment).

Internal Annular Ring Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.

Concern: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.



1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards", Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Internal Annular Ring Less Than 2.0 mil

Contributors

- Drilled-hole pattern not matching the lands on the internal layers (Misregistration).
- Lamination process.
- Prelamination treatments that involve scrubbing or bending may stretch the thin laminate, which will then shrink after it is etched and baked dry.
- Application of specification or drawing notes.

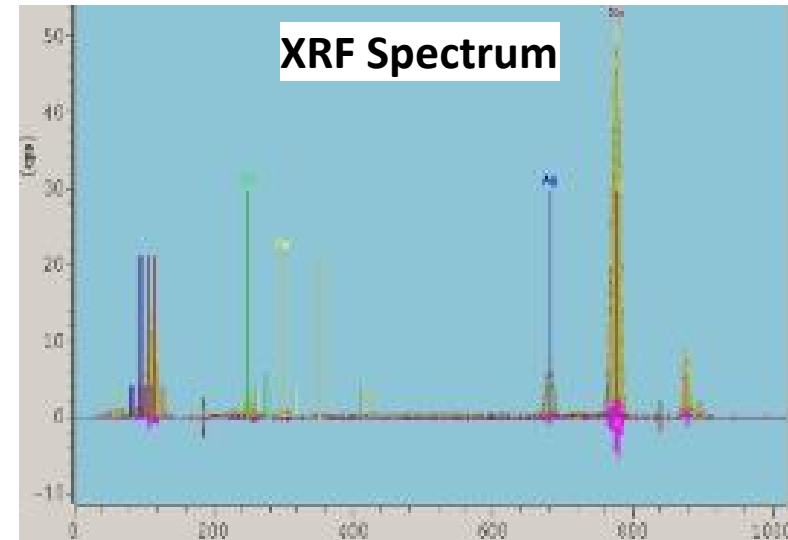
Resolution

- Better material selection of laminate, improved cleanliness, and reduction in the amount of volatiles.
- Confirm whether or not it is operator error.
- Update drawing notes to bring the notes in line with current industry maturity levels.

ENIG (Au or Ni) Less than the Minimum

Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (118 micro-inches for Ni and 2 micro-inches for Au).

Concern: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.



1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

ENIG Less than Minimum

Contributors

- Improper cleaning of surfaces.
- Improper or inadequate rinsing.
- Bath parameters not being followed (pH and chemical).
- Bath temperature too low.
- Copper surface not clean of oil or inhibiting film.

Resolution

- Re-clean copper using chemical cleaners or mechanical
- scrubbing Institute micro-etch step to improve cleaning
- Improve rinsing(Check flow, agitation and water quality)
- Raise temperature per supplier specifications
- Readjust to supplier operational parameters

Summary of Supplier Study

- The test data is analyzed using statistical method to provide trend analysis for all suppliers.
 - Root cause(s) and key contributors are identified.
 - Mitigation plan is included for the root cause of nonconformance.
- Provide recommendations to the supplier's process, identification and prediction of nonconforming process limit criterion, and to improve test standards.
- New technologies (example: smaller annular rings, via-in-pads, thinner laminates or newer plating) are implemented on the basis of supplier maturity and reported NCs.

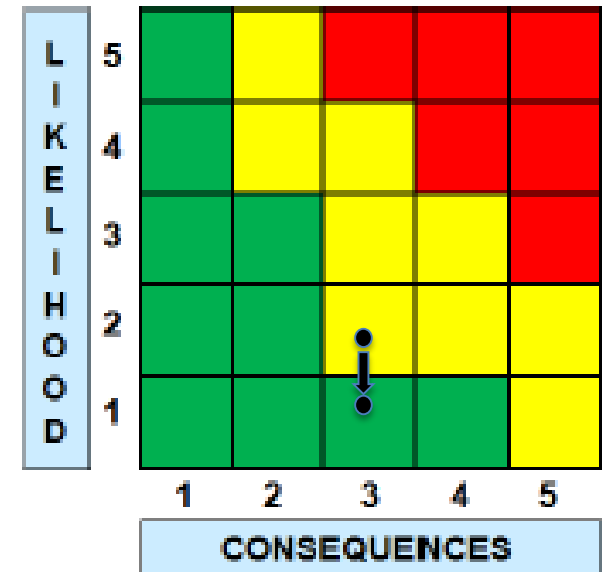
NASA Goddard Risk Assessment Process

What is Risk?

Risk is an expectation of loss in statistical terms.

Definition: the combination of

- a) the probability (qualitative or quantitative) that an undesired event will occur, and
 - b) the consequence or impact of the undesired event
- Flavors of risk (consequences)
 - Technical (failure or performance degradation on-orbit)
 - Cost (\$ it will take to fix the problem)
 - Schedule (time to fix the problem)
 - Safety (injury, death, or collateral damage)



Communicating risk is key to portraying the status of a new technology and project in development.

Why Do We Worry About Risk?

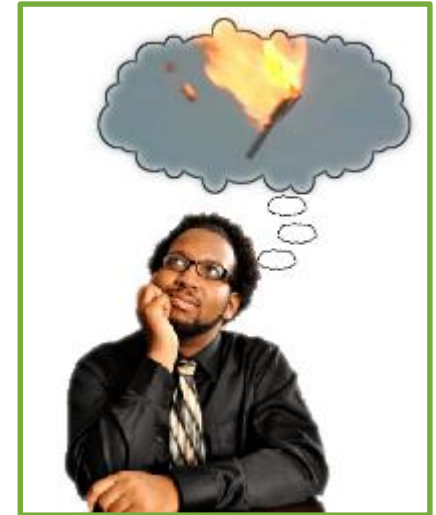
- **We don't want bad things** to happen
- The only way to avoid risk is to avoid doing anything
- Understanding risk is key to engineering the system
 - Establishing requirements
 - Responding to undesired or unexpected events
 - Choosing between different options
- Communicating risk is key to portraying the status of a project in development



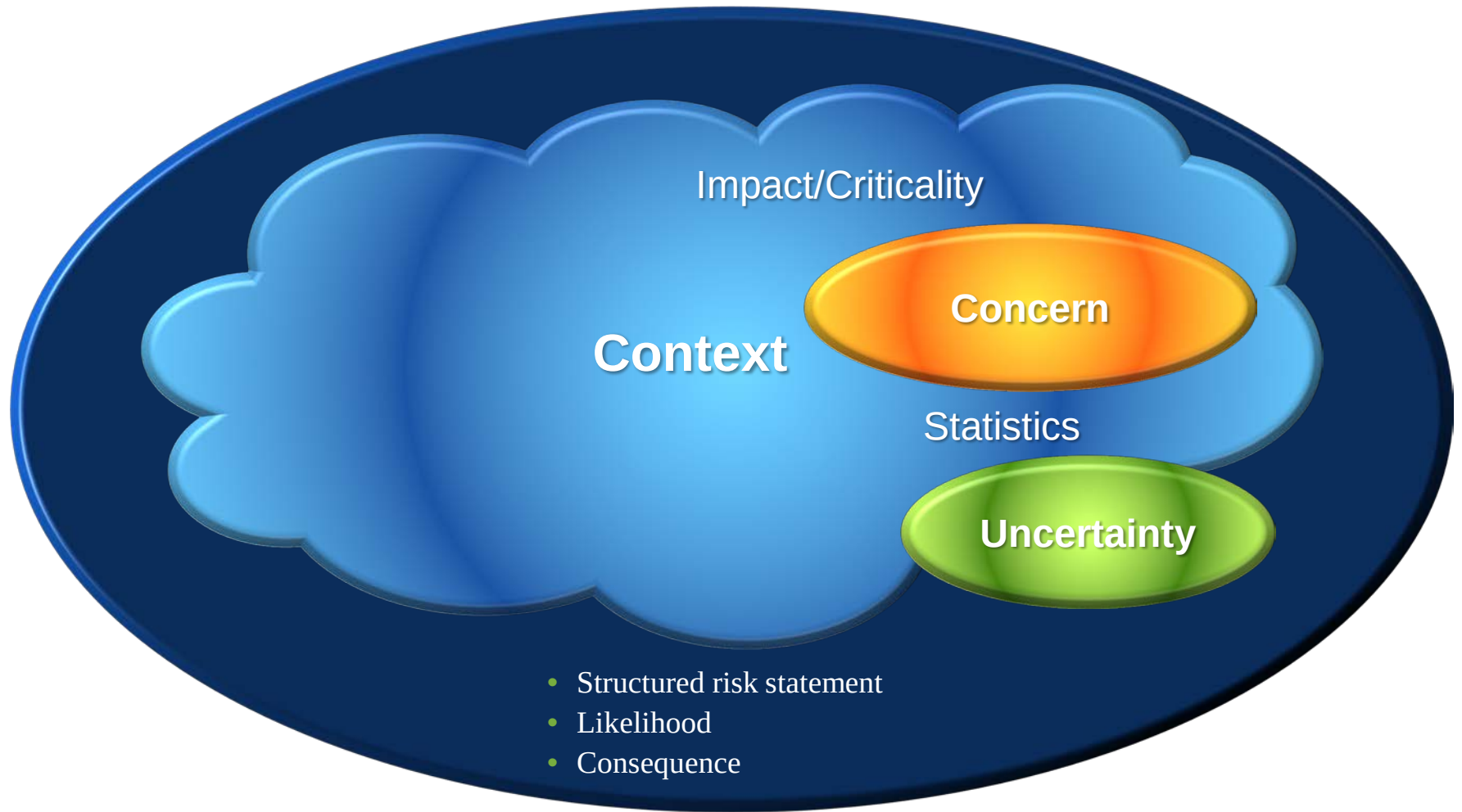
Proton Failure

Risk vs. Possibility

- Failure modes and mechanisms can appear through
 - Analysis and simulation
 - Observation
 - Prior experiences
 - Brainstorming “what if” scenarios
 - Speculation
- These all constitute *possibilities*
- There is a tendency to take action to eliminate severe consequences regardless of the probability of occurrence
- When a possibility is combined with an environment, an operating regime, and supporting data, a risk can be established.
- Lack of careful and reasoned analysis of each possibility in terms of the conditions that results in the consequence and the probability of occurrence will result in excessive cost and may increase the overall risk



Anatomy of a Risk



Concern

- Definition: A logical determination that an undesired event may occur or that the protections against such an event may not be sufficiently well understood based on available data
- This is the core element upon which a risk is founded
- In some sense, it is the risk without the context, likelihood or consequence.
- Can come in the same “flavors” (categories) as risks
 - Technical
 - A part may fail
 - Cost
 - Cost of an item may grow
 - Schedule
 - Delivery may be delayed
 - Safety
 - The spacecraft may fall off the crane

Balanced Risk (maintaining a level waterbed)

A systems approach of looking across all options to ensure that mitigating or eliminating a particular risk does not cause much greater risk somewhere in the system

Try to maintain the level waterbed

Pushing too hard on individual risks can cause other risks to be inordinately high

What is Risk Classification?

- Establishment of the level of risk tolerance from the stakeholder, with some independence from the cost
 - Cost is covered through NPR 7120.5 Categories
- If we were to try to quantify the risk classification, it would be based on a ratio of programmatic risk tolerance to technical risk tolerance.
 - For Class A, we take on enormous levels of programmatic risk in order to make technical risk as close to 0 as possible. The assumption is that there are many options for trades and the fact is that there must be tolerance for overruns.
 - For Class D, there will be minimal tolerance for overruns and a greater need to be competitive, so there is a much smaller programmatic risk “commodity” to bring to the table.
- The reality is that the differences between different classifications are more psychological (individual thoughts) and cultural (longstanding team beliefs and practices) than quantitative.

Risk Classification—(NPR 7120.5 Projects)

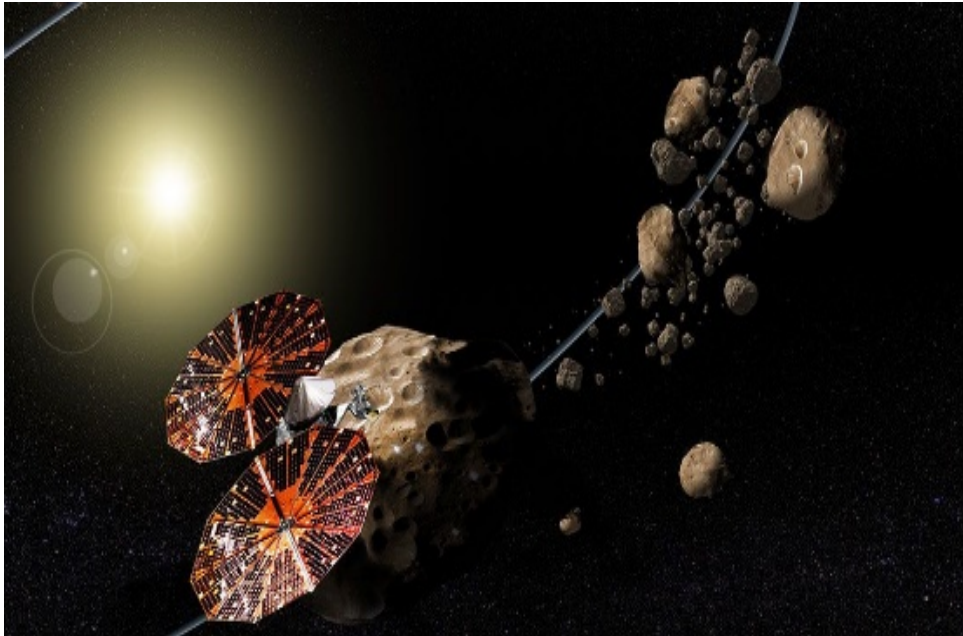
- **Class A: Lowest risk posture by design**
 - Failure would have extreme consequences to public safety or high priority national science objectives.
 - In some cases, the extreme complexity and magnitude of development will result in a system launching with many low to medium risks based on problems and anomalies that could not be completely resolved under cost and schedule constraints.
 - Examples: HST and JWST
- **Class B: Low risk posture by design**
 - Represents a high priority National asset whose loss would constitute a high impact to public safety or national science objectives
 - Examples: LUCY, JPSS, and OSIRIS-REX
- **Class C: Moderate risk posture by design**
 - Represents an instrument or spacecraft whose loss would result in a loss or delay of some key national science objectives.
 - Examples: LRO, MMS, TESS, and ICON
- **Class D: Cost/schedule are equal or greater considerations compared to mission success risks**
 - Technical risk is medium by design (may be dominated by yellow risks).
 - Many credible mission failure mechanisms may exist. A failure to meet Level 1 requirements prior to minimum lifetime would be treated as a mishap.
 - Examples: LADEE, IRIS, NICER, and DSCOVR

Risk Classification—(Non-NPR 7120.5 Projects)

- **NPR 7120.8 “class”—Technical risk tolerance is high**
 - Some level of failure at the project level is expected; but at a higher level (e.g., program level), there would normally be an acceptable failure rate of individual projects, such as 15%.
 - Life expectancy is generally very short, although instances of opportunities in space with longer desired lifetimes are appearing.
 - Failure of an individual project prior to mission lifetime is considered as an accepted risk and would not constitute a mishap. (Example: ISS-CREAM)
- **“Do No Harm” Projects**—If not governed by NPR 7120.5 or 7120.8, we classify these as “Do No Harm”, unless another requirements document is specified
 - Allowable technical risk is very high.
 - There are no requirements to last any amount of time, only a requirement not to harm the host platform (ISS, host spacecraft, etc.).
 - No mishap would be declared if the payload doesn’t function. Note: Some payloads that may be self-described as Class D actually belong in this category. (Example: CATS, RRM)

7120.8 and “Do No Harm” Projects are not Class D

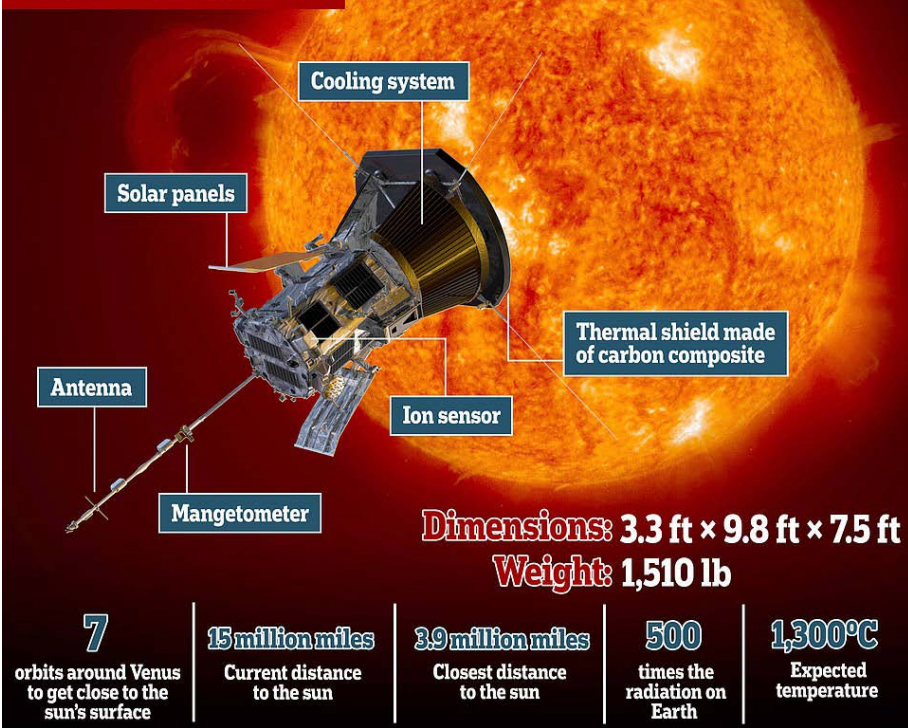
LUCY



Lucy is a planned NASA space probe that will tour five Jupiter trojans, asteroids which share Jupiter's orbit around the Sun, orbiting either ahead of or behind the planet and one main belt asteroid. All target encounters will be fly-by encounters

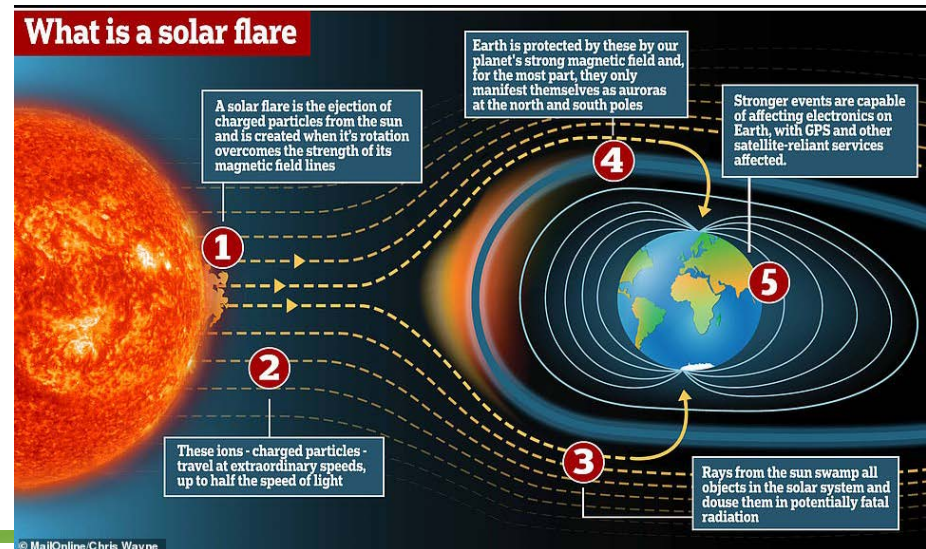
PSP (Parker Solar Probe)

The Parker Solar Probe

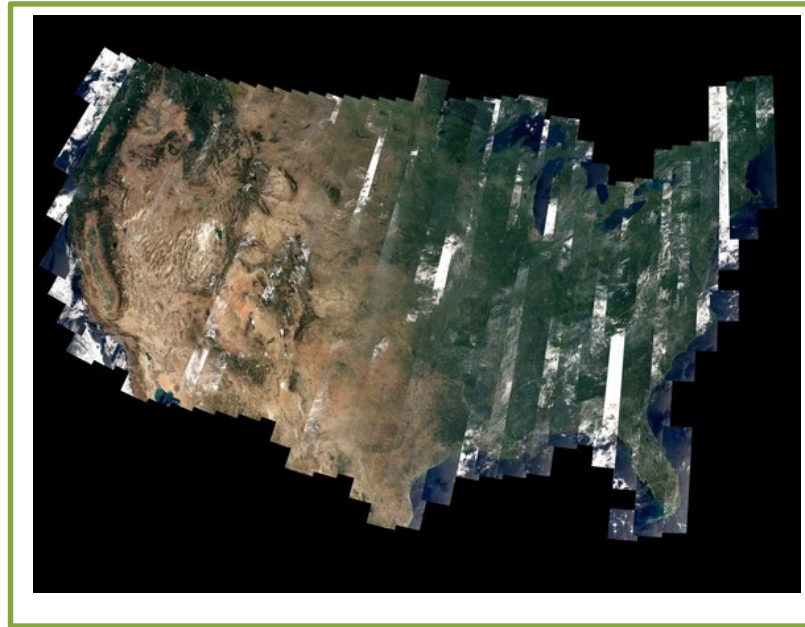


The Parker Solar Probe is a NASA robotic spacecraft launched in 2018 with the mission of making observations of the outer corona of the Sun. It will approach to within 9.86 solar radii from the center of the Sun, and by 2025 will travel, at closest approach, as fast as 690,000 km/h, or 0.064% the speed of light

What is a solar flare



LandSat – 9



Landsat 9 is a planned Earth observation satellite, scheduled for launch on 8 April 2021. NASA is in charge of building, launching, and testing the system, while the United States Geological Survey will process, archive, and distribute its data.

OSIRIS – REX



The OSIRIS-REx is a NASA asteroid study and sample-return mission. The mission's primary goal is to obtain a sample of at least 60 grams from 101955 Bennu, a carbonaceous near-Earth asteroid, and return the sample to Earth for a detailed analysis

OSIRIS-REx: unlocking the secrets of our Solar System

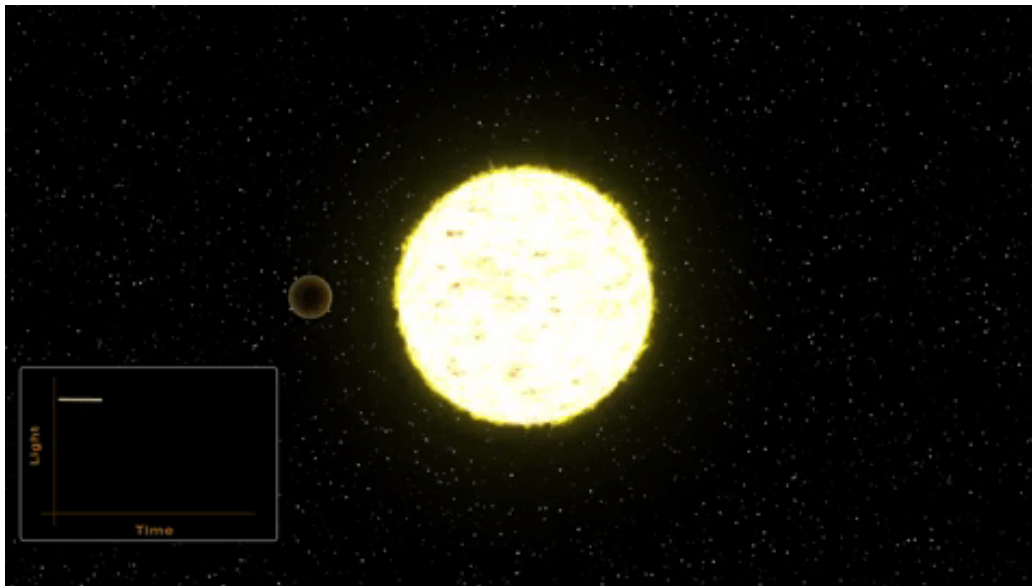
The robotic spacecraft will travel to the Bennu asteroid and bring back samples that may teach us more about the origins of life



Transiting Exoplanet Survey Satellite (TESS)

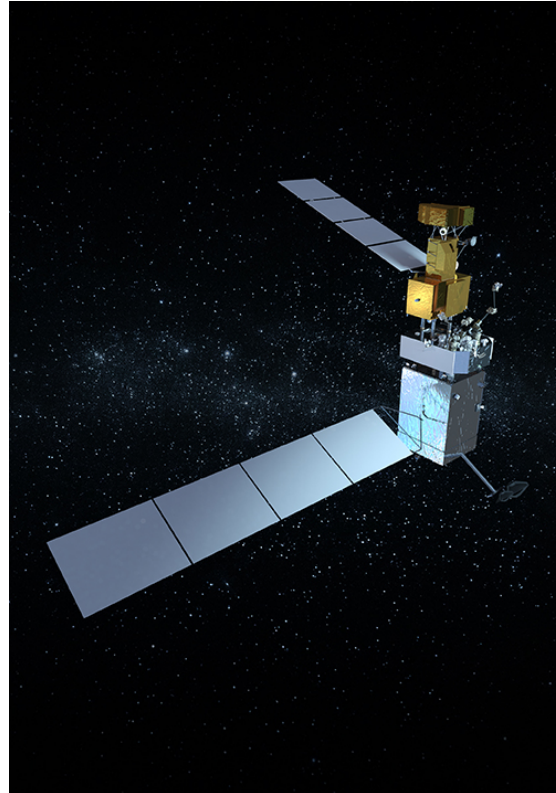
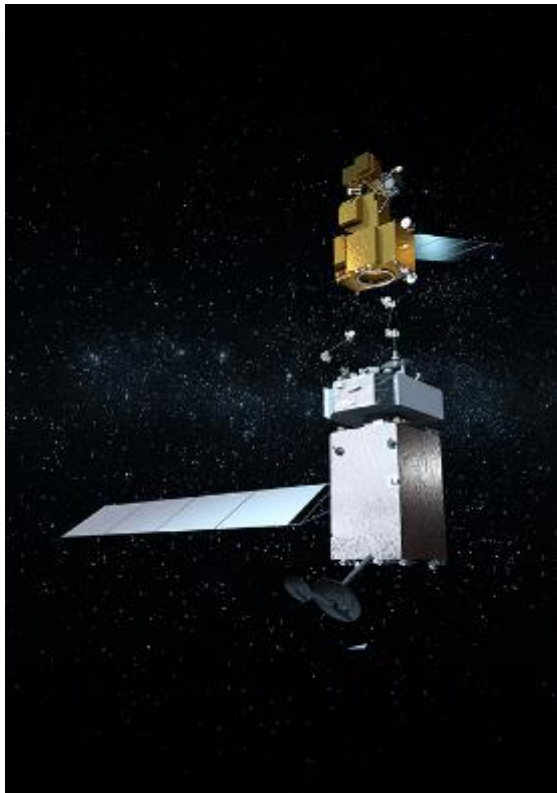


TESS is the next step in the search for planets outside of our solar system, including those that could support life. The mission will find exoplanets that periodically block part of the light from their host stars, events called transits. TESS will survey 200,000 of the brightest stars near the sun to search for transiting exoplanets. TESS launched on April 18, 2018, aboard a SpaceX Falcon 9 rocket.



OSAM – 1 (On Orbit Servicing)

On-orbit Servicing, Assembly, and Manufacturing 1 (OSAM – 1), a robotic spacecraft equipped with the tools, technologies and techniques needed to extend satellites' lifespans - even if they were not designed to be serviced on orbit.



- Enabling new architectures and capabilities for a wide range of government and commercial missions
- Enabling In-space construction of large communications antennae and telescopes
- Eliminating volume limits imposed by rockets
- Replacing some astronaut extravehicular activity tasks with precision robotics
- Introducing the potential for longer mission durations enabled by planned or unplanned maintenance

NASA is incorporating elements of the core OSAM-1 technologies into the architecture for the Journey to Mars.

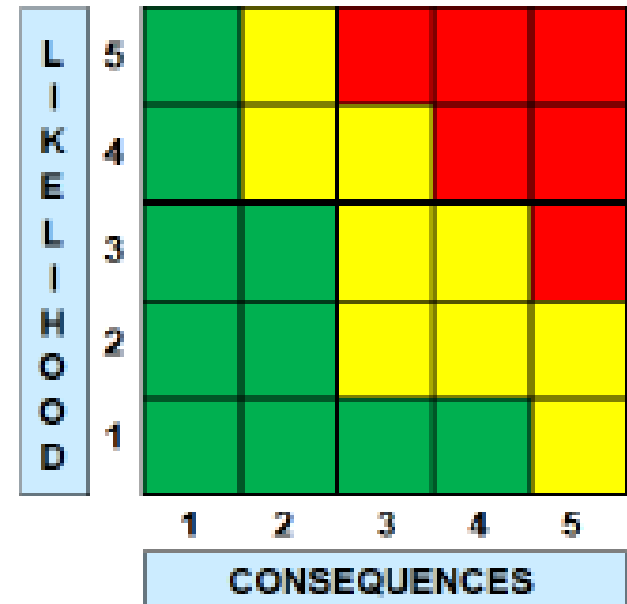
Risk of Conformance vs. Risk of Nonconformance

- Were requirements imposed based on an understanding of the risks within a project?
- What are the risks associated with the enforcement of requirements?
- What is the risk associated with a particular nonconformance?
- Should we immediately assume that a nonconforming item is risky for the application?
- In many cases there is a good reason why a product is nonconforming

**Do not reject a nonconforming item without understanding the risk.
Determine the cause of NC before reproducing the item.**

Impact of PCB Non-conformances

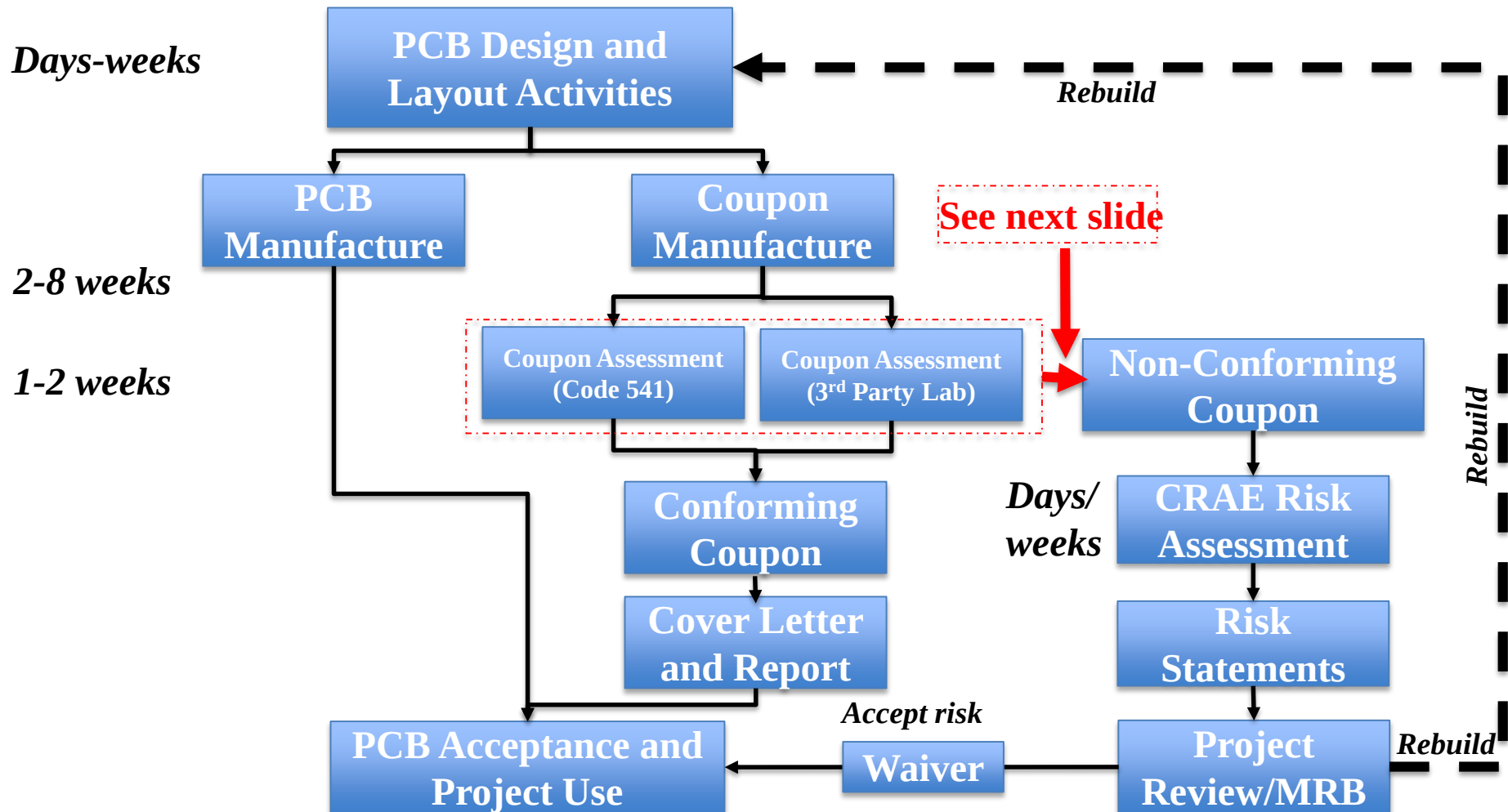
- Bare boards cost \$\$ and build schedules – expensive!!
- But failures are even more expensive!
- Test sample nonconformance is not the same as PCB failure.
- Risk-based decisions are used for disposition of non-conformances.
- Non-conformances may have little to no impact per application.
- Began to explore origins and merit of requirements (more later).



Risk Assessment Process

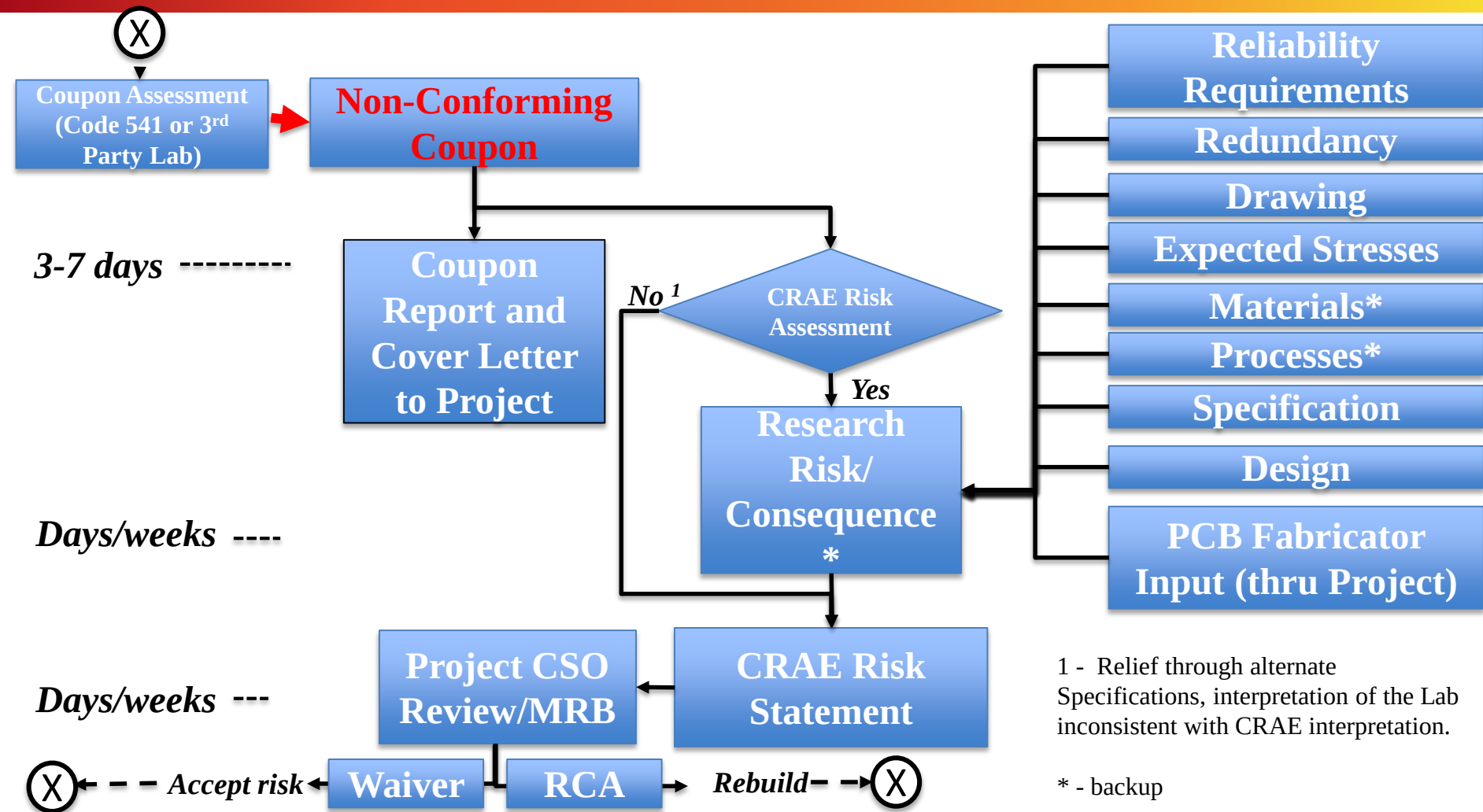
- Traceable PCB test coupons (designed per specs. such as IPC-2221B) are submitted to GSFC or to a GSFC-assessed laboratory.
- Reports that indicate nonconformance are dispositioned by risk assessment performed prior to refabricating or populating the PCB.
 - If risk assessment indicates elevated risk due to the nonconformance, then use is dispositioned by MRB.
- Risk assessment process eliminates waste and saves money and schedule, lowers overall risk for the project.
- The process reduces the need for repeated attempts to refabricate.

PCB Assurance At NASA Goddard



Code 300 determines the risk, project decides whether to accept the risk.

Risk Assessment Approach



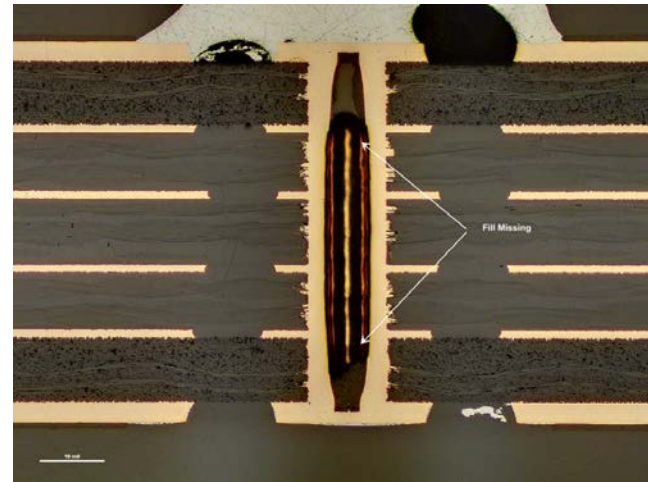
Sampling of Risk Assessments – 1

Copper wicking in excess of 2.0 mil



The wicking is well-enclosed within the annular rings with significant margin, and should not violate electrical spacing. When inspected with IPC-6012 DS, these boards would be compliant (max 3.5 mil wicking + etchback).

Capped via with fill less than 75%



Voiding is contained and enclosed within the fill material (with matches in CTE with the PCB laminate), and does not appear to have an interface with the cap where contaminants could potentially trap.

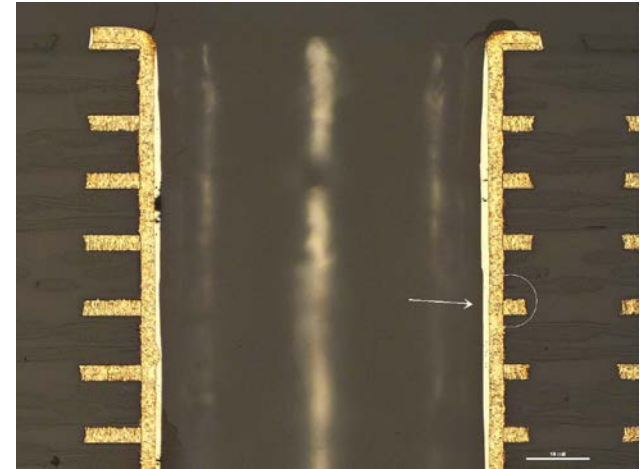
Sampling of Risk Assessments – 2

Dielectric layer less than 3.0 mil



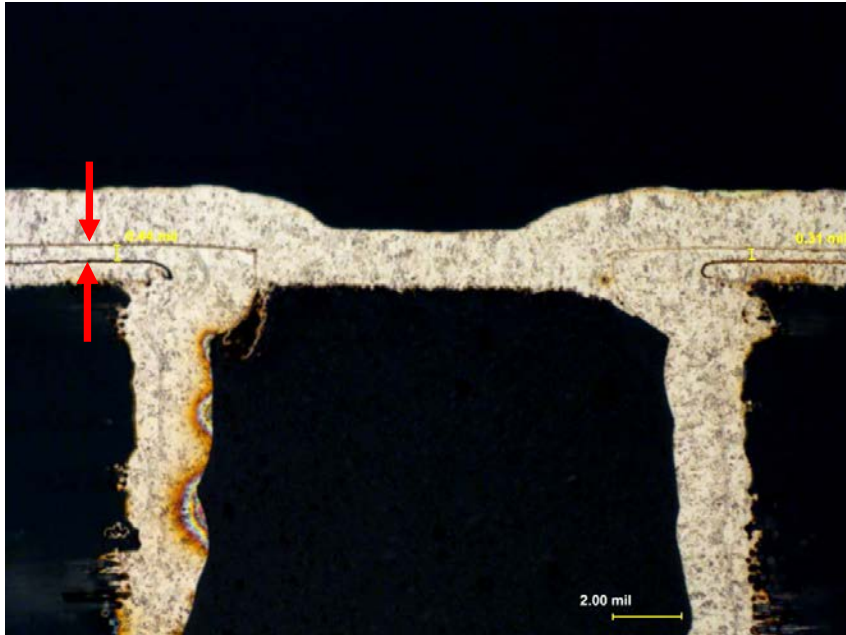
A 40kV dielectric breakdown strength, combined with a 28V service voltage provides a sufficient dielectric clearance at 2.8mil. There are at least two layers of dielectric material present.

IAR less than the minimum 5.0 mil



Out of date drawing notes containing a minimum 5.0mil annular ring and other requirements.

PTH Copper Wrap Thickness Requirement



- Thermal cycle stresses act on interfaces, outer layers experience the greatest stress.
- Reason: materials selection and geometry.

Per IPC-6012D for through-holes:

Class 1	AABUS
Class 2	5 μm [197 μin]
Class 3 & 3/A	12 μm [472 μin]

AABUS = As Agreed Between User and Supplier

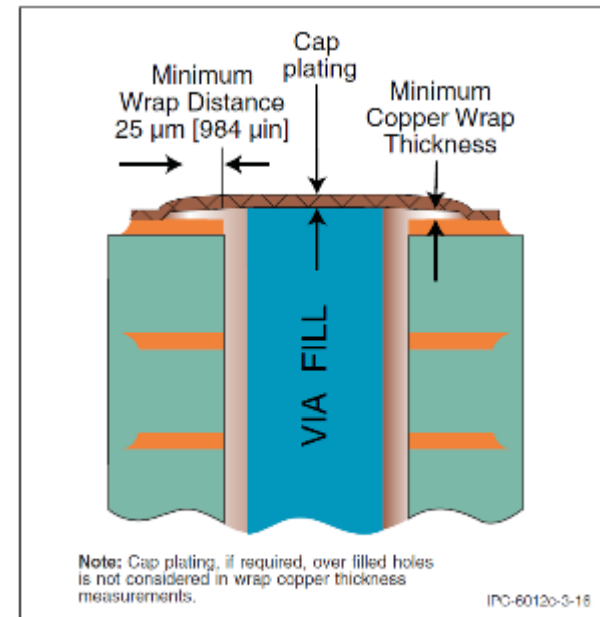


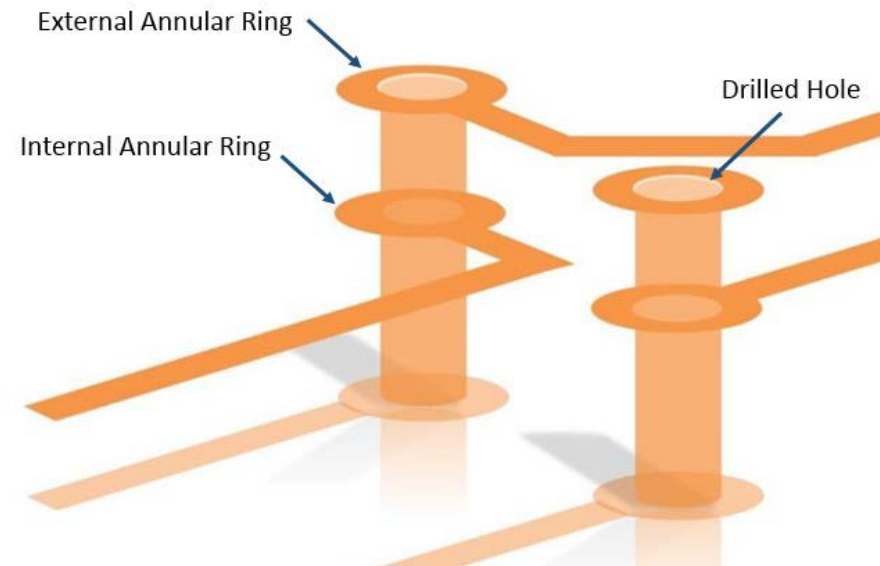
Figure 3-16 Surface Copper Wrap Measurement
(Applicable to all filled PTHs)

PTH Copper Wrap Thickness: Disposition

- GSFC Mission had populated and integrated board with zero wrap, wrap planarization can cause 0.3mil or more variance in panel; manufacturers must target more wrap.
 - Wrap cannot be achieved at required thickness for designs with tight line-width spacing and/or with multiple lamination/plating steps
- Requirement was introduced to IPC with minimal data
 - Reliability reported to be better with wrap vs. butt joint
 - Half of barrel plating thought to be “good enough”
 - Higher quality limit used as safety margin against manufacturing variation during planarization
- **GSFC Studies:** Determined the impact of copper wrap plating thickness on PCB reliability, as characterized by thermal cycles to failure.
 - Able to determine acceptability of wrap defect based on reliability testing and analysis in context of mission environment and duration.
 - IPC voted to change the requirement (amendment in Rev. D and revisions in Rev. E).

Internal Annular Ring (IAR) Assessments

- The goal is to design in variations in the internal annular ring geometries in printed circuit board and correlate the effects of these variations as a source of risk for PCB failure in GSFC test and mission environments.
- Reliability tests such as temperature cycling and mechanical flexure are conducted on test samples constructed with control IAR widths, sub-optimal IAR widths and other configurations such as teardrops.
- **Outcome:** On the basis of this work, it is determined, on a per design basis that IAR should be between 1 mil and 2 mils or it can be lower than 1 mil (0.5mil) or in a teardrop configuration if IAR size does not have an adverse effect on the reliability of PCBs and does not increase the risk of failure for GSFC missions.

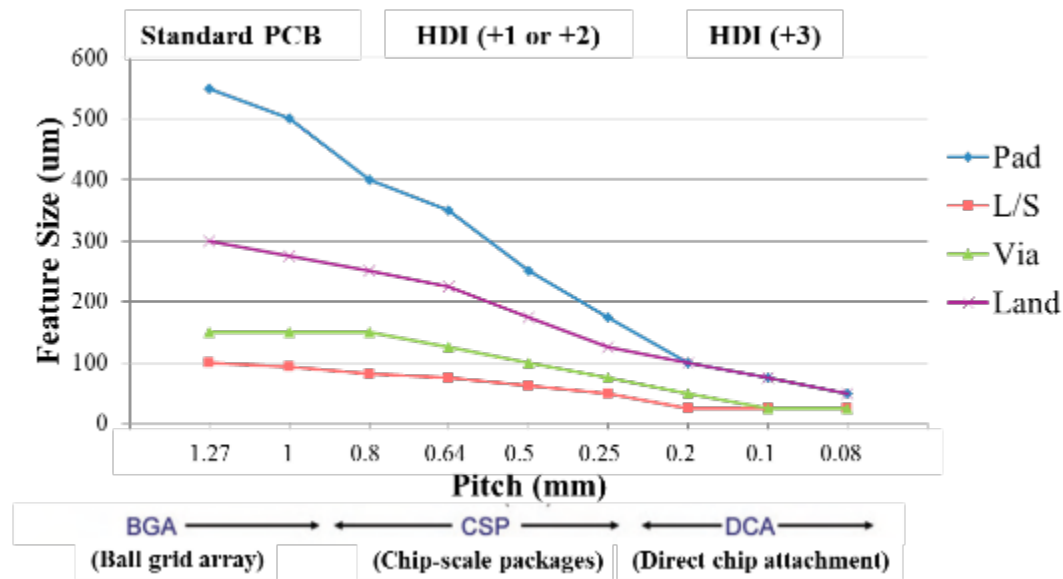


Concerns with IST Specifications

- High density interconnect (HDI) testing is performed with interconnect stress testing (IST) using a methodology documented in the IPC test methods manual TM650, Method 2.6.26.
- Elevated temperatures exceeding 220°C are sometimes used to cause HDI failures.
- Although IST can be an effective screen for process, materials, design and workmanship, it is not recommended as a predictor of reliability.
- Increasingly, IST test results that are generated at elevated and highly accelerated test condition are being used for predicting operational reliability of HDI PCBs.

MicroVia – Background

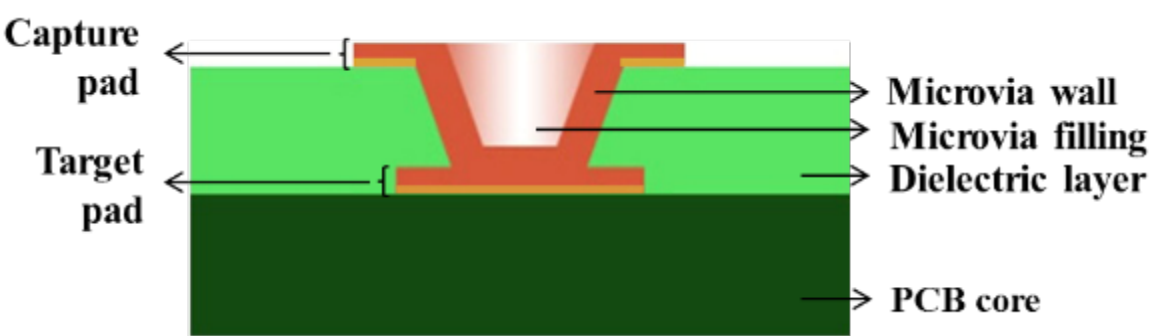
The continuous increase in component performance and lead density and reduction in package sizes, along with hand-held applications, have driven the need for high density interconnects (HDIs).



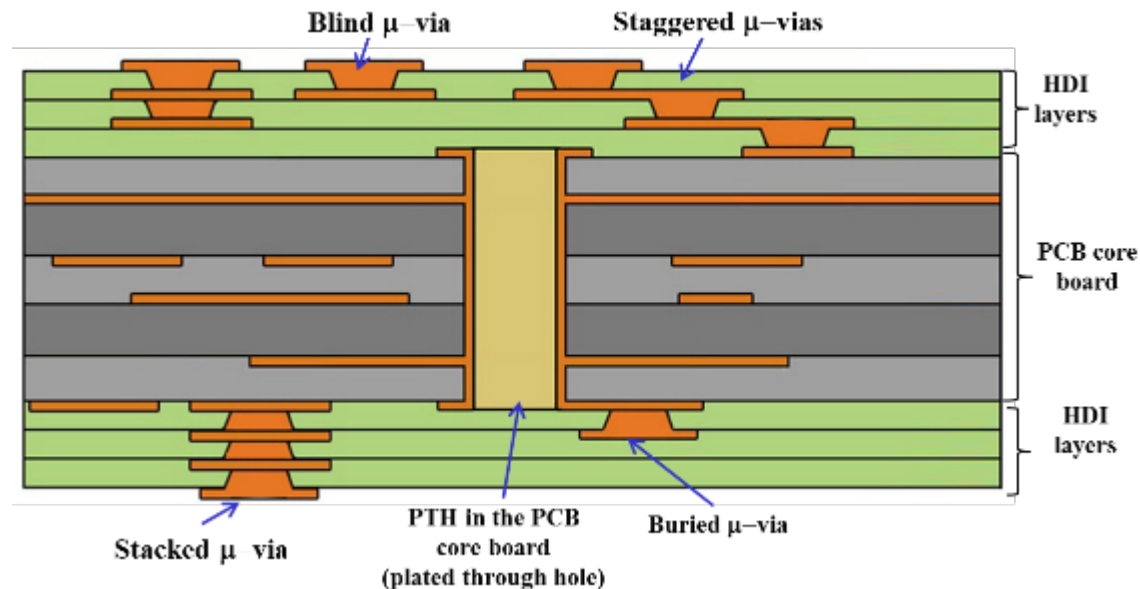
IC packaging feature roadmap with via size, via-pad size, lines and spaces (L/S), and SMT land size*

* - Holden, Happy, J. Andresakis, E. Bogatin, M. Carano, K. Carpenter, K. H. Dietz, M. Laing, C. Vaucher, P. Viklund, and M. Wuensch. "The HDI handbook."

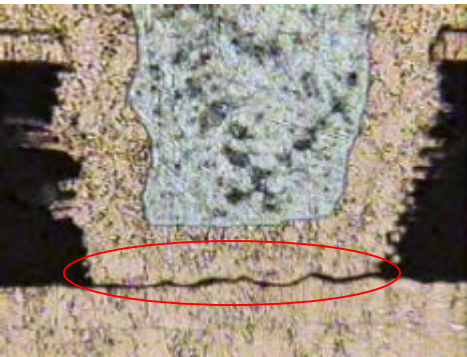
Microvia and HDI Boards



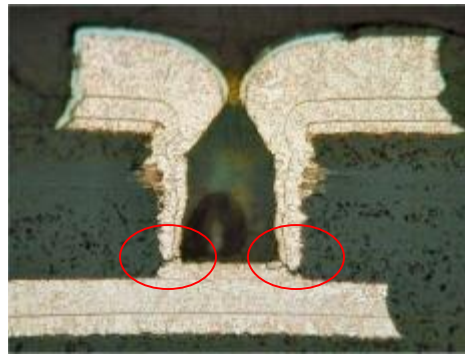
Microvias are blind or buried vias that are equal to or less than $150\text{ }\mu\text{m}$ in diameter and have a target pad equal to or less than $350\text{ }\mu\text{m}$.



Known Microvia Failure Mechanisms



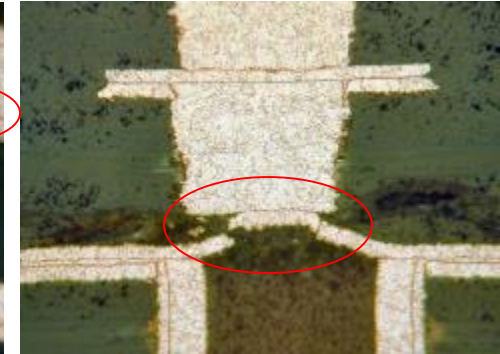
Interfacial separations*



Barrel cracks*

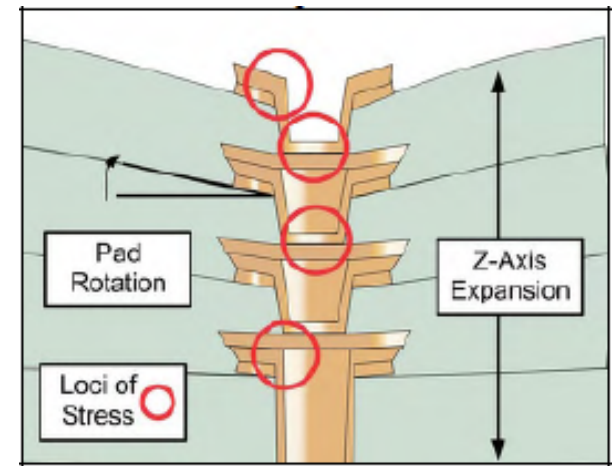


Corner/knee cracks*



Target pad cracks*

- Failures result from the thermomechanical stresses caused by coefficient of thermal expansion (CTE) mismatch between metallization in the microvia structure and the dielectric materials in the board thickness direction (Z-axis) .
- Typical CTE of copper = 17 ppm/°C; CTE of dielectric in Z-axis > 50ppm/°C.



* - B. Birch, "Reliability Testing for Microvias in Printed Wire Boards", Circuit World, Vol 35, No. 4, pp.3 – 17, 2009

Microvia Current Questions

- Determine the effects of processes, materials, design and qualification tests on reliability of microvias
 - Identify failure mechanisms and failure sites of staggered and stacked microvias under varying loads (thermo-mechanical loads).
 - Determine the difference in lifetimes (cycles to failure) between fully and partially filled microvias.
 - Develop a physics-of-failure model to predict the fatigue life of microvias.

Summary

- Risk is a central element of space system development
- Understanding of risk is key to effectively engineering the system
- Lessons learned are at the core of the methodology
- This understanding is used to prioritize resources in development and to convey the status to the project stakeholders
- Confusion between severity of consequence, scenarios, probability and relationship to other categories (safety, technical, and programmatic) can lead to unnecessarily high costs, unbalanced risk, and an overall higher risk posture for a project.

Acknowledgements

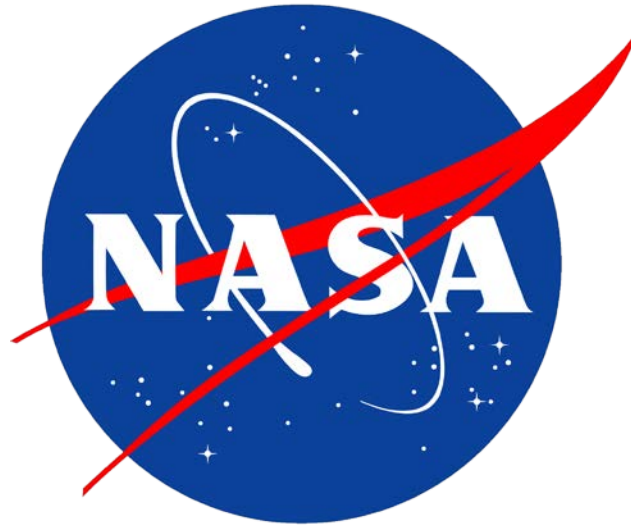
NASA Workmanship
Program

NASA Office of Safety
and Mission Assurance,
Quality Program

NASA Goddard Risk
and Reliability Branch

About Me

- Member of 40 IPC Subcommittees and Task Groups.
 - Chair IPC-7092: Design and Assembly Process Implementation for Embedded Components.
 - Member of A-Team
 - ✓ Microvia Weak Interfaces
 - ✓ J-STD-001
 - ✓ IPC-6017 Specification for Printed Boards Containing Embedded Circuits
- | | |
|-----|--|
| 1. | 1-10C Test Coupon and Artwork Generation Task Group |
| 2. | 3-11 Laminate Prepreg Materials Subcommittee |
| 3. | 3-11G Corrosion of Metal Finishes Task Group |
| 4. | 3-12D Woven Glass Reinforcement Task Group |
| 5. | 3-12E Base Materials Roundtable Task Group |
| 6. | 4-14 Plating Processes Subcommittee |
| 7. | 4-33 Halogen-Free Materials Subcommittee |
| 8. | 5-21F Ball Grid Array Task Group |
| 9. | 5-21H Bottom Termination Components (BTC) Task Group |
| 10. | 5-21M Cold Joining Press-fit Task Group |
| 11. | 5-22A J-STD-001 Task Group |
| 12. | 5-22A-SKELETON J-STD-001 X-Ray Requirements |
| 13. | 5-22ARR J-STD-001 Conformal Coating Material & Application Industry Assessment |
| 14. | 5-22AS J-STD-001 Space Electronic Assemblies Task Group |
| 15. | 5-24B Solder Paste Task Group |
| 16. | 5-32A Ion Chromatography Ionic Conductivity Task Group |
| 17. | 5-32B SIR and Electrochemical Migration Task Group |
| 18. | 5-32E Conductive Anodic Filament (CAF) Task Group |
| 19. | 6-10C Plated-Thru Via Reliab.-Accelerated Test Methods |
| 20. | 7-12 Microsection Subcommittee |
| 21. | 7-23 Assembly Process Effects Handbook Subcommittee |
| 22. | 7-24 Printed Board Process Effects Handbook Subcommittee |
| 23. | 7-24A Printed Board Process Effects Handbook Task Group |
| 24. | 7-31FS IPC WHMA-A-620 Space Electronic Assemblies Addendum Task Group |
| 25. | 7-32C Electrical Continuity Testing Task Group |
| 26. | 6-10D SMT Attachment Reliability Test Methods TG |
| 27. | D-55A Embedded Circuitry Guideline Task Group |
| 28. | B-11 3-D Electronic Packages Subcommittee |
| 29. | D-13 Flexible Circuits Base Materials Subcommittee |
| 30. | D-22 High Speed High Frequency Board Performance Sub-committee |
| 31. | D-24C High-Frequency Test Methods Task Group Frequency-Domain Methods |
| 32. | D-31B IPC-2221 2222 Task Group |
| 33. | D-32 Thermal Stress Test Methodology Subcommittee |
| 34. | D-33A Rigid Printed Bd. Performance Specifications TG |
| 35. | D-33AS IPC-6012 Aerospace Addendum Task Group |
| 36. | D-35 Printed Board Storage and Handling Subcommittee |
| 37. | D-55 Embedded Devices Process Implementation Subcommittee |
| 38. | D-55-AT IPC-6017A A-Team |
| 39. | V-TSL-MVIA-CHEMPR-AT Chemical Processes and Metallurgy A-Team |
| 40. | V-TSL-MVIA-SIMMOD-AT Simulation and Modeling A-Team |



Bhanu Sood, PhD

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