

Threats to Resiliency of Redundant Systems Due to Destructive SEE

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Abstract— Destructive SEE pose serious challenges for the reliable use of COTS devices in space systems. We used system-level modeling to determine SEL rates that would likely compromise system reliability, resilience and capabilities. We then assembled a representative dataset of COTS CMOS parts and used nonparametric statistical techniques to assess the threat posed to redundant systems by destructive SEE.

Index Terms— single-event effects, single-event latchup, reliability estimation, quality assurance; statistical techniques

I. INTRODUCTION

Single-event effects (SEE) pose challenges for use of Commercial Off The Shelf (COTS) parts in high-reliability space systems. Not only are COTS devices usually fabricated with little regard for the SEE susceptibility, the large variety of COTS vendors and parts make it unlikely that space system designers will find data on their part of choice in existing data archives—particularly given the short design cycles for many COTS parts. Testing complex, commercial microcircuits is expensive and time consuming, often requiring sophisticated test equipment, and often, the results will cover only some of the part’s operating state space. These challenges have strained conventional approaches to SEE analysis and mitigation.

In designing reliable hardware despite incomplete understanding of SEE performance, system-level mitigation offers many advantages.[1,2] System-level techniques tend to be “broad-spectrum,” requiring no detailed knowledge of proximate causes of the errors in the system constituents beyond a bound on rate and consequences. One of the most common and powerful system-level approaches has been use of redundancy—that is, instantiation of multiple copies of hardware “units,” and running the same operation on them in parallel with the goal of detecting and correcting errors that occur at the unit level. If the redundancy is truly independent, operation may continue (albeit with reduced capability or resilience) even if a redundant units fails.

Redundancy like this has been more common in aircraft than in space systems, mainly because it is expensive in terms of size, weight and power (SWaP).[3] More commonly in space systems, errors have been mitigated within a circuit or subsystem. However, such internal mitigation usually requires

detailed understanding of the error/failure susceptibilities of parts in the system—e.g. transient duration to determine capacitive filtering or multi-bit upset susceptibility to determine the appropriate error correction codes (ECC). Moreover, miniaturization of microelectronics has decreased SWaP penalties for system redundancy, and system redundancy is effective against a broad range of error and failure modes.

We examine how destructive SEE (DSEE) affect the resilience of a simple redundant model. Rather than examining realistic space systems, we seek to illustrate the sensitivities of this simple system to unit-level destructive and nondestructive SEE (NDSEE). We then summarize recent research and experience with Single-Event Latchup (SEL) susceptibility in COTS Complementary Metal Oxide Semiconductor (CMOS) parts and examine the implications of relying heavily on COTS parts for the resilience of redundant systems. SEL susceptibility in COTS CMOS parts is widespread and widely variable, making it difficult to predict how a given part is likely to perform prior to heavy-ion SEE testing. However, this lack of predictability at the part level is advantageous for modeling SEL at the system level, allowing application of nonparametric statistical techniques and SEL risk to be bounded with some confidence as a function of system complexity (# of susceptible parts, etc.).

II. SIMPLIFIED REDUNDANT SYSTEM WITH REPAIR

We study the simplest model that illustrates the threat DSEE pose to resilience of redundant architectures. This model incorporates three independent, identical “units”—individual instantiations of hardware—performing identical operations in parallel, with the results of these operations voted or compared to detect/correct errors in individual units. We call the three-unit ensemble an “element.” Each unit is susceptible to random non-radiation failures at some low failure rate (e.g. 1 failure in 200 missions for the system) and to DSEE. The DSEE cause permanent failure with a constant rate λ_{DSEE} . The units also experience nondestructive SEE (NDSEE) at rate λ_{NDSEE} . NDSEE knock the affected unit off line for an interval called the repair time, T_R , after which the repaired unit comes back on line. Table I summarizes the states of operation for the element and its constituent units.

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If an error occurs in a unit with rate λ , then the probability of such errors occurring in $N \leq 3$ of the three units in an element during an interval τ is given by:

$$P(N \text{ events}) = \binom{3}{N} P(\tau)^N (1 - P(\tau))^{3-N} \quad (1)$$

where $P(\tau)$ is the cumulative exponential probability of an event within the interval τ . If $\lambda = \lambda_{\text{DSEE}}$ and τ is the mission duration, then (1) gives the probability of N destructive failures during the mission. For $\lambda = \lambda_{\text{NDSEE}}$ and $\tau = T_R$, the refresh time, (1) for $N=1,2$ and 3 gives the probabilities, $P1I$, $P2I$ and $P3I$, or seeing 1, 2 or 3 errors occurring in a single repair interval (INTV). Although T_R is short, making the probability of one or more SEE in that interval very small, there are many repair intervals in a mission. As such, we can represent the intervals as binomial trials. For example, the probability of two NDSEE occurring in one or more of the repair intervals in the mission can be written as a binomial probability—

$$P(2 \text{ outages in an INTV}) = 1 - \text{Binom}(0, N_I, P2I) \quad (2)$$

Table I: Element Operating States due to Errors and Failures

Mission Intvl. \	0 DSEE	1 DSEE	2 DSEE	3 DSEE
0 Errors	Nominal	Perm. Degraded	Perm. Degraded	Failed
1 Error	Temp. Degraded	Perm. Degraded	Outage	Failed
2 Errors	Temp. Degraded	Outage	N/A	
3 Errors	Outage	N/A	N/A	

The probabilities of 1 or 3 outages in some interval during the mission are obtained by substituting $P1I$ or $P3I$ for $P2I$ in (2). Total failure of the element occurs if all three units experience a DSEE (black column on the right in fig. 1). If each of the three units experience a fault (3 NDSEE, 1 DSEE and 2 NDSEE or 2 DSEE and 1 NDSEE), the element experiences an outage. Recovery from such an outage, if possible, would likely take much longer than a single repair interval.

An element may continue to operate after one or two DSEE or NDSEE, but its operation and resilience to additional faults is degraded either for a single repair interval (NDSEE) or permanently (DSEE). This can be particularly important if the redundancy in the system serves multiple purposes—e.g. detection/correction of SEE-induced errors as well as improvement of reliability and availability. The impact of operating in the degraded states (grey) in Table I depends on the criticality of the services the redundant elements were performing and of the phase of the mission when the degraded operation occurs. For example, if the redundancy is used to correct unit-level errors by triplicate voting unit outputs, loss of one unit (absent other mitigation) would result in the loss of error correction, while operating with two units disabled would mean errors could be neither corrected nor detected.

Moreover, while redundancy and repair can significantly improve system reliability, this improvement is not cost free. Repair may require a short, controlled outage of services while all three units are re-initialized and resynchronized. During some missions or operational phases, performance of the primary function may be critical and such an outage may not be

possible. During such phases, there will be no choice but degraded operation until the critical phase has finished.

The non-radiation failure rate provides a natural scale for evaluating the effects of SEE. Figure 1 explores how DSEE failures result in degraded operation over the unit DSEE rates (per mission) that results in element failure with probabilities from 1% to 10% of the nominal non-radiation failure rate—that is from 0.005% to 0.05% per mission. Over this same range, the probability of at least two units lost to DSEE goes from 0.4 to 1.8% and of at least one unit lost from 11% to 22%.

The full study is detailed in a report[4] sponsored by the NASA Engineering and Safety Center (NESC). This study extends the simulations to more complicated systems, including those composed of multiple elements with different susceptibilities to destructive and nondestructive SEE. For this paper, we restrict consideration to the simplest system that illustrates the system-level effects of destructive and nondestructive SEE susceptibilities on a repairable, redundant system—a single element.

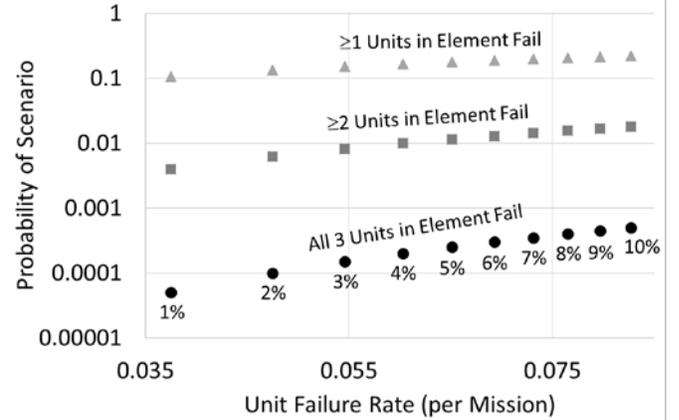


Fig. 1 Although a redundant system may be robust to failure (adding less than 1-10% to the overall random failure rate for the element), the probability that the units constituting that redundant element may fail may be much higher, resulting in degraded resilience or capability, depending on the services the redundancy was performing.

III. SIMULATIONS AND RESULTS

We ran the simulations using both analytical and Monte Carlo methods, looking at how outage probabilities depended on a range of repair times T_R , mission durations and rates for of DSEE and NDSEE. Figure 2 illustrates the basic issue—that susceptibility to DSEE (or any other permanent failure) causes the outage rate to rise nonlinearly with mission duration, with the coefficient of the 2nd order term of a quadratic fit increasing roughly linearly with the destructive SEE rate.

The nonlinearity in Figure 1 arises due to potential loss of redundant units in the element due to DSEE. Even if the system is built with parts immune to destructive SEE, the outage rate curves upward with increasing mission length due to the low rate of random non-radiation. Absent any destructive failures, with all SEE modes being repairable, outage probability would increase linearly with mission length. Outage rates also increase roughly linearly with increasing repair time. These curves are best viewed as outage rates for an ensemble of identical missions, since each unique mission realizes only one outcome, with its own history of DSEE, NDSEE, outages and failures.

In general, for short missions or mission phases (e.g. minutes to hours), failures are unlikely to accumulate sufficiently to affect reliability significantly even for DSEE rates significantly higher than those observed ($\ll 1$ per day for most missions). However, if redundancy in the systems serves more than one function—e.g. detection/correction of SEE-induced errors as well as improvement of reliability and availability—then outages may not be the only concern. For the grey-shaded states in Table I, the system may be operating in a degraded condition, and recovery may require a brief outage for resynchronization as noted above.

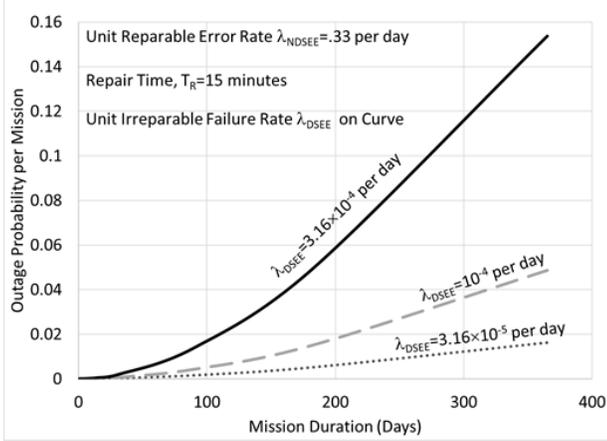


Fig. 2 In redundant systems, DSEE susceptibility causes outage and failure rates to increase nonlinearly, with the nonlinearity scaling roughly as the DSEE rate.

In Figure 3, we presume that the ensemble performs a critical mission function and is required to experience outages with a probabilities ranging from $<5\%$ to $<0.1\%$ during missions of varying length. The shorter the mission, the more failures/outages are driven either by DSEE or NDSEE rates—as indicated by the steepness of the decline in ability to mitigate NDSEE as the DSEE rate approaches a critical level. For longer missions, the accumulating probability of DSEE degrades element resilience, with failure rates being driven by scenarios involving one or two DSEE followed by NDSEE in subsequent operation (indicated by the more rapid onset and shallower slope in the decline of NDSEE mitigation ability especially for 1- and 5-year missions). Moreover, regardless of outage tolerance, DSEE rates near 0.1 per day are problematic even for 1-day missions and rates of ~ 0.01 per day pose a significant threat for missions on the order of 2 weeks. In contrast, if the DSEE rate is $\ll 10^{-5}$ per day, even a 5-year mission stands a reasonable chance of being completed without an outage. If the DSEE rate nears the knee of the curve, this indicates that the system is at risk of exceeding its outage limitation, and it may be appropriate to mitigate some of the error and failure modes internal to the units—DSEE by current limitation or SEL circumvention for example and NDSEE by improving Error Detection and Correction (EDAC), transient filtering, etc.

The results for this idealized system have important consequences given our current knowledge of COTS parts susceptibilities to one DSEE—SEL in Complementary Metal Oxide Semiconductor (CMOS).

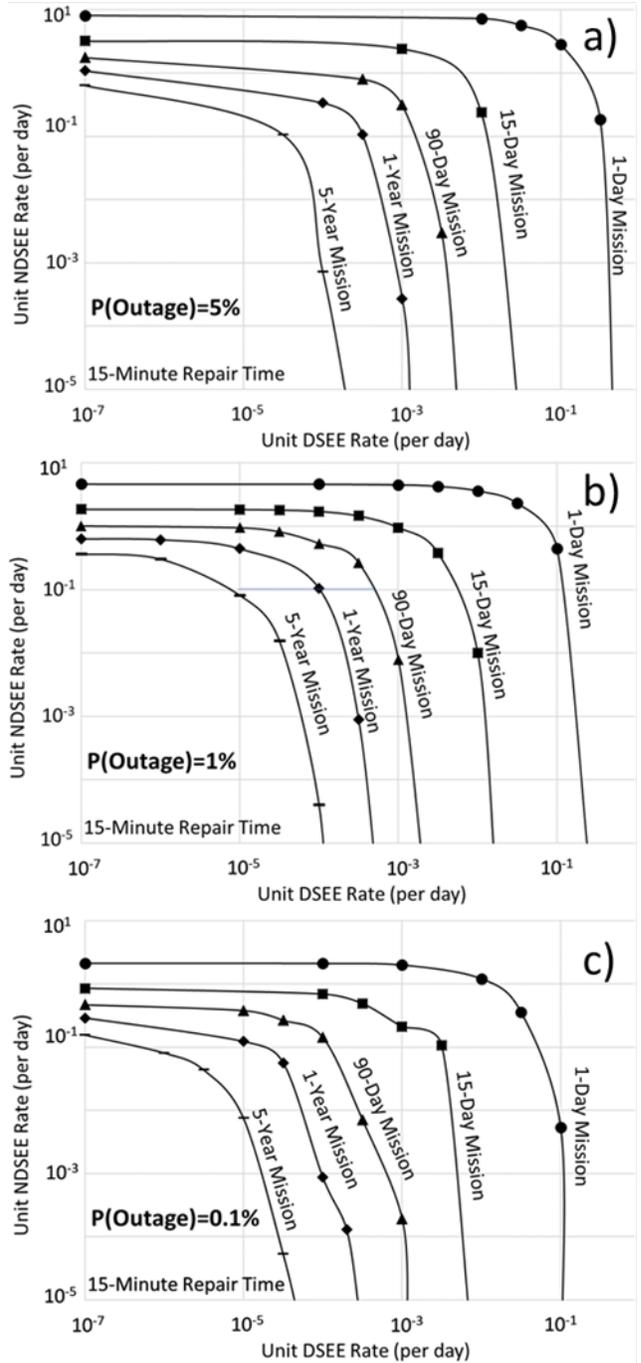


Fig. 3 Since both DSEE and NDSEE rates contribute to outages, for any DSEE rate, there will be a corresponding NDSEE rate that gives rise to a given outage probability rate for a mission of a given length. The contours shrink with both mission duration and decreasing outage tolerance, especially for DSEE rate.

IV. SINGLE-EVENT LATCHUP IN COTS

The previous section revealed that DSEE susceptibilities as low as once in 30 years can undermine system resilience and reliability of even highly redundant systems for missions longer than a year. However, to date, no effective method has been developed for a priori screening of CMOS microcircuits for SEL susceptibility—albeit not due to lack of trying. Ref. [5] looked at what could be discerned about SEL susceptibility from data for similar parts fabricated in the same CMOS process and found that both SEL rates and limiting cross

sections spanned orders of magnitude and that even the distribution of onset LET was broad and possibly bimodal. This work also found that the process in which a part was fabricated was not a reliable predictor for its SEL susceptibility. Ref. [6] found that the deep sensitive volumes associated with many SEL mechanisms make protons an unreliable guide to a part's heavy-ion SEL sensitivity.[6]

Rudakov *et al.*[7] found a similarly muddled picture: a broad range of rates with few handholds to guide *a priori* in part selection. Allen *et al.*[8] conducted go/no-go high-fluence tests with high Linear Energy Transfer (LET) ions on a large numbers of CMOS COTS parts and found about 50% were susceptible to SEL and that SEL was destructive in half of the susceptible parts. Whether the remaining 50% suffered latent damage from the nondestructive events was not determined. Review of several recent reports on SEL susceptibility [8-14] carried out for this work found similar prevalence of susceptibility for a total of 170 part types tested or used on satellite designs since 2015.

The general 50% rate of susceptibility held across many part types—with significant deviations only for Analog-to-Digital and Digital-to-Analog Converter (ADCs and DACs—72% likely to be SEL susceptible) and high-density memories (with no Dynamic Random Access Memories (DRAMs) and only 20% of FLASH memories susceptible. Vendor and fabrication process provided no *a priori* predictive power. Again, roughly 50% of the SEL susceptible parts exhibited destructive failure.

Unfortunately, most SEL data are not sufficiently detailed to reliably estimate rates, since observation of SEL at high LET usually does not allow for enough cross section vs. LET datapoints, and observation at low LET often means the part is abandoned as unacceptable without gathering additional data to determine saturated cross section. For this work, we gathered cross section vs. LET for 19 part types covering several vendors and part functions (see Table II) and fit the data to a standard Weibull form. We required cross sections for at least 4 LETs, (most had 6 or more)—a minimum given the 4-parameter Weibull fit. We endeavored to make this dataset as complete and representative of the sorts of COTS CMOS parts space missions have used over the past 5 years.

We also note that the parameters in the Table II cover similar ranges to those from past studies. Columns in Table 2 from left to right give the manufacturers part number, the manufacturer, the part function and the Weibull saturated cross section σ_{sat} , onset LET (LET_0), and shape and width parameters s and w .

For practical reasons, and because we are mainly concerned with trends generated by our models, we use the Figure of Merit (FOM) method [15] to estimate SEL rates

$$R_{FOM} = C_E \times \frac{\sigma_{sat}}{(LET_{0.25})^2} = C_E \times \frac{\sigma_{sat}}{(LET_0 + w * 0.288^{1/s})^2} \quad (3)$$

where C_E is a constant specific to the radiation environment. FOM rates tend to agree with CRÈME-96 rates unless the limiting cross section is too small ($<10^{-6} \text{ cm}^2$)

Table II: SEL Data for Representative COTS CMOS Parts

Part # [REF]	Mfg.	Function	σ_{sat}	LET_0	Shape	Width
LTC1409 [10]	LTC/ADI	14-Bit ADC	0.000007	55.0	3.1	36
LTC1604 [10]	LTC/ADI	16-Bit ADC	0.000009	53.0	1.5	32
LTC3708 [13]	LTC/ADI	Buck Controller	0.000006	8.1	3.2	18.5
MAX2981 [9]	Maxim	Line Driver	0.000011	12.5	3.4	21
MAIA ROIC [14]	SMC/ASIC	Detector Read-out IC	0.000065	20.5	1.75	53.3
AD7714 [9]	ADI	24-bit ADC	0.00014	26.5	1.6	90
TP551200RDC [13]	TI	Regulator	0.000036	10.7	2	31.3
LTC2271 [12]	LTC/ADI	16-Bit ADC	0.000020	12.5	5.2	10
AD7609 [9]	ADI	Data Acq. Sys.	0.00002	3.5	1.5	21
LTC2502 [9]	LTC/ADI	Op. Amp.	0.00013	7.0	1.5	53
ADS8320 [13]	TI	16-Bit ADC	0.000068	17.0	4.8	6
93LC96BT [9]	Microchip	EEPROM	0.000250	9.5	2.1	31
LTC1595 [9]	LTC/ADI	16-Bit ADC	0.00012	8.2	3.3	14.6
SIG60 [9]	YAMAR	XCVR	0.00112	11.7	2.5	25.5
AD5328 [11]	ADI	12-bit DAC	0.00044	0.8	3.8	22
TMS320F2906 [9]	TI	DSP	0.019	17.5	4.6	26
MAX2992 [9]	Maxim	XCVR	0.0070	6.8	3.3	18
dsPIC30F6014A [11]	Microchip	Micro-controller	0.0616	3.1	2.4	23
ADV212 [12]	ADI	Vid. Codec	0.065	0.2	2	16

Analysis of scatterplots and correlation coefficients (CC) revealed no strong relationships between the different parameters (see Table III). Nor were any trends with vendor or process evident in the fit parameters. Figure 4 histograms SEL rates estimated for Geostationary orbit for parts in Table 2 using both the FOM (blue) and CRÈME96 methods (orange—assuming 10 μm charge collection depth and 100 mils Al equivalent shielding). As can be seen, the two methods agree well except for parts with $\sigma_{sat} < 10^{-6} \text{ cm}^2$, where FOM is known to overpredict SEE rates. This extends the CRÈME96 rate distribution to the left, but as shown in Fig. 3, SEL rates below $\sim 10^{-5}$ per day do not drive system outage or reliability in most systems.

Table III: Correlation Coefficients for SEL σ vs. LET Fit Parameters

	σ_{sat}	LET_0	s	w
σ_{sat}	X	X	X	X
LET_0	-0.31	X	X	X
s	-0.10	-0.09	X	X
w	-0.19	0.33	-0.58	X

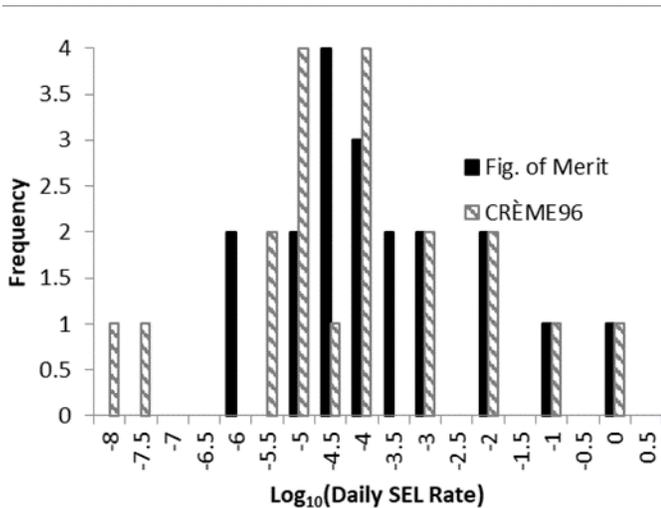


Fig. 4 SEL rates for a representative selection of 19 COTS CMOS parts spans over 7 orders of magnitude and may have indications of bimodality. The rate distribution estimated with the Figure of Merit method agrees moderately well with CRÈME96 estimates down to $\sim 10^{-5}$ SEL per day—below which the DSEE rate affects element resilience to only a limited degree in Fig. 3.

V. CAPITALIZING ON LACK OF CORRELATION

Although the absence of useful correlations or relations precludes prediction of SEL performance for any particular part, the same lack of restrictions presents an opportunity to make general observations about SEL susceptibility in systems using COTS parts. Since there are no useful correlations to restrict associations of any one Weibull fit parameter with any other, a bootstrapped distribution based on rates determined by the 130,321 permutations of fit parameters for the 19 parts in Table II replaces the sparse histograms in Figure 4 with a distribution of SEL rates that is much closer to continuous and therefore easier to use for assessing the susceptibilities of simulated systems. To ensure that the distribution is not overly conservative, we censor the upper tail at the value of the highest SEL rate in Figure 4—which removes only the highest 331 entries, or 0.25%. (Figure 5 shows the resulting quantile plot for both the original data from Figure 4 and the bootstrapped distribution, as well as the corresponding probability density function—pdf—as an inset.) Because NDSEE resilience is driven by devices with SEL rates exceeding 10^{-5} per day, where FOM and CRÈME96 rates generally agree, use of FOM rates in the subsequent analysis does not affect the results.

The most notable characteristics of Table II and of Figures 4 and 5 is the significant probability of COTS parts with high SEL rates and the bimodality of SEL rates—suggested in Figure 4, but clear in both the pdf and cumulative distributions in Figure 5. As such, units fabricated with more than a few COTS parts could have SEL susceptibilities that compromise the element’s ability to mitigate NDSEE. We define the ensemble as compromised when the NDSEE rate it can reliably mitigate decreases by $\sim 10\times$ from that for negligible SEL susceptibility, (the “knees” of the curves in Figure 3). The SEL rate where this occurs decreases in a nearly linear fashion with mission duration. Figure 6 shows the probability that a COTS part will not significantly compromise NDSEE mitigation if COTS SEL susceptibility follows the curve in Figure 5.

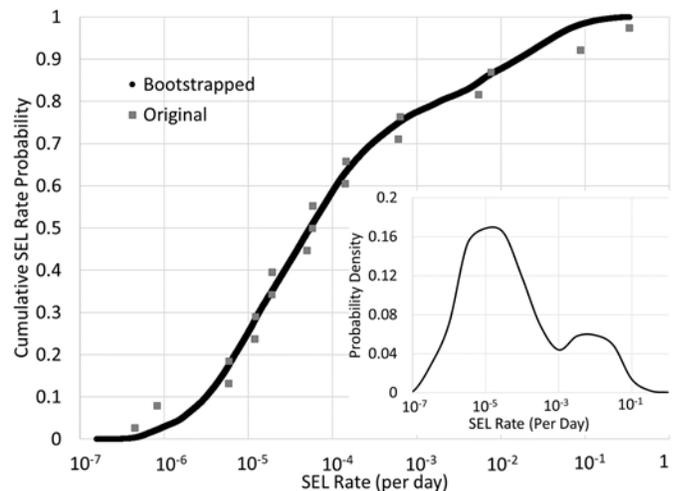


Fig. 5 The lack of correlation between parameters of Weibull fits to σ vs. LET for parts in Table II and Fig. 4 means no one combination is more likely than any other. Under such circumstances, one can nonparametrically “fill in” the rate distribution by bootstrapping. The resulting bootstrapped distribution yields a similar rank plot to the parts in Table II/Fig. 4, but much denser. As a result, features like the bimodality suggested in fig.3 are revealed much more clearly, and the bootstrapped distribution makes it easier to assess the impact of real CMOS COTS parts on element reliability and resiliency.

VI. DISCUSSION: SEL THREAT AND REPRESENTATIVE DATA

The analysis above suggests that SEL in COTS CMOS poses a significant threat to reliability, and that the greatest threats arise from parts in the upper mode in the pdf in Figure 5. This and the lack of screening techniques for SEL susceptibility short of heavy-ion testing pose a significant obstacle to reliable use of COTS CMOS parts in space systems. Thus, it is important to validate the assumptions that feed into the distributions illustrated in Figure 5—mainly that fit parameters are uncorrelated and the selection of parts in Table II.

Not only do the correlation coefficients in Table III reveal no significant correlations between Weibull fit parameters, examination of scatter plots similarly finds no correlation. Moreover, the strongest correlations either have little influence on SEL rate (e.g. that between w and s), or they would tend to increase rates (e.g. negative correlation between LET_0 and σ_{sat}). A strong correlation would require a more sophisticated analysis reflecting this relationship. For example, a Markov Chain Monte Carlo (MCMC) would allow distributions of, for example, onset LET, that depended on the value of saturated cross section selected. We conclude based on the lack of correlation seen here that such techniques are not needed.

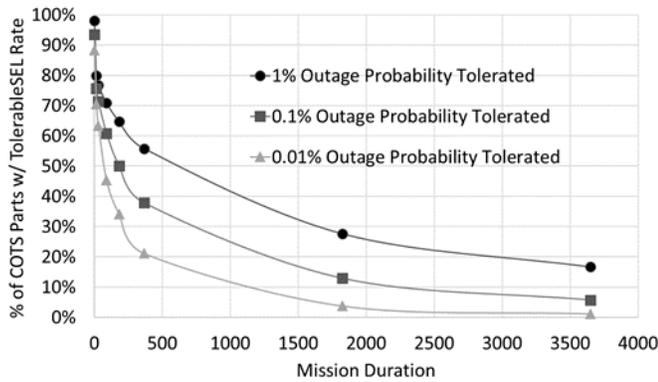


Fig. 6 As mission duration increases, parts with lower SEL rates impact the ability of redundant elements to mitigate outages. The lower the requirement, the more rapid the decrease in the proportion of parts with tolerable SEL rates.

Potentially more significant is the selection of parts used in the analysis—particularly the Microchip dsPIC30F6014A and Analog Devices ADV212, which have SEL rates 11.5 and 44 times the third highest rate). To assess the degree to which these results are driven by these two parts, we repeated the analyses, omitting the ADV212, then the dsPIC30F6014A, and finally both. As expected, omission of these worst-case (WC) parts shifts the cumulative distribution for SEL rates to the left and reduces the upper mode for the pdf, but only slightly. In particular, whether one omits the WC or 2nd WC part makes little difference, with the SEL rates differing by less than 15% compared to the 19-part distribution up to the 99% CL and by less than 36% even for the worst-case rate. Even omitting both WC parts results in SEL rates that differ by less than a factor of 10 compared to the case for all 19 parts shown in Fig. 5.

Comparison to the analysis of Rudenkov *et al.*[7] also provides a way to assess whether the data used to generate Fig. 5 are representative of SEL susceptibility in commercial CMOS. Rather than looking in detail at fit parameters for recent vintage parts, ref. [7] attempted to amass as large a selection of commercial CMOS parts as possible and examine the distributions of the two most important determinants of SEL rate (LET_0 and σ_{sat}) for a large number of part types. This work found that of the 68 part types for which die area was determined, just over 20% had SEL limiting cross section exceeding 5% of die area, with the largest observed being about 14% of die area. (For comparison, the ADV212 σ_{sat} exceeded 10%.) Similarly, roughly 24% of devices in [7] exhibited SEL susceptibility with onset LET less than 12 MeVcm²/mg. Taken together, these results suggest that at least 5% of the parts examined by Rudenkov *et al.* would have fallen into the upper mode of SEL sensitivity in Figures 5 and 7. Moreover, the dataset in [7] excludes ADCs and DACs, which, as noted above, are about 1.5 times as likely to be SEL sensitive as other CMOS parts.

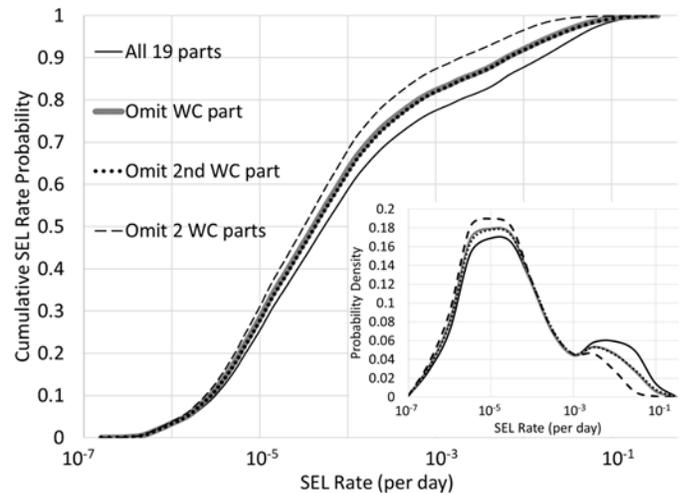


Fig. 7 The significant probabilities of high SEL rates are not driven solely by the worst-case parts (ADV212 and dsPIC30F6014A). Omitting these parts does move the distribution to the left and reduces the proportion of parts in the upper mode of the pdf. However, the 90% CL rate remains well above levels that could compromise system reliability for missions as short as a few months, as indicated in Fig. 3.

Given these considerations, the 19 parts used for the current analysis seem to be fairly representative of the population of commercial CMOS, although they may exaggerate slightly the size of the upper mode in figure 5. Whether this is true, and any remedies needed would both be resolved by adding more parts as they become available.

VII. ION LET AND TEST EFFICACY

The foregoing analysis indicates that the threat from SEL in commercial CMOS parts arises less due to gradual accumulation of multiple parts with small but finite SEL rates than from the non-negligible probability of including one or more highly susceptible parts (those from the upper mode in Figures 5 or 7). This has important implications for mitigating the SEL threat in spacecraft designs. First, it emphasizes the importance of heavy-ion SEL testing to ensure detection of the few parts that pose the greatest risk. SEL current-limiting and power cycling can concentrate on high-SEL-rate parts that are essential to the design and identified by testing. However, identifying the parts with the highest SEL rates means developing test and analysis methodologies that apply even though onset LET is multimodal and σ_{sat} is not only multimodal but also spans several orders of magnitude.

To better understand SEL test efficacy, we look at LET dependence of SEL by combining the dataset used here with that of Rudenkov *et al.* shown in his Figure 4 and present the resulting data as a quantile plot rather than a histogram (black, solid curve in Fig. 8). Because our requirement of cross section measurements for ≥ 4 LETs prevents use of data with very high LET_0 , we restrict ourselves to the data in [7] with $LET_0 \leq 55$ MeVcm²/mg (omitting <12% of data in [7]). Unfortunately, the authors of [7] could not make the raw data available due to nondisclosure agreements. Instead, to convert the data from histogram format to a quantile plot, we generated data randomly distributed with equal probability replicating the contents of each bin in Fig. 4 of reference [7]. This generates a quantile plot that is easier to combine with new data and smoother than

would result from the histogram bin contents, but still consistent with the information in the original data. Fig. 8 also shows the quantile plot vs. LET₀ for parametric combinations from Fig. 4 yielding rates exceeding 10⁻² and 10⁻⁵ SEL per day.

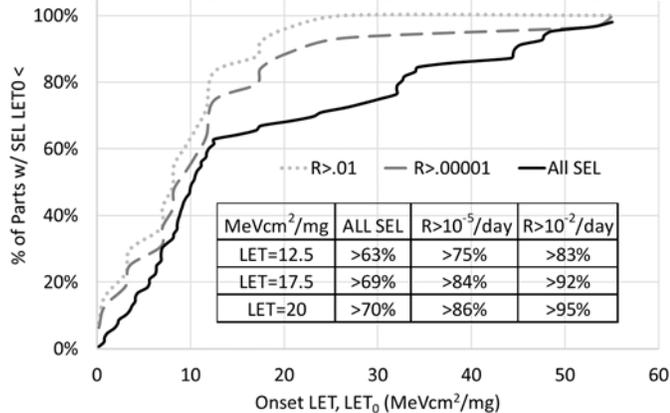


Fig. 8 The percentage of parts having LET₀ below a given value based on historical data serves as a guide to the proportion of SEL susceptible features that would be revealed by a high-fluence test with ions exceeding that LET. Moreover, if the primary concern arises from parts with anomalously high LET, the higher the threshold of concern, the more likely a test to a given LET would detect a SEL mode of concern if it were present.

The curves in Fig. 8 can be viewed as measuring the likelihood that a test with an ion of a given LET would detect any SEL susceptibility (solid line labeled All SEL) an SEL susceptibility resulting in a GEO rate exceeding 10⁻⁵ per day (dashed line labeled R>.00001) and an SEL with rate exceeding 0.01 per day (dotted line labeled R>.01).

The table inset in Fig. 8 illustrates the effectiveness of ions of varying LET in detecting all SEL modes as well as those with rates exceeding 10⁻⁵ and 10⁻² per day. The data at LET~12.5 MeVcm²/mg is illustrative. Tests with a sufficiently high fluence of ions with LET above this level would detect >63% of all SEL modes, >74% of modes occurring more often than once in 10⁵ days and over 83% of modes occurring more often than once in 100 days. Because roughly half of proton-Si recoil ions have LET in the 10-12 MeVcm²/mg range, it is tempting to conclude that a proton test with sufficient fluence would be an effective SEL screen. Unfortunately, proton recoils often have ranges significantly less than the depth of an SEL sensitive volume, and achieving a sufficiently high recoil ion fluence for a good SEL test can result in TID levels of hundreds of krad(Si), often exceeding the radiation capability of the part. In general, as discussed in detail in reference [6], protons will be an effective screen for SEL only if the part is sufficiently hard to TID and the SEL SV is known to be less than ~5 μm.

Independent of whether protons are an appropriate probe for SEL susceptibility, understanding how test efficacy increases with ion LET is advantageous. In tests with ultra-high energy ions, as at the NASA Space Radiation Laboratory (NSRL), ion LET is much lower than that at more commonly used facilities. For instance, the incident LET for Au at NSRL is 15 MeVcm²/mg versus >80 MeVcm²/mg at the Texas A&M University Cyclotron Institute (TAMU). Fig. 8 provides some assurance that even if testing a circuit board with multiple parts having varying overburden, a test with Au would detect >85% of all SEL modes having a GEO rate 0.01 per day and 77% having rates exceeding 10⁻⁵ per day.

VIII. SIMULATION AND SENSITIVITY

The quantile plots in Figs. 5 and 7 are useful for simulations exploring whether a design may be compromised by SEL. Sensitivity results such as those discussed in sections III and IV indicate the threshold values where destructive SEE rates begin to compromise system performance and resilience. The quantile plots in Fig. 4 or 8 allow the SEL rate for an arbitrary CMOS part to be bounded with any desired confidence. For example, >90% of parts are likely to have SEL rates in GEO less 0.015 events per day (or 0.006 per day if one uses one of the curves in Fig. 8 with only one of the two worst case parts in Table II).

More interesting is estimating unit SEL rates. For this exercise, we start with the observation that 50% of commercial CMOS parts are SEL sensitive (or 72% for ADCs and DACs). In half of those susceptible parts, the SEL is destructive. Moreover, for this analysis, we have limited our consideration to parts with SEL onset LET < 55 MeVcm²/mg, or ~88% of all SEL susceptible parts per [7]. Thus, the potential SEL rates represented in Figs. 5 apply for ~2 of 5 (44%) commercial CMOS parts, or ~1 in 5 latching destructively. Rather than apply a single bounding rate to all susceptible parts, we randomly assign rates from Fig. 5 to 44% of the CMOS parts according to the distribution in Fig. 5.

For this exercise, we assume that the application is a cubesat intended for a 300 km altitude, 30° inclination orbit, for which SEE rates are ~45x lower than those in GEO (note, that since we are using FOM rates, the only change required is the constant corresponding to the environment). We performed a Monte Carlo simulation of 10000 identical systems, examining changes in confidence that the system will meet design requirements as the # of COTS CMOS parts (a proxy for system complexity) increased from 10 to 50. The pdf in Fig. 9 shows that as the count of potentially susceptible parts increases, the influence of the lower mode in Fig. 5 diminishes, and the system response is dominated by a few parts with high rates. Moreover, the distribution of system rates narrows, with the coefficient of variation (ratio of standard deviation to mean system SEL rate) decreasing from ~1.76 to ~0.55.

Combining the results in Fig. 3a with those in Fig. 9, roughly 85% (85% confidence) of systems with up to 10 COTS CMOS parts randomly chosen would meet the requirement of <5% chance of an outage for a 90-day mission. That confidence decreases to 26% for systems with 50 potentially susceptible parts. If one restricts the concern to parts with destructive SEE modes (with nondestructive SEL mitigated—e.g. power cycled and current limited—internal to the unit) (~22%), the corresponding confidence levels are 93% and 52%. Figure 10 illustrates the dependence for all SEL and destructive SEL. Although this analysis is carried out at a high level of abstraction and cannot predict the SEL rate for a specific system, the trends it reveals provide important information for the designer:

- 1) indicating when the system has a reasonable probability of meeting requirements and when SEL testing or internal mitigation (e.g. current-limiting and SEL circumvention) may be needed to reduce risk to acceptable levels;
- 2) showing the different levels of risk associated with

- Systems with COTS—where a few COTS parts augment performance of a mainly space-grade system
- Systems of COTS—where COTS parts predominate, but mitigation can be implemented if required
- COTS Systems—where the system is not only made mainly with COTS, but the configuration is not under control of the user, so mitigation is not feasible

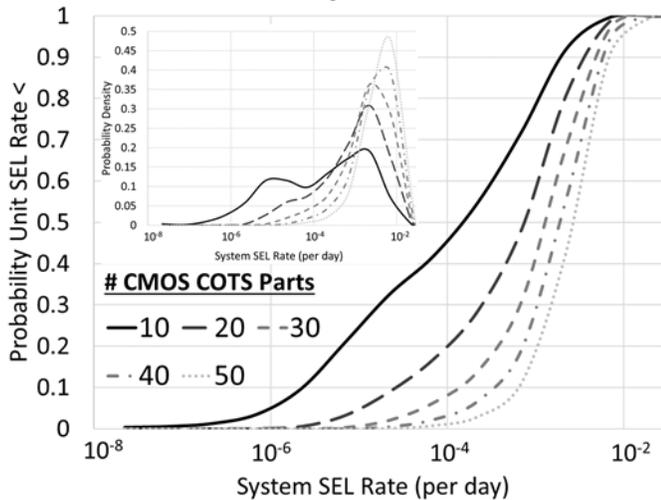


Fig. 9 For low part counts, the bimodal nature of the part SEL distribution is evident in the unit SEL rate distributions, while for higher part counts, the distribution narrows and the rate is dominated by the upper mode in the part SEL distribution. Rates are for a cubesat at altitude 300 km, inclination 30°.

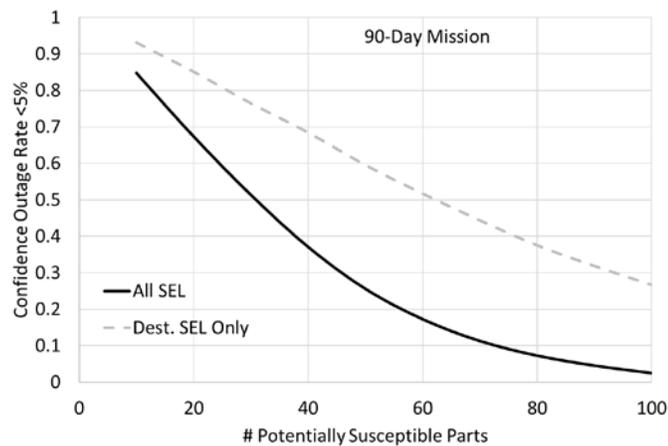


Fig. 10 For a 90-day mission at 300 km, 30° inclination, the confidence one can achieve an outage rate <5% decreases steadily as the number of potentially susceptible parts increases. However, if nondestructive SEL can be handled internal to the unit (e.g. by current limiting and ability to power cycle), the decline in confidence is much less rapid.

It may be possible to carry out a more specific analysis if the die area of each COTS CMOS IC is known. Unfortunately, we know die areas for only a few of the parts in our sample. However, [7] has published a distribution of the ratio of σ_{sat} to die area in the form of a histogram (their Fig. 3), and previous studies [5] have yielded results consistent with theirs. Combining these sources and following a procedure similar to that outlined in section VII for LET_0 results in Fig. 11. Unfortunately, normalizing σ_{sat} to the die area does not improve

the distribution significantly, as the ratio of σ_{sat} to die area still spans more than 3 orders of magnitude [5,7] from <0.01% to >10%, with suggestions of multimodality. Instead, it allows us to model SEL cross sections and rates consistent with known die areas for parts actually used in our system.

Using the distribution for σ_{sat} /die area in Fig. 11, we proceed in a manner similar to that which generated Figs. 9 and 10, with a few modifications. Each part in the analysis is assigned a die area and random numbers determine the percentage of the die area susceptible to SEL. Then we generate another random number to select the denominator for the FOM SEE rate:

$$(LET_{0.25})^{-2} = (LET_0 + w * 0.288^{1/s})^{-2} \quad (4)$$

Fig. 12 shows the distribution of $(LET_{0.25})^{-2}$ determined in the same manner as Fig. 5 by bootstrapping the 3 fit parameters LET_0 , w and s (e.g. omitting σ_{sat}).

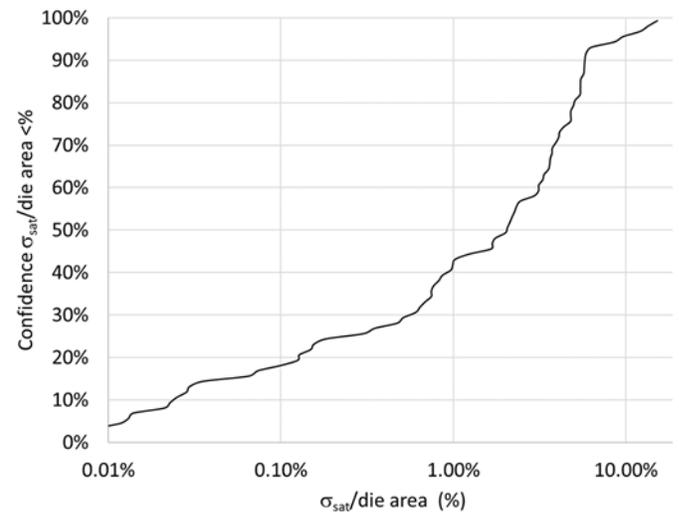


Fig. 11 Quantile/confidence plot of % die area susceptible to SEL at saturation (σ_{sat} /die area) incorporating data from [7], [4] and the current work.

We assume the same environment used to generate Figs. 9 and 10 (300 km altitude, 30° inclination). Each COTS CMOS IC in the study is assigned an area that remains constant. In one scenario, the IC areas are assigned randomly over a range from ~0.002 to 0.4 cm², averaging ~0.2 cm² (consistent with typical ranges for SOTA COTS CMOS parts). This is called the Uniform Density case. In the other scenario, the die are mostly small—typical of ADCs, DACs, amplifiers, etc.—but with about 20% having areas >0.1 cm² (average ~0.06 cm²). We randomly assign % die areas for SEL cross section from Fig. 11 and for $(LET_{0.25})^{-2}$ from Fig. 12. As we did for Figs. 9 and 10, we also treat the case where all SEL susceptible die pose a threat (44% of all COTS CMOS—labeled ALL SEL) and that where only destructive SEL (~22%) pose a threat (labeled Dest. SEL). Fig. 13 illustrates the 90% WC system SEL rate resulting from 10000 Monte Carlo simulations as the number of COTS CMOS parts in the system increases for each of these 4 scenarios. Also shown are the unit SEL rates that compromise system resilience (NDSEE rate on contour decreased by 10x) determined from 3 scenarios in Fig. 3. The advantages of being able to recover from nondestructive SEL, and of limiting both the number and die areas of potentially vulnerable parts are evident.

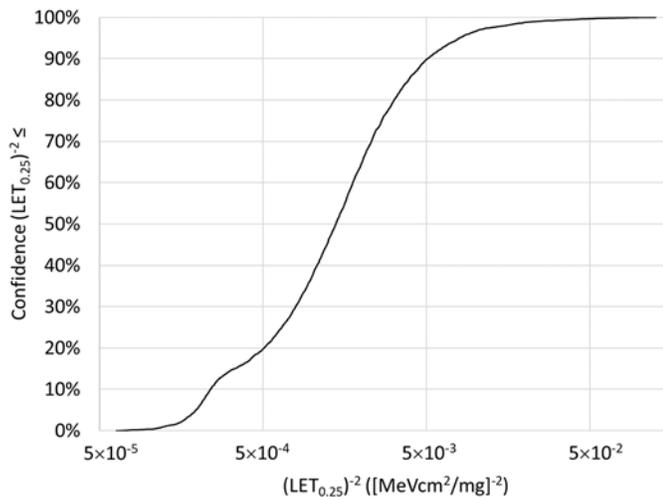


Fig. 12 Confidence/quantile plot of inverse square of LET0.25, the LET where the cross section reaches a quarter of σ_{sat} , which when multiplied σ_{sat} yields the FOM, to be used in conjunction with Fig. 11 for system simulations where die sizes or σ_{sat} values are known.

IX. DISCUSSION AND CONCLUSIONS

SEL susceptibility has been a formidable obstacle to reliable inclusion of COTS CMOS parts in spaceflight applications. Not only are a high proportion of such parts SEL susceptible, SEL rates for susceptible parts span six orders of magnitude. Attempts to correlate susceptibility with vendor, fabrication process and part function[5,7] have yielded little guidance for reducing SEL risk, and testing with protons has not proven reliable due to the low cross section for proton recoil ions and the short ranges of proton recoil ions coupled with the deep sensitive volumes associated with SEL.[6] To date, heavy-ion testing is the only reliable method for estimating SEL susceptibility of a COTS CMOS parts.

Here, we instead looked at SEL risk at the system level. We have applied system-level reliability modeling to estimate the rates where destructive and nondestructive SEE rates begin to have a significant effect on system reliability, resilience and performance of a highly redundant, simplified system.

Knowing the range of rates that threaten system reliability, we then we looked at SEL susceptibilities of COTS CMOS parts. Unfortunately, the multimodality and broad range of SEL rate and fit parameter distributions are ill suited to standard parametric statistical analysis. However, the very characteristics that frustrate parametric modeling render the situation well suited to nonparametric analysis techniques. As such, we derived a prior probability distribution for SEL rate by bootstrapping the minimally correlated Weibull fit parameters to estimate FOM rates for each permutation. Although the bootstrapped distribution contains no more information than the original data, it clearly reveals characteristics such as the bimodality in Figure 4 and makes it easier to determine the proportion of parts that pose a reliability threat.

One of the most significant findings is that a high system SEL rate is more likely to arise from one or more high-SEL-rate parts than from gradual accumulation of parts with lower SEL rates. This again emphasizes the importance of detecting high-rate parts before they work their way into the design through heavy-ion testing. The results in Figs. 3(a)-(c) illustrate that for relatively short missions, the level of concern for the unit SEL

rate is on the order of 10^{-4} or even 10^{-3} per day, using tolerance (from 0.1-5%) for outage as a driving requirement. For missions longer than a few days, even unit rates as low as 10^{-5} per day can be problematic. An advantage of the bootstrap procedure used here is that when the range of concern for system SEL rates is known, the fit parameters and the interrelationships thereof associated with those rates can be investigated. For example, section VII discusses the dependence of different SEL rate ranges on LET_0 and its importance for potential screening through heavy-ion testing. The analysis reveals that high-LET ions may not be required to achieve adequate confidence in success for short missions, simplifying issues associated with tests using ultra-high energy ions to ensure penetration of package overburden.

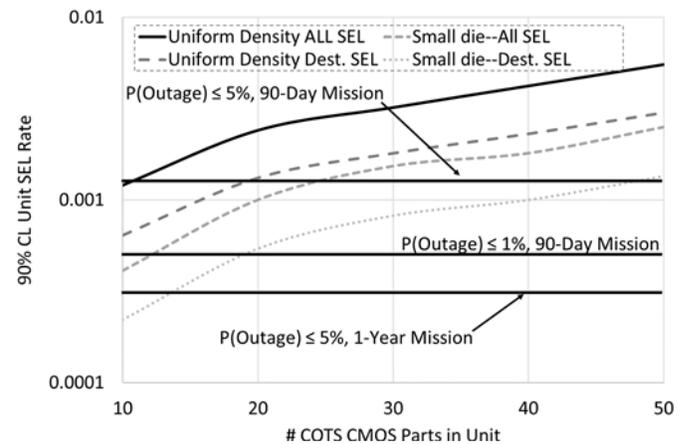


Fig. 13 90% WC unit SEL rates estimated under 4 scenarios (described above) versus unit COTS CMOS part count for the same environment as Fig. 9 (300 km altitude, 30 degrees inclination). Also shown (solid black horizontal lines) are the SEL rates of concern for various allowed outage requirements and mission durations determined from Fig. 3.

The analyses in section VIII illustrate the advantages of treating SEL at the system level. Not only do system-level simulations reveal the rates that pose concerns for the system, a system approach allows consideration of the class of COTS CMOS parts in aggregate rather than by the piece part. The effect of this can be seen in Fig. 9, where for small part counts, the response is bimodal, reflecting the underlying bimodality in Fig. 5. However, as the count of COTS CMOS parts increases, the upper mode in the rate distribution becomes dominant and the distribution of rates narrows. This indicates that the rates for more complex hardware are less variable and simulated rates are more likely to conform to actual rates. The two simulation techniques in this section also present different options for modeling the system—based on potentially susceptible part count or the sum of die areas of potentially susceptible parts. The improved result for systems that can recover from nondestructive SEL illustrates the potential value for treating these modes within the unit, as well as the benefit that would accrue if the family of parts from which the design is constructed starts with a lower overall failure rate.

The techniques used here are generally applicable. The system-level modeling applies for other destructive failure modes. The nonparametric techniques such as bootstrapping and Markov Chain Monte Carlo are well suited to failure modes such as SEL where relevant parameters cannot be reduced to compact, well-behaved distributions. Moreover, the approach is

not unreasonable, since the bootstrapped distributions are produced starting with parametric fits to real SEL cross section data.

The use of Figure of Merit error estimates is not essential to the method. In principle, rates could be estimated for all parametric combinations in the bootstrapped distribution using a standard Rectangular Parallelepiped (RPP) based routine such as CRÈME-96, especially if using a stand-alone version of the routine. In our case the FOM approach is justified, because the results are driven by combinations having $\sigma_{\text{lim}} > 10^{-4} \text{ cm}^2$ (where FOM rates agree well with RPP rates), and in any case the important results depend on the trends identified in the systematic analyses rather than specific numerical values. The FOM approach also makes it easy to adapt rates estimated for one environment to another by multiplying by the ratio of C_E values in eq. 3.

Limitations of these methods are most likely to arise if the dataset of susceptible parts is not representative. This could arise in several ways. For our dataset, the requirement that the σ_{SEL} vs. LET curve include at least 4 points (6 preferred) so that a valid Weibull curve can be estimated could bias the data set toward lower onset LETs. However, comparison of LET dependence for this work with that for other works [5,7] suggests that the bias is small (~12%), and that it is reasonable to interpret the current results as being valid if we consider parts having $\text{LET}_0 > 55 \text{ MeVcm}^2/\text{mg}$ as being effectively immune in terms of driving unit failure rates. Bias could also arise as parts in the database fall out of use and are replaced by new ones. We have sought to avoid this bias by limiting ourselves largely to results reported in recent publications or used for recent satellites. It is also possible that devices with particularly high σ_{lim} or low LET_0 will be overrepresented in the literature because their novelty makes them more likely to be reported. The analysis in section IV illustrated that such effects, if present, likely do not drive the results presented here, and the similarity between our data and that in [7] suggests this bias is likely minor.

In any case, the remedy to any of these biases is adding more data to the database. Moreover, since it is unlikely that adding more data will significantly change the notable characteristics of the database—particularly the lack of compactness, multimodality, etc., the same techniques developed here will be well suited to making sense of the resulting data.

In developing new systems, these techniques provide a way of assessing when the risk posed by the COTS CMOS parts in the system begin to pose an unacceptable risk to meeting requirements and when testing or mitigation internal to the unit (e.g. current limiting, the ability to power cycle and recover from a nondestructive SEL, SEL circumvention for critical parts, etc.) is desirable. It presents a self-consistent method for assessing the impact of potentially SEL susceptible parts and for comparing robustness to these effects for different design strategies or different categories of parts (e.g. automotive vs. broader COTS).

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