National Aeronautics
and Space Administration

Wide Bandgap Power – SiC, GaN – Radiation Reliability

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To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020

Outline

- **Overview**
  - Bandgaps: the simple explanation
  - Wide-bandgap (WBG) technology advantages & applications
  - Inherent radiation hardness from WBGs
- **Single-Event Effects in Discrete Silicon Power Devices**
  - Single-event gate rupture (SEGR) in power MOSFETs
  - Single-event burnout (SEB) in power MOSFETs and diodes
- **SiC and GaN Power Device Heavy-Ion Effects**
  - SiC Diodes and MOSFETs
  - GaN High Electron Mobility Transistors (HEMTs)
- **Radiation Hardness Assurance Challenges**
  - Test methodology
  - Rate prediction and reliability uncertainty
  - Beyond radiation effects: additional reliability challenges
- **A Look to the Future: Ga_2O_3 Ultra-WBG Power Technology**

SEB in SiC Schottky Diode

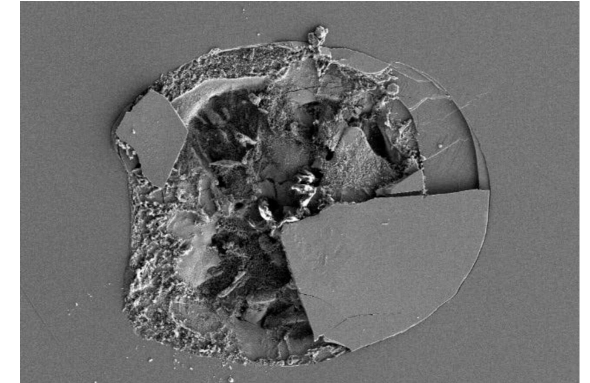
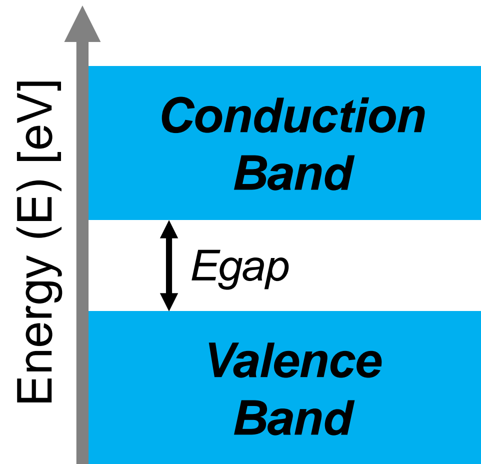


Image: A. Woodworth, NASA

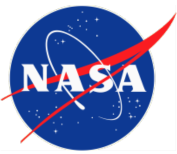
Wide-Bandgap Technology Overview: What's a Bandgap? (Simply Speaking)

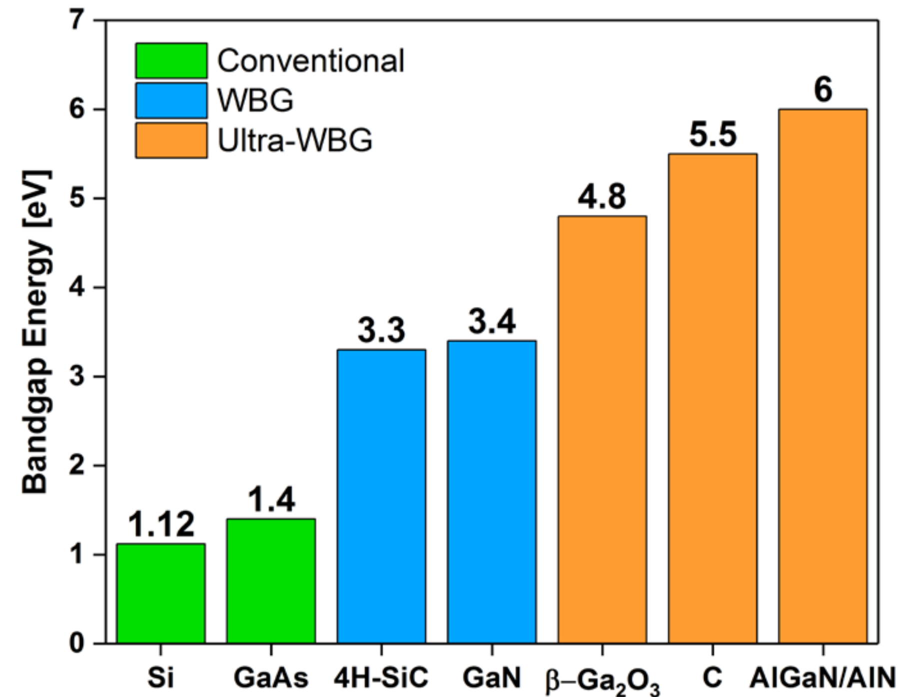


- **As atoms come together to form a crystal, their electron shells form bands:**
  - **the highest-energy band containing electrons at 0 K = *Valence Band***
  - **the next highest energy band = *Conduction Band***
    - Electrons in the conduction band (and subsequent holes in the valence band) are able to move freely about the lattice and thus conduct current
- **In order to become conducting, an electron must have enough energy to jump the gap**
  - **this jump can be assisted by traps, or energy states, located in the band gap**

Wide bandgap materials have different electrical properties than conventional bandgap materials (e.g., Si) due to their different band structure and band gap

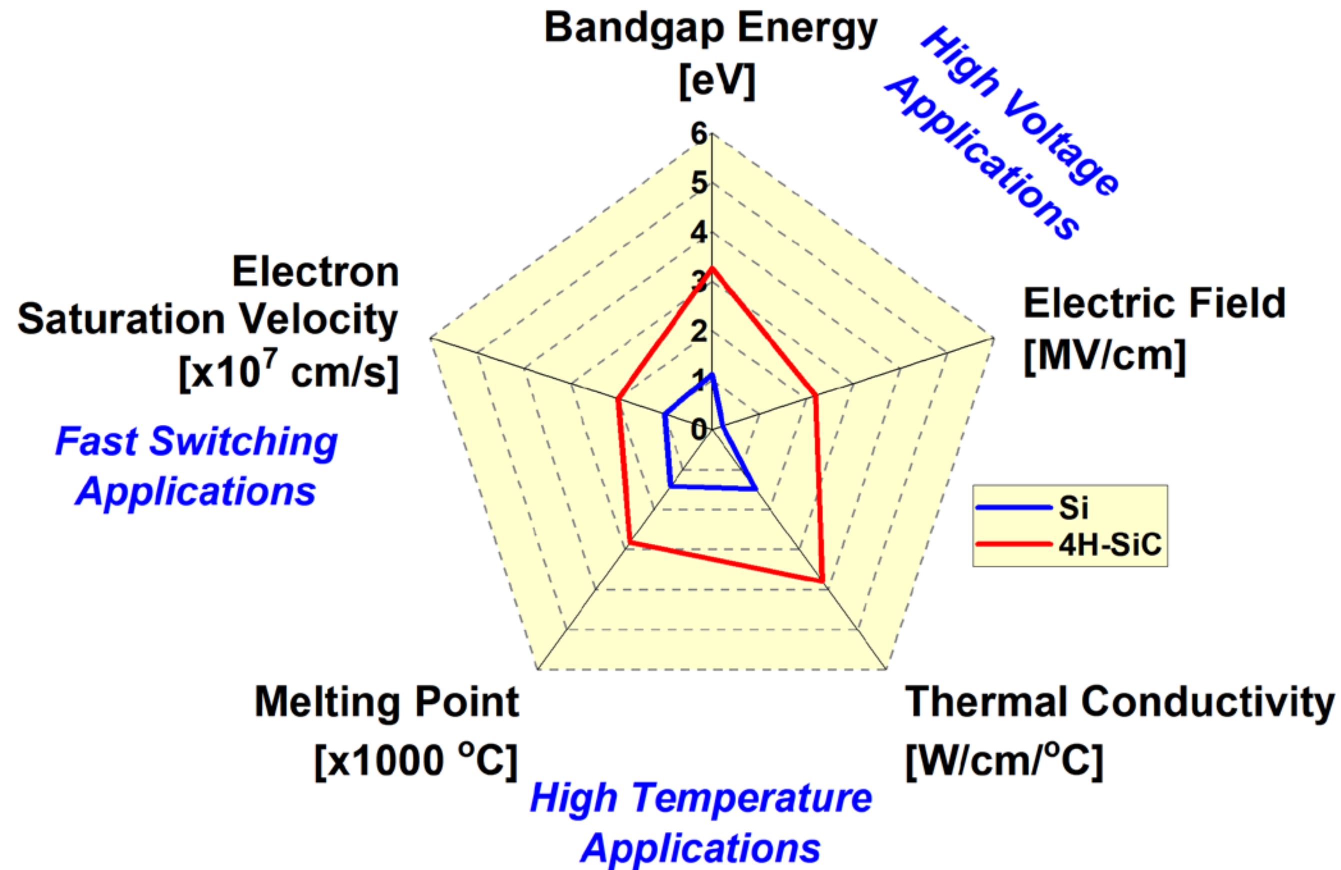
Wide-Bandgap Technology Overview: Properties Associated with the Bandgap





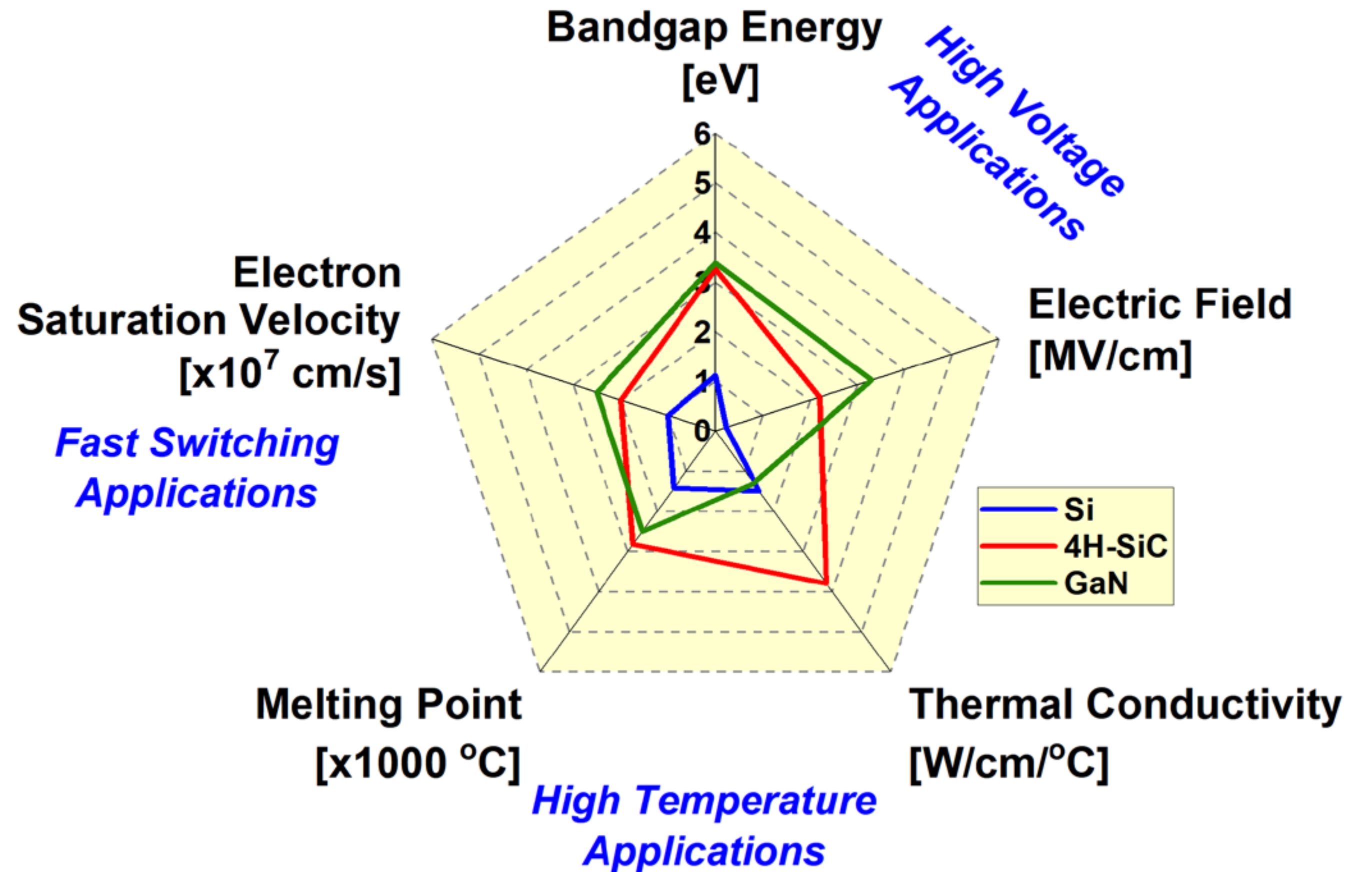
- **WBG semiconductors can:**
  - **Block higher voltages for a given thickness of material (breakdown voltage $\propto (E_{gap})^4$)**
  - **Switch at higher speeds due in part to higher saturation velocities**
  - **Operate at higher temperatures without "going intrinsic"**
  - **… and other WBG-material specific advantages**

A Closer Look: SiC vs. Si



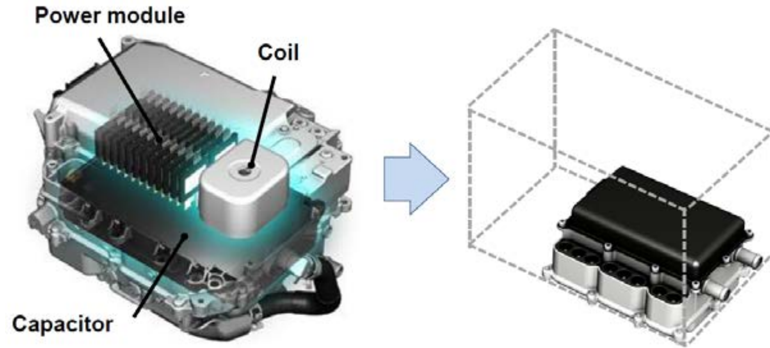
SiC out-performs Si on 5 different parameters, lending itself to high-power, high-temperature, and fast-switching applications

A Closer Look: GaN vs. SiC vs. Si



To date, GaN's upper limit on voltage rating is dictated primarily by device reliability issues

WBG Technology: It's About the SWaP!



Toyota estimates 80% volume reduction of Prius power control unit using SiC vs. Si

https://newsroom.toyota.co.jp/en/detail/2656842 (Image used with permission)

Source: Department of Energy

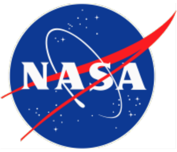
- **Technology Niches:**

GaN	SiC	Ga_2O_3
≤ 650 V Fast Switching	600 V – 10 kV Fast Switching High Current	> 5 kV Fast Switching

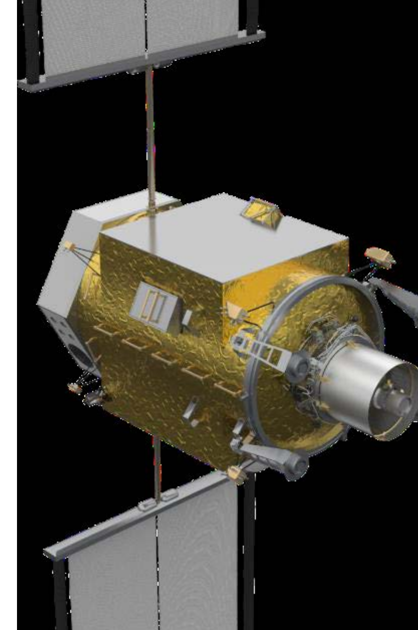
Superjunction technology keeps Si MOSFETs competitive in the 200 V – 700 V range

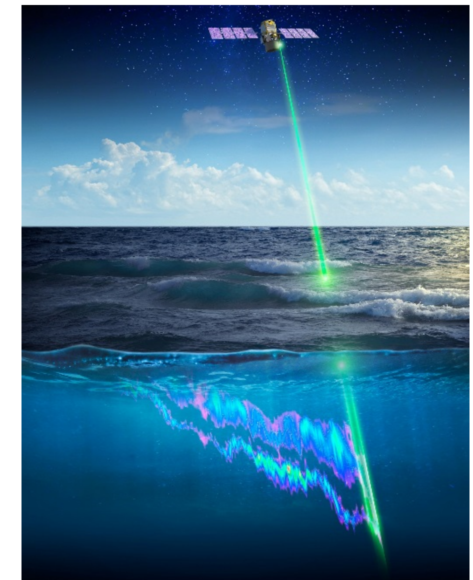
(SWaP = size, weight, and power)

Aerospace Drivers for WBG RHA



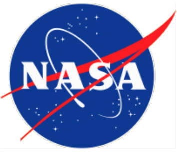
- **Spacecraft and Avionic Power Systems**:
  - Lunar Gateway and Mars Transport
  - Small Fission Reactors
  - Lunar and Planetary Surface Power
  - Electric Aircraft
  - Small Sats
- **Science Instruments & Payloads**
  - Mass Spectrometers
  - LIDAR
  - Improved SWaP = More Science

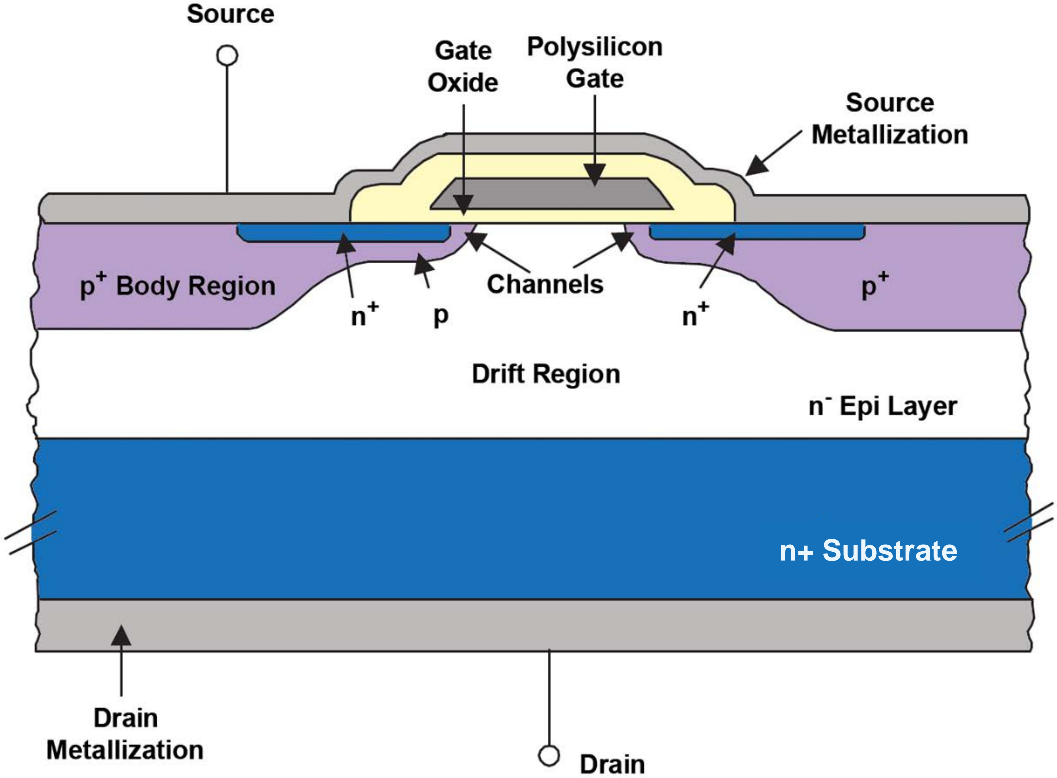




Images: NASA

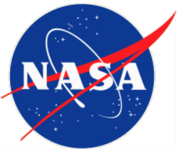
Common Power Device Structures: MOSFET

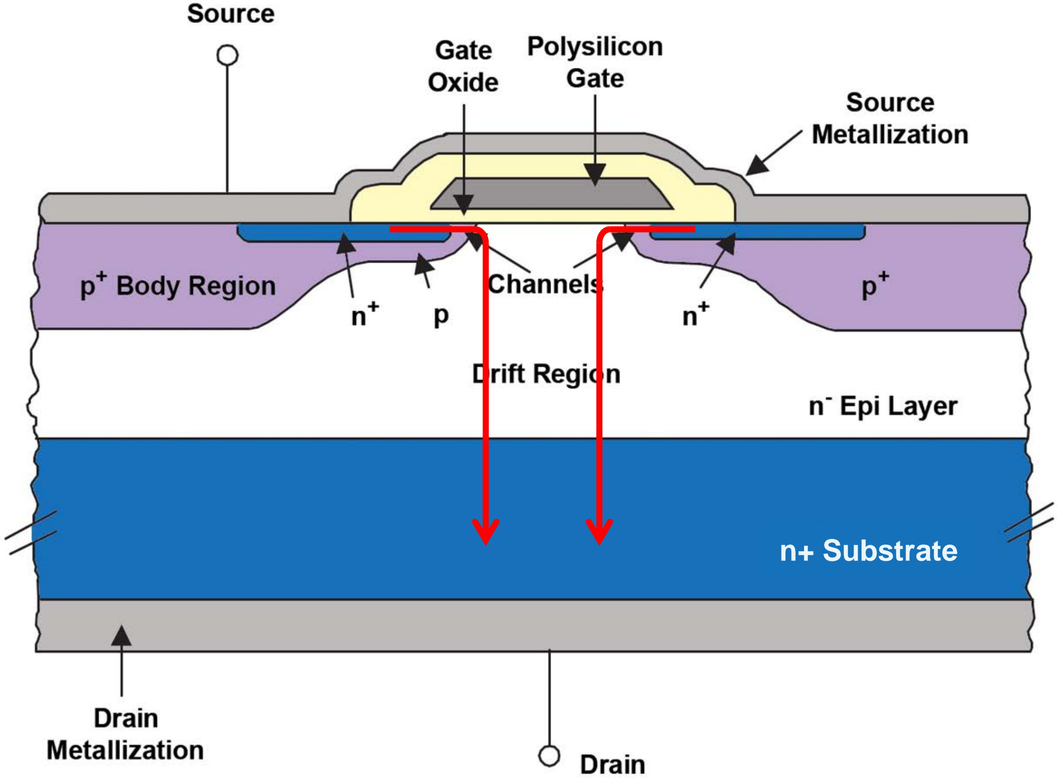




- **Vertical structure:**
  - **Drain contact at the bottom**

Common Power Device Structures: MOSFET

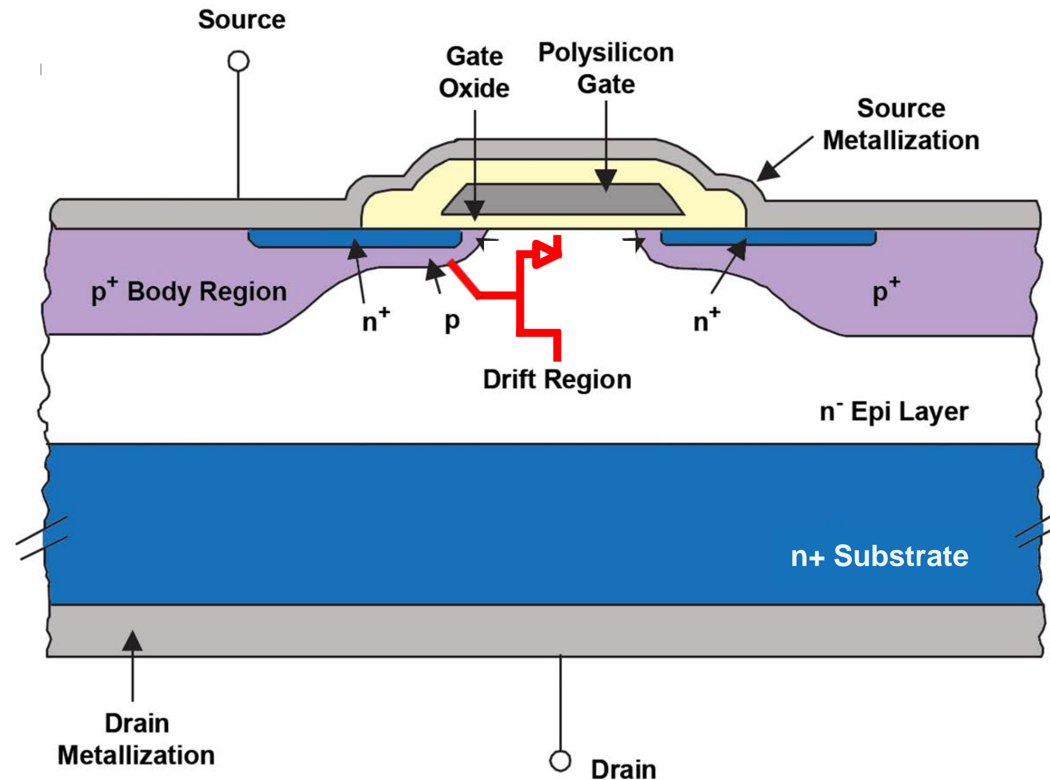




- **Vertical structure:**
  - **Drain contact at the bottom**
    - **Electron current flows through channels down through drain region**

Common Power Device Structures: MOSFET

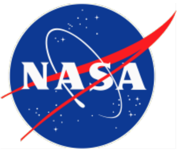
Vertical Double-Diffused Power MOSFET (VDMOS)



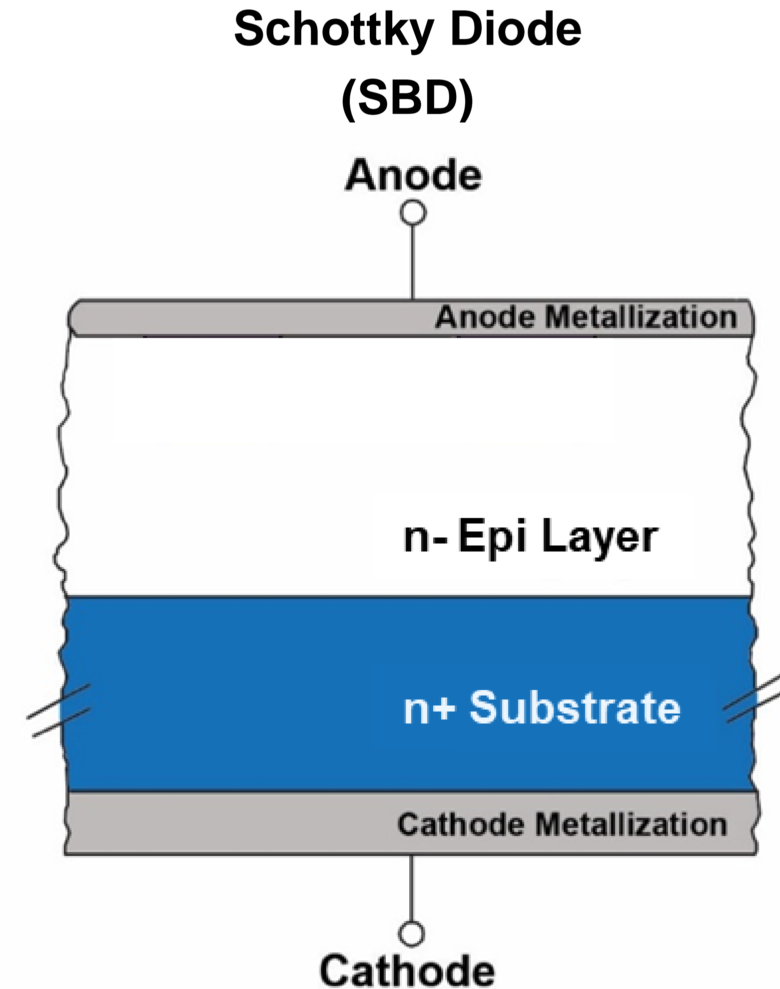
- Large n- drain region:
  - Enables high V_{DS} blocking
  - Increases on-state resistance (R_{DS_ON})
    - Parasitic JFET in neck region
    - Light doping of epilayer
- *SiC properties result in 10x reduction in epi thickness and higher doping*
  - Enable high-voltage MOSFETs with low power losses

SiC MOSFETs are often planar-gate VDMOS;
Other vertical topologies such as trench-gate structures are used in modern Si MOSFETs and some SiC MOSFETs

Common Power Device Structures: Schottky Diode

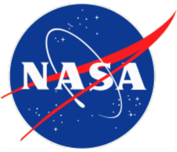


Schottky diodes
- Majority-carrier devices = fast switching
- Low on-state voltage drop
  - High off-state leakage current



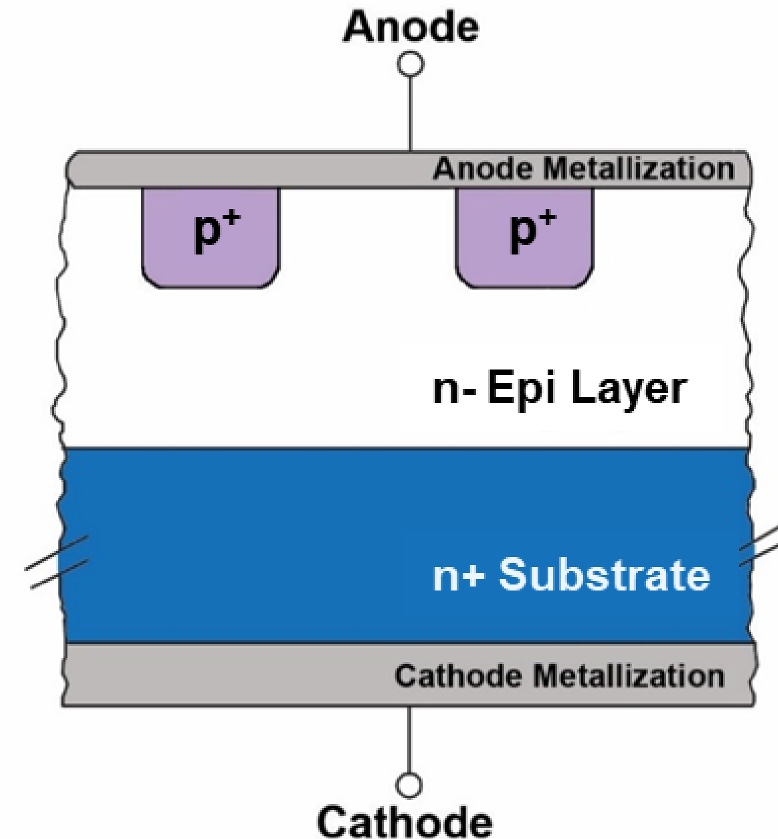
Upper limit of voltage rating set by power losses from resistance of thicker epilayer: SiC enables high-voltage Schottky diodes with low power losses

Common Power Device Structures: Schottky Diode



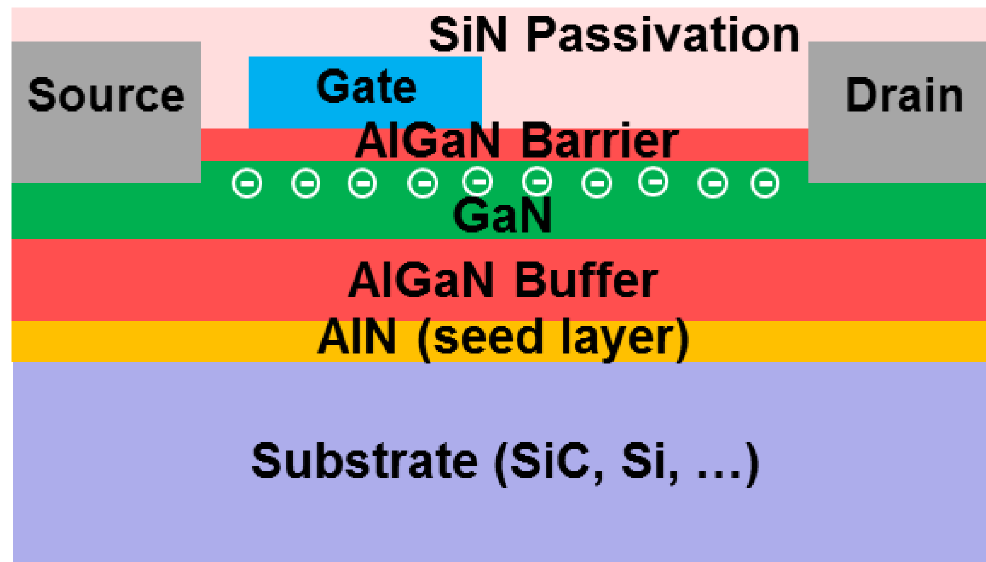
- Schottky diodes
  - Majority-carrier devices = fast switching
  - Low on-state voltage drop
    - High off-state leakage current
- JBS structure
  - Combines Schottky and ohmic contacts
    - Low forward voltage benefit of Schottky diode
    - Low leakage current of PiN diode

Junction Barrier Schottky Diode
(JBS Diode)

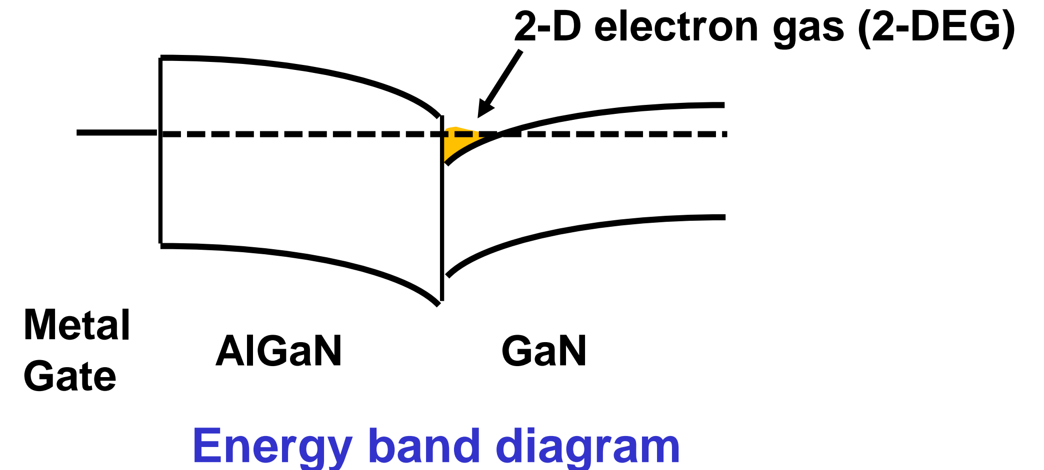


Upper limit of voltage rating set by power losses from resistance of thicker epilayer: SiC enables high-voltage Schottky diodes with low power losses

Common Power Device Structures: High Electron Mobility Transistor (HEMT)



- **GaN HEMT structure creates 2-dimensional path for electrons to flow**
  - **Lattice strain and charge polarization between the AlGaN barrier and the GaN layer**



Energy band diagram

High mobility of GaN HEMT is achieved without doping

WBG Inherent Radiation Tolerance

- **"Inherent" radiation hardness of WBG semiconductors typically refers to their tolerance of total dose:**
  - Both the ionization energy and threshold energy for defect formation (atomic bond strength) exceed that for Si
  - Early WBG devices did not have gate oxides
  - Operation of WBG devices at high temperature may help alleviate dose effects

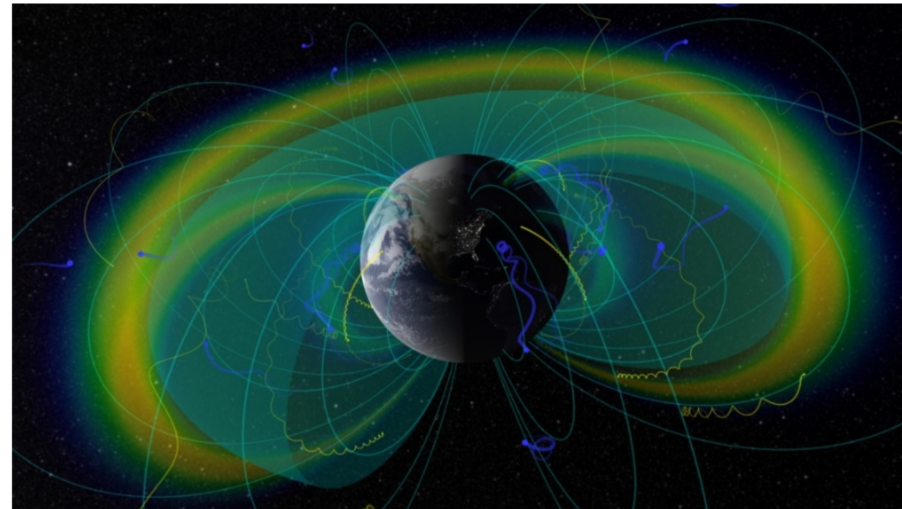


Image: NASA

WBG Achilles' Heel: Single-Event Effects

SiC Diode

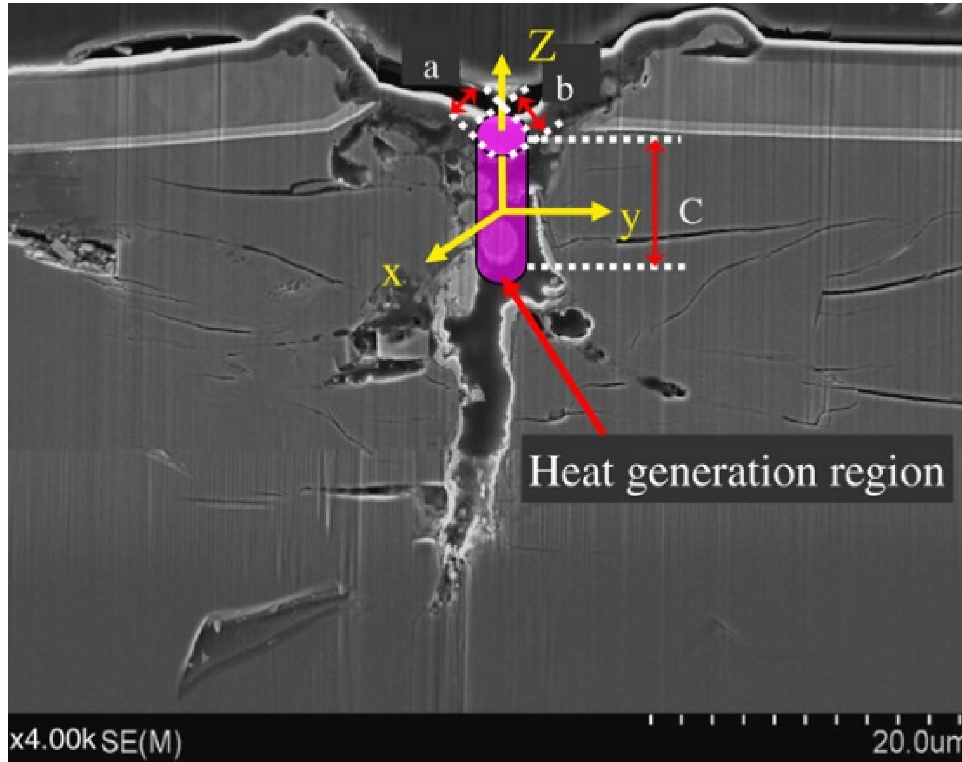


Image: Shoji, et al., © (2014) The Japan Society of Applied Physics, used with permission.

GaN HEMT

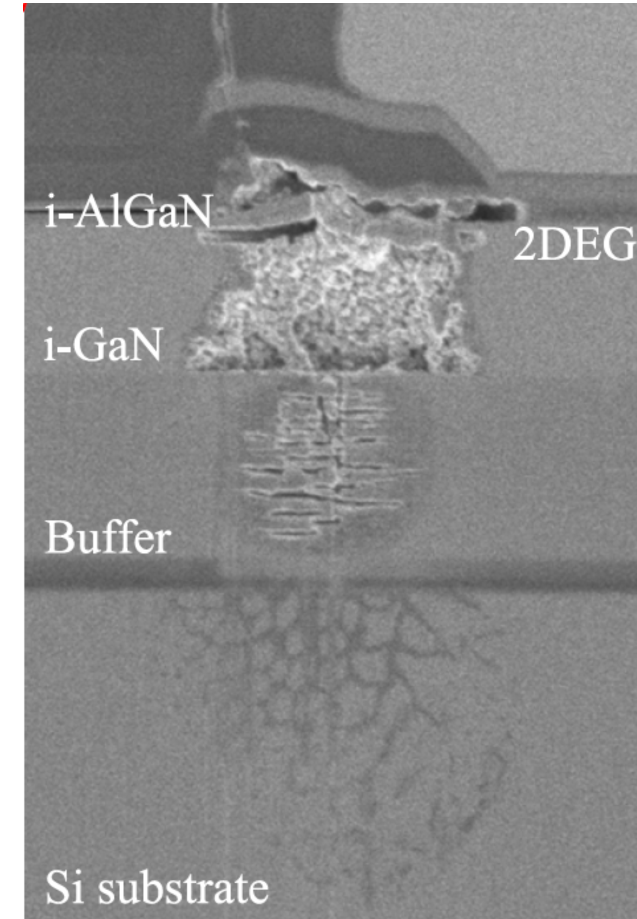
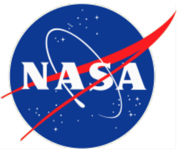


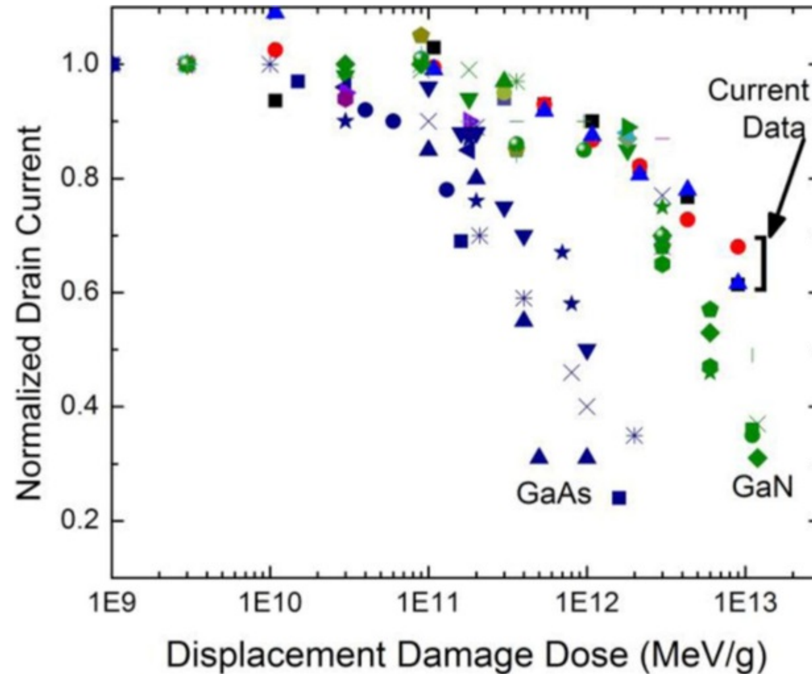
Image: Mizuta, et al., IEEE TNS 2018

Heavy-ion induced catastrophic single-event burnout in SiC and GaN power devices: Higher energy for charge ionization doesn't provide SEE immunity

Displacement Damage Dose (DDD) Effects: GaN HEMTs



GaN HEMTs out-perform GaAs HEMTs

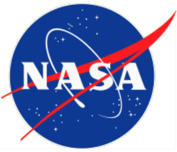


Weaver et al. ECS J. Solid State Sci. Technol. 2016. Used with permission.

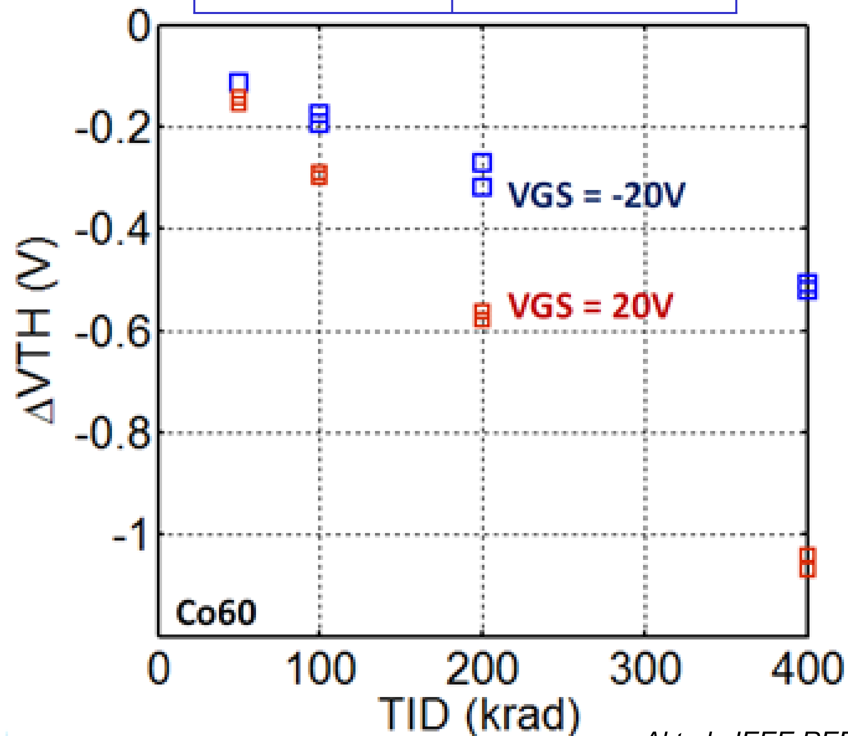
- **Parametric degradation in GaN HEMTs occurs at DDD levels above those for typical space applications**
  - Weaver, *et al.*, 2015 show order-of-magnitude better performance of GaN vs. GaAs HEMTs
- **GaN HEMT DDD effects include**
  - Decreased drain current
  - Threshold voltage shift (typically positive)
  - Decreased mobility and transconductance
- **DDD susceptibility is greater when:**
  - **parts are biased during irradiation**
  - **parts have had prior hot-carrier stress**
    - see Chen, *et al., IEEE TNS* 2015

GaN device DDD test conditions are important

Total Ionizing Dose Effects: SiC MOSFETs



Orbit	~1-year TID krad(Si)
Jovian	300
GEO	150
Polar LEO	5
ISS LEO	1



Akturk, IEEE REDW, 2017

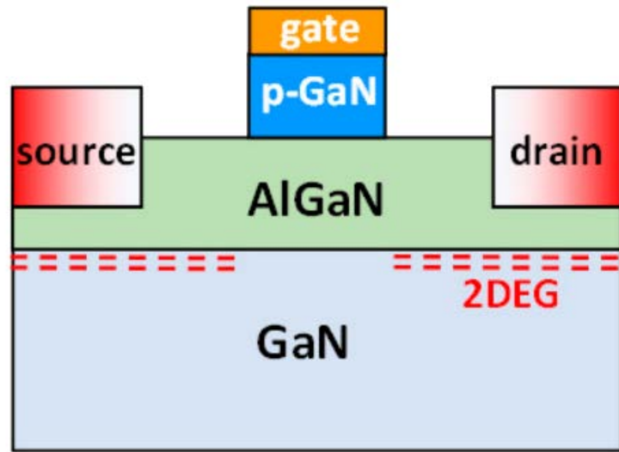
Despite thick oxides, SiC MOSFETs can be TID-robust:

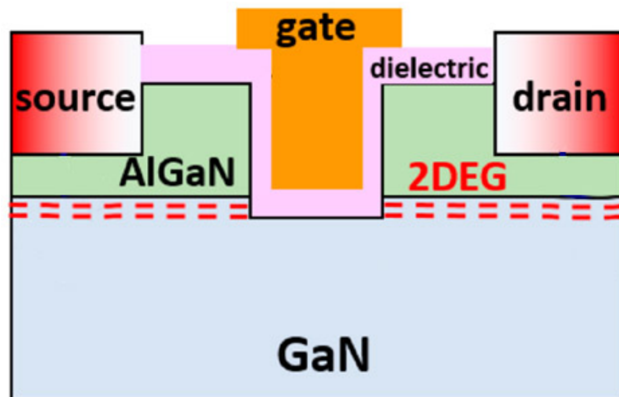
- **Cree Gens 1 & 2 in spec up to 100 krad(Si)**
  - Above 300 krad(Si), significant gate-drain capacitance changes can strongly impact switching performance
- **Expect variability between manufacturers and processes**
  - Hole trapping depends strongly on NO anneal time and temperature
  - Interface state formation with radiation can vary
  - Substantial fundamental differences between radiation responses of Si and SiC MOSFETs found via electrically detected magnetic resonance (EDMR)

TID hardness is coincidental and may change

Total Ionizing Dose: GaN HEMTs

p-GaN and MISHEMT Gate Structures





Images modified from:
Roccaforte, Materials, 2019. CC BY license.

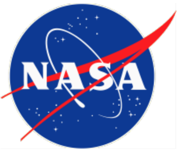
Many gate designs:

- **Schottky gate (normally on)**
  - Aktas, 2004 demonstrated 0.1 V threshold shift after **6 Mrad(Si)** γ irradiation
  - Harris, 2011 demonstrated no significant shift after **15 Mrad(Si)** proton irradiation
- **p-GaN gate (normally off)**
  - **500 krad(Si)** γ irradiation: < 18% Vth shift (Lidow, 2011)
- **Cascode design (normally off)**
  - No public data
  - Commercial designs are likely to be sensitive to TID effects: gate controlled by low-voltage n-type Si MOSFET
- **MISHEMT (normally off)**
  - Oxide/insulator under recessed gate

GaN HEMT TID effects may vary as a function of gate design

SILICON POWER DEVICE SINGLE-EVENT EFFECTS

Si Power MOSFET Single-Event Gate Rupture (SEGR)

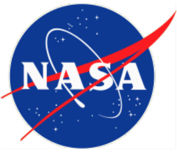


Planar-gate vertical double-diffused MOSFET "VDMOS"

Source
Gate Oxide
ysilicon Gate
Oxide effects: ƒ(Z, θ, LET)
p^+ Body Region
n^+
Epilayer effects: ƒ(E, LET, θ)
p^+
n^- Epi Layer
n+ Substrate
Drain Metallization
Drain

Z = Ion Species
E = Energy
LET = Linear Energy Transfer
θ = Angle of Incidence

Si Power MOSFET Single-Event Gate Rupture (SEGR)



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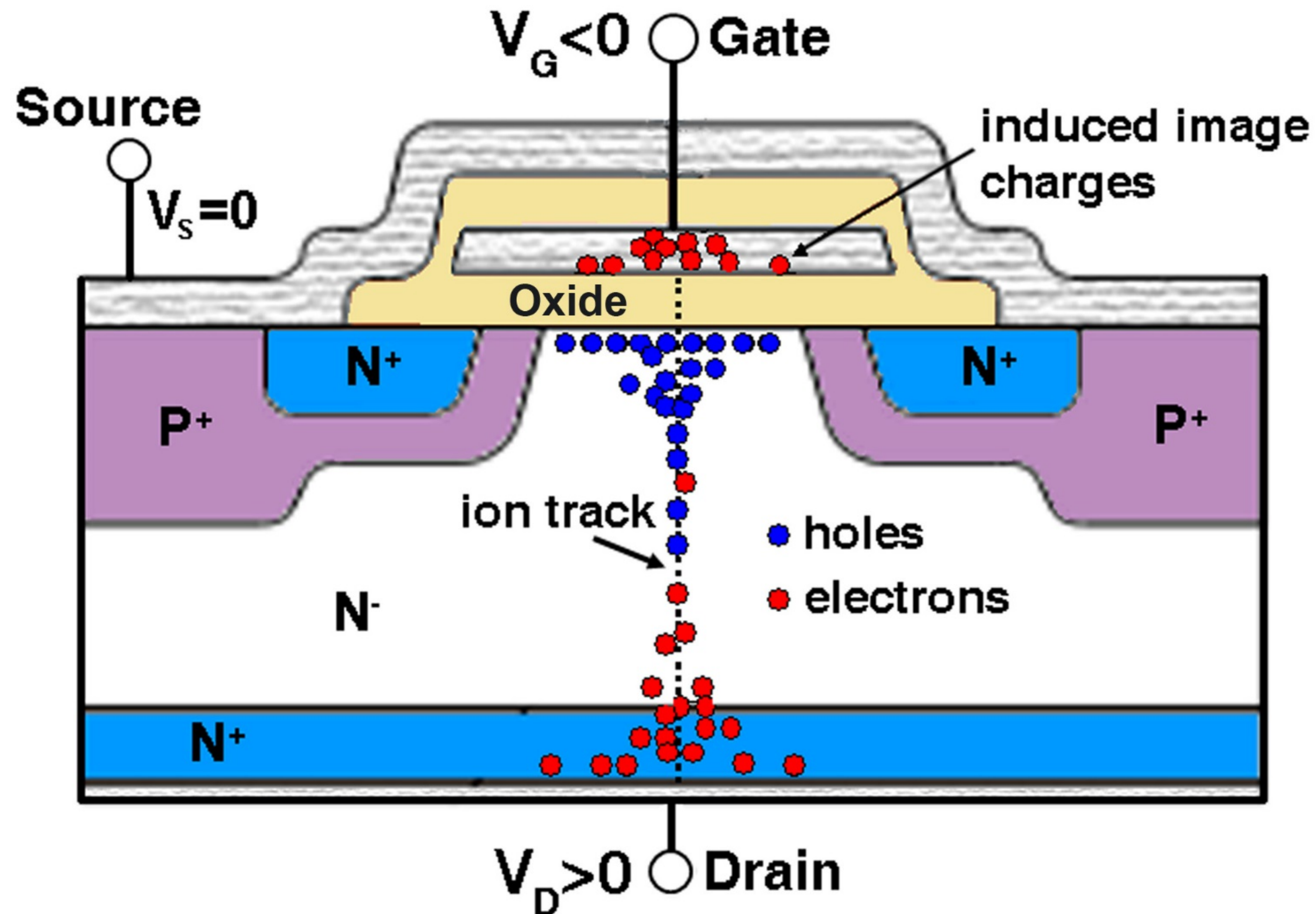
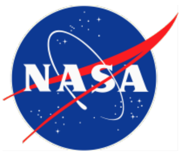


Si Power MOSFET Single-Event Burnout (SEB)

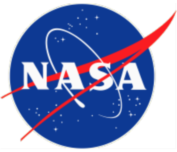


= electric field
= electron
= hole

Source
Gate Oxide
Polysilicon Gate
Source Metallization
$\vec{E}$
Depth
n
n^+
p
Channels
n
p^+
Drift Region
n^- Epi Layer
n+ Substrate
Drain Metallization
Drain

1. Ionized charge distorts depletion region
   - Increased V_{BODY} turns on BJT
   - I_{BODY} sustains BJT on-state

Si Power MOSFET Single-Event Burnout (SEB)



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1. **Ionized charge distorts depletion region**
   - **Increased V_{BODY} turns on BJT**
   - **I_{BODY} sustains BJT on-state**
2. **High current collapses depletion region**

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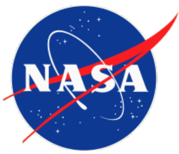
Si Power MOSFET Single-Event Burnout (SEB)



- - - = electric field
● = electron
● = hole

Source

Gate Oxide

Polysilicon Gate

Source Metallization

$\vec{E}$

Depth

n

n^+

p

Channels

n

p^+

Drift Region

n^- Epi Layer

n+ Substrate

Drain Metallization

Drain

1. **Ionized charge distorts depletion region**
   - **Increased V_{BODY} turns on BJT**
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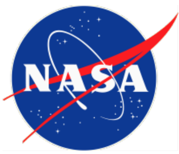
2. **High current collapses depletion region**
   - **As electron concentration > donor concentration, peak field moves to epi/substrate interface**

Si Power MOSFET Single-Event Burnout (SEB)



= electric field
= electron
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Source
Gate Oxide
Polysilicon Gate
Source Metallization
$\vec{E}$
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n^+
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Drift Region
n^- Epi Layer
n+ Substrate
Drain Metallization
Drain

1. **Ionized charge distorts depletion region**
   - **Increased V_{BODY} turns on BJT**
   - **I_{BODY} sustains BJT on-state**
2. **High current collapses depletion region**
   - **As electron concentration > donor concentration, peak field moves to epi/substrate interface**
3. **Band-band tunneling provides regenerative current**
   - **Second breakdown & SEB**

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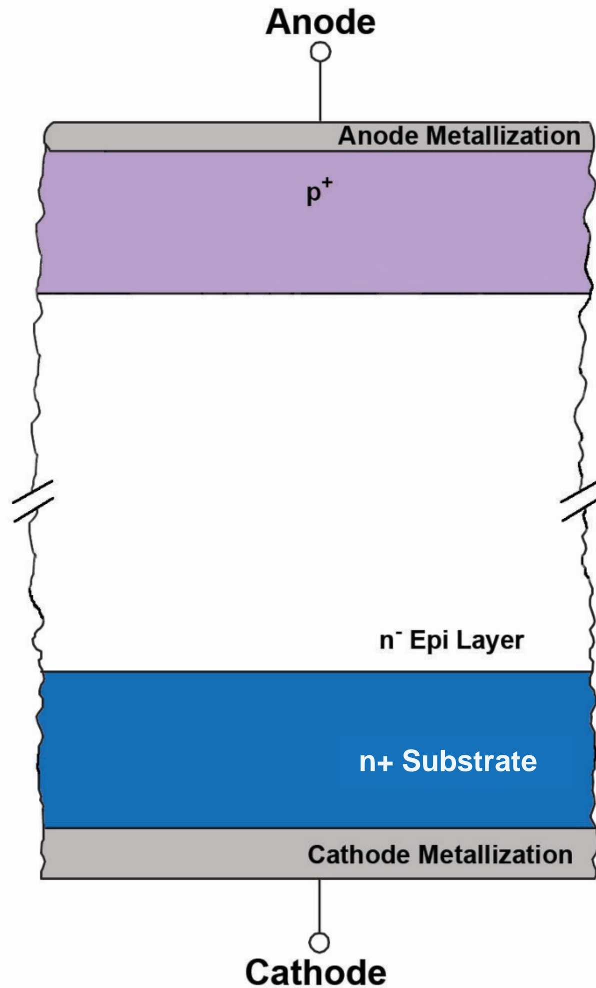
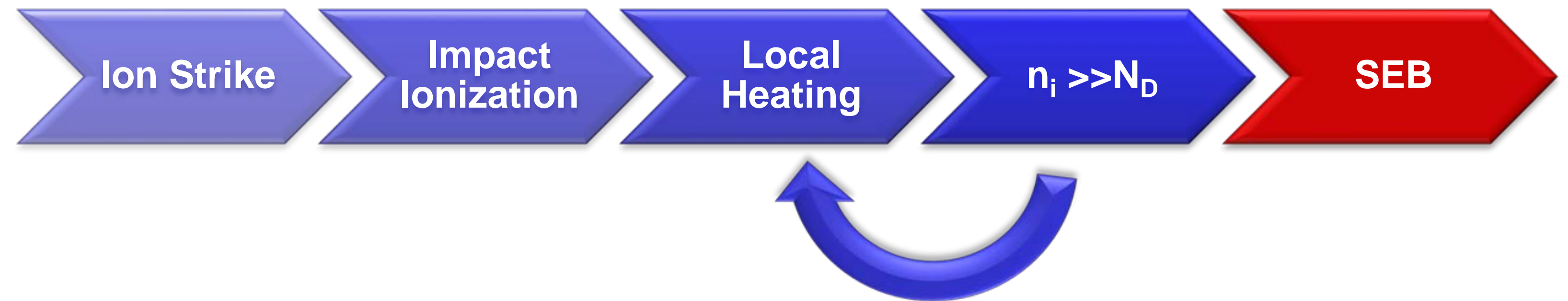
Si Power PiN Diode Single-Event Burnout (SEB)

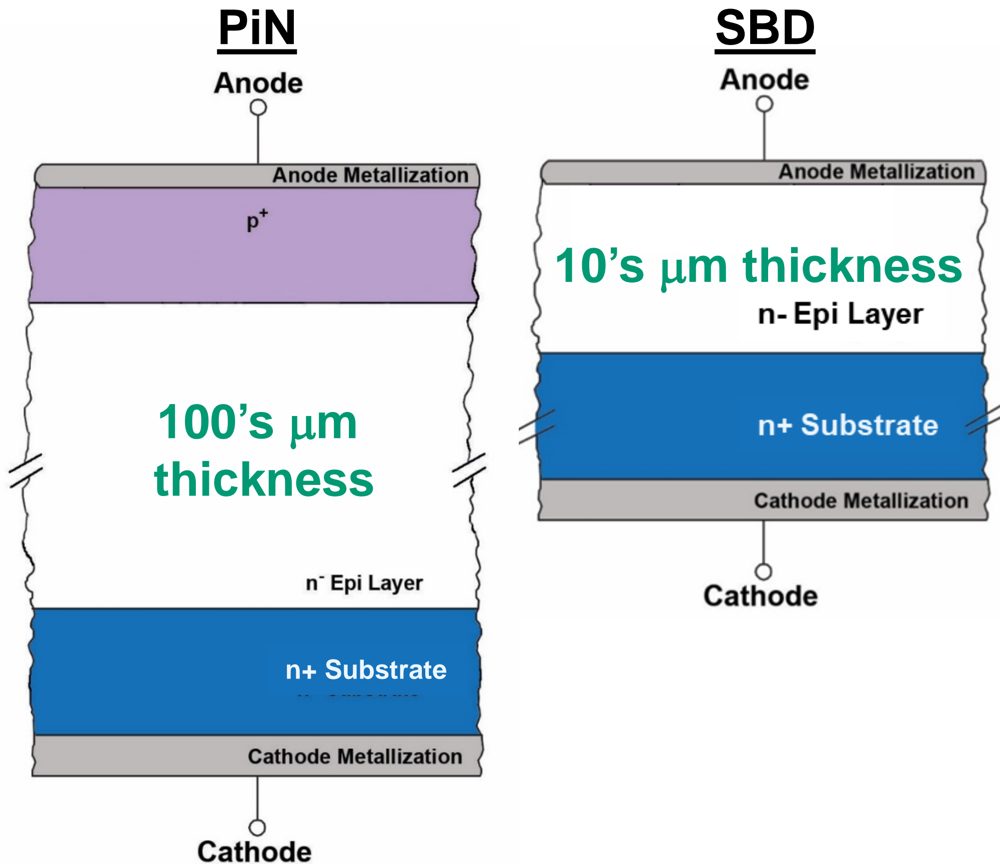


- **No BJT mechanism**
- **Impact ionization deemed insufficient for SEB**
- **Self-heating suggested as critical mechanism**
  - Intrinsic carrier concentration rises, setting off feedback loop



Joule heating causes intrinsic carrier concentration to dominate, leading to thermal runaway

Si Schottky Diode Single-Event Burnout (SEB)

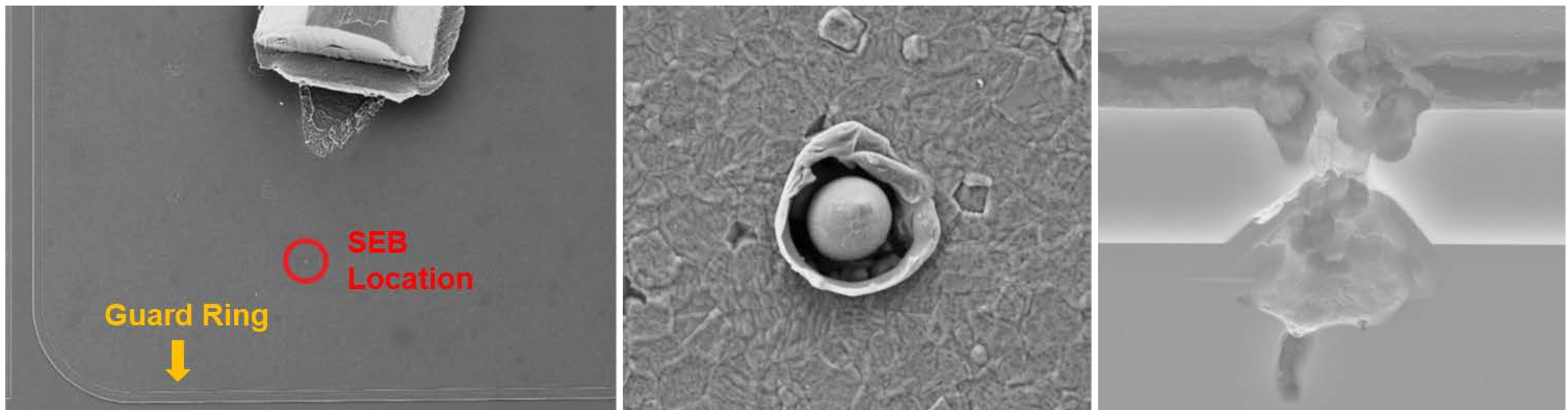


- **SEB in Schottkys unexpected**
  - Much lower voltage rating
  - Thinner epi = less impact ionization current
- **Heavy-ion energies during testing permit penetration through entire epilayer**
  - More efficient shorting of anode/cathode
- **Guard ring for field termination disruption results in high fields at edge of anode**
  - Impact ionization and Joule heating
- **Trench style diodes more susceptible due to trench edge high field**

High-field locations may be sensitive to ion-initiated Joule heating and intrinsic carrier current triggered thermal runaway

Si Schottky Diode Single-Event Effects

- Problem: Not all Schottkys fail at guard ring
- Survey of Silicon SBDs revealed trends for SEB susceptibility:
  - Higher barrier height
  - Lower I_R rating

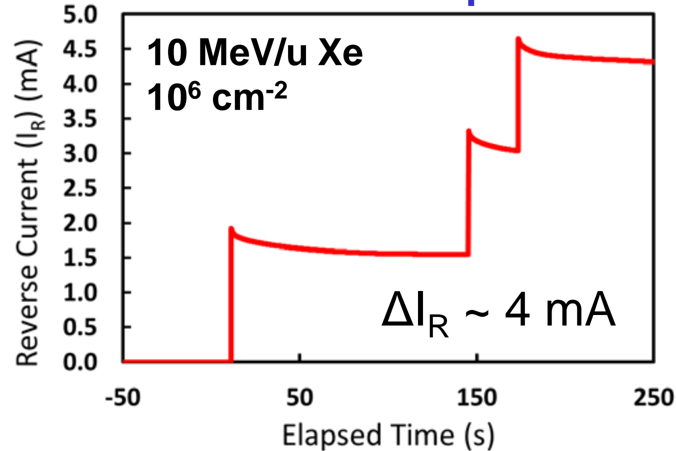


Images: Casey, et al., IEEE TNS 2017

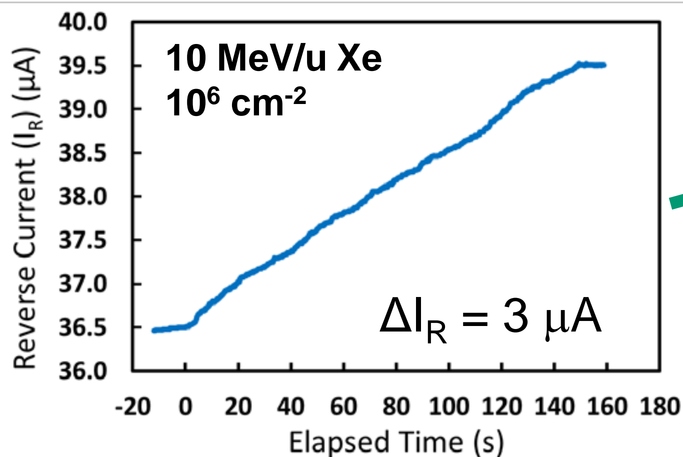
Derating below 50% of rated V_R recommended to reduce SEB risk

Additional Si Schottky Diode Single-Event Effects

Stepped degradation; diode out of spec



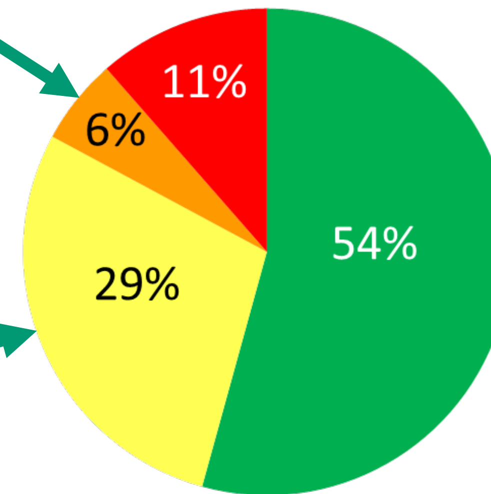
Continuous degradation; diode remained in spec



Plots: Casey, et al., IEEE TNS 2015

- Non-catastrophic permanent degradation
  - Increased reverse current
  - Only ~ 6% of samples degraded out of spec at LET = 59 when biased at 75% of rated V_R

75 % Reverse Voltage

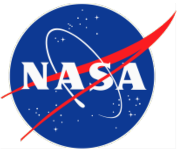


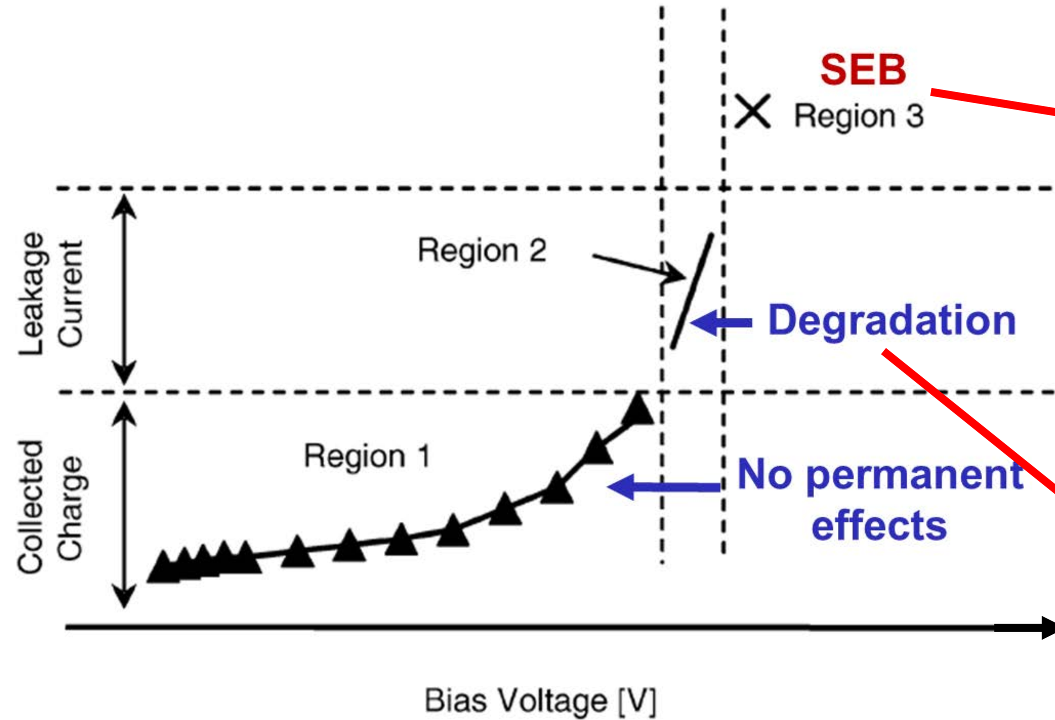
Pass
Degradation and Pass
Degradation and Failure
Catastrophic SEB

Non-catastrophic SEE occurs in a small sampling of Si SBDs at high V_R

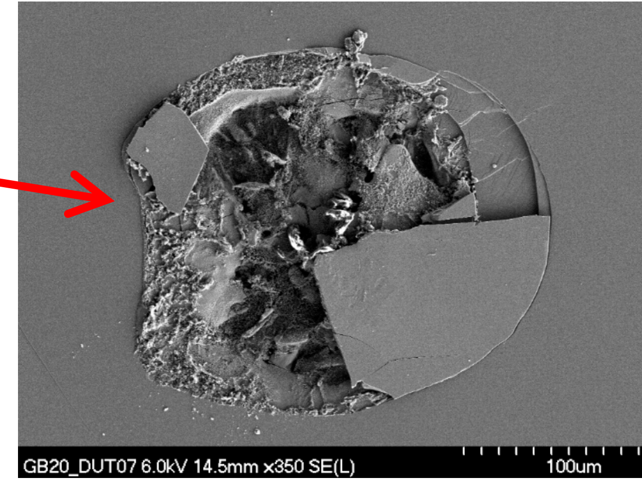
SILICON CARBIDE POWER DEVICE SINGLE-EVENT EFFECTS

Silicon Carbide Single-Event Effects: Diodes

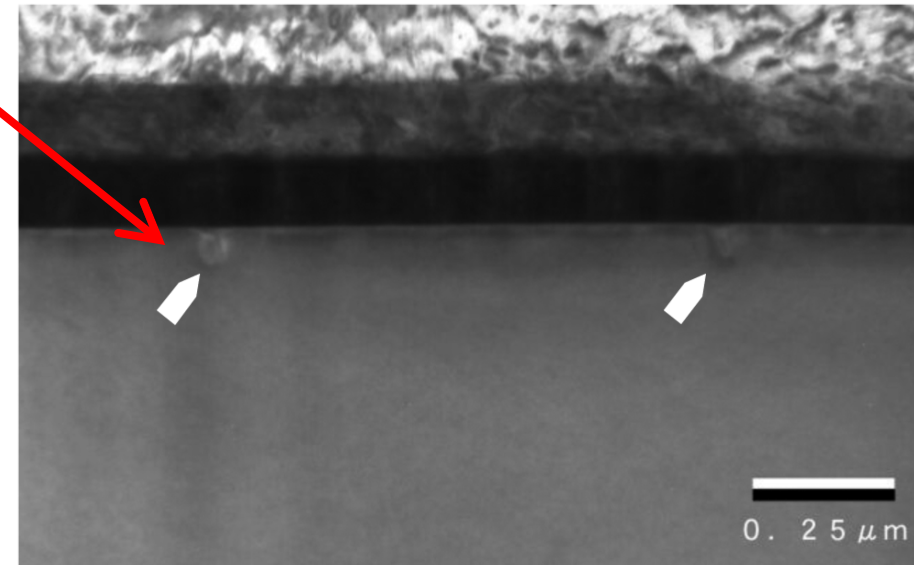




After Kuboyama, IEEE TNS, 2006



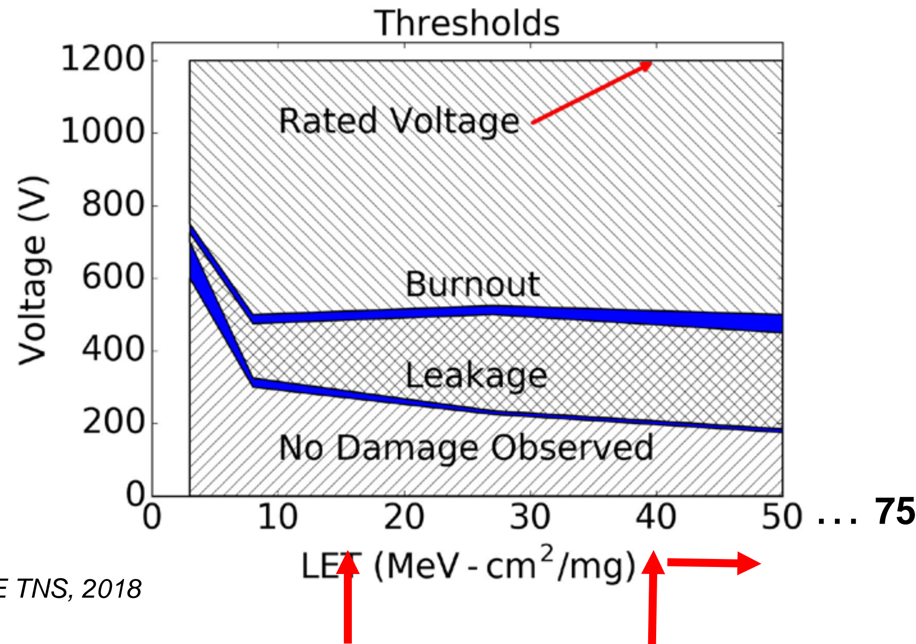
NASA GRC: A. Woodworth, 2015



Kuboyama, IEEE TNS, 2006

- **SEEs in SiC Schottky diodes include:**
  - **Transient charge collection**
  - **Permanent increased leakage current**
  - **Catastrophic single-event burnout (SEB)**

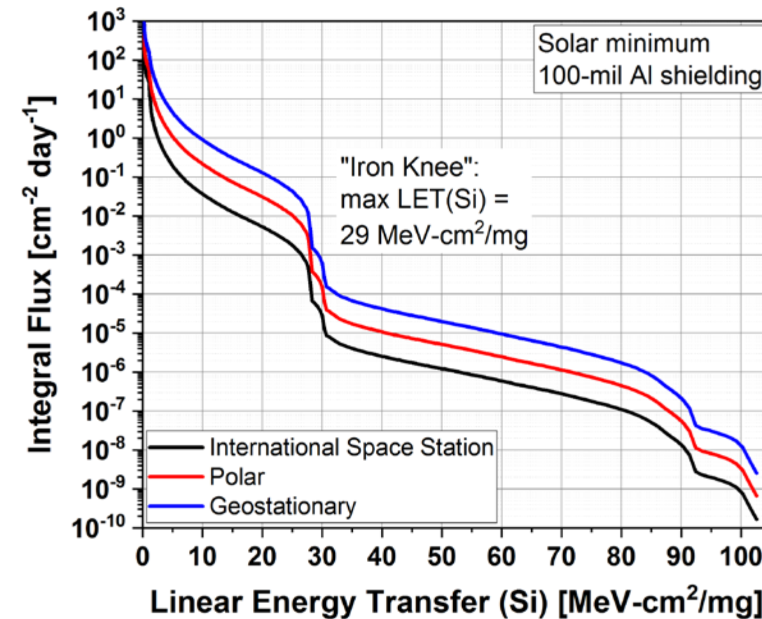
Silicon Carbide Schottky Diode SEE Thresholds



Witulski, IEEE TNS, 2018

Atmospheric Neutrons

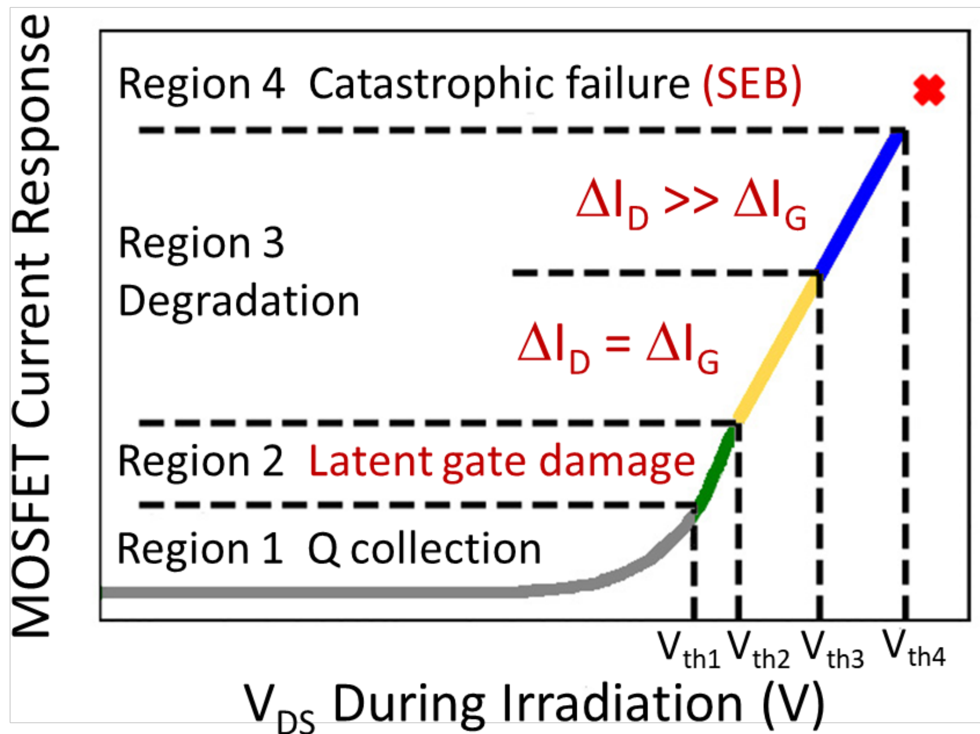
GCRs



- **Onsets for ion-induced leakage current and single-event burnout saturate quickly with linear energy transfer (LET)**
  - Saturation occurs before the high-flux iron knee of the GCR spectrum

Risk-avoidant mission LET requirements for SEB vary by application: All fall within the saturation region of SEE sensitivity

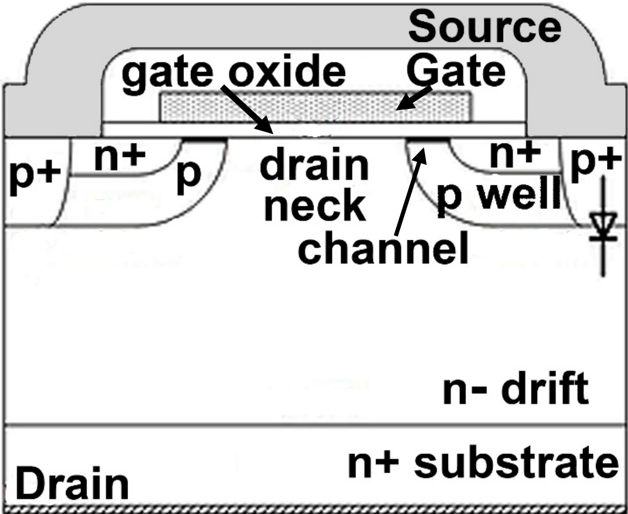
Silicon Carbide Single-Event Effects



After Martinella, IEEE TNS, 2020

- **SEEs in SiC MOSFETs include gate effects**
  - **Latent gate damage**
  - **Permanent increased leakage current**
    - Drain-Gate or Drain-Source leakage pathway
      - see Martinella, IEEE TNS 2020
- **Catastrophic single-event burnout (SEB)**
- **SiC JFETs have similar behavior except:**
  - Rare to have drain-source leakage
    - Drain-gate leakage is main degradation pathway
  - No latent gate damage (no gate oxide)

Silicon Carbide Single-Event Effects



Li, Micromachines, 2019
CC BY 4 license

No Effect | Latent Gate Degradation | $\Delta I_D = \Delta I_G$ | $\Delta I_D >> \Delta I_G$ | SEB

Drain-Source Voltage (V): 0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500

(to 3300)

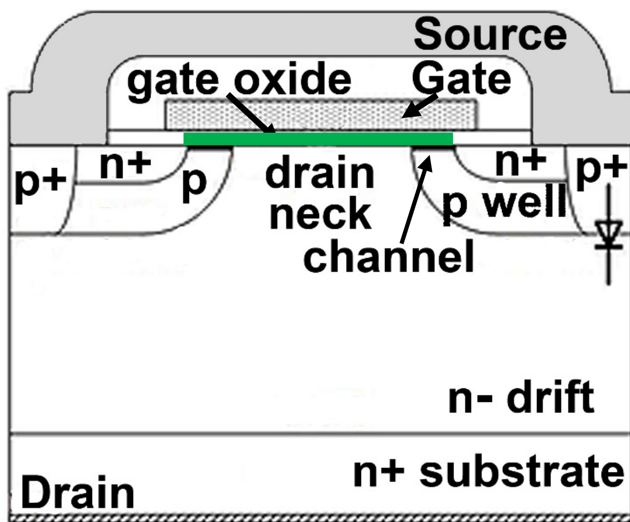
No Data

No Data

Ion/LET [MeV-cm²/mg(SiC)]:	B 1.0	Ar 9.3	Ar 11	Cu 24	Ag 49	Xe 66
Device:	M1	M2 M7	M1	M2 M3	M4 M5	M2 M3 M4 M6 M7 M8

Silicon Carbide Single-Event Effects

- **Latent gate damage reduced with lower LET/lighter ions**
  - (green regions)
  - At high LETs, onset at ~50 V to 75 V!



Drain-Source Voltage (V)

Legend: No Effect | Latent Gate Degradation | $\Delta I_D = \Delta I_G$ | $\Delta I_D >> \Delta I_G$ | SEB

(to 3300)

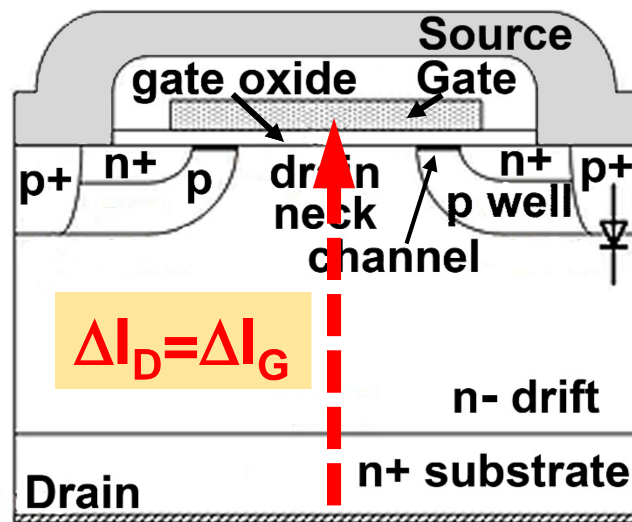
Device:	M1	M2	M7	M1	M2	M3	M4	M5	M2	M3	M4	M6	M7	M8
Ion/LET: [MeV-cm²/mg(SiC)]	B 1.0	Ar 9.3		Ar 11	Cu 24		Ag 49		Xe 66					

No Data

No Data

Silicon Carbide Single-Event Effects

- **Not all MOSFETs have drain-gate leakage**
  - **(yellow regions)**
  - **Leakage thru oxide over drain "neck" region**
  - **Design techniques may eliminate this effect**



(to 3300)

No Effect | Latent Gate Degradation | $\Delta I_D = \Delta I_G$ | $\Delta I_D >> \Delta I_G$ | SEB

Drain-Source Voltage (V)

1500, 1400, 1300, 1200, 1100, 1000, 900, 800, 700, 600, 500, 400, 300, 200, 100, 0

No Data

No Data

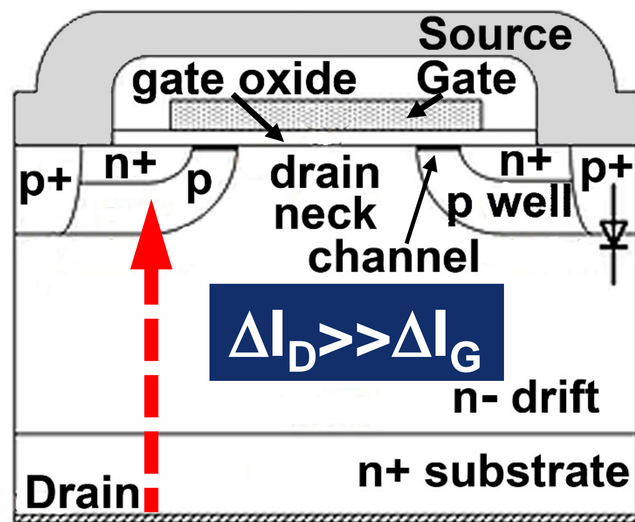
Device: M1 | M2 M7 | M1 | M2 M3 | M4 M5 | M2 M3 M4 M6 M7 M8

Ion/LET: B 1.0 | Ar 9.3 | Ar 11 | Cu 24 | Ag 49 | Xe 66

[MeV-cm^2/mg(SiC)]

Silicon Carbide Single-Event Effects

- **Drain-source leakage least influenced by LET or electric field**
  - **(blue regions)**
  - see Johnson, IEEE TNS 2020
  - **Sensitive region is p-n junction (body-drain)**



No Effect | Latent Gate Degradation | $\Delta I_D = \Delta I_G$ | $\Delta I_D >> \Delta I_G$ | SEB

(to 3300)

Drain-Source Voltage (V)

1500, 1400, 1300, 1200, 1100, 1000, 900, 800, 700, 600, 500, 400, 300, 200, 100, 0

No Data

No Data

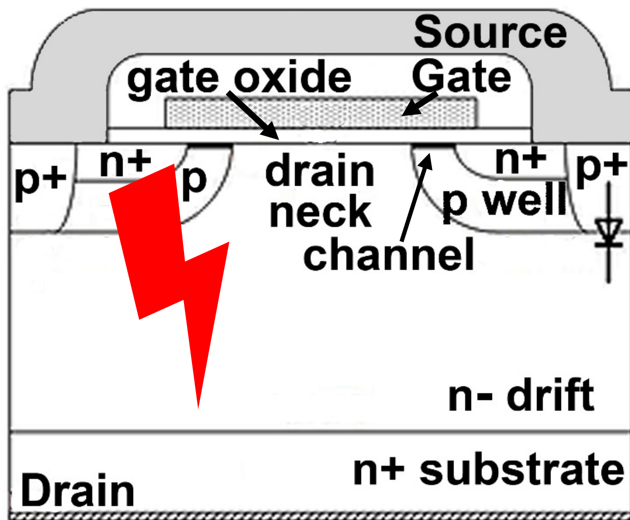
Ion/LET:	B 1.0	Ar 9.3		Ar 11	Cu 24		Ag 49		Xe 66					
Device:	M1	M2	M7	M1	M2	M3	M4	M5	M2	M3	M4	M6	M7	M8

[MeV-cm^2/mg(SiC)]

To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020

Silicon Carbide Single-Event Effects

- **Max cross-section for SEB at ~50% of rated V_{DS}**
  - **(red regions)**
  - **Susceptible at very low LET**
    - Proton/neutron risk



(to 3300)

No Effect | Latent Gate Degradation | $\Delta I_D = \Delta I_G$ | $\Delta I_D >> \Delta I_G$ | SEB

Drain-Source Voltage (V)

1500, 1400, 1300, 1200, 1100, 1000, 900, 800, 700, 600, 500, 400, 300, 200, 100, 0

No Data

No Data

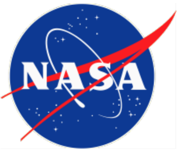
Device: M1 | M2 M7 | M1 | M2 M3 | M4 M5 | M2 M3 M4 M6 M7 M8

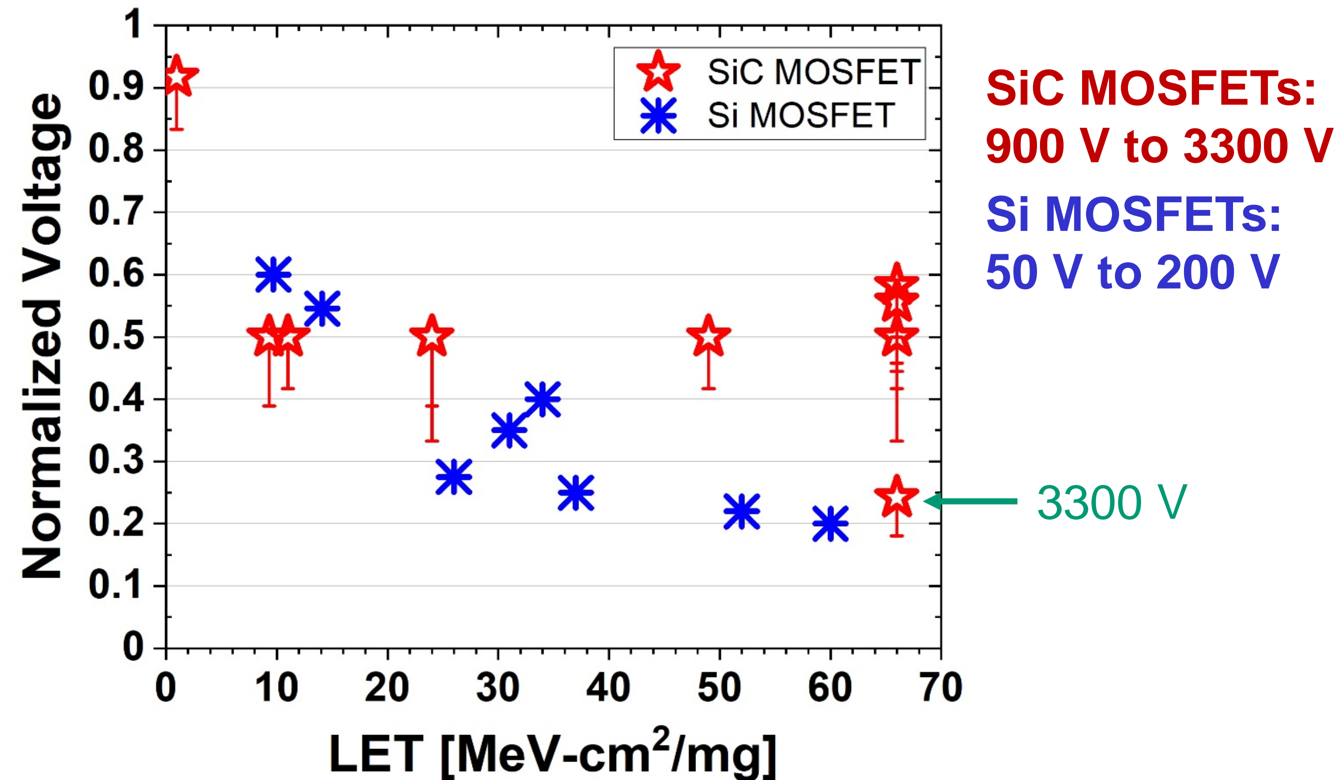
Ion/LET: B 1.0 | Ar 9.3 | Ar 11 | Cu 24 | Ag 49 | Xe 66

[MeV-cm²/mg(SiC)]

To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020

Silicon Carbide vs. Unhardened Silicon: Power MOSFET SEB Susceptibility





SiC MOSFETs: 900 V to 3300 V

Si MOSFETs: 50 V to 200 V

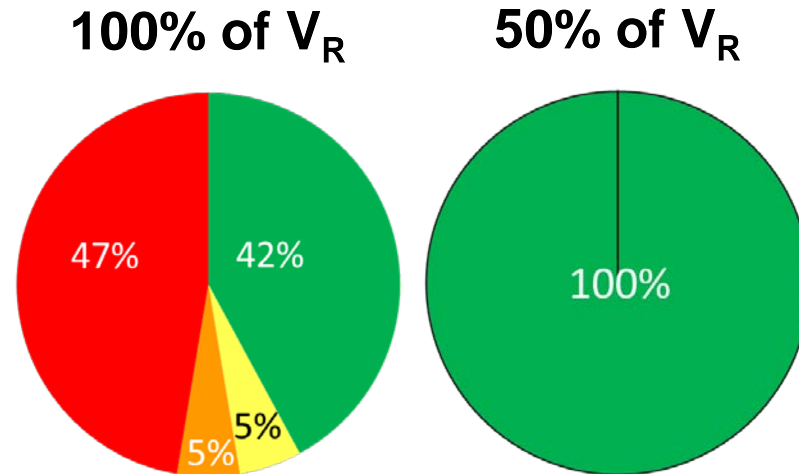
3300 V

SiC MOSFETs are generally less susceptible to SEB than unhardened, commercial silicon MOSFETs **

**** Not shown: SiC MOSFETs are more susceptible to permanent, non-catastrophic damage effects.**

Silicon Carbide vs. Silicon: Schottky Diode SEB Susceptibility

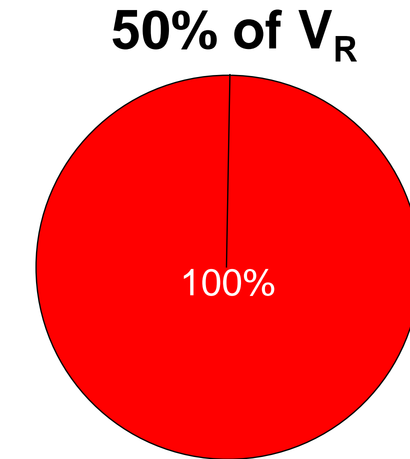
Silicon



No SEB at 50% of V_R
(LET = 59 MeV-cm²/mg(Si))

Plots: Casey, IEEE NSREC, 2015

Silicon Carbide



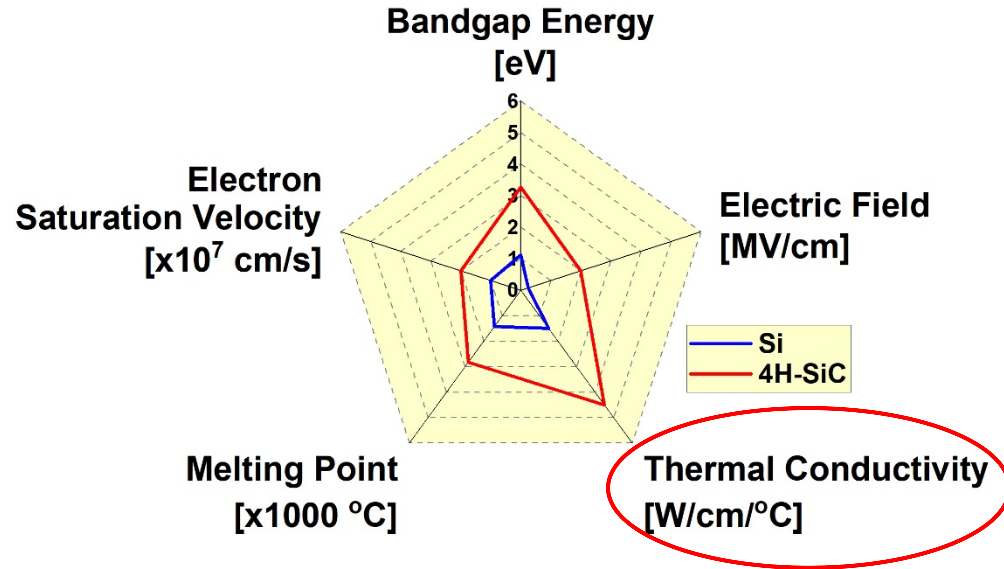
SEB at ~ 50% V_R
(LET << 59 MeV-cm²/mg(SiC))

Data from: Lauenstein, MRQW, 2018

- **SiC Shottky diode susceptibility to SEB occurs at < 50% of avalanche V_R**
- **Si Schottky diodes pass at this derating level, with almost half passing at 100%**

To date, no tested commercial SiC diodes pass above ~50% of rated V_R at mission LET requirement levels

SiC Properties Revisited: Thermal Conductivity



- **High thermal conductivity, but not instantaneous**
  - Heat removal via acoustic phonons
  - **≥ ns to start conducting heat away**
    - See Akturk, IEEE TNS, 2018

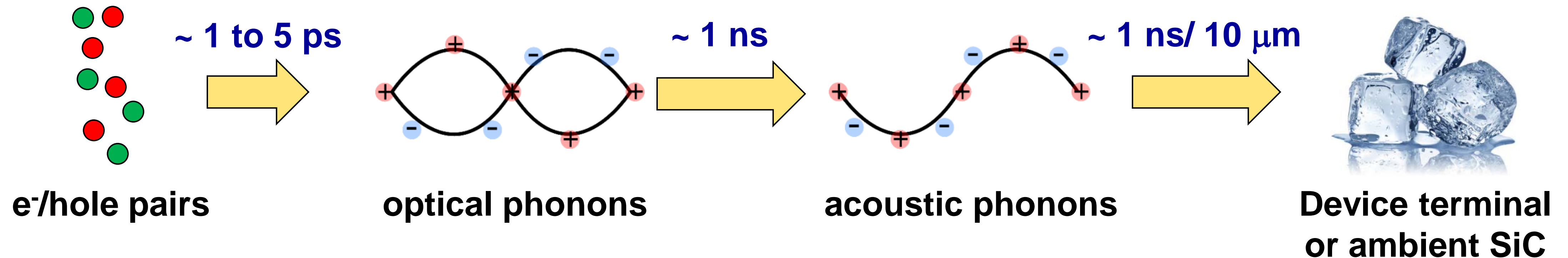
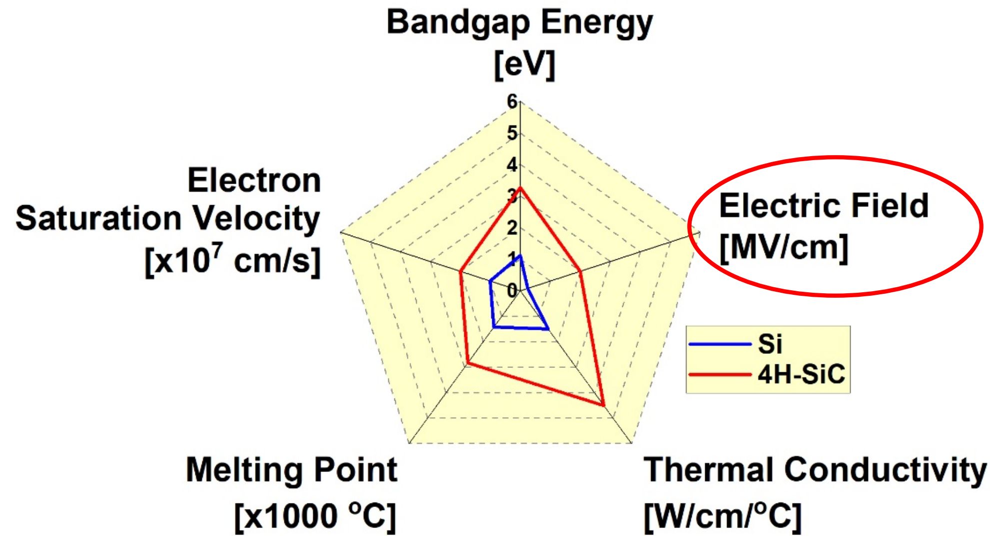


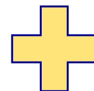
Image: Creative Commons, M. Griffith, 2017

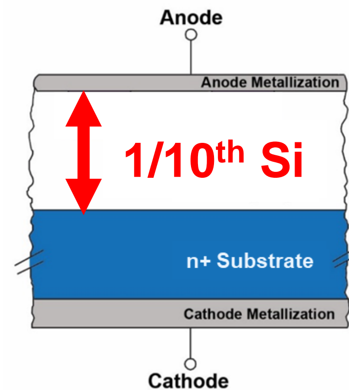
SiC Properties Revisited: Electric Field

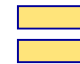


- Peak $\vec{E}_{SiC}$ > 10x peak $\vec{E}_{Si}$ means 100x higher heat generation density
  - More rapid rise in temperature (T)
  - ΔT = time × power / heat capacity (C)
    - C ∝ heated volume
  - SiC sublimation in picoseconds
    - See Shoji, JJAP 2014 & Akturk, IEEE TNS 2018

$$\text{Power} = \frac{V^2}{R}$$







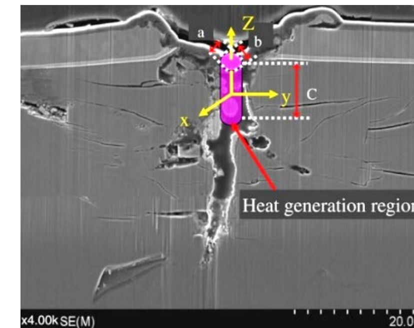
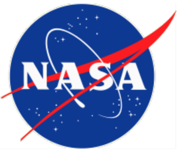


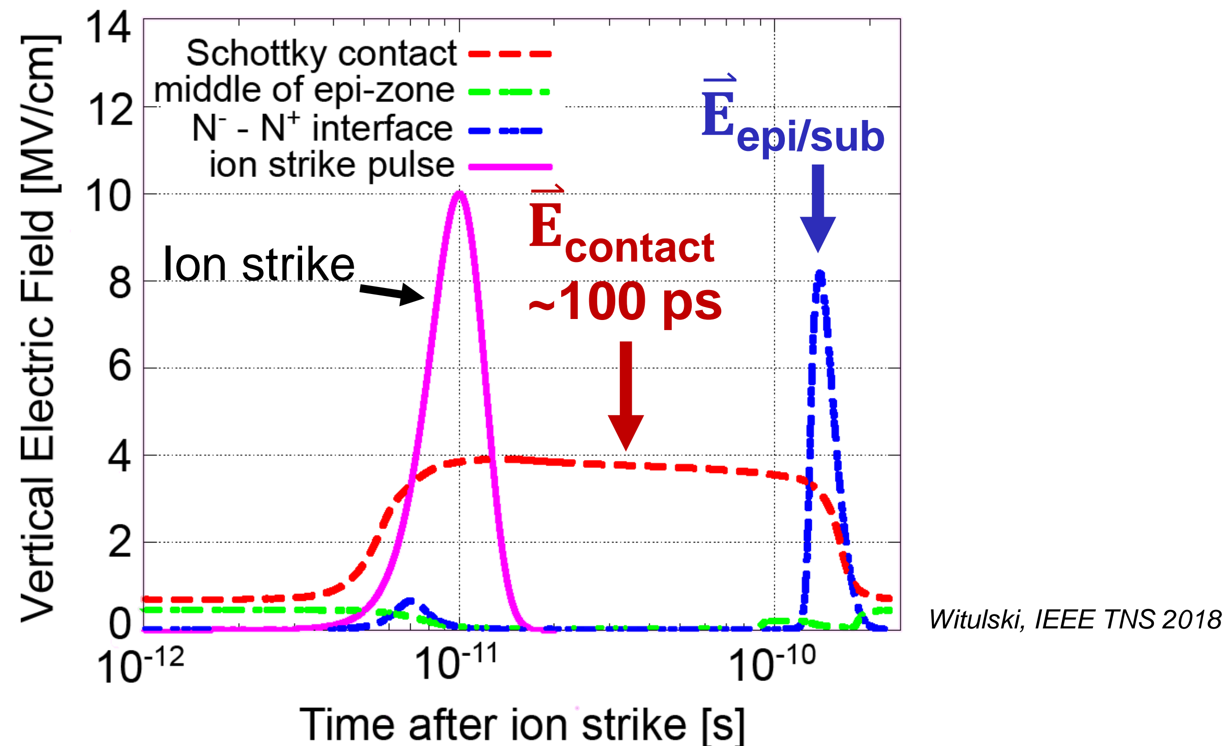
Image: Shoji, et al., © (2014) The Japan Society of Applied Physics, used with permission.

Joule's law | SiC epi thickness | SEB

Source of High Power Density for SEB in Schottky Diodes

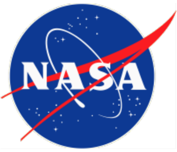


- **Key components for SEB in SiC Schottky diodes identified via TCAD:**
  - Duration of high $\vec{E}$-field at Schottky contact
  - Impact ionization then regenerative Schottky contact electron injection for thermal runaway at the contact interface
    - See Kuboyama, IEEE TNS, 2019

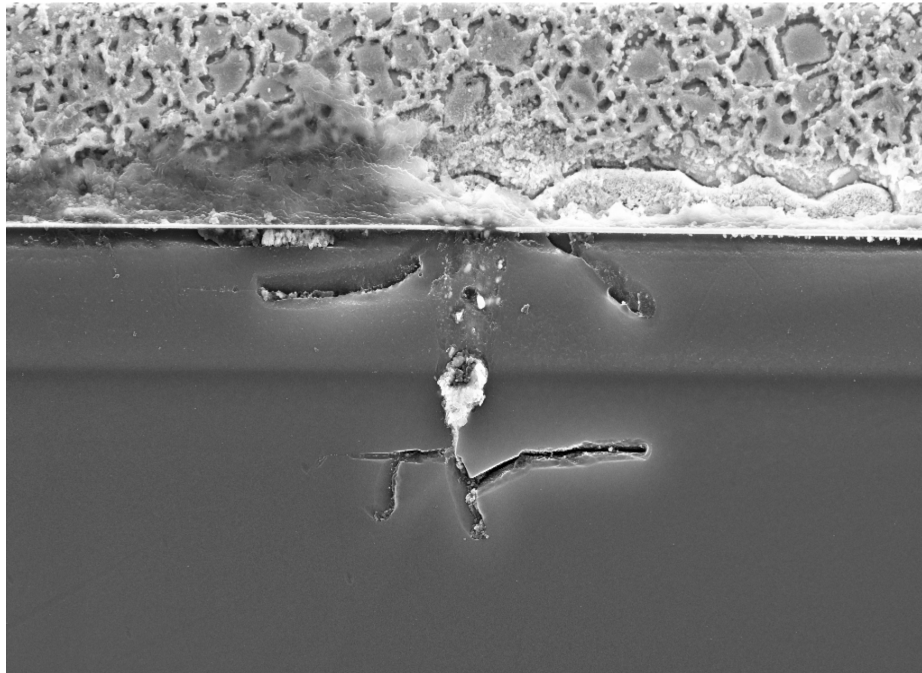


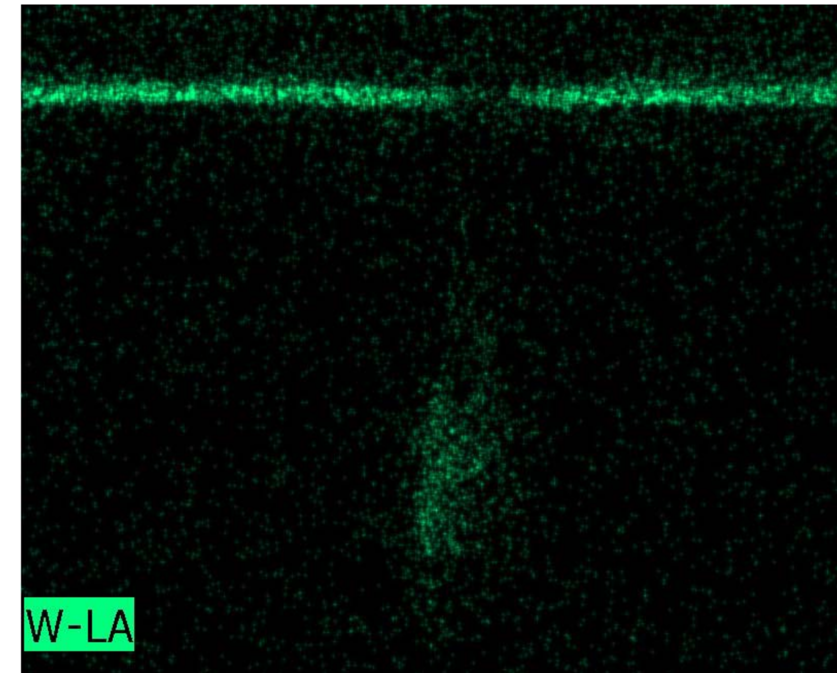
Witulski, IEEE TNS 2018

Source of High Power Density for SEB in Schottky Diodes

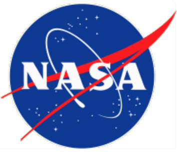


- **Failure analysis in silicon Schottky diodes:**
  - Significant heat at both interfaces causes cracking of the silicon
  - Schottky metal at the epi/substrate interface
  - Origin of SEB may be at the Schottky contact interface

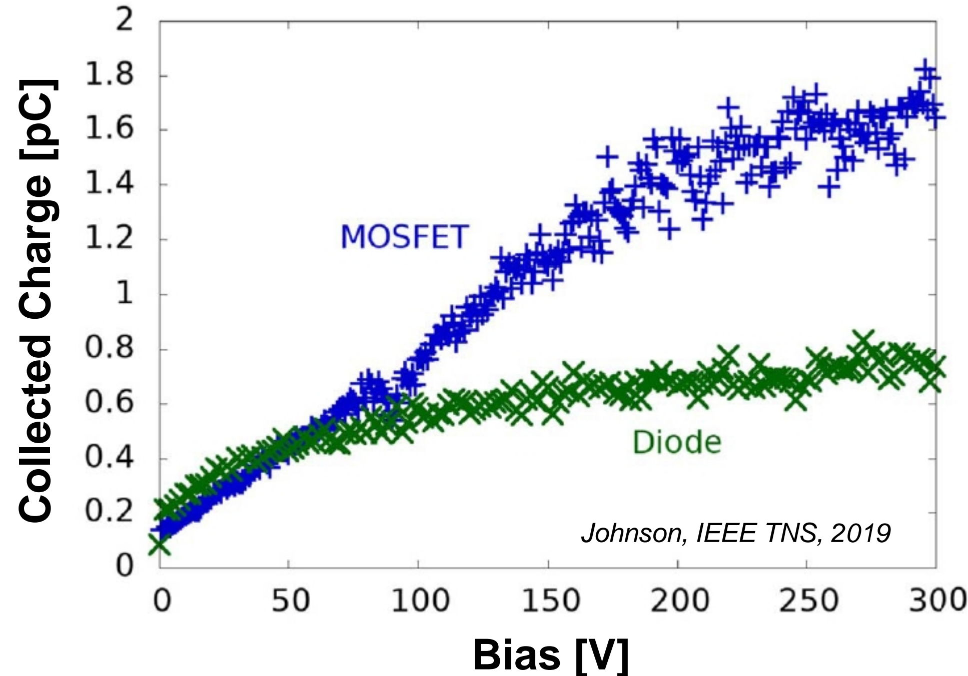




SiC MOSFET SEB: Minimal Parasitic BJT Involvement

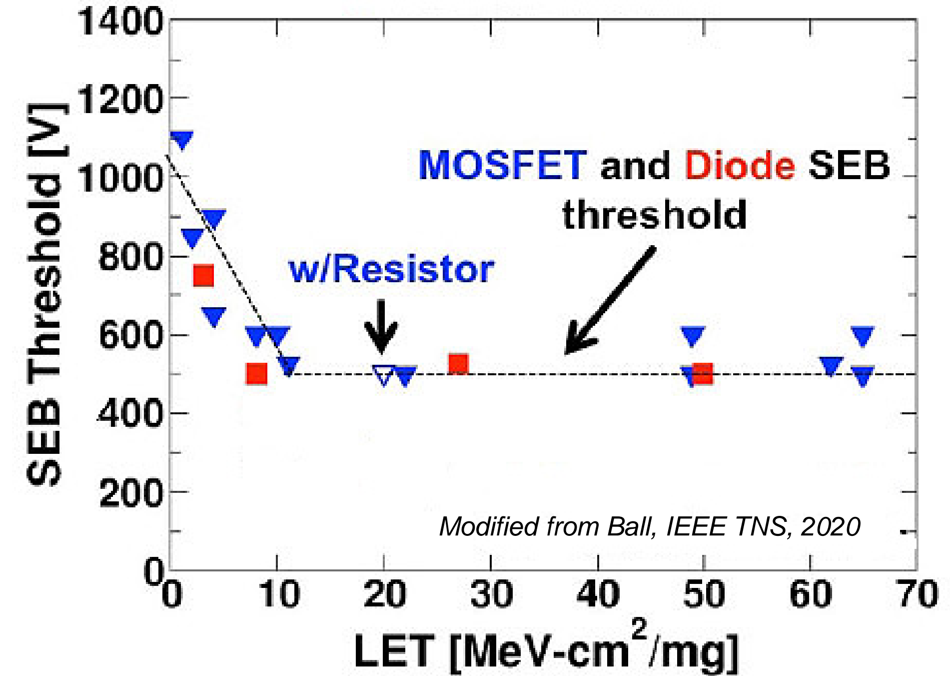


Evidence of BJT Turn-On



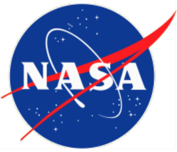
- Pulsed laser tests of matched MOSFET & diode show MOSFET charge amplification
  - Johnson, IEEE TNS, 2019
- TCAD simulations show run-away current
  - Witulski, IEEE TNS, 2018

Data Do Not Support BJT Involvement

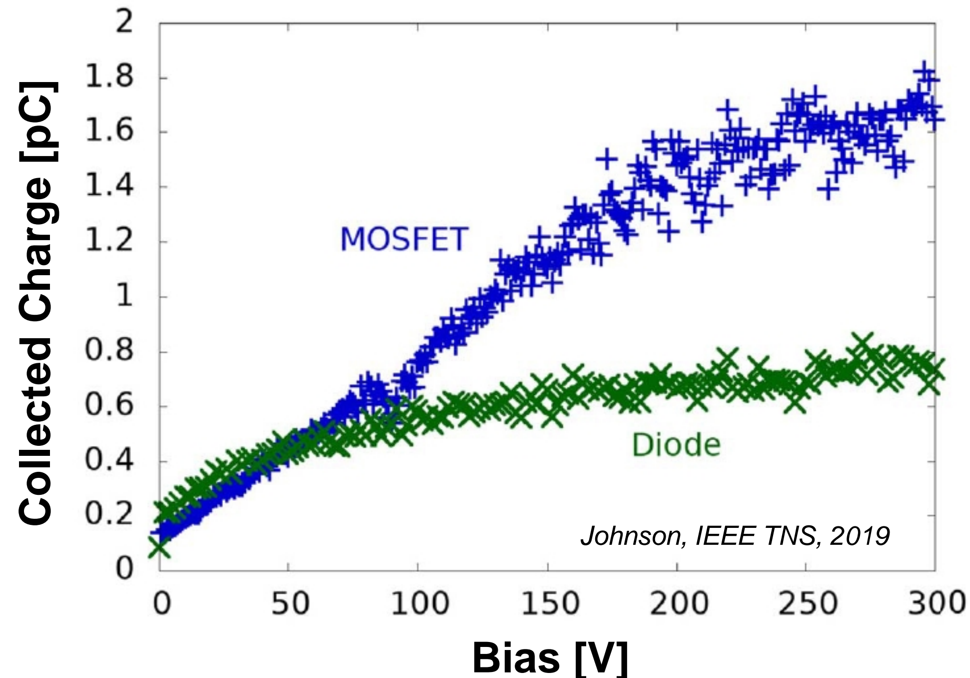


- SEB voltage in MOSFET = Diode
- SEB protective mode testing fails
  - Ball, IEEE TNS, 2020
- Removal of MOSFET n+ source implant yielded similar simulated max lattice temperature
  - Shoji, Microelectronics Reliability, 2015

SiC MOSFET SEB: Minimal Parasitic BJT Involvement

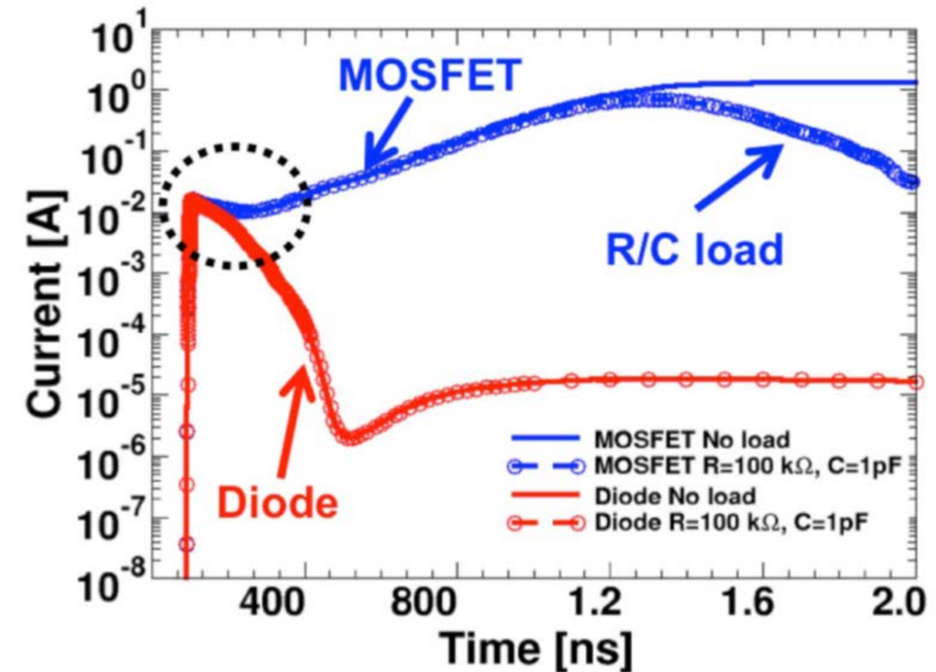


Evidence of BJT Turn-On



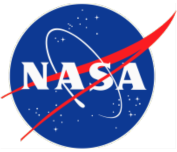
- Pulsed laser tests of matched MOSFET & diode show MOSFET charge amplification
  - Johnson, IEEE TNS, 2019
- TCAD simulations show run-away current
  - Witulski, IEEE TNS, 2018

TCAD Explanations



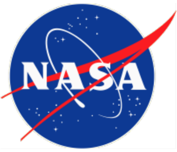
- MOSFET & diode similar only in first ~100 ps
- SEB protection circuitry too slow
  - Ball, IEEE TNS, 2020
- Note TCAD sims of increased substrate resistance showed decreased max temperature
  - Abbate, IEEE TNS, 2015

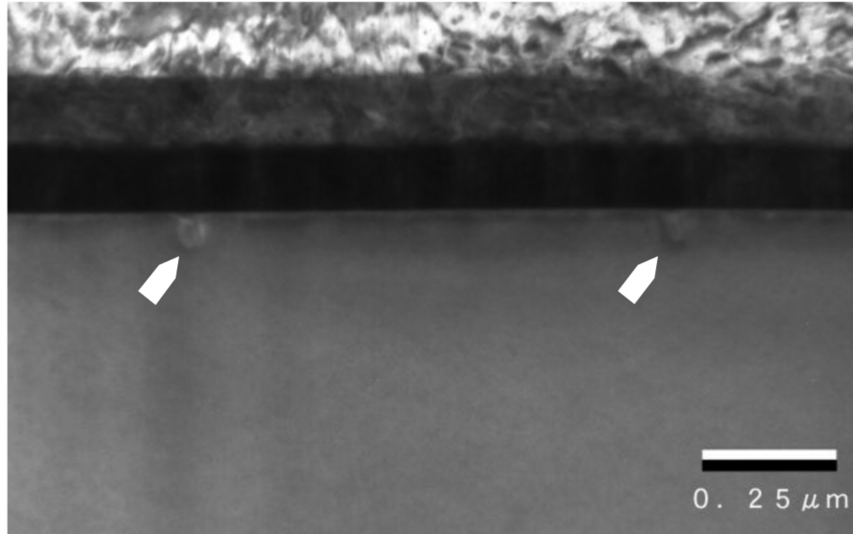
SiC SEB Mechanism Identification Still a Work in Progress



- **Areas of agreement:**
  - Electric field strength causing high power density
  - Rapid time to failure (10's to ~100 ps)
  - Similar mechanisms between diodes and MOSFETs (no parasitic BJT involvement)
  - Impact ionization necessity
  - Need for sustained electric field
- **Areas for refinement:**
  - Mechanisms for sustaining the electric field
  - Location of peak temperature
  - Conflict between data and TCAD simulations given similarity of MOSFET and Schottky diode SEB susceptibility
    - Peak temperature at Schottky contact vs. MOSFET epi/substrate interface
    - Role of Schottky contact electron tunneling

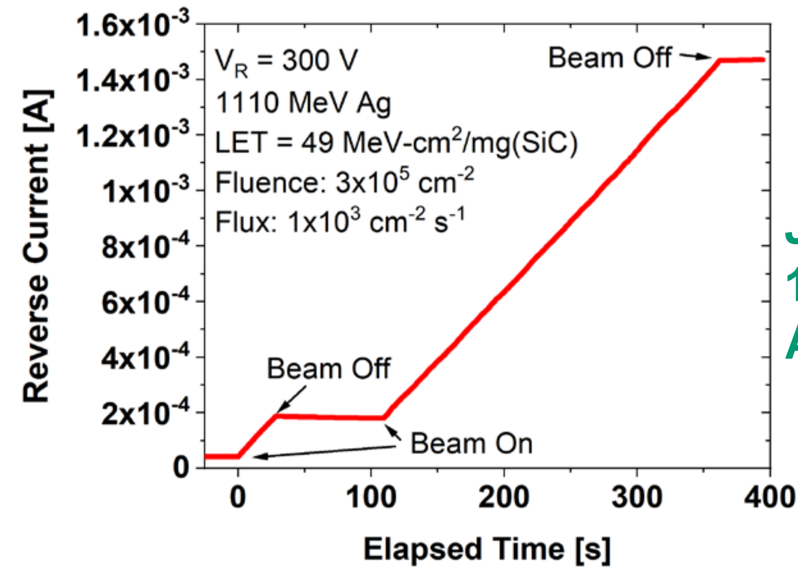
SiC Single-Event Effects – Leakage Current



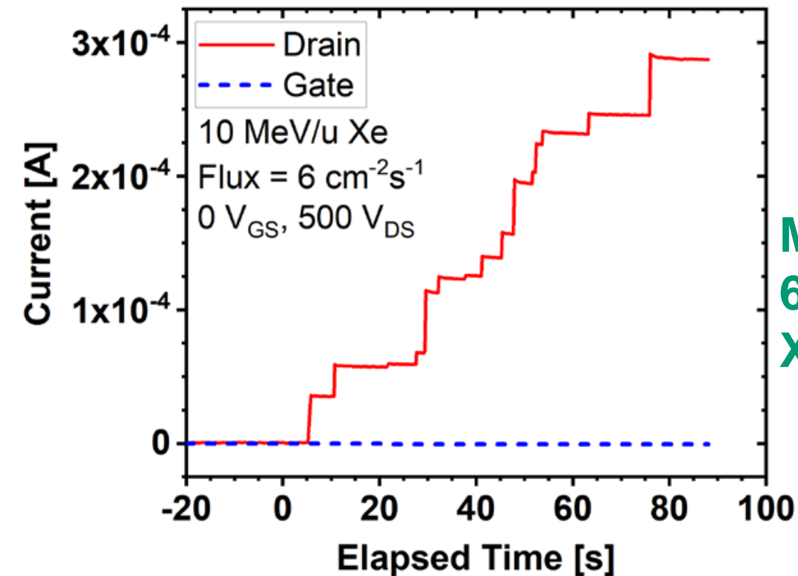


50 nm x 70 nm damage sites in SiC SBD: 3 MeV/u Xe while at 26% of rated V_R

Kuboyama, IEEE TNS, 2006



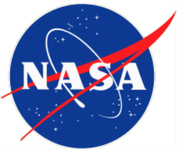
JBS I_R during $1x10^3$ cm^{-2} s^{-1} Ag exposure



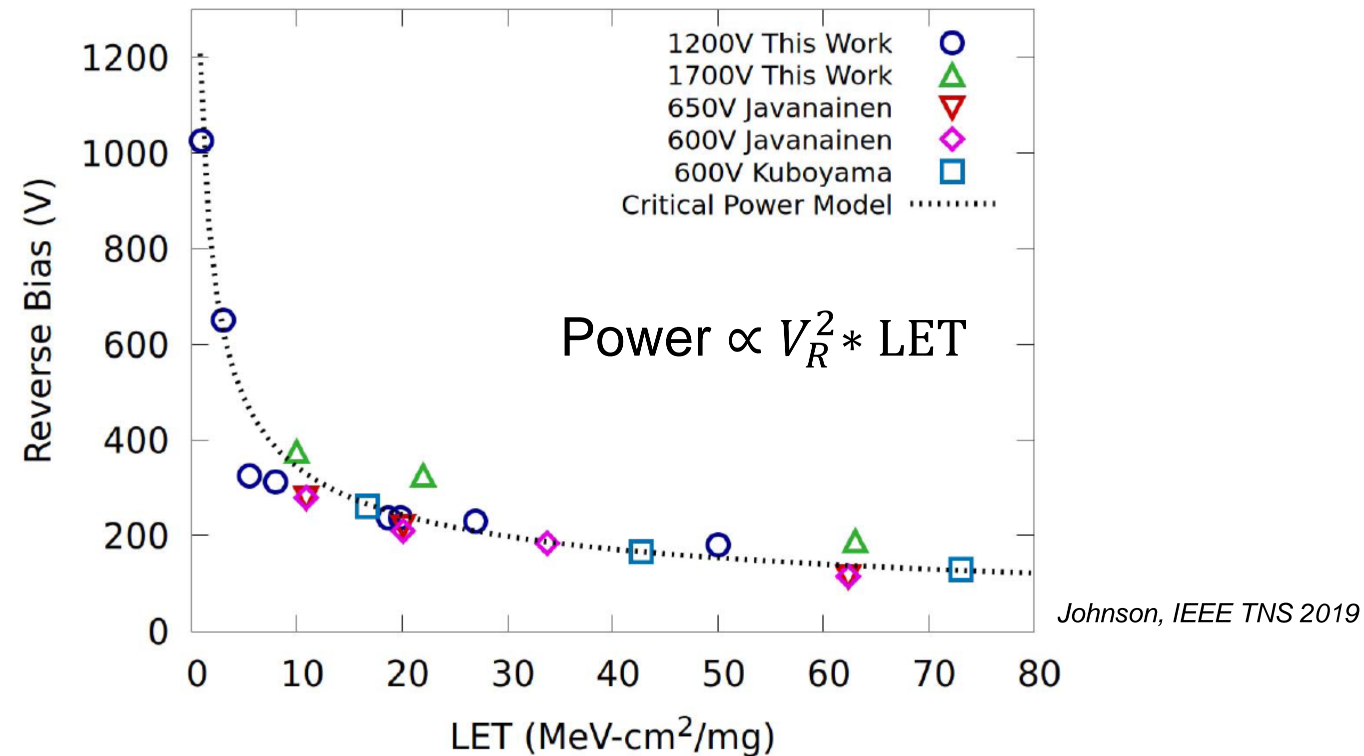
MOSFET I_D 6 cm^{-2} s^{-1} Xe exposure

Individual ion strikes create areas of thermal damage that differ from displacement damage

Degradation Mechanisms: SiC Schottky Diodes



- **600 V – 1700 V SBD & JBS diodes require the same critical power density for onset of damage**

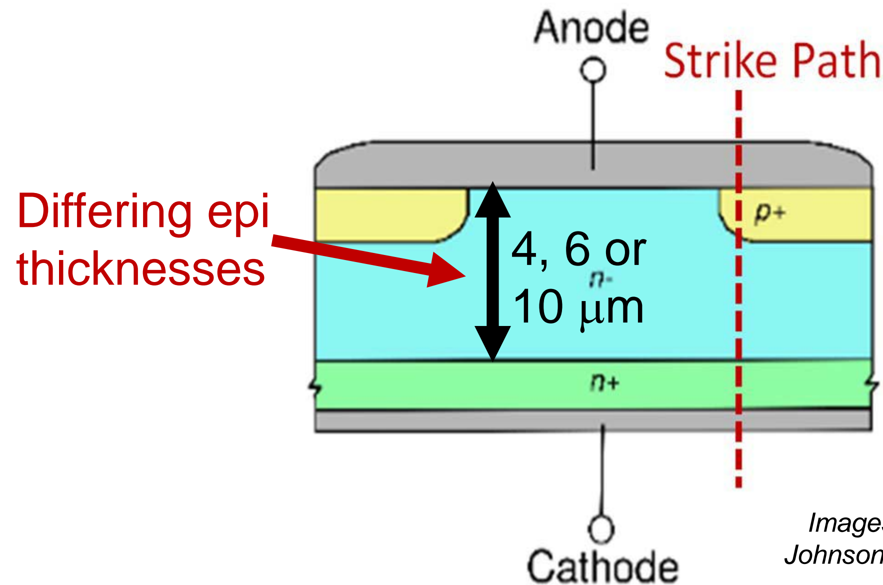


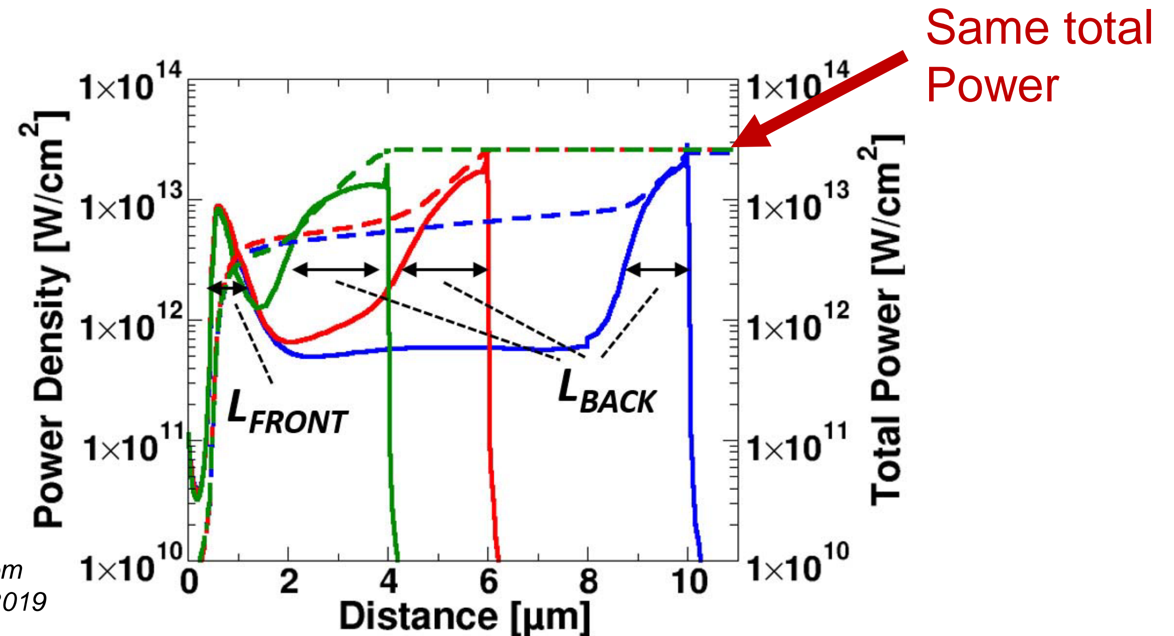
Johnson, IEEE TNS 2019

Degradation has minimal dependence on rated breakdown voltage

Minimal Dependence on Rated Breakdown Voltage Explained

- $\vec{E}$-field maxima at the epi/sub. interface & near the Schottky contact due to ion strike
- Much of the epilayer thickness is not dissipating significant power
- Thus similar total power dissipation regardless of epi thickness & rated voltage

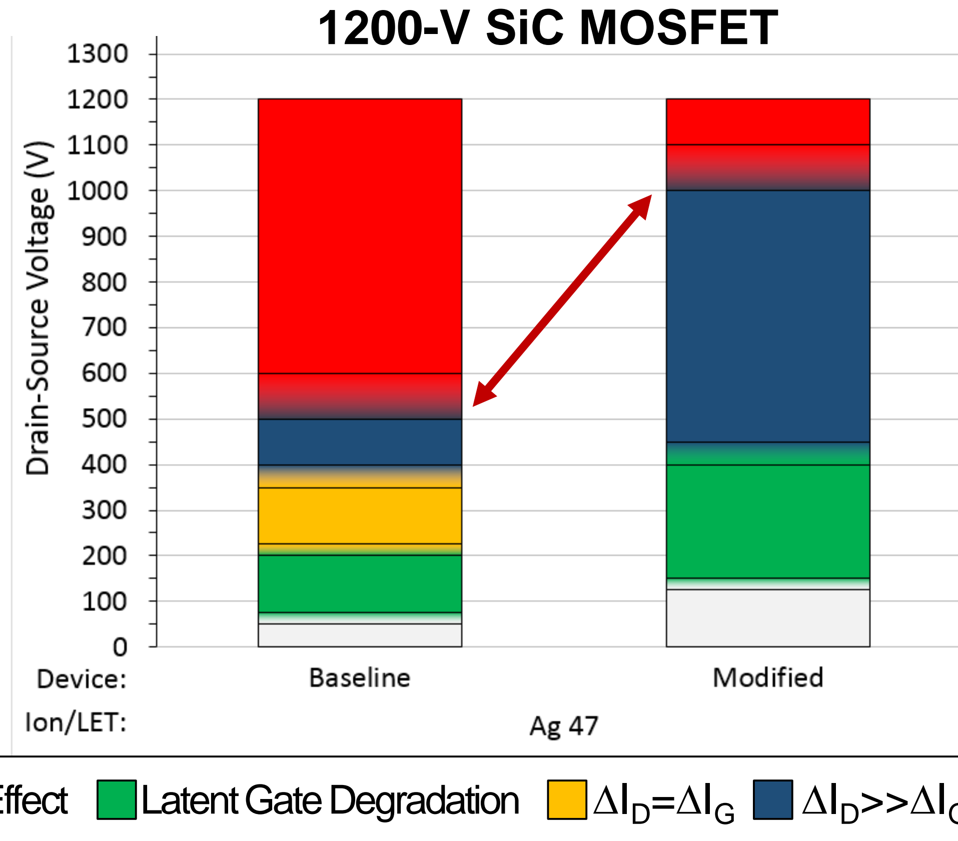




Images modified from Johnson, IEEE TNS 2019

Implication: Minimal benefit from derating higher-voltage parts vs. using a part with lower breakdown rating!

Mechanisms in Action: Hardening by Process

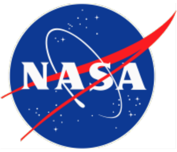


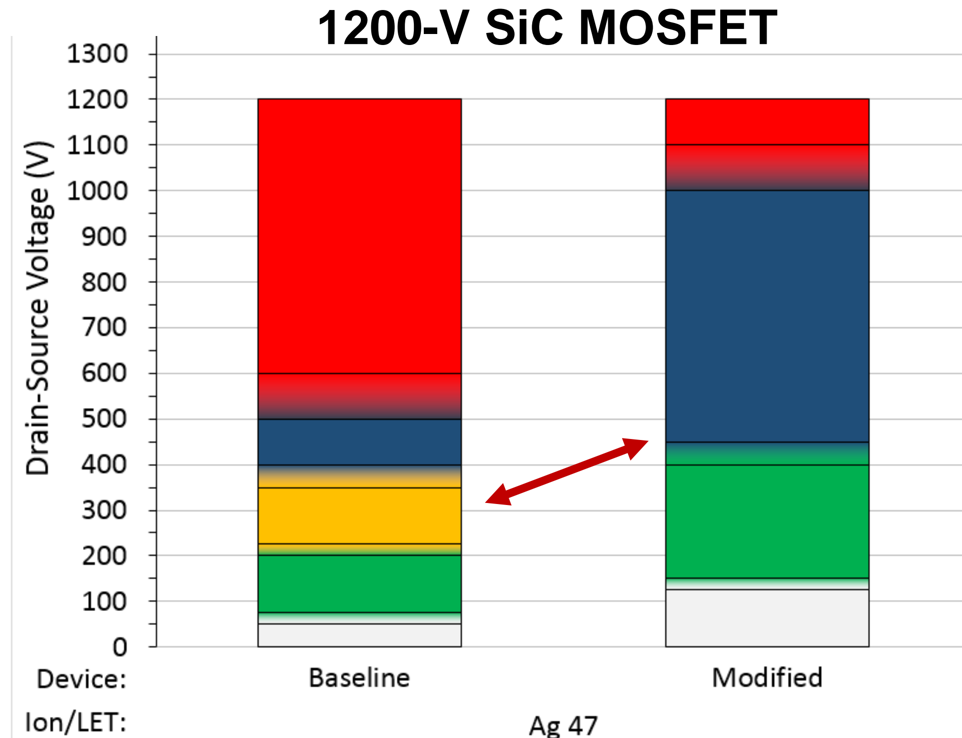
After Zhu, X., et al., 2017 ICSCRM

- **Reduced SEB susceptibility**
  - Thicker epilayer

Just as with silicon MOSFETs, epilayer optimization must be done to balance SEE tolerance with on-state resistance (R_{DS_ON}) performance

SiC Radiation Hardness by Process: 1200 V MOSFET



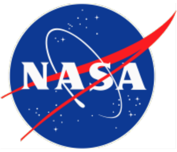


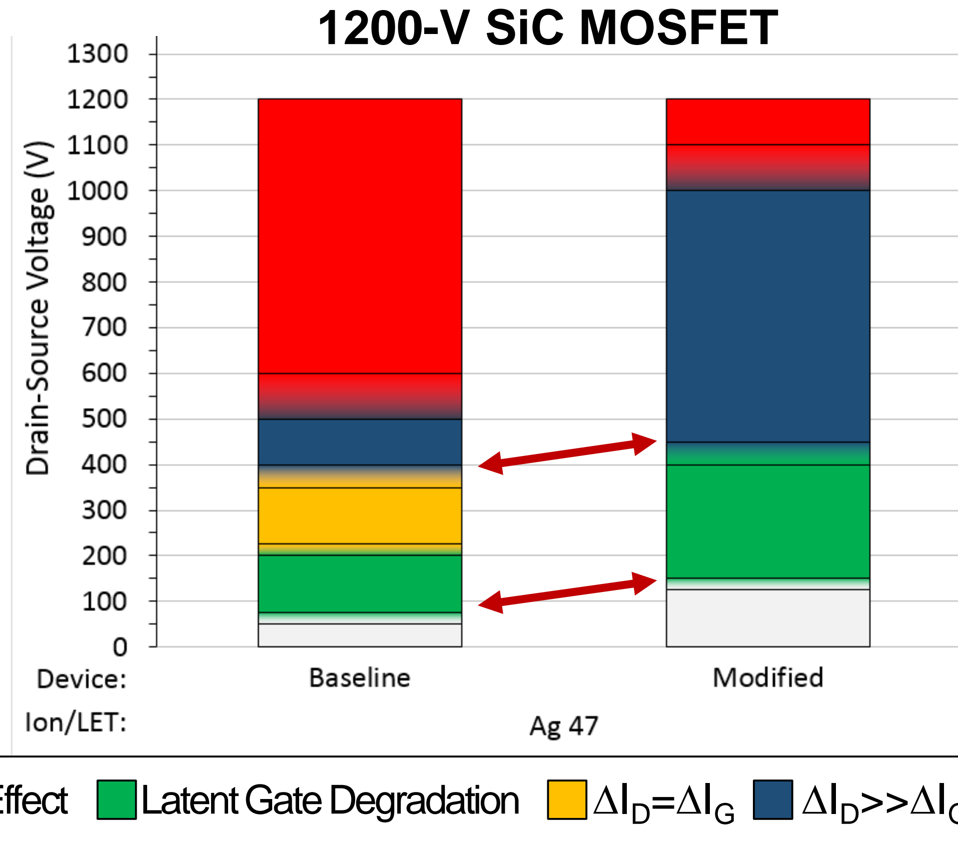
After Zhu, X., et al., 2017 ICSCRM

- **Reduced SEB/GR susceptibility**
  - Thicker epilayer
- **Degradation of I_{DG} eliminated**
  - Drain neck width reduction

Elimination of drain-gate leakage current degradation mode is possible through established silicon MOSFET hardening techniques

SiC Radiation Hardness by Process: 1200 V MOSFET

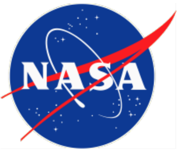




After Zhu, X., et al., 2017 ICSCRM

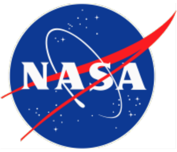
- **Reduced SEB/GR susceptibility**
  - Thicker epilayer
- **Degradation of I_{DG} eliminated**
  - Drain neck width reduction
- **Minimal change in onset of other degradation effects:**
  - $\Delta I_D >> \Delta I_G$
  - latent gate damage
- **Rate of degradation at a given voltage is likely reduced**

Continued research and development efforts are necessary to understand residual degradation mechanisms!

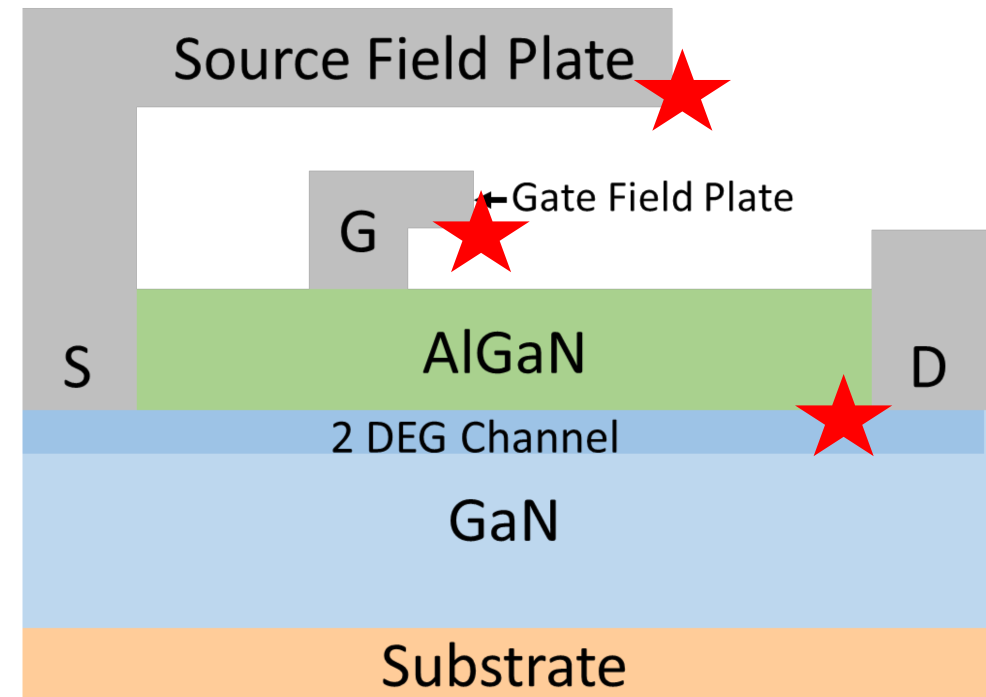


GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) RADIATION EFFECTS

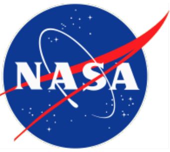
GaN HEMT Single-Event Effects



- **Power GaN HEMT structure**
  - Lateral device
  - Insulators under field plates
  - Possible gate oxide/insulator
  - No p-n junction - cannot avalanche
  - Breakdown voltage >> rated voltage
- **SEEs include:**
  - Leakage current degradation
  - Single-event burnout
  - Single-event dielectric rupture (SEDR)

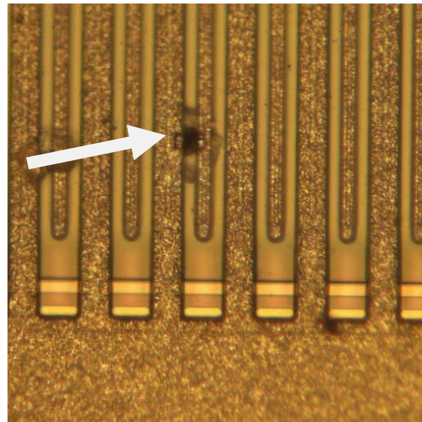


GaN HEMT SEE Failure Thresholds



- **SEE data vary:**
  - Multiple HEMT designs
  - Lot-lot variability
  - Generational variability
- **Guaranteed SEE-free HEMTs exist**
  - Max 300 V

SEB mark on gate contact

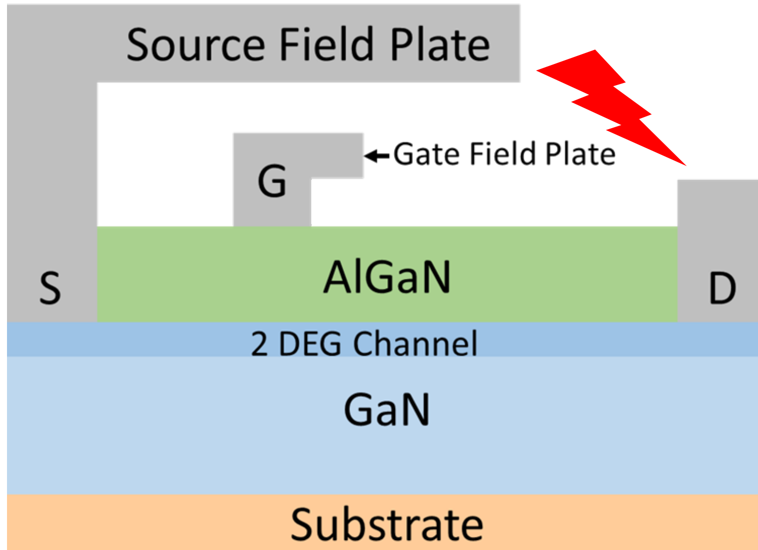


Images: NASA JPL, courtesy of L. Scheick

- **Susceptibility tends to increase with voltage rating, with exceptions**
  - Expect 40 V parts to pass at 40 V
  - 100 V & 200 V parts:
    - some only degradation;
    - others SEB susceptibility
  - Expect SEB in ~ 600 V p-gate parts ~50% of rating at LET ~ 40 MeV-cm^2/mg(Si)

GaN HEMT SEE thresholds vary; Guaranteed SEE-free parts are available

GaN HEMT Dielectric Rupture



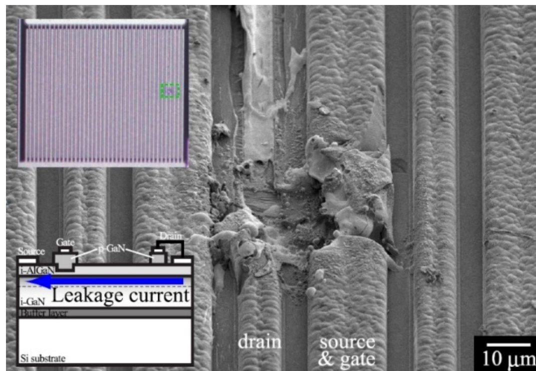


Image: Mizuta, et al., IEEE TNS 2018

- **SEDR: Source-Drain Shorting**
  - Worst-case angle parallel to channel
    - Also occurs at normal incidence
  - Simulations suggest ion strike at edge of field plate necessary at normal incidence
    - see Zerarka, IEEE TNS 2017
  - Low cross section for failure
    - Supports simulation findings

Field plate design will likely affect SEDR susceptibility

GaN HEMT Single-Event Burnout

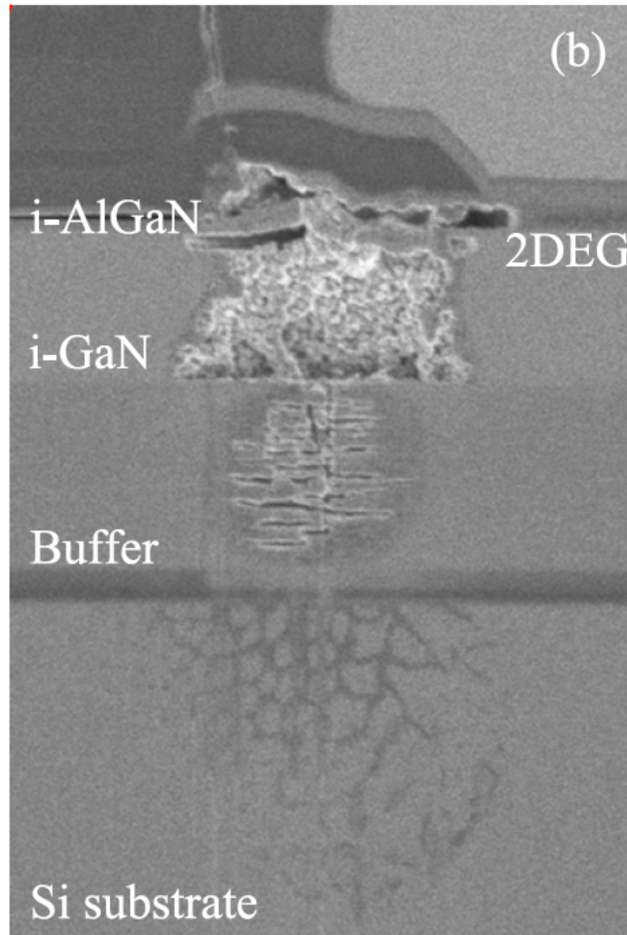
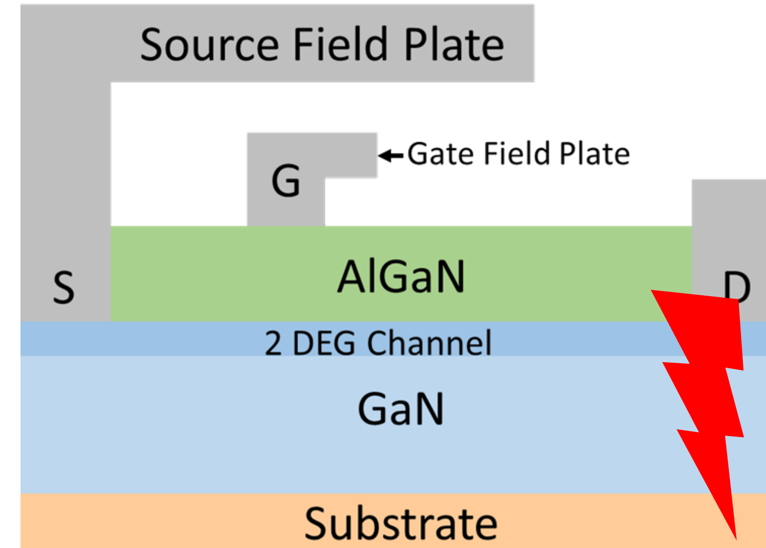


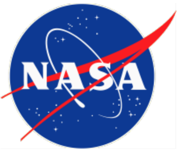
Image: Mizuta, et al., IEEE TNS 2018



- **SEB: Drain-substrate**
  - Requires ion range into substrate
    - see Zerarka, IEEE TNS 2017
  - Higher threshold V than for SEDR (for same part type) but higher cross section too

GaN HEMTs can have multiple catastrophic SEE failure modes

GaN HEMT Single-Event Leakage Current



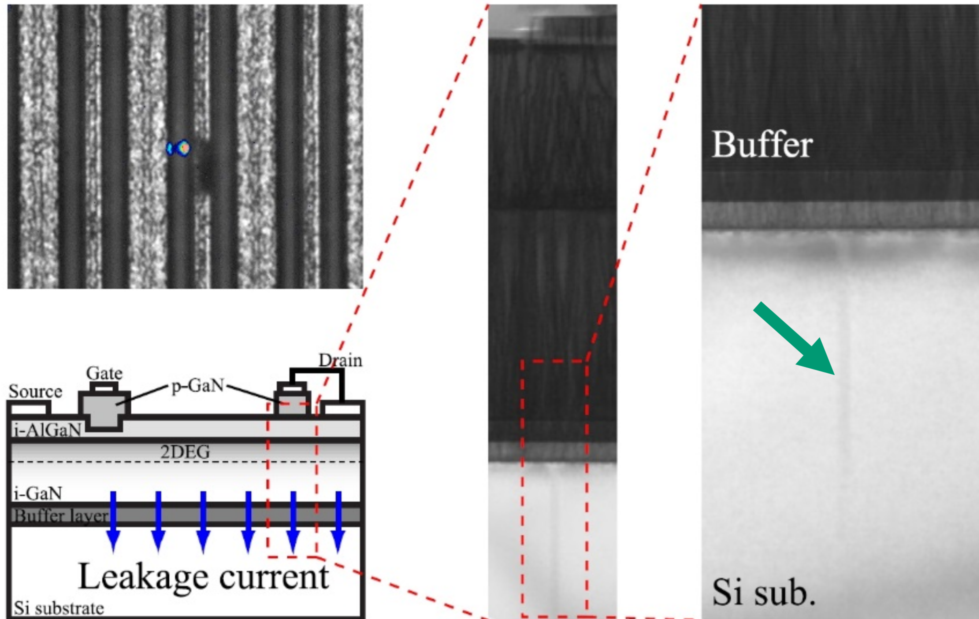
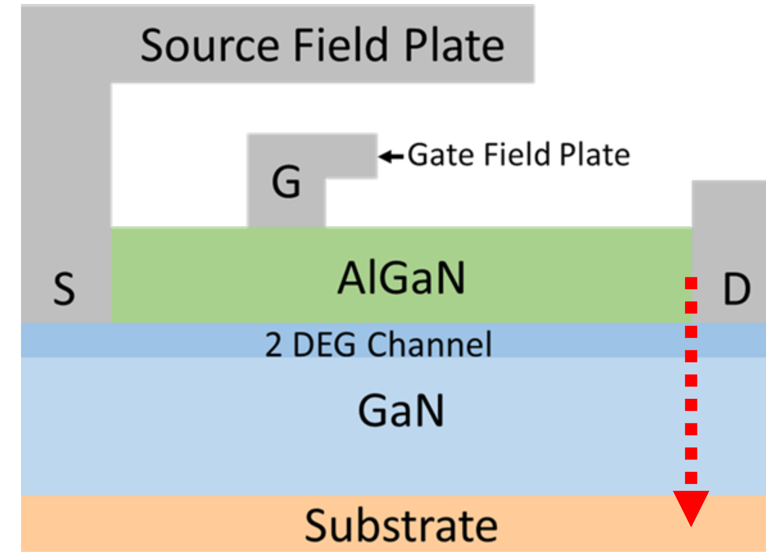


Image: Mizuta, et al., IEEE TNS 2018

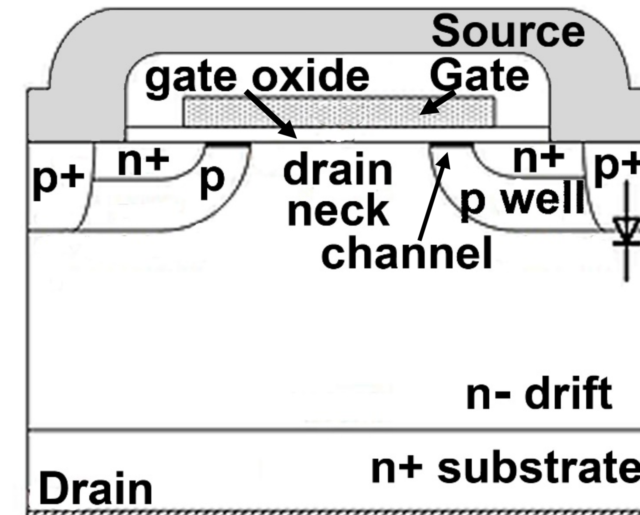


- **Drain-substrate non-catastrophic leakage current degradation**
  - Large drain SETs correlated with leakage current increase
    - see Abbate, Microelectron Reliab, 2015
- **Drain-Gate leakage current degradation reported in normally-on GaN HEMTs**
    - see ex/ Kuboyama, IEEE TNS 2011

RADIATION HARDNESS ASSURANCE CHALLENGES

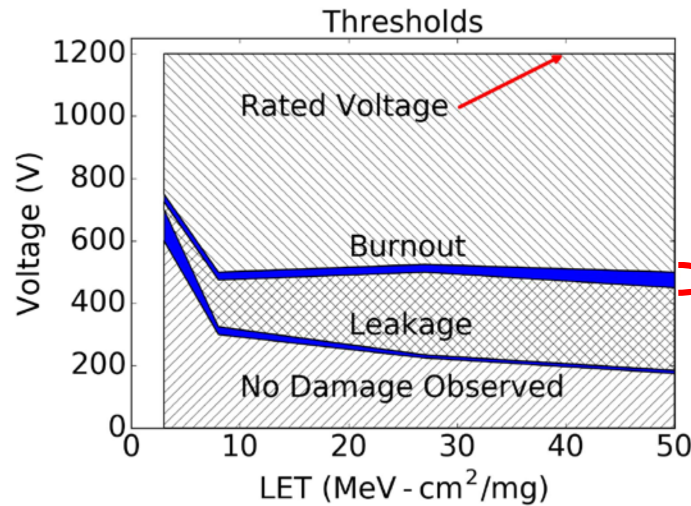
Heavy-Ion Test Methodology for Silicon Power MOSFETs

- **Worst-case ion beam conditions for VDMOS (and the JESD57 standard)**
  - Normal incidence
  - Ion Bragg peak at epi/substrate interface
- **Rationale**
  - Allows more accurate comparison of SEE tolerance between device offerings
  - Eliminates bond-wire shadowing effects
  - Safe-operating area accurate for all lighter ions
- **Test Goals**
  - Define safe operating area, and/or
  - Obtain SEB cross-section curves

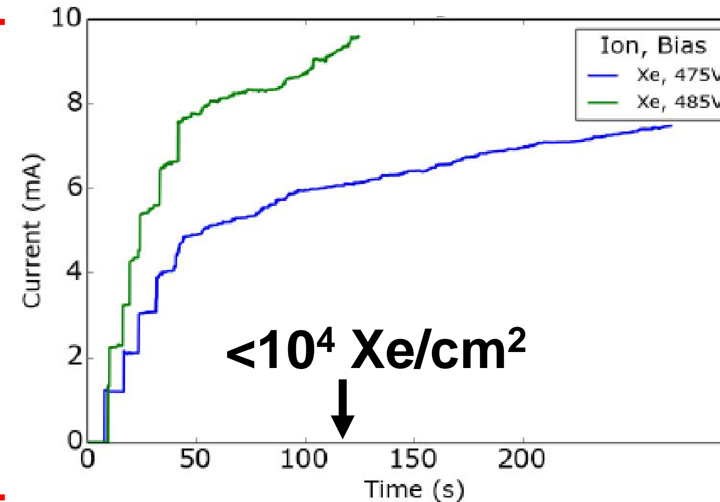


Silicon power MOSFET test methods are based on decades of test data and research into the mechanisms of failure in VDMOS

Silicon Carbide SEB Test Challenges



Witulski, IEEE TNS, 2018

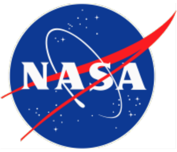


Witulski, IEEE TNS, 2018

- **Ion-induced leakage current (I_R) can impact SEB susceptibility if SEB does not occur early in the beam exposure**
- **Achievement of test method fluence levels may not be possible, and may provide misleading data**

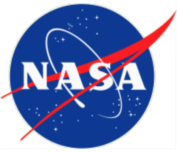
Difficult to obtain accurate SEB safe operating area

RHA Guidance: SiC Testing Recommendations



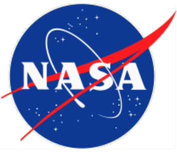
- **Ion beam selection:**
  - **Thinner epilayer means lower-energy ions can penetrate into the substrate**
  - **In addition to mission requirement conditions, consider lighter ion/lower LET tests to:**
    - Aid on-orbit risk assessments
    - Reveal differences between parts
- **Test fluence:**
  - **Dictated by test goals and degradation response of the device**
  - **Non-catastrophic damage can *increase* the threshold voltage of SEB**
    - Identification of the threshold voltage yielding the maximum cross section will be identified instead
  - **Rate of degradation of leakage current is not dependent on prior history**
    - Until the rate is no longer constant
- **Temperature:**
  - **Unestablished effects on SEB**
    - Impact ionization is hole-driven unlike in silicon
  - **Some data suggest non-catastrophic degradation rate increases with temperature**

RHA Guidance: GaN HEMT Test Recommendations



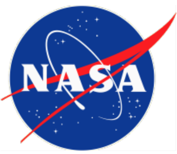
- Ion beam selection
  - Safe operating areas (SOAs) can be identified
    - Valid for the tested lot only
    - Part-part variability reduces confidence – larger sample sizes advised
    - Effects are LET-dependent; range should penetrate into the substrate
- Sample and test setup considerations
  - Lot-specific heavy-ion testing is necessary until consistency becomes routine
    - Each wafer is often one “lot”
  - Packaging is designed for minimal inductance and maximum heat extraction
    - Consider impact of decapsulation, wire-bonding, and restricted die access
  - Susceptibility may depend on test circuit design and methods
    - Voltage stress introduces defects: do not exceed rated voltage on the drain during post-rad characterizations
    - Gate structures have limited voltage ratings – minimize systematic transients
- Temperature Effects are not established

RHA Guidance: Risk Assessment

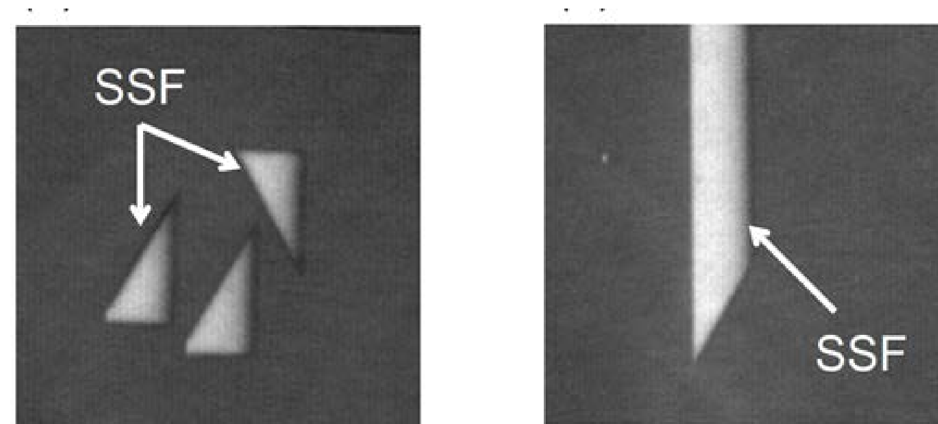


- **(Unvalidated) failure rate prediction methods developed for Si and SiC power devices may provide an upper bound**
  - Allow additional margin for uncertainty of SiC SEB voltage threshold
  - Consider that steradian window of vulnerability may change with voltage
    - see Javanainen, IEEE TNS, 2017
    - For risk-tolerant applications, margin and unpowered redundancy is advised
- **Non-catastrophic damage has unknown longer-term effects**
  - Extent of damage is part-to-part variable
  - Consider application temperature and functional lifetime requirements
    - For risk-tolerant applications, margin and unpowered redundancy is advised
  - Life tests of damaged parts may reveal higher-likelihood failure modes - sample size will limit discovery of rarer modes

Beyond Radiation Effects: Other Reliability Challenges
SiC



- **Threshold gate voltage instability**
  - MOS oxide near-interface positively-charged trap switching due to tunneling electrons
  - Degree of instability depends on temperature, gate bias, and duration of the bias
  - **Reliability concern when threshold voltage drifts negative and increases leakage current during high drain blocking conditions**
- **Large Shockley stacking faults (SSF) can form from basal plane defects**
  - Due to carrier injection and energy release from recombination
  - **Cause increase in leakage current and on-state resistance, and decrease reliability**

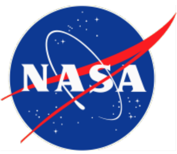


Images: Kimoto, IEEE IRPS, 2017

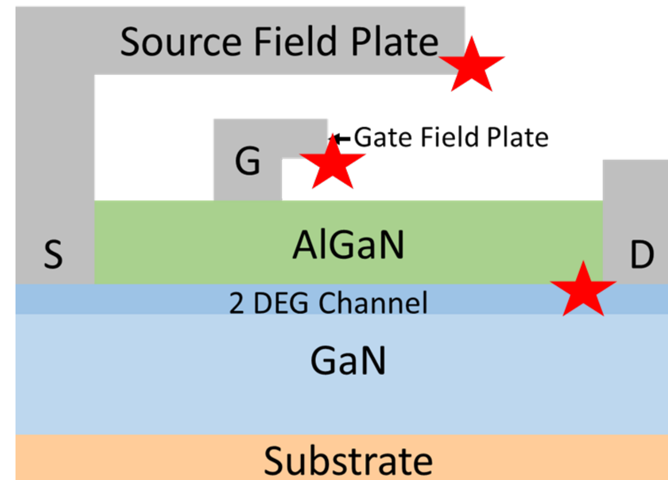
200 µm

→ [11$\bar{2}$0]

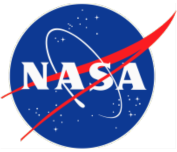
Beyond Radiation Effects: Other Reliability Challenges GaN



- **High-field induced degradation under normal operation**
  - In blocking state, time-dependent degradation between drain-side of gate and channel due to degradation of gate passivation
  - High fields in p-doped gate increase gate leakage current
  - Vertical fields degrade pathway between drain and substrate
- **Dynamic on-state resistance (R_{DS_ON}) (same as current collapse)**
  - Increased R_{DS_ON} due to electron trapping in off-state; recovers as electrons detrap during device turn-on, but causes variable power efficiency
  - Value of R_{DS_ON} dependent on measurement procedure
    - JEDEC guideline released to standardize measurement of R_{DS_ON}

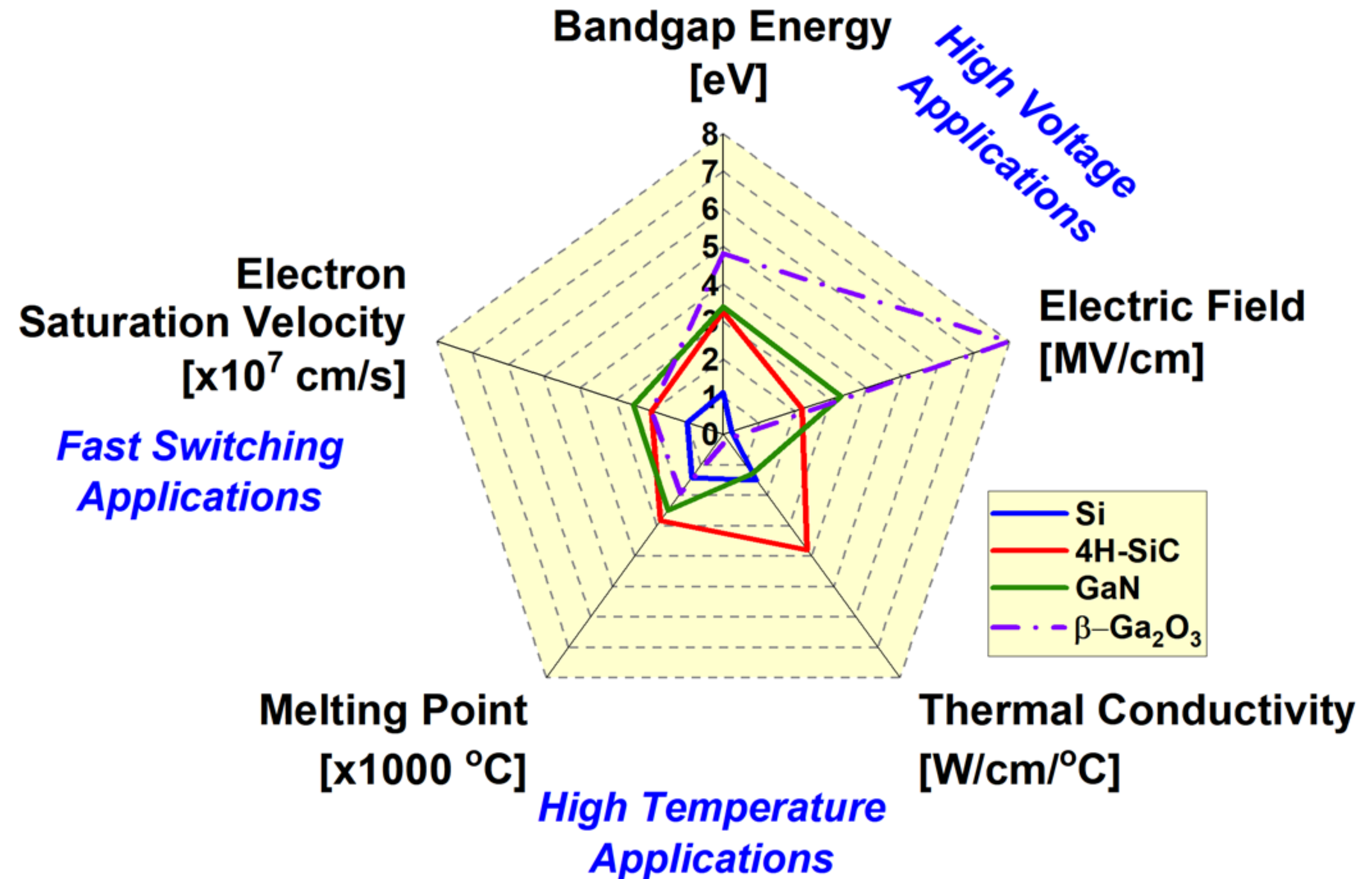


To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020



A LOOK TO THE FUTURE:
GA_2O_3 ULTRA-WBG POWER TECHNOLOGY

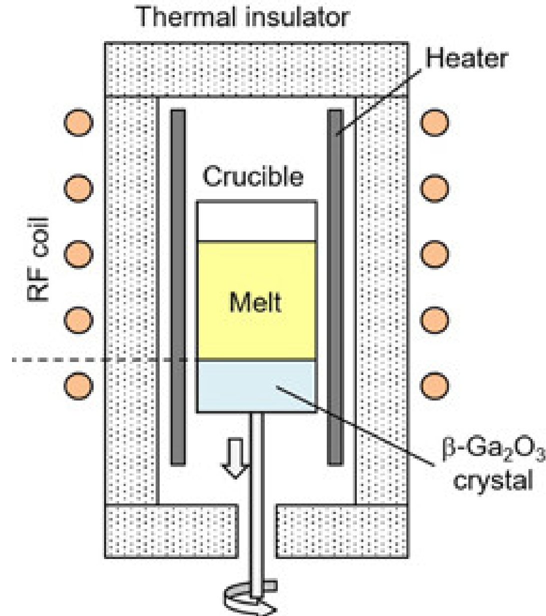
Overview: Ga_2O_3 vs. Si, GaN, and SiC



Ga_2O_3 offers a breakdown electric field over 2x larger than that of SiC or GaN – for high-voltage, low-loss applications

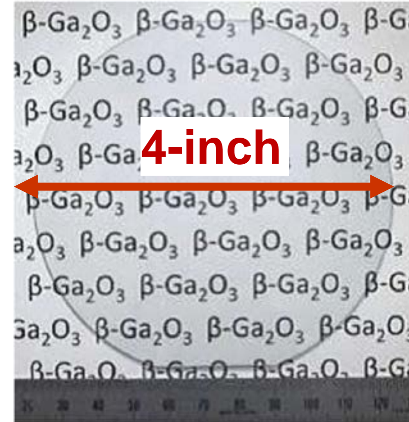
The Promise of Gallium Oxide

β-Ga_2O_3 grown from melt, not vapor



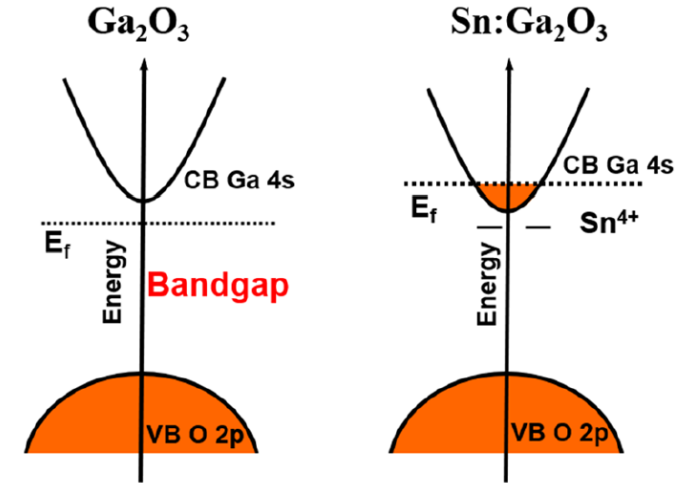
Ahmadi, JAP, 2019. Used with permission.

4" wafers now 6" demonstrated



Modified from Hidahiwaki,, © IEEE, 2015

Easy activation of n-type dopants



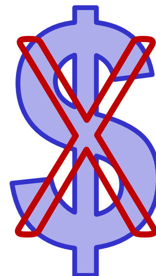
Zhang, APL Mater, 2020. CC BY license.

Modeled 6" wafer cost:

SiC: $916

Ga_2O_3: $283

Reese, *et al.*, Joule, 2019



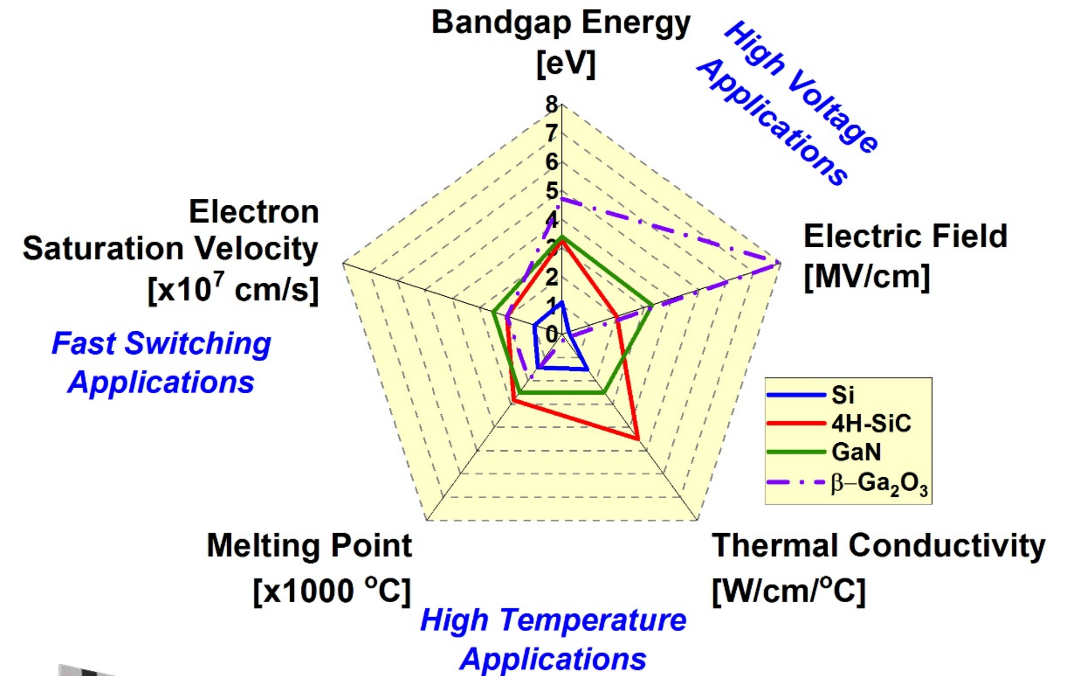
Large automotive supplier has invested in α-Ga_2O_3

DENSO and Kyoto University Startup FLOSFIA will Develop Next-Gen Power Semiconductor Device for Electrified Vehicles

Denso.com news release, Jan. 4, 2018

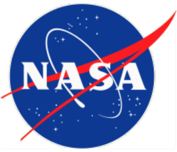
The Challenge of Gallium Oxide

- **p-type conductivity not expected**
  - Challenge for normally-off transistors
  - Impacts field termination techniques
- **Ga_2O_3 e^- mobility << SiC or GaN**
  - some offset by high v-sat and E-field
- **Low thermal conductivity**
  - Must mitigate for mid-high speed use



Material property hurdles will require creative breakthroughs

The Status of Ga_2O_3 Power Device Development



NICT
BGO MESFET [86]

Notre Dame
Exfoliated BGO FET [95]

AFRL
BGO FET with E_{crit} > GaN, SiC [89]

AFRL
BGO FET Switch Loss < Si [114]

NICT
Implanted BGO MOSFET [46]

AFRL
HV E-MODE BGO MOSFET [111]

OSU
Delta-doped BGO FET [26]

NICT
BGO MOSFET [45]

2012 2013 2014 2015 2016 2017 2018 2019

NICT
HV BGO FP-MOSFET [88]

AFRL
RF BGO FET [116]

Buffalo
> 1kV Lateral BGO MOSFET [132]

OSU, UCSB
MODFET Si-doped [24], Ge-doped [140]

BGO = β-Ga_2O_3
HV = High Voltage
FP = Field Plate
E-Mode = Enhancement Mode

Chart from: Chebak, Semicond Sci Technol, 2019. https://doi.org/10.1088/13616641/ab55fe.
Used under CC BY 3.0 license

Despite hurdles, many advances have occurred since the early 2010's!

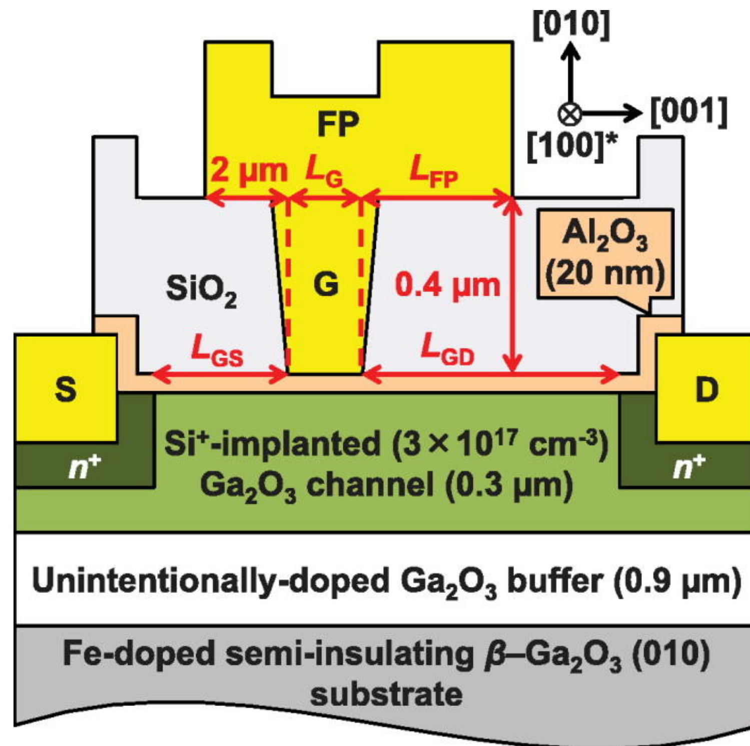
Ga_2O_3 Radiation Effects: Displacement Damage

- **Expect similar DDD hardness as GaN:**
  - Similar atomic bond strength
  - Ga vacancies are dominant defects in both
- **Carrier removal rate found to be similar to SiC and GaN,**
  - but thinner active area of Ga_2O_3 devices should be an advantage
- **Significant recovery with 500 °C annealing**

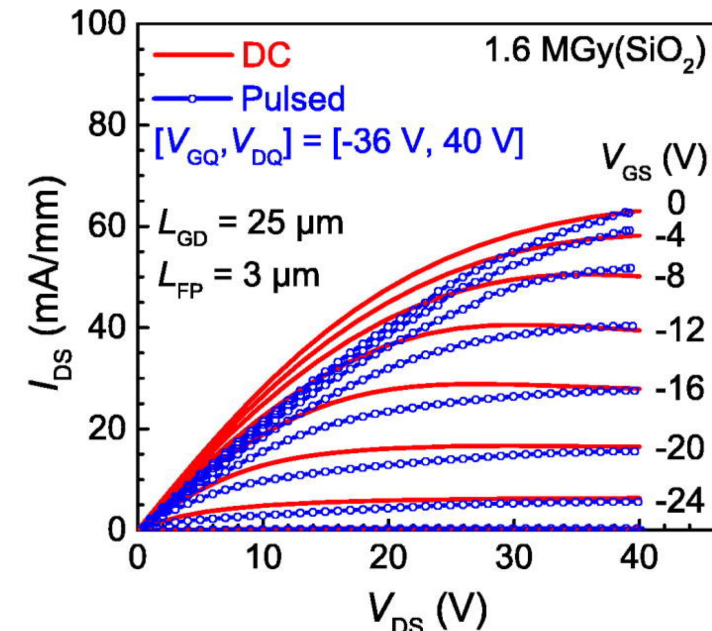
β-Ga2O3 shows good DDD performance comparable to SiC and GaN

Total Ionizing Dose Effects in a β-Ga_2O_3 MOSFET

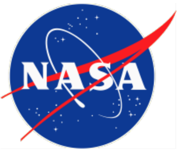
- **MOSFET & MOSCAPs**
  - 20 nm Al_2O_3 gate dielectric
  - 400 nm SiO_2: support field plate and passivate
- **Unbiased during ^{60}Co irradiation**



- **Gate leakage via trap-mediated conduction above 7 Mrad(SiO_2)**
- **160 Mrad(SiO_2):**
  - 10% - 20% increase in interface trapped charge based on flatband voltage shift
  - Charge trapped mainly at SiO_2/Al_2O_3 interface
    - **Caused dynamic R_{on}, and I_{DS} collapse**



Images: Wong, Appl Phys Lett, 2018. DOI: 10.1063/1.5017810. *Used with permission.*



Thank you for your attention!
Be sure to attend the SiC and GaN presentations during the Technical Sessions