National Aeronautics and Space Administration

On-orbit Servicing Assembly and Manufacturing (OSAM)

Technology Transfer Workshop

Journeying Longer and Seeing Farther

Sept 22-23, 2020

SpaceCube Technology Overview

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Science Data Processing Branch

Software Engineering Division

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Greenbelt, MD, USA

Outline

- Who Are We?
- What is SpaceCube?
  - Approach / Technical Design
  - Performance
  - Overview of Family Capability
- How Can SpaceCube Help?
  - Application Hardware Acceleration
  - Configurable Design System
- Conclusion

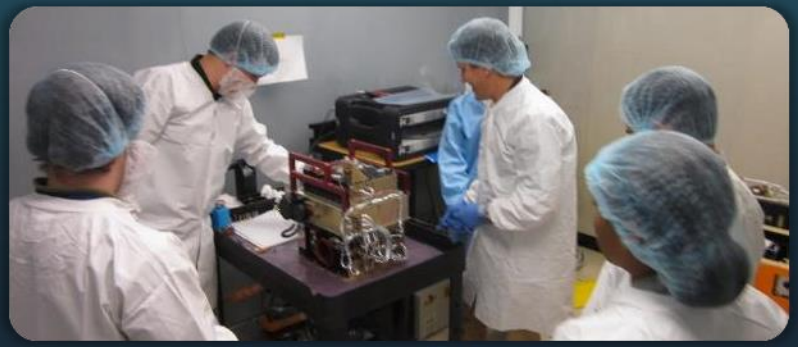
Science Data Processing Branch
Embedded Processing Group (EPG)

EPG Group Specializes in Embedded Development

- Hardware acceleration of algorithms and applications
- Intelligence, autonomy, and novel architectures
- Flight software integration for development platforms
- Advanced architectures and research platforms

Advanced Platforms for Spaceflight

- SpaceCube v2.0 and v2.0 Mini
- SpaceCube v3.0 and v3.0 Mini
- SpaceCube Mini-Z and Mini-Z45



Key Tools and Skills

- **Flight Software**: core Flight System (cFS)[1], driver integration, flight algorithms
- **Ground Support Equipment (GSE)**: COSMOS, GMSEC, system testbeds
- **FPGA Design**: Hardware acceleration, fault-tolerant structures
- **Mission Support**: Supporting flight cards, algorithm development
- **On-board Autonomy and Analysis:** deep-learning and machine-learning frameworks, unique architectures

SpaceCube v2.0[2]

[1]2020 NASA Software of the Year
[2]2020 NASA Government Invention of the Year Runner-Up

What is SpaceCube?

NASA SpaceCube

A family of NASA developed space processors that established a hybrid-processing approach that provides a **blend of the best advantages** of both commercial and radiation-hardened technologies to yield unparalleled next-generation systems

Merits of approach recognized by peers with Award for **2020 NASA Government Invention of the Year Runner-Up** for SpaceCube v2.0

Flown 11 systems in space to date

Heritage

SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5

SMART (ORS)

SpaceCube v2.0-EM

STP-H4, STP-H5

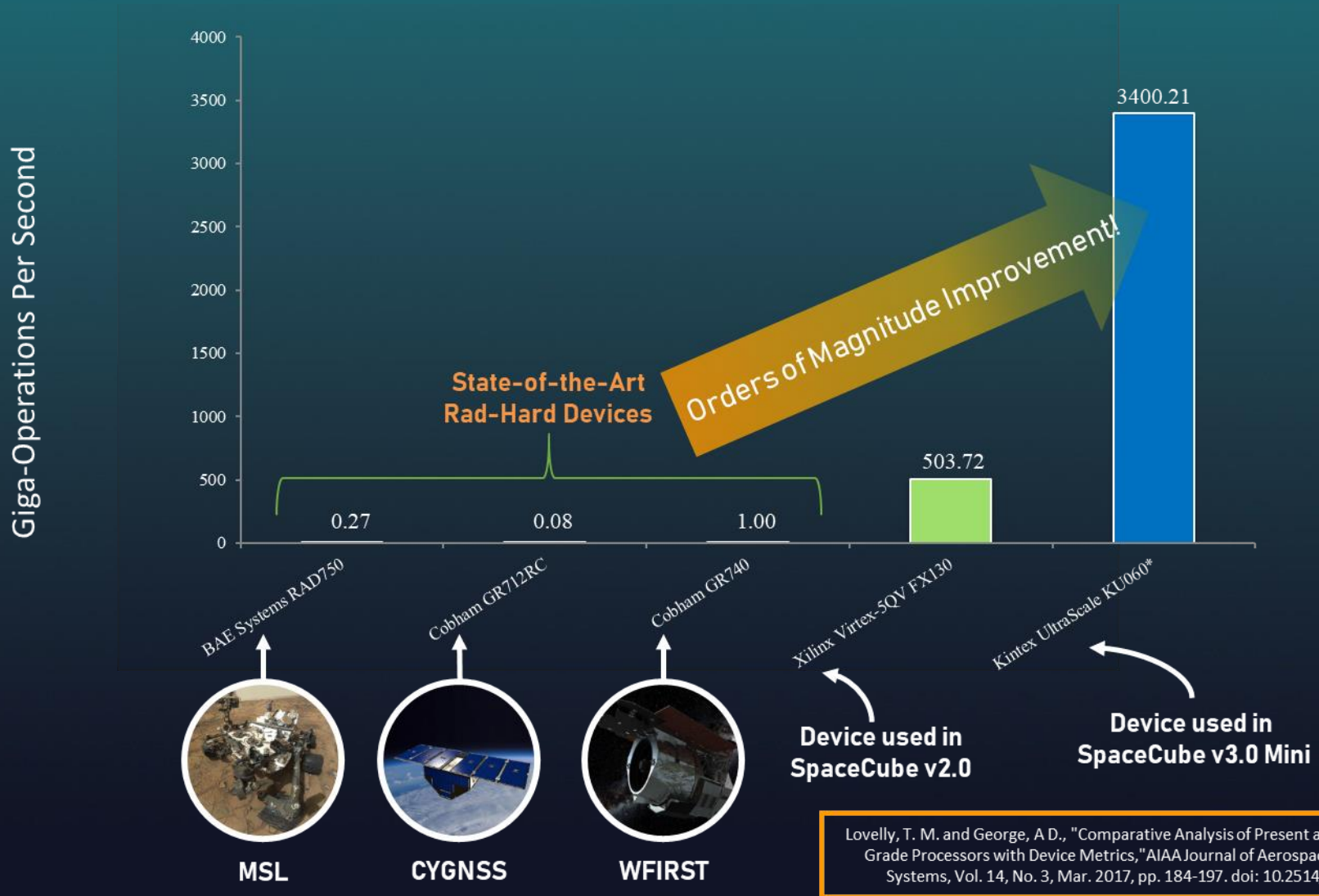
SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

SpaceCube Performance



Lovelly, T. M. and George, A D., "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics," AIAA Journal of Aerospace Information Systems, Vol. 14, No. 3, Mar. 2017, pp. 184-197. doi: 10.2514/ 1.I010472

8-Bit Integer Operations
*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

SpaceCube for Many Missions!

Family of Options

SpaceCube v3.0

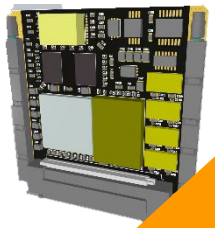
3U-SpaceVPX design with huge FPGA and SoC w/ lots of IO

SpaceCube v3.0 Mini

Miniaturized SmallSat design featuring huge FPGA and high-speed IO

SpaceCube Mini-Z

Miniaturized SmallSat design with FPGA+CPU SoC for low power



SpaceCube Mini-Z45

Miniaturized SmallSat design with FPGA+CPU SoC with high-speed IO

SpaceCube Family

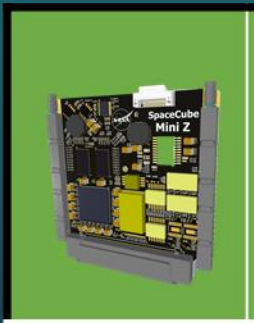
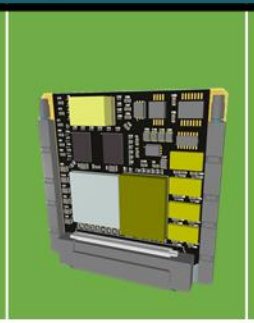
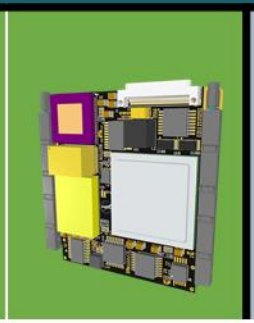
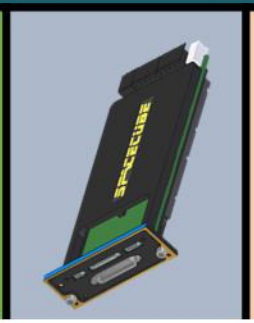
Number of products with varying capabilities to support diverse set of mission-specific needs

SpaceCube v2.0

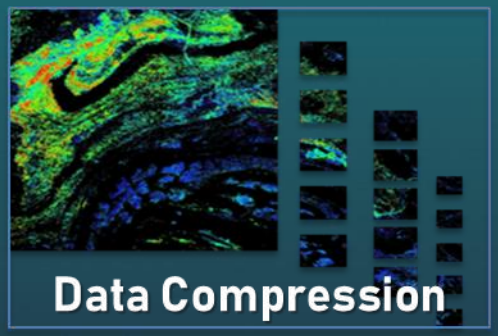
3U-cPCI design with extensive heritage for high-rel apps

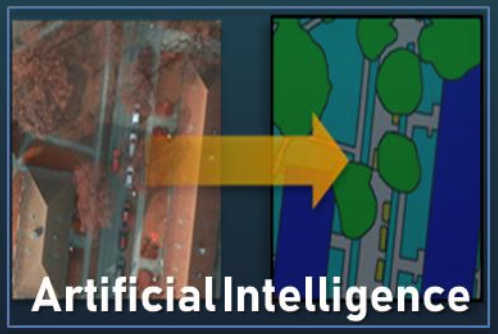
2020 NASA Government Invention of the Year Runner-Up

Current Catalog SpaceCube Family

							
	SpaceCube Mini Z/Z+ (SC Mini-Z)	SpaceCube Mini Z45 (SC Mini-Z45)	SpaceCube v3.0 Mini (SCv3-Mini)	SpaceCube v3.0 (SCv3-VPX)	SpaceCube v2.0 (SCv2)	SpaceCube Emulated Platform	SpaceCube Cloud Virtual Platform
Form Factor	CubeSat Card Standard (CS2)	CubeSat Card Standard (CS2)	CubeSat Card Standard (CS2)	3U SpaceVPX SmallSat	3U cPCI SmallSat	Desktop	Server
Storage	4 GB	16 GB	32 GB	48 GB	8 GB	Variable	Variable
RAM	1 GB DDR3	3 GB DDR3	2 GB DDR3	4 GB DDR3	2 GB DDR	Variable	4-16 GB DDR4
FPGA Resources	+	++	+++	+++++	++	Configurable	+++
Processor(s)	Dual ARM Cortex-A9	Dual ARM Cortex-A9	MicroBlaze / RISC-V	Quad ARM Cortex-A53 / Dual Cortex-R5 / MicroBlaze / RISC-V	PPC440 / MicroBlaze	QEMU Emulated	AWS Host / MicroBlaze / RISC-V
MGTs	N/A	3.125 Gbps/lane	12.5 Gbps/lane	6.0-12.5 Gbps/lane	3.125 Gbps/lane	N/A	PCIe Gen3 x16 or Gen4 x8

Key Applications



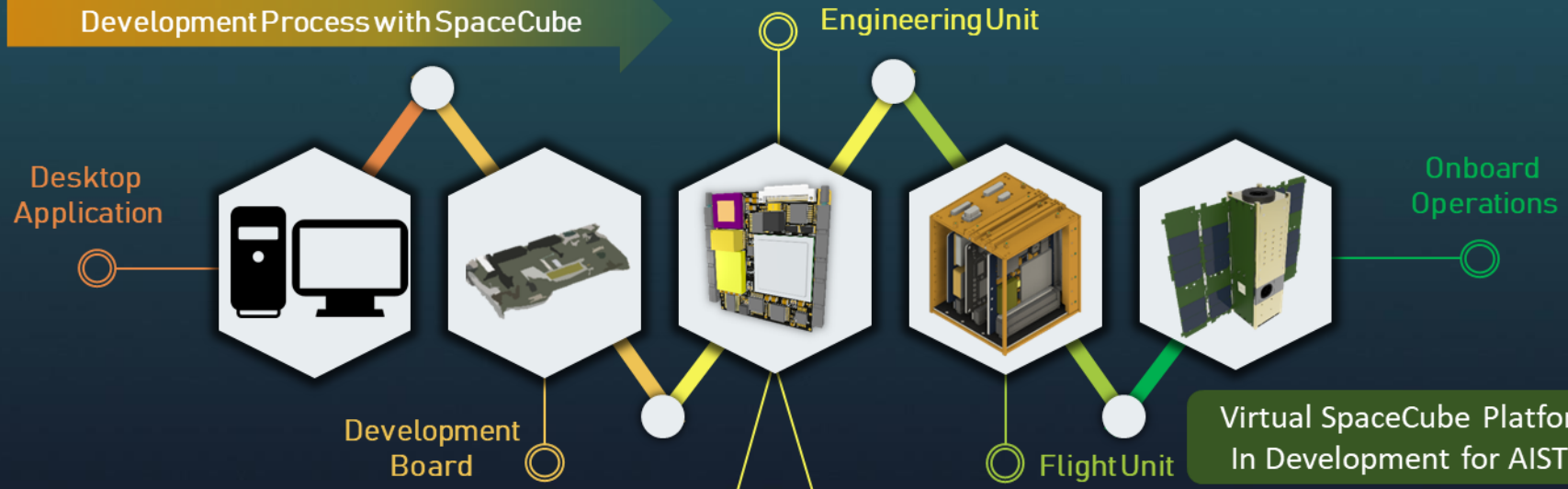


How Does SpaceCube Help?

SpaceCube helps scientists convert their applications from desktop to FLIGHT

SpaceCube can hardware accelerate applications BEYOND embedded expectations

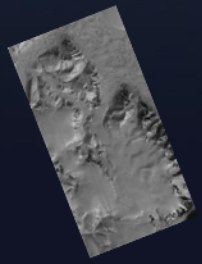
Development Process with SpaceCube



Virtual SpaceCube Platforms In Development for AIST18

Machine Learning App: Classification and Detection

Demonstrated massive **1733× speedup** over purely software baseline run on single processor



Lossless Compression: JPEG-LS

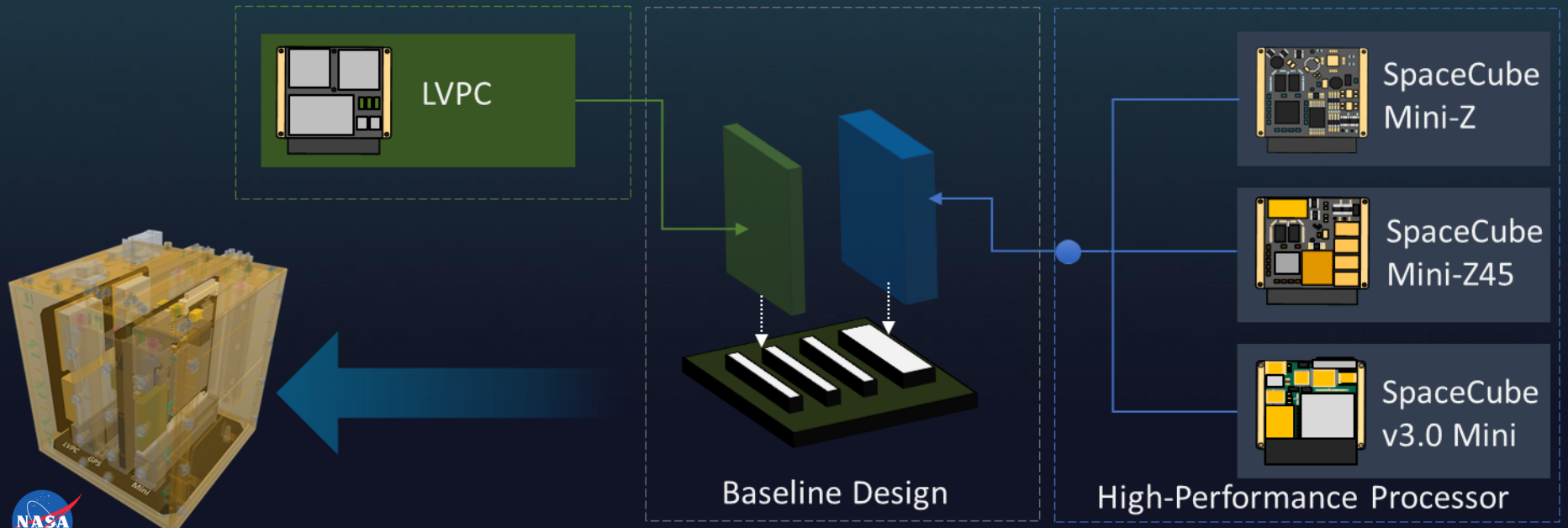
Demonstrated **61.68× speedup** on LandSat-8 Dataset over single processor (~2 hrs to 2 min)

SpaceCube Intelligent Multipurpose System Concept Overview

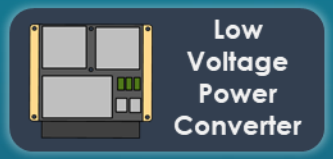
Diverse set of payloads can be realized with same baseline infrastructure of key reused cards and simple addition of one or two cards for mission-specific needs

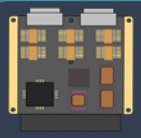
SpaceCube provides high-performance computing designs to be combined with added features from catalog of supporting cards

Designs are reusable and can be reconfigured for multiple mission classes (or varying orbits/environments) and science objectives



Configurable Slices

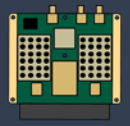

Low Voltage Power Converter


General Interface


Software Defined Radio


Lidar Interface


TTE / Ethernet Router


GPS

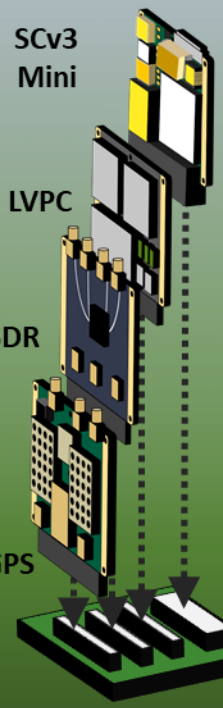

AI Accelerator


Solid-State Data Recorder

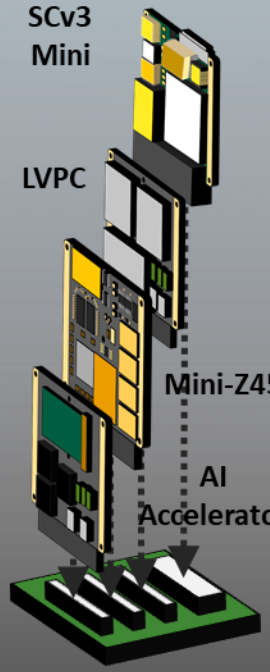

ADC Readout


SpaceWire Router

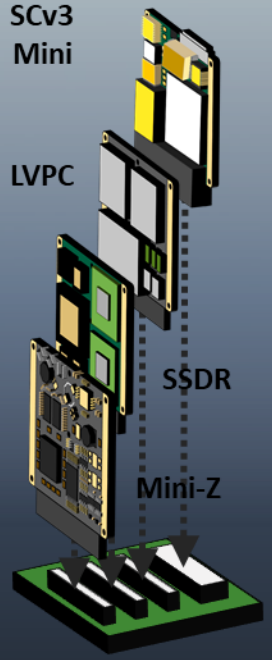
CS2 1U CubeSat Card Catalog



Comm. and Nav.



Artificial Intelligence

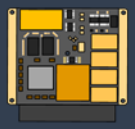


Cyber Security

TTE/DTN Node (Lunar Enabling)


SpaceCube v3.0 Mini


SpaceCube Mini-Z


SpaceCube Mini-Z45

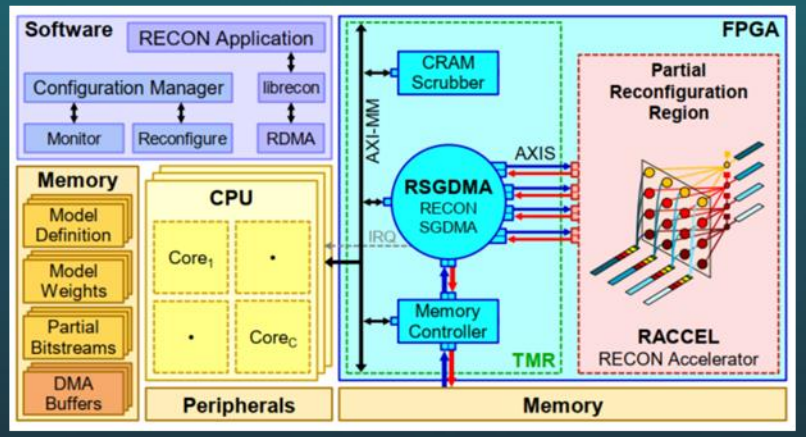
Processors

Multi-Purpose Box Configurations

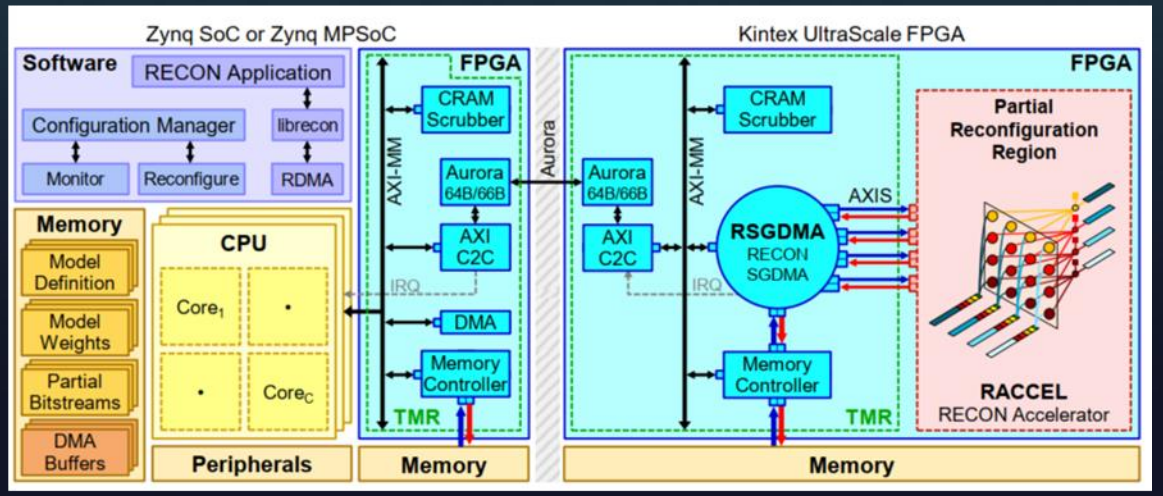
AI Case Study Overview

- AI processing unit is strategic for both science and defense applications
- Semantic Segmentation
  - Computer Vision / Machine Learning Process
  - Learns to assign label to all pixels of image
  - Pixels with same label share semantic characteristics
  - Application deployed on reconfigurable CNN Acceleration framework (called **RECON**)
- Architecture configurations
  - **Original**: Single Zynq SoC or MPSoC device
  - **AI Processing Box**: Combines Zynq SoC with Kintex UltraScale

Semantic Segmentation Example



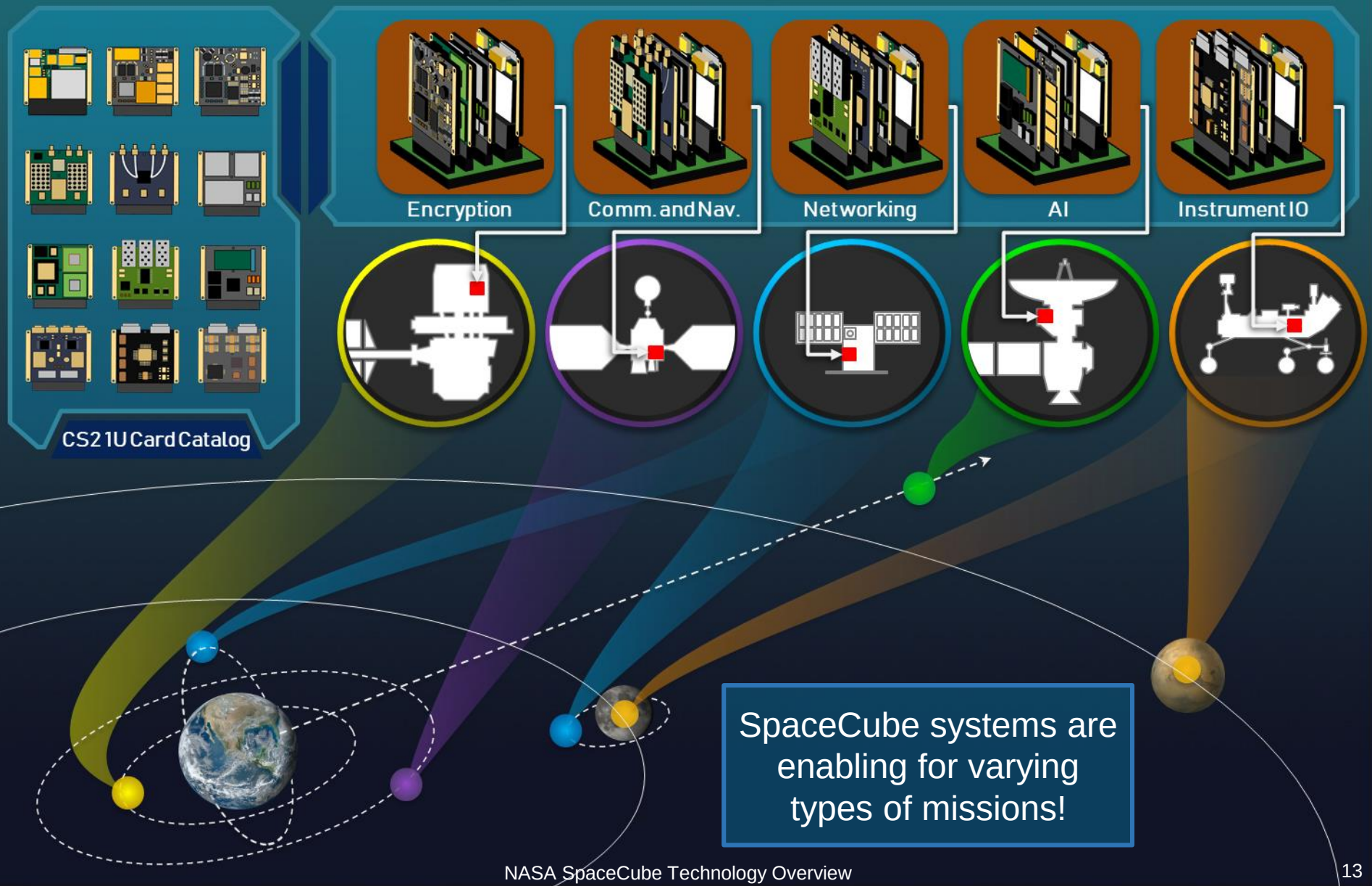
RECON Architecture on Single Zynq SoC or MPSoC



RECON Architecture on Combined Zynq SoC and Kintex UltraScale

S. Sabogal, A. D. George, and G. Crum, "ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs," 12th Space Computing Conference, July 30 – August 1, 2019.

Cross-Cutting Concept



SpaceCube systems are enabling for varying types of missions!

Conclusion

*SpaceCube is a **MISSION ENABLING** technology*

Delivers exceptional computing power in **number of form factors**

Cross-cutting technology for Communication and Navigation, Earth and Space Science, Planetary, and Exploration missions

CubeSat Card Standard (CS^2) provides flexibility and interoperability to mix-and-match varying designs to construct new system

SpaceCube Intelligent Multi-Purpose System (IMPS) provides **processing baseline** and expandable architecture for payloads

Designs support AI applications for autonomy and analysis onboard

Seeking commercialization partner to enable more rapid turn-key SpaceCube solutions in support of next-generation missions

Thank you! Questions?

Contact Us

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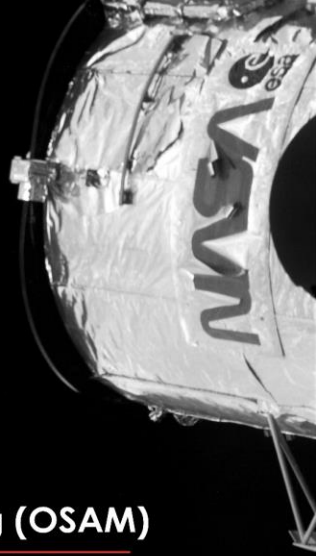
NASA/GSFC Internal Research and Development (IRAD), NASA GSFC Crosscutting Technology and Capabilities Office, NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP)
Javier Valle from Texas Instruments and Dylan Lang from Samtec

National Aeronautics and Space Administration



On-orbit Servicing Assembly and Manufacturing (OSAM)

Journeying Longer and Seeing Farther

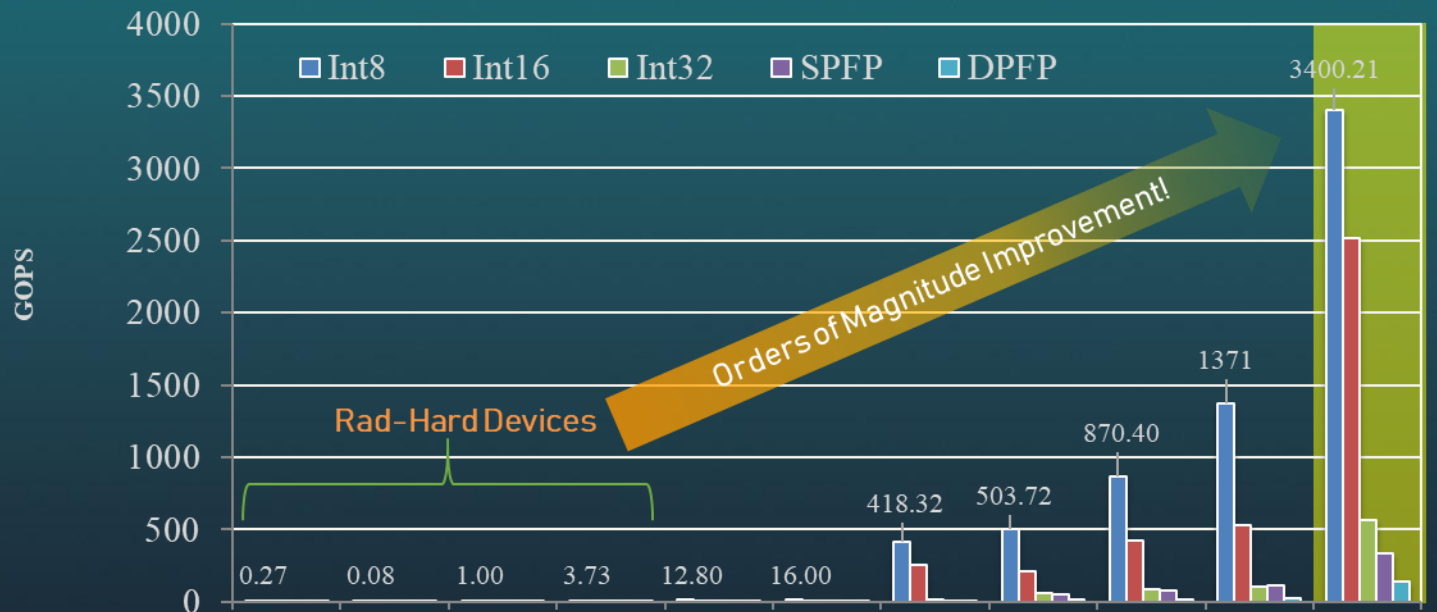
Space is vast. For the most part, when a satellite is launched, it's on its own, regardless of whether it ever needs assistance or not. It launches, operates, and is decommissioned alone, its lifespan limited by consumables, imperfect human design, the exceedingly harsh space environment, and technical obsolescence. **But what if we could fix, upgrade, and augment existing satellites to enable more science for longer?** Technically and economically feasible refueling, repair, and upgrade of satellites has remained elusive—until now. OSAM technology will enable more science by assisting existing telescopes, but also lay the groundwork for future endeavors once thought to be impossible.

To arrange further discussion of on-orbit servicing technologies contact Tammy Brown (301-286-5753 or Tammy.L.Brown@nasa.gov)

Background Graphic: OSAM technologies continue the legacy of the Hubble Space Telescope (HST) Servicing Missions, and will be implemented to assist astronauts span and expand orbiting stations like the International Space Station (ISS). OSAM technologies will also support lunar surface and orbiting operations.

Appendix

SpaceCube Performance (Expanded)



MSL

CYGNSS

WFIRST

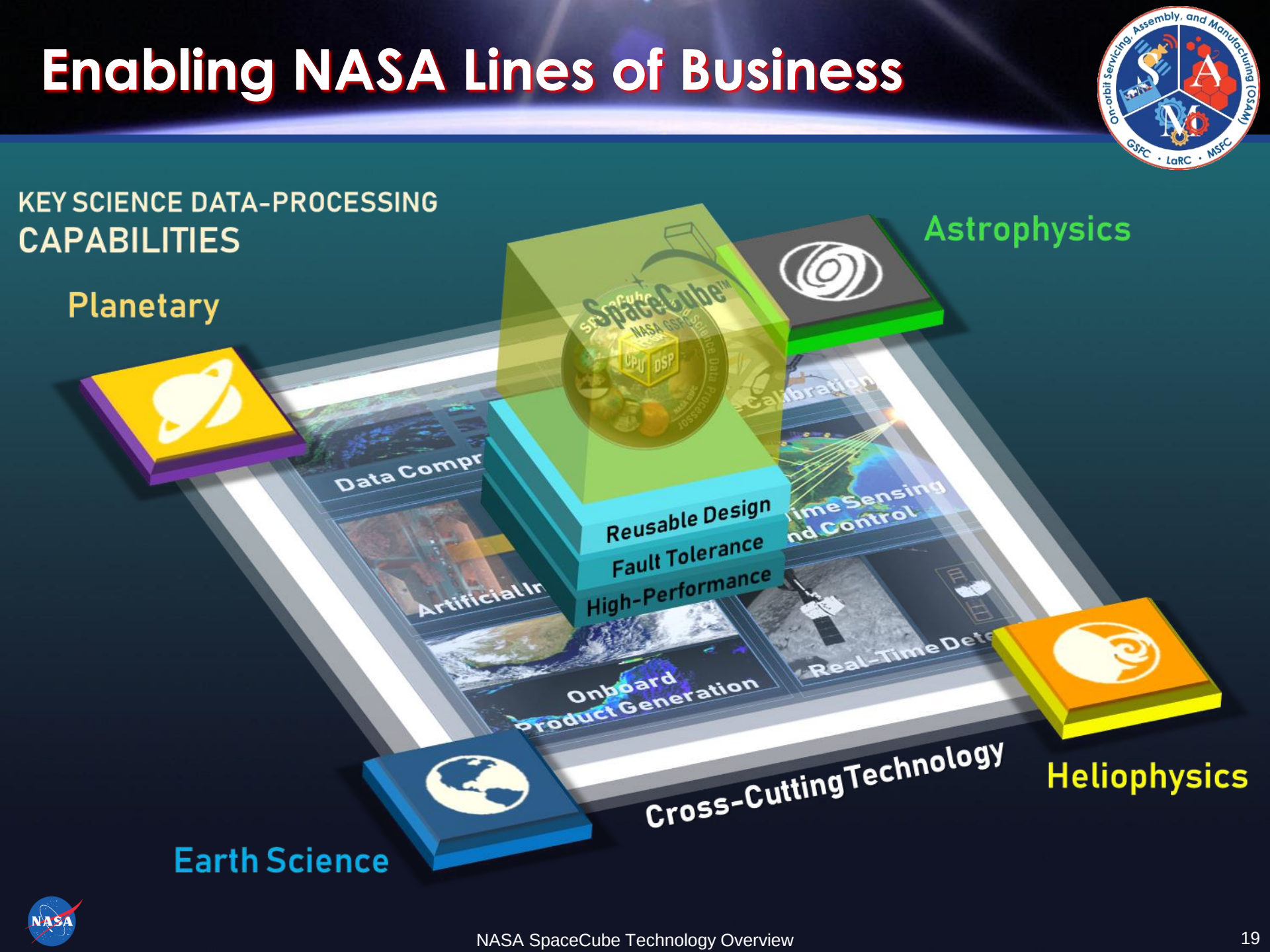
Device used in SpaceCube v2.0

Device used in SpaceCube v3.0 Mini

Lovelly, T. M. and George, A D., "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics,"AIAA Journal of Aerospace Information Systems, Vol. 14, No. 3, Mar. 2017, pp. 184-197. doi: 10.2514/ 1.I010472

GOPS=Giga-operations per second
*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

Enabling NASA Lines of Business

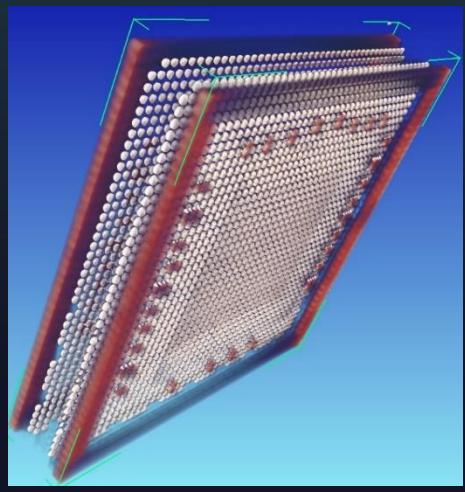


SpaceCube v2.0 Processor Card

Overview

- TRL9 flight-proven processing system with unique Virtex **back-to-back** installed design methodology
- **3U cPCI** (190 mm × 100 mm) size
- Typical power draw: 8-10W
- 22-layer, via-in-pad, board design
- IPC 6012B Class 3/A compliant

Back-to-Back FPGA Design



High-Level Specifications

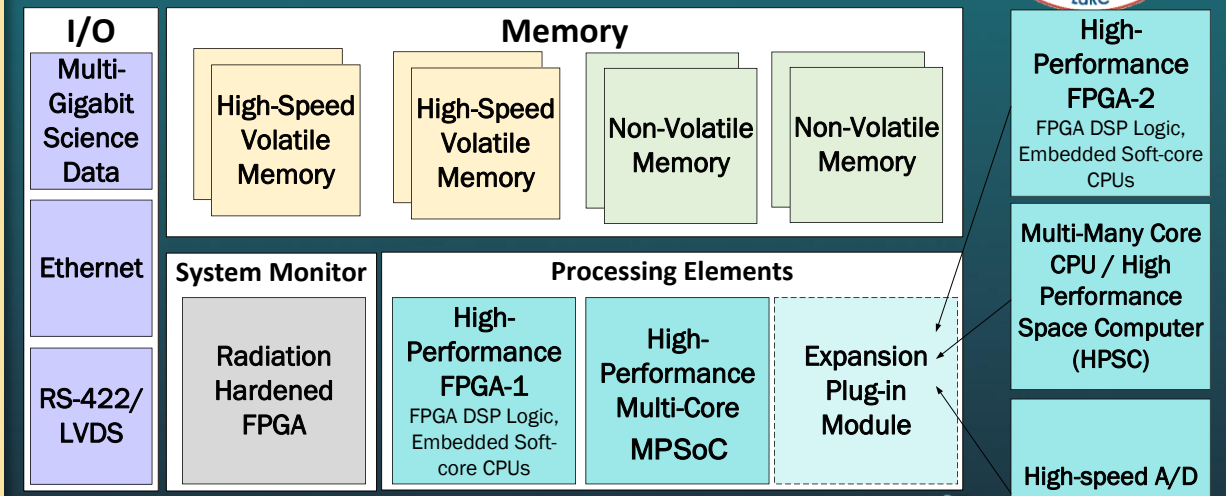
- 2x Xilinx Virtex-5 (QR) FX130T FPGAs (FX200T Compatible)
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 4x 512 MB DDR SDRAM
- 2x 4GB NAND Flash
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 16-channel Analog/Digital circuit for system health
- Mechanical support for heat pipes and stiffener for Xilinx devices
- External Interfaces
  - Gigabit interfaces: 4x external, 2x on backplane
  - 12x Full-Duplex dedicated differential channels
  - 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Debug Interfaces
  - Optional 10/100 Ethernet interface

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot

SpaceCube v3.0 Architecture



High-Level Specifications

1x Xilinx Kintex UltraScale

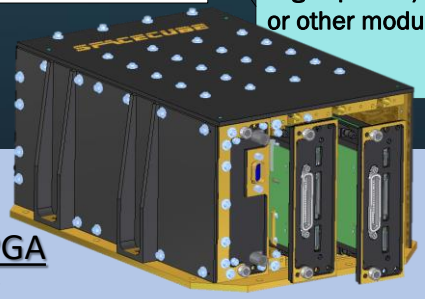
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

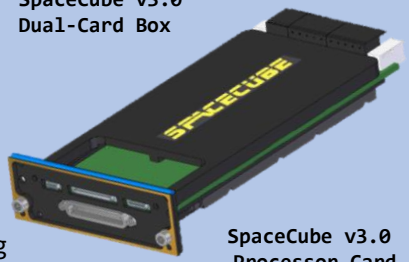
- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring



SpaceCube v3.0 Dual-Card Box



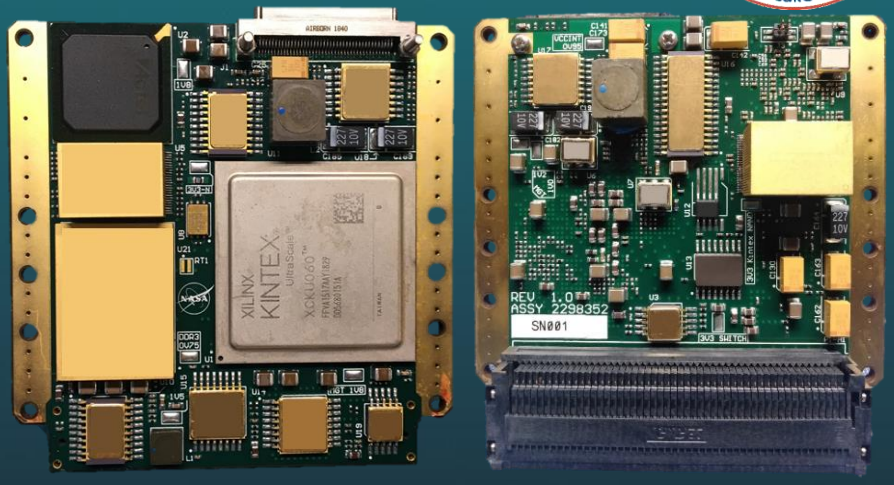
SpaceCube v3.0 Processor Card

SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES
- Evaluation board available with common interfaces for rapid prototyping and debug
- Conforms to CubeSat Card Standard (CS^2)

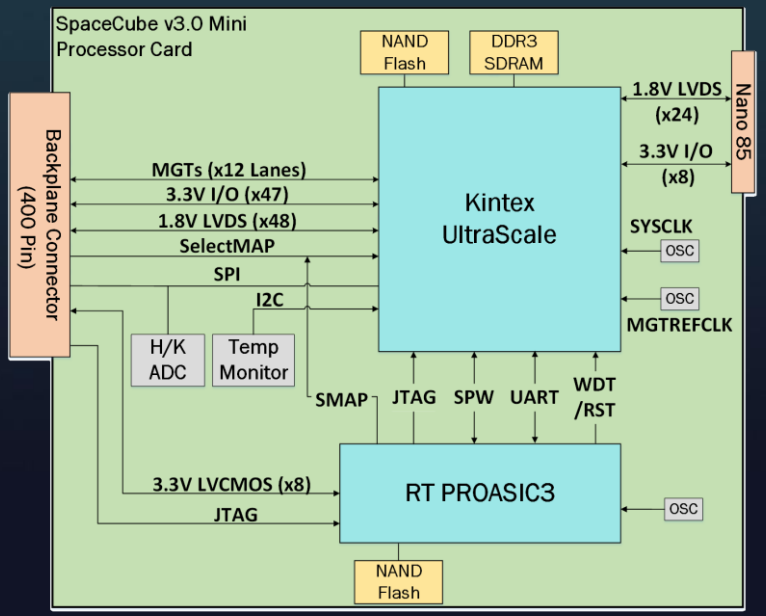
[CS]²



High-Level Specifications

Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



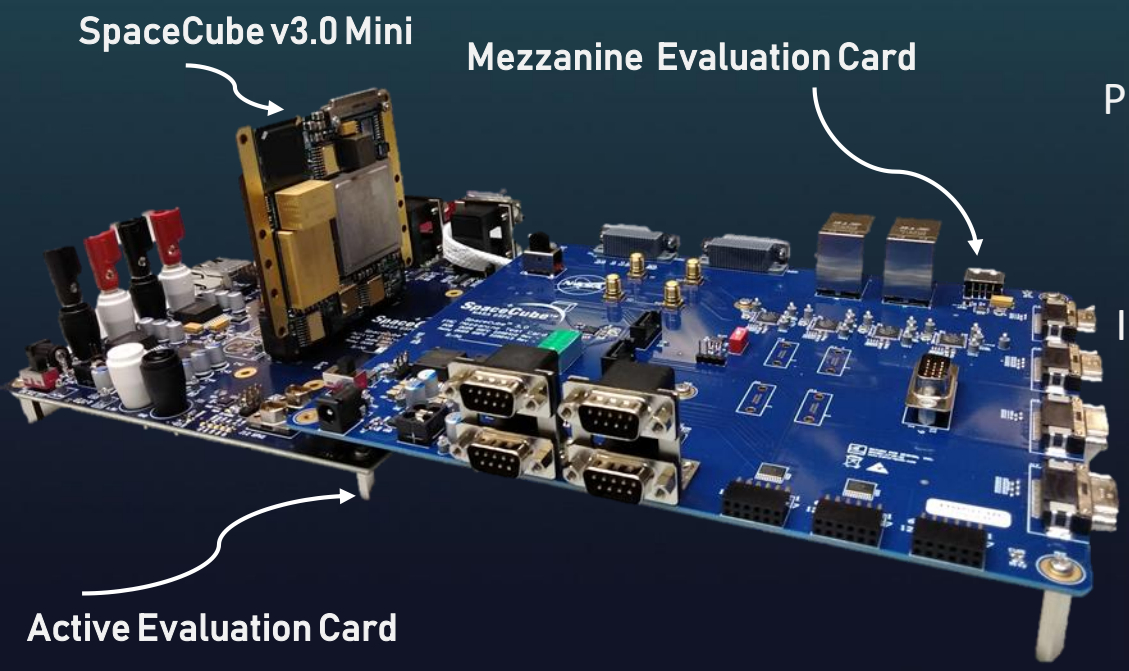
SpaceCube Mini Development Kit

Active Evaluation Card

- Gigabit Ethernet (RJ45/SGMII)
- USB Debug / JTAG
- JTAG headers (Xilinx and Microsemi)
- SelectMAP Header
- 2x SpaceWire ports
- 4x RS422 ports
- FMC+ Connector
  - 11 MGT lanes
  - 46x LVDS or 92x 1.8V GPIO
  - 22x 3.3V GPIO

Mezzanine Evaluation Card

- 3x SpaceWire Ports
- 4x RS-422 Ports
- 2x Gigabit Ethernet (RJ45-SGMII)
- 2x Camera Link (Base/Medium)
- 1x USB 2.0
- 1x SATA
- 1x CAN Bus
- 8x MGT lanes (1x SMA, 7x verSI)
- 9x LVDS
- 3x 3.3V GPIO



Provides **easy development platform** to support SpaceCube v3.0 Mini rapid prototyping and design

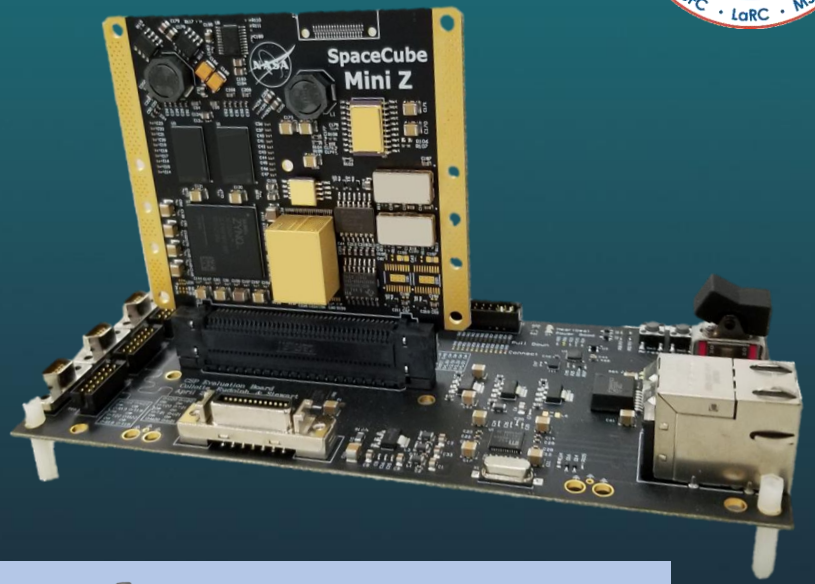
Includes several common interfaces for programming and debug

Incorporates FMC+ Connector to support future Mezzanine and commercial vendor designs

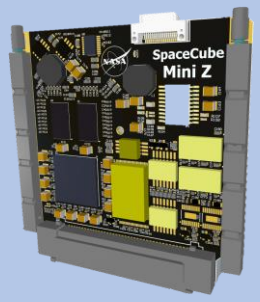
SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture



High-Level Specifications



Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

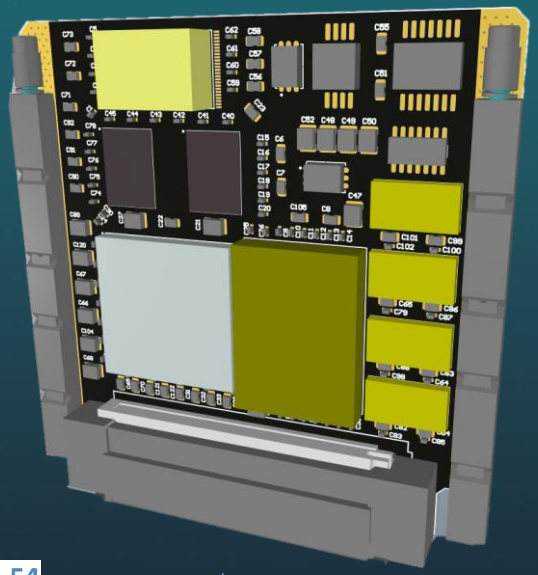
Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

SpaceCube Mini-Z45 Specification

Overview

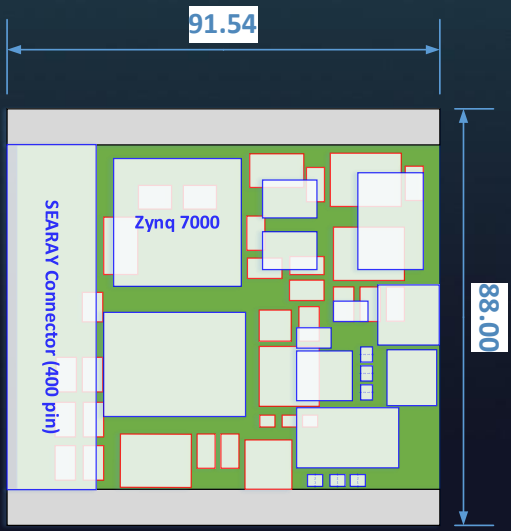
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory



High-Level Specifications

1x Xilinx Zynq 7000 System-on-Chip

- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (voltage selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG



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