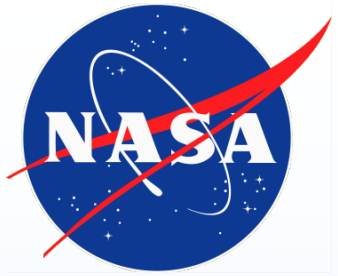

Combined Total Ionizing Dose and Single-Event Effects on a 22-nm Fully-Depleted Silicon-on-Insulator Test Vehicle

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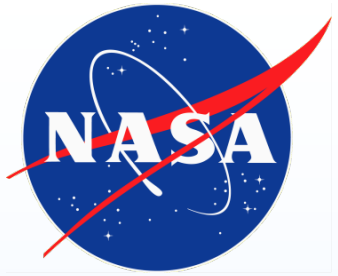
To be presented by Megan Casey at the Nuclear & Space Radiation Effects Conference (NSREC) virtually December 2, 2020.

Acronyms



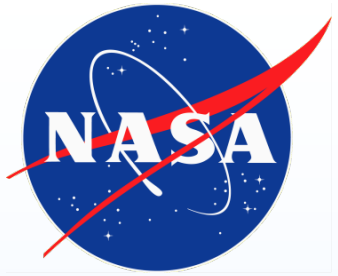
- BOX – Buried Oxide
- DUT – Device Under Test
- FBB – Forward Body Bias
- FDSOI – Fully-Depleted Silicon-on-Insulator
- finFET – Fin Field Effect Transistor
- LBNL – Lawrence Berkeley National Laboratory
- nMOS – N-Channel Metal Oxide Semiconductor
- pMOS – P-Channel Metal Oxide Semiconductor
- PDSOI – Partially-Depleted Silicon-on-Insulator
- REF – Radiation Effects Facility
- RBB – Reverse Body Bias
- SEE – Single-Event Effects
- SOI – Silicon-on-Insulator
- SRAM – Static Random Access Memory
- STI – Shallow Trench Isolation
- TID – Total Ionizing Dose
- UTBB – Ultra-Thin-Body and BOX
- VNW – N-Well Bias Voltage
- VPW – P-Well Bias Voltage

Introduction

- As scaling trended downward from technology feature sizes in the 100s of nm down to 32 nm, the effect of TID in PDSOI devices decreased[1,2]
  - At smaller technology nodes, like 22 or 14 nm, where device manufacturers switched to finFET technology or UTBB, the effect of TID has re-emerged[2] due to the large number of STI interfaces[3]
- It was also hypothesized that deep submicron scaling had eliminated TID effects in FDSOI devices, particularly threshold voltage shifts[4], as ultra-thin gate oxides do not trap charge the way older technologies did
  - In these FDSOI technologies, charge accumulates in the STI[5] similarly to 14 nm finFET technologies
- Previous IBM SOI technology generations were PDSOI, and exhibited minimal TID effects due to both the physical thickness of and high doping in the silicon body of the devices[8]
- Manufactured FDSOI test structures in IBM 45 nm saw substantial TID sensitivity due to lightly-doped BOX and charge trapping in the BOX[8]
- These results have led to considerable interest in the total ionizing dose sensitivity of FDSOI at highly-scaled technology nodes

1 Q. Zheng, *IEEE TNS*, April 2019.
2 H. Hughes, *IEEE REDW*, 2015.
3 N. Rezzak, *IEEE Int'l SOI Conf*, 2010.
4 M. Turowski, *IEEE TNS*, Dec. 2004.
5 M. R. Shaneyfelt, *IEEE TNS*, Dec. 1998.
8 N. Rezzak, *IEEE Int'l SOI Conf*, 2012.

Background

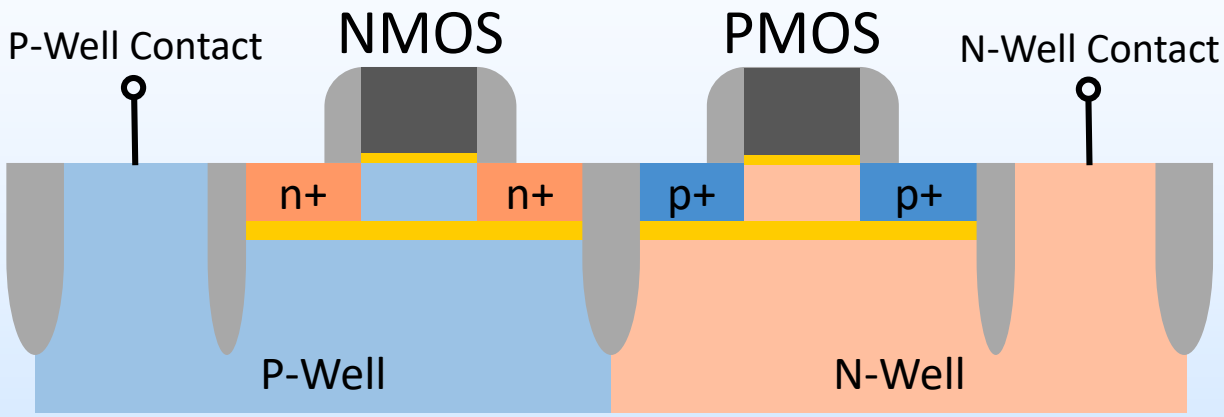


- GlobalFoundries' 22FDX process is a 22 nm fully-depleted SOI process[9]
  - Previous generations were PDSOI (45 nm, 32 nm)
- It employs planar transistors (rather than novel designs like finFETs used in other highly scaled processes) with high-κ dielectric gates
  - Planar transistors are simpler and less expensive to design and manufacture than 3D
- FDSOI supports body biasing, which can significantly reduce energy consumption

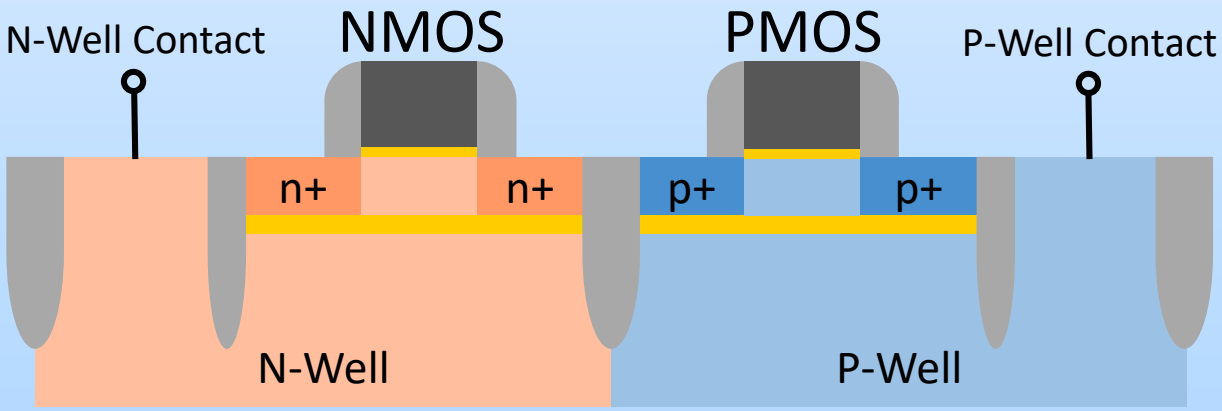
9 V. Joshi, *Symp on VLSI Tech*, 2017.

Body Biasing

Standard Well Configuration



Flipped Well Configuration

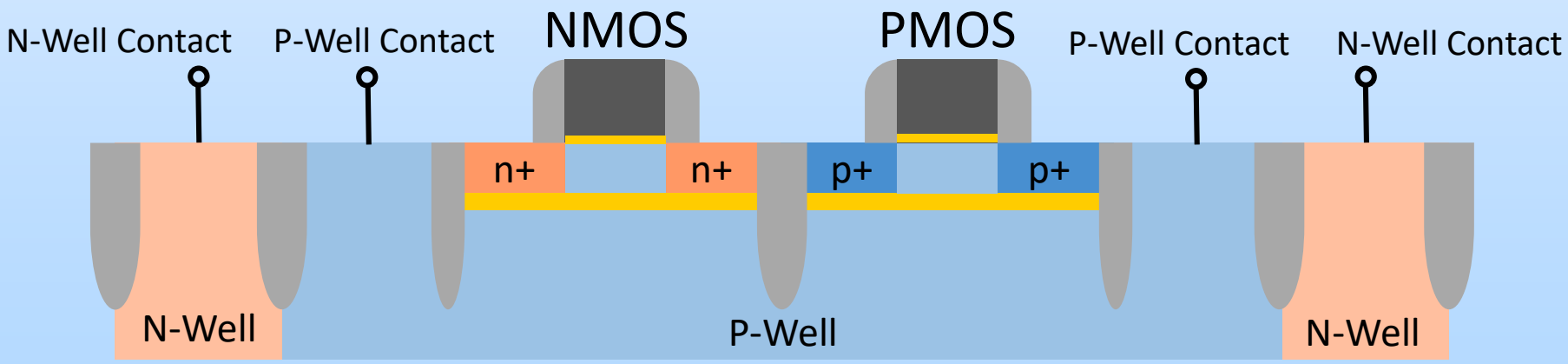


- 22FDX offers two well configurations[10]
  - Standard: NMOS are located in p-wells and PMOS are located in n-wells
    - Allows for reverse body biasing the transistors and reduces leakage currents[11]
  - Flipped: NMOS are located in n-wells and PMOS are located in p-wells
    - Allows for forward body biasing and higher performance operation[12]
- P-well voltage can decrease from nominal 0 V to -2 V[10]
- N-well voltage can increase from nominal 0 V to 2 V[10]

10 R. Srinivasan, *SNUG*, 2016.
11 O. Thomas, *IEEE Int'l Elect. Dev. Mtg*, 2014.
12 GlobalFoundries, "Introducing the 22FDX 22nm FD-SOI Plaform from GLOBALFOUNDRIES," March 2016. [Online].

Test Vehicle

- DUTs are a 128-Mb SRAM line monitor circuit
- Nominal supply voltage is 0.8 V, but voltages as low as 0.4 V and as high as 1.08 V are supported by the technology
- The bit cell array in this device is manufactured with all transistors in a p-well, while the n-well is implanted to isolate the SRAM bit cell array
  - NMOS are in the standard configuration (allows reverse body biasing)
  - PMOS are in the flipped well configuration (allows forward body biasing)
- As a result of the n-well only being used for isolation, n-well biasing was expected to have a limited effect on the radiation response of the SRAM



Bias Conditions and Test Technique

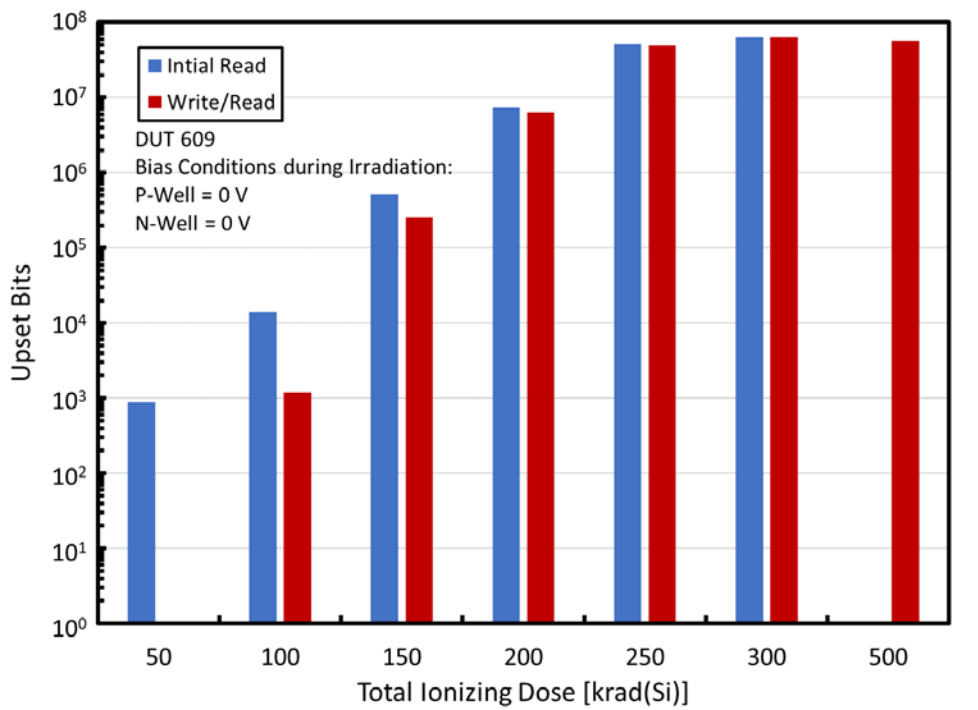
DUT	Array Voltage	N-Well Voltage	P-Well Voltage	Dose Step Size	Total Dose
609	0.8 V	0 V	0 V	50 krad(Si)	500 krad(Si)
601	0.8 V	2 V	-2 V	50 krad(Si)	500 krad(Si)
602*	0.8 V	2 V	-2 V	50 krad(Si)	300 krad(Si)

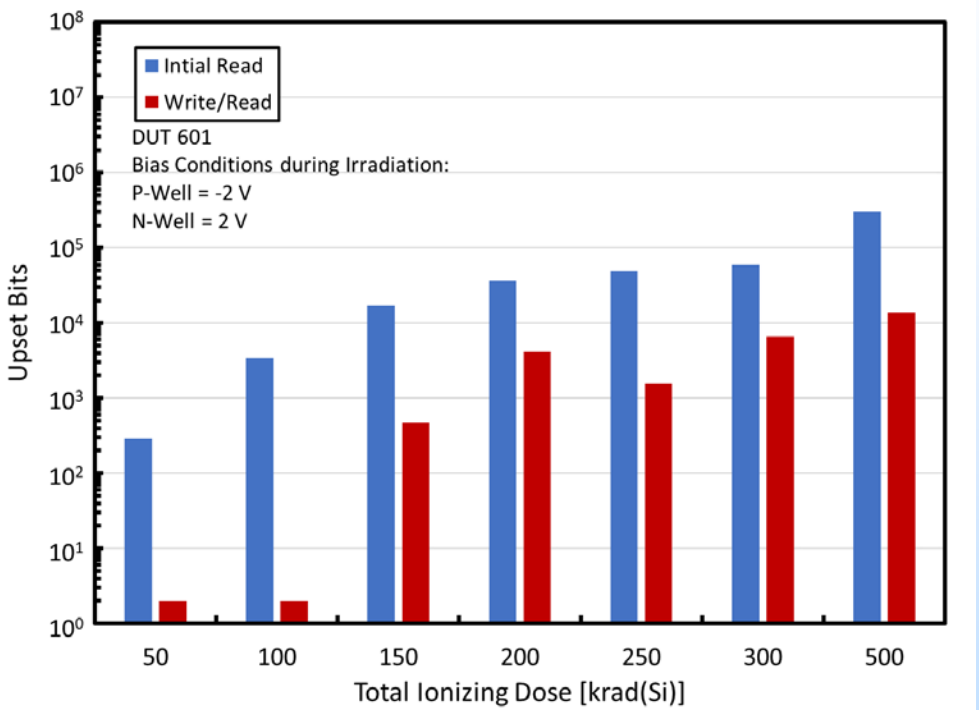
- Pattern was written before irradiation and read back and the number of upset bits was recorded
- After irradiation, cells were read back again and number of upsets were recorded
  - If any cells were incorrect, then the memory was rewritten and read back to see if the number of incorrect cells changed
- Post-Irradiation Measurements:
  * Sweep array voltage (0.7 V to 1.08 V), holding n- and p-well voltages constant
  - Sweep p-well voltage (0 V to -2 V), holding n-well voltage at nominal
  - Sweep n-well voltage (0 V to 2 V), holding p-well voltage at nominal
  * Sweep p- (0 V to -2 V) and n-well (0 V to 2 V) voltages
  - Vary input pattern (00, FF, AA), holding array voltage, n-well, and p-well voltages constant
  * Measure retention voltage at nominal well voltages

*Full results covered in the paper, but not in this presentation

Total Ionizing Dose Test Results

Initial Upsets and Upsets after Write/Read

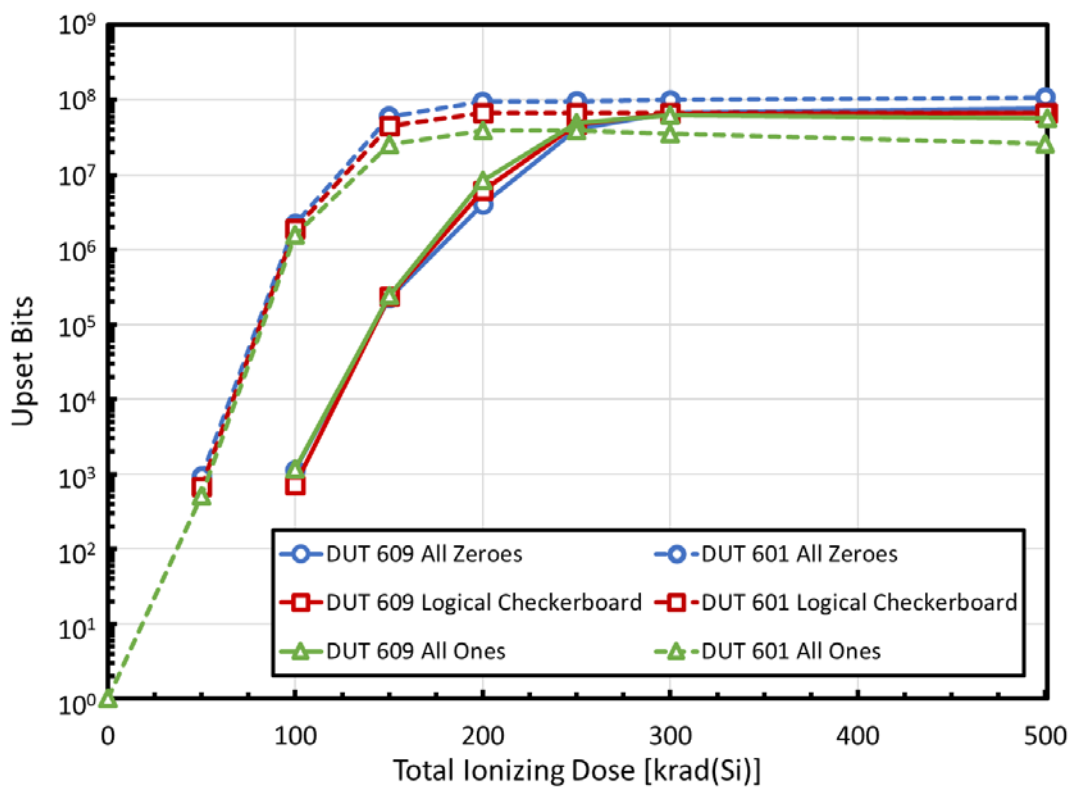




- More upset bits in DUT 601 than in DUT 609 across all doses
  - Number of stuck bits after re-write is also lower
- At 500 krad(Si), DUT 601 has more than 200x fewer errors than DUT 609 after the initial read and 4133x fewer errors after write/read

Total Ionizing Dose Test Results

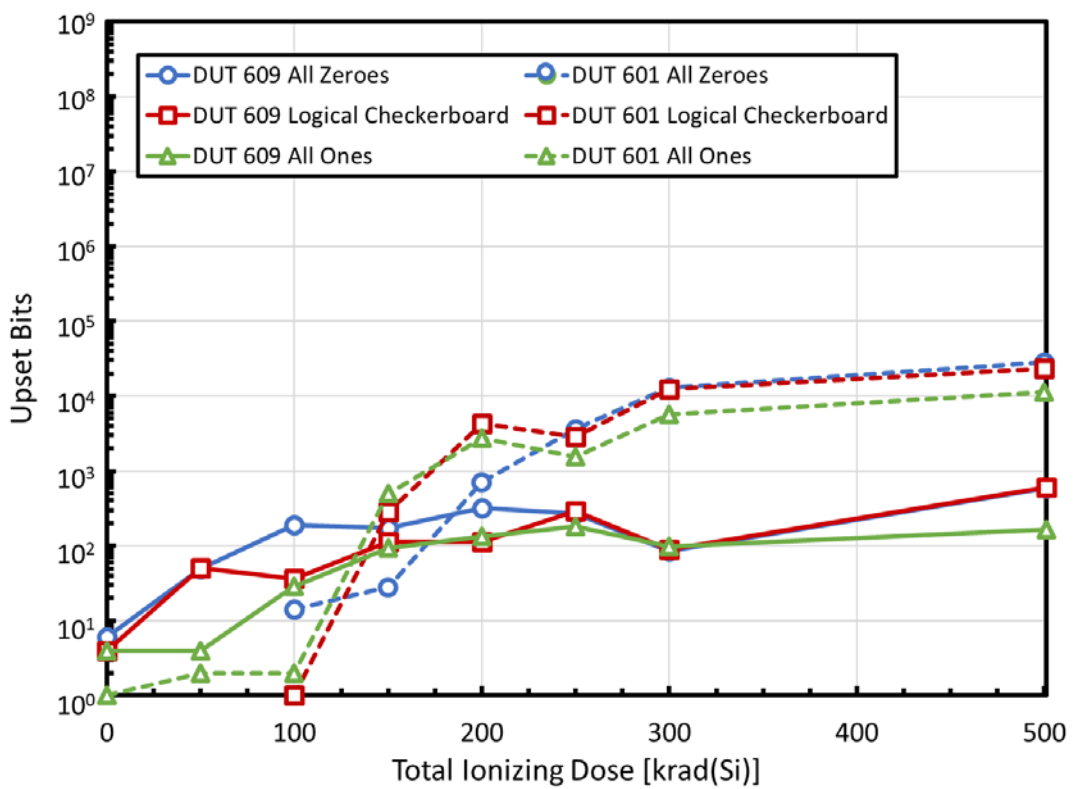
Input Pattern Dependence with Nominal Bias Conditions



- Upsets are observed, and number of upsets saturates, at a lower dose in DUT 601 than 609
- DUT 609 shows no pattern dependence, but after 150 krad(Si), DUT 601 has significantly more errors with 00 then FF
  - Logical checkerboard (AA) falls between 00 and FF
- Historically, with TID, PMOS exhibit greater leakage current than NMOS, so maintaining high nodal voltages becomes increasingly difficult
  - As evidenced by greater number of errors with 00 input pattern, NMOS appear to be experiencing greater leakage than PMOS

Total Ionizing Dose Test Results

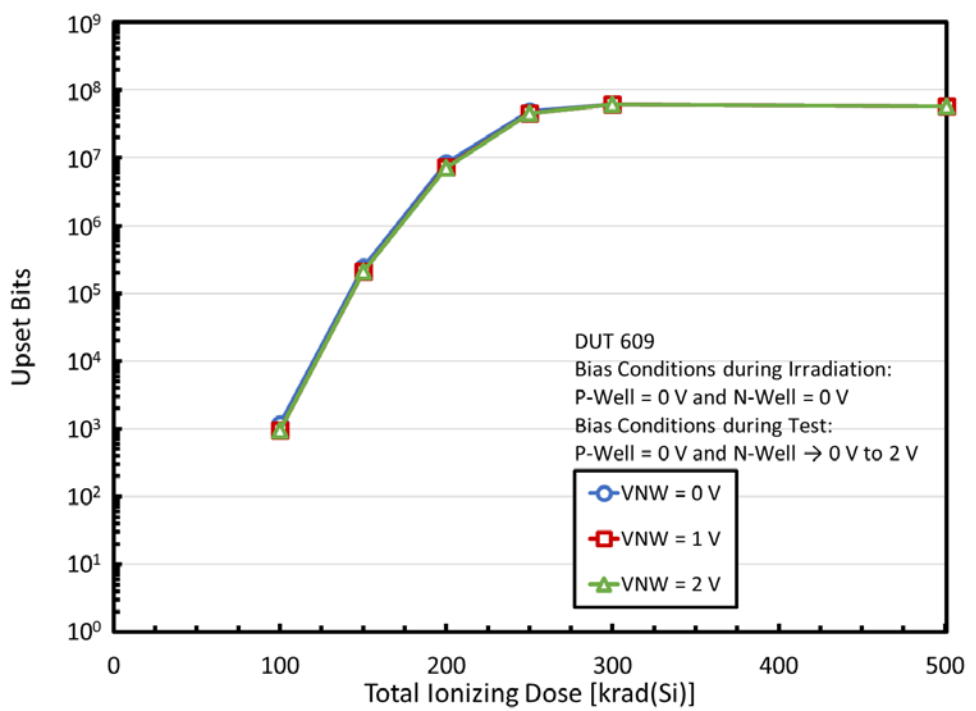
Input Pattern Dependence with Extreme Bias Conditions

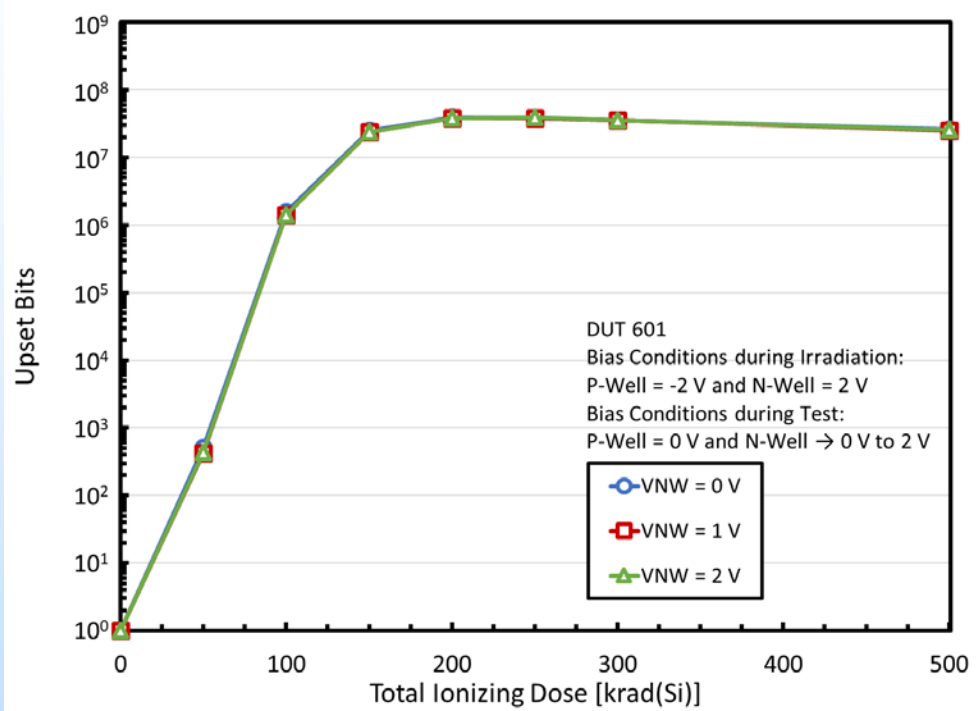


- Input pattern dependence disappears when DUTs are biased with extreme well conditions
- Total number of errors decrease compared to the nominal well bias voltages for both DUTs
- DUT 601 now has a more errors after 150 krad(Si) than DUT 609

Total Ionizing Dose Test Results

Impact of Changing the N-Well Bias Voltage

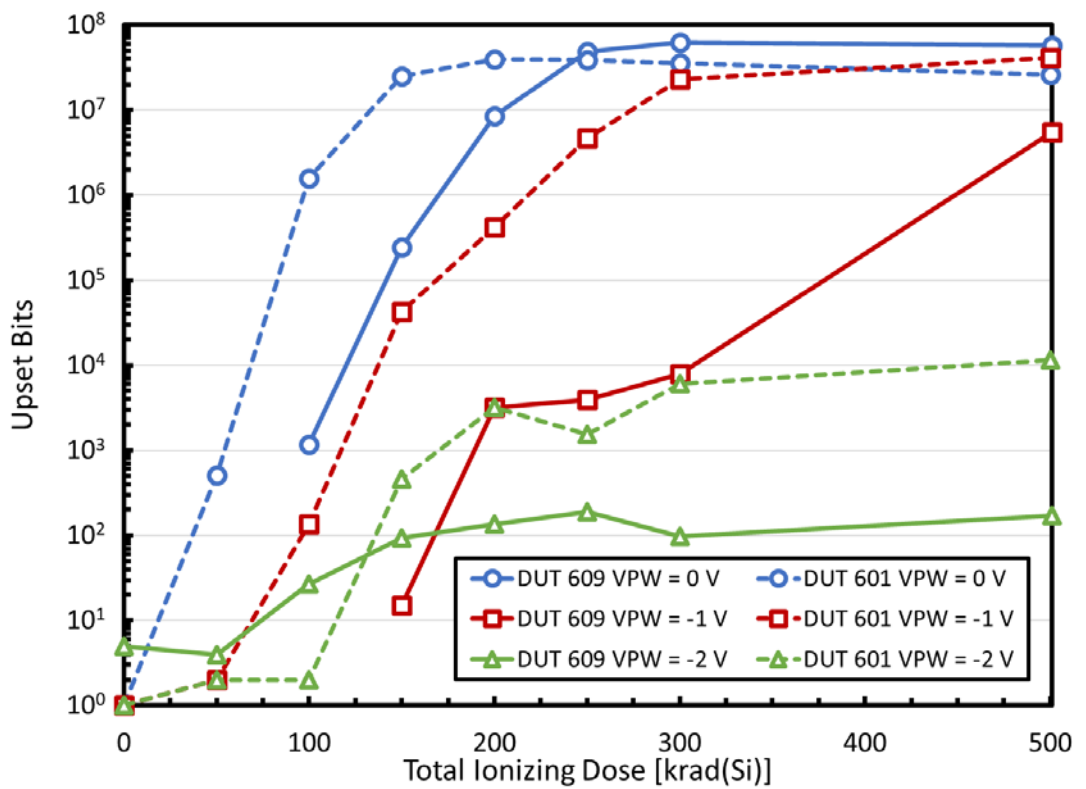




- No change in number of errors when p-well voltage was held at 0 V and n-well voltage was increased up to maximum of 2 V
  - This is expected since the n-well is only used for isolation around the SRAM cell arrays

Total Ionizing Dose Test Results

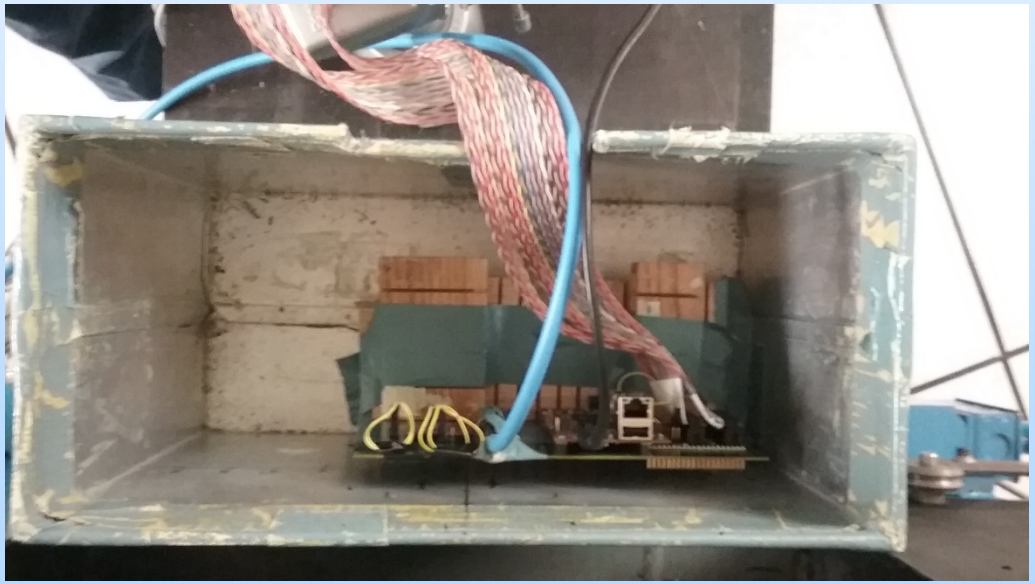
Impact of Changing the P-Well Bias Voltage

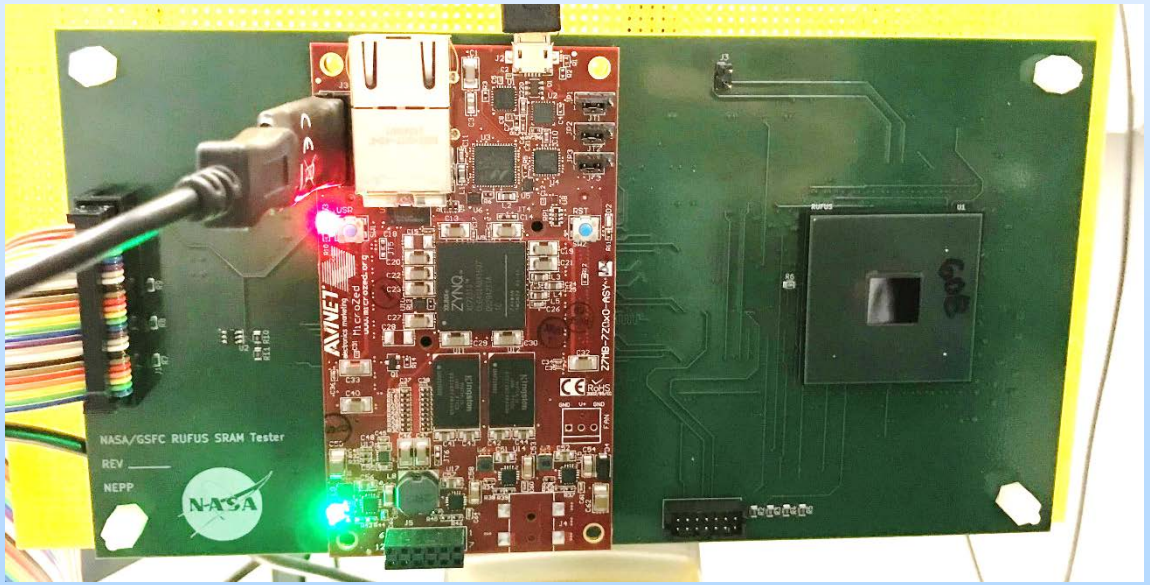


- DUT 601 has a greater number of upset bits than DUT 609
- While n-well voltage has no effect on SRAM response, changing p-well voltage substantially changes number of upset bits
- When p-well voltage decreases, number of errors decreases by orders of magnitude
  - From 0 V to -2 V at 500 krad(Si), ~2300x upset bits in DUT 601 and over 34,000x fewer in DUT 609
- Because n-well voltage had no effect, p- and n-well voltage results look identical to p-well only results

Combined Total Ionizing Dose and Single-Event Effects Testing

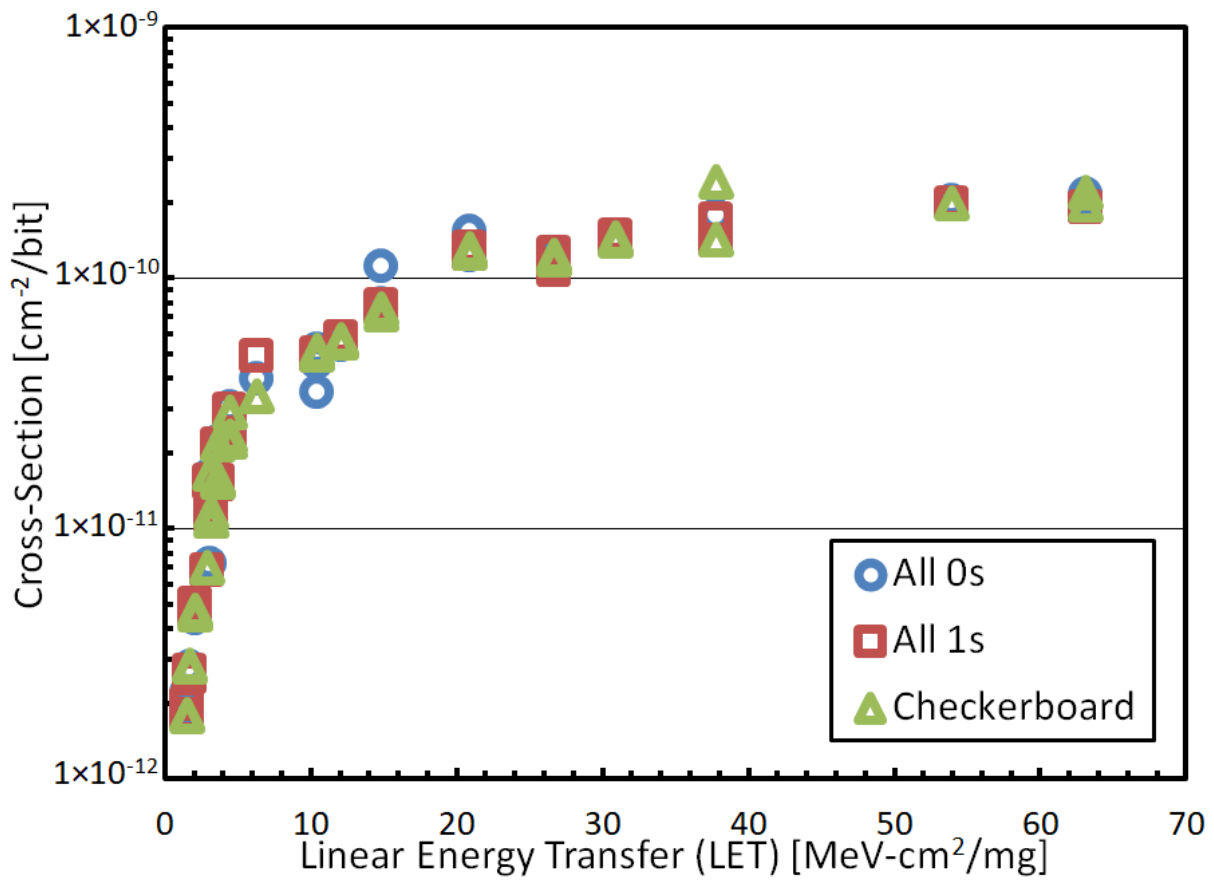
- After TID irradiation, DUTs were stored on dry ice to ensure no annealing and were then transported to LBNL and subjected to heavy ion irradiation
- Due to high levels of gamma dose, on average, about half of all bits were upset before heavy-ion irradiation
  - Made measuring the single-event contribution to the number of upset bits difficult to obtain





Previous SEE Testing

Non-TID-Irradiated SRAMs

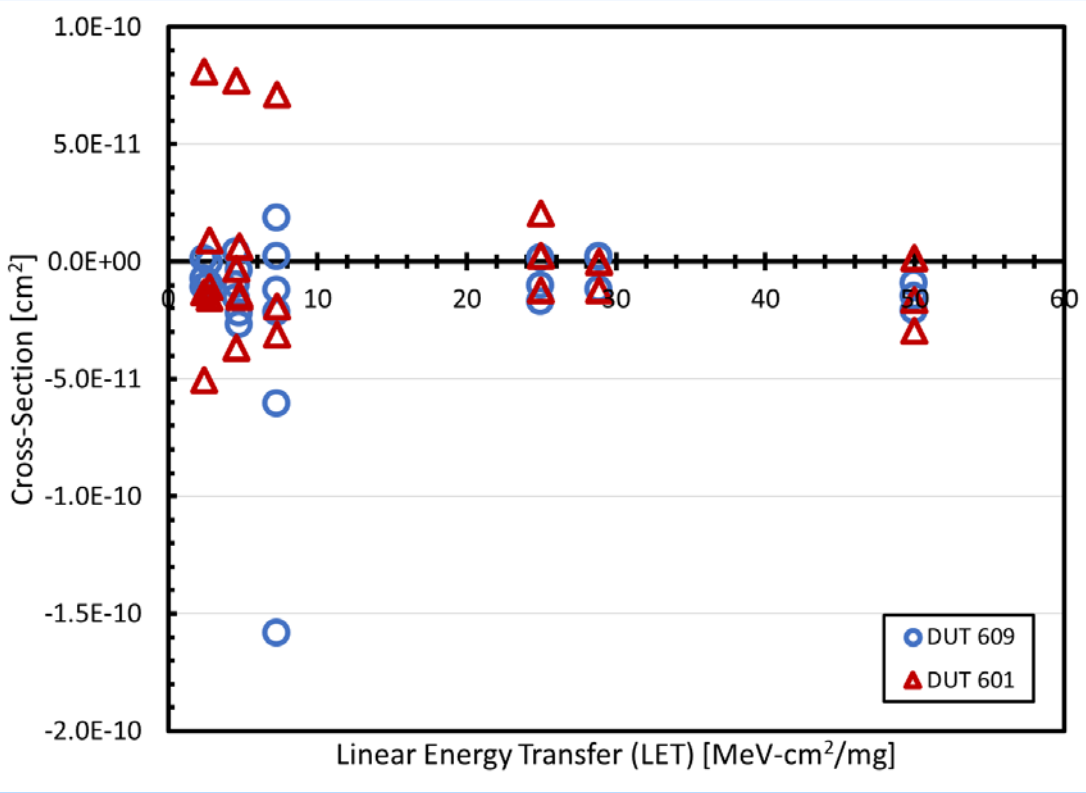


Previous SEE testing conducted on devices that were not TID-irradiated showed no pattern dependence

15 M.C. Casey, submitted to *IEEE TNS*, 2020.

Combined Effects Test Results

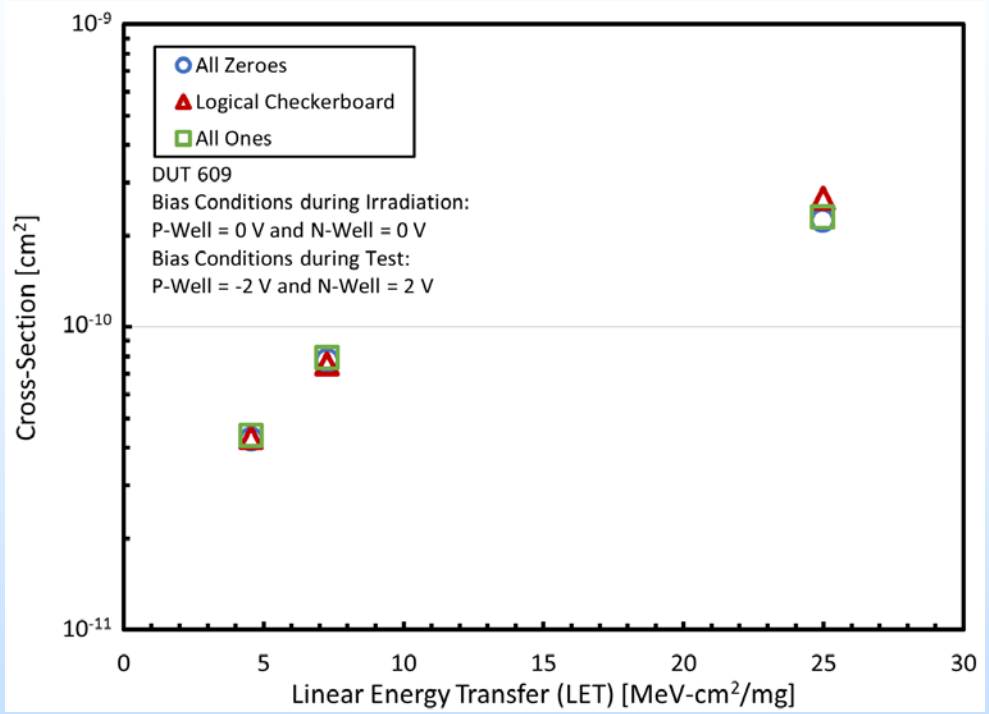
Heavy-Ion Irradiation with Nominal Well Bias Conditions

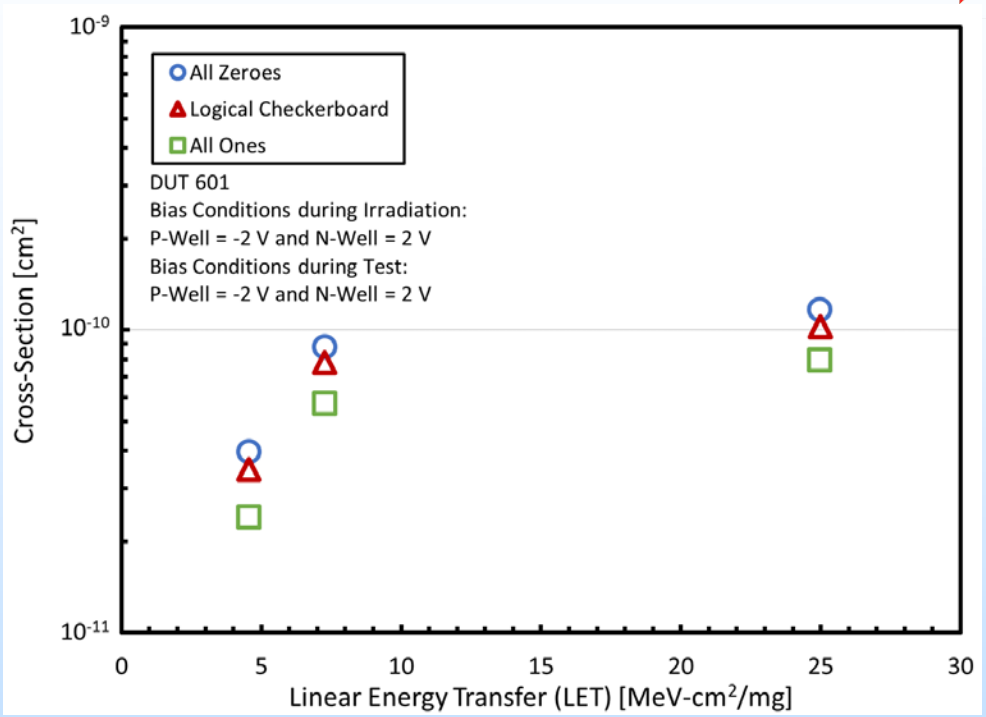


- Because there were so many pre-SEE-testing upset bits, a large portion of the SEE-induced bit flips resulted in corrections from the incorrect memory state to the correct one
  - Results in negative cross-sections that are actually bits that were corrected after heavy ion irradiation
- These results look like the SRAMs are no longer functioning properly

Combined Effects Test Results

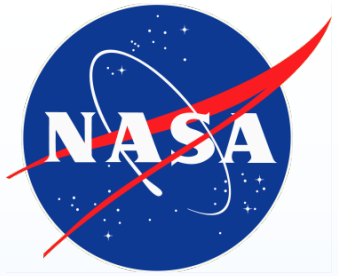
Heavy Ion Irradiation with Extreme Well Bias Conditions





- After changing well biases from nominal to the extreme voltages, more standard cross-section curves emerge
- Same pattern dependence observed in DUT 601 TID data also becomes apparent in the cross-section curves

Conclusions



- TID results suggest by applying well voltages, SRAM memory cells fabricated in GlobalFoundries' 22FDX process have fewer stuck bits than when irradiated with nominal supply voltages
- Input pattern dependence was observed with parts irradiated with extreme well biases, but not in the part with nominal well biases
  - Pattern dependence was also found in the combined effects testing in the device TID-irradiated with the extreme well bias voltages and then SEE-irradiated with the same bias conditions
- Adjusting body biasing through the well voltages provides a TID mitigation strategy
  - N-well bias voltages had no impact on the TID response of the SRAMs
  - P-well voltages had a substantial impact on the TID response
  - All of these results are specific to transistors in these well configurations – flipped-well PMOS transistors and standard-well NMOS transistors