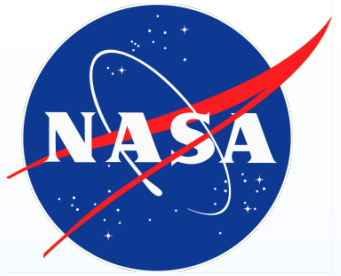

Direct Ionization from Low-Energy Electrons in a Highly-Scaled CMOS Process

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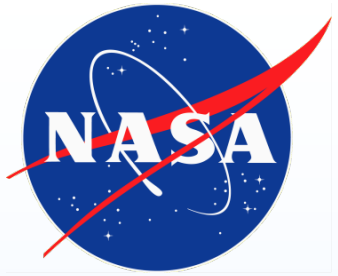
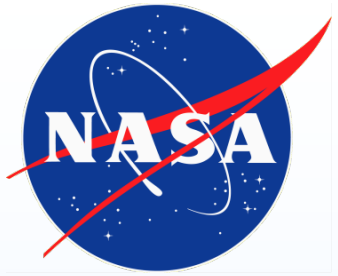
Acronyms



- BOX – Buried Oxide
- DUT – Device Under Test
- FDSOI – Fully-Depleted Silicon-on-Insulator
- GSFC – Goddard Space Flight Center
- NASA – National Aeronautics and Space Administration
- REF – Radiation Effects Facility
- SEE – Single-Event Effects
- SOI – Silicon-on-Insulator
- SRAM – Static Random Access Memory
- STI – Shallow Trench Isolation
- SV – Sensitive Volume

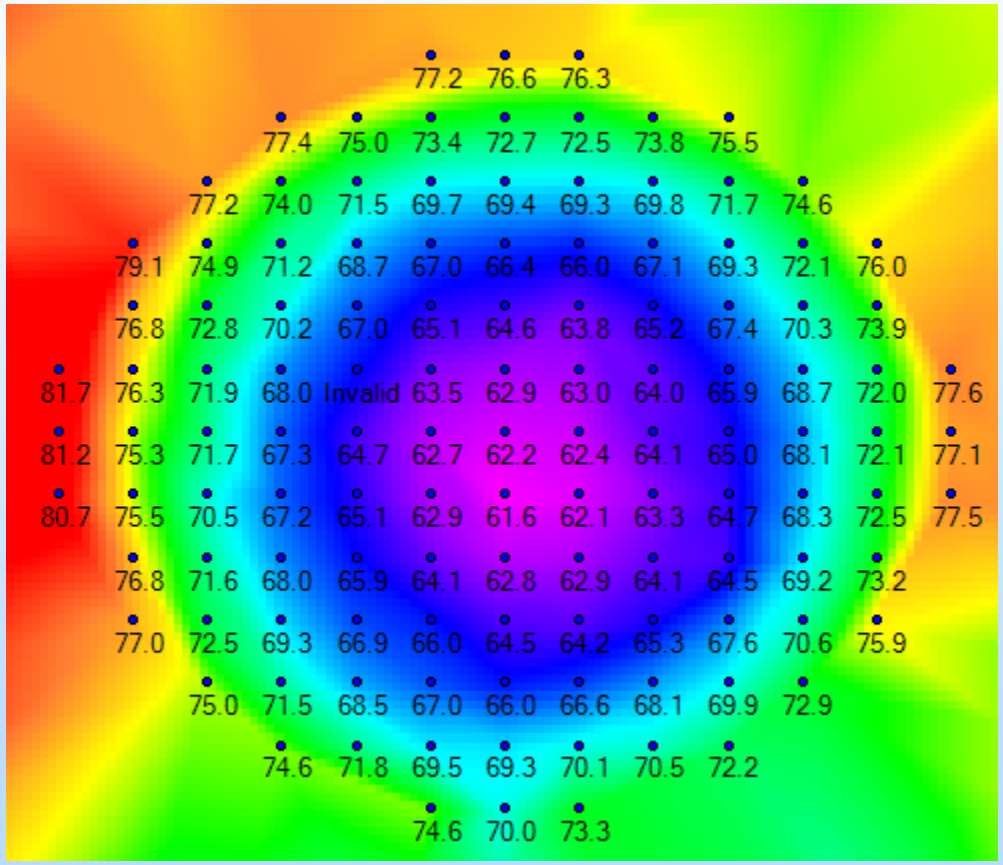
Introduction



- For the past several years, as technology is scaling well into the deep submicron regime SEUs due to direct ionization from protons, muons, and electrons have been observed
- Simulations originally predicted the likelihood of these upsets
- A Monte Carlo Radiative Energy Deposition (MRED) code study verifies that the measured experimental SEU cross-section is consistent with the simulated cross-section

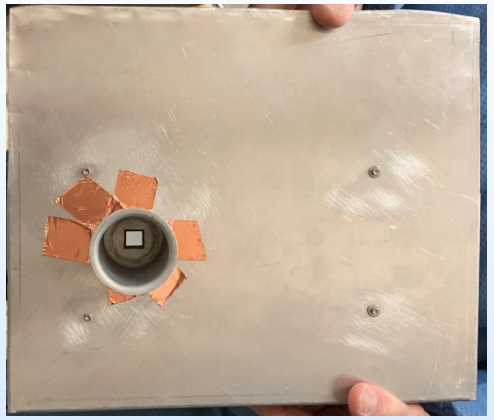
Device Tested

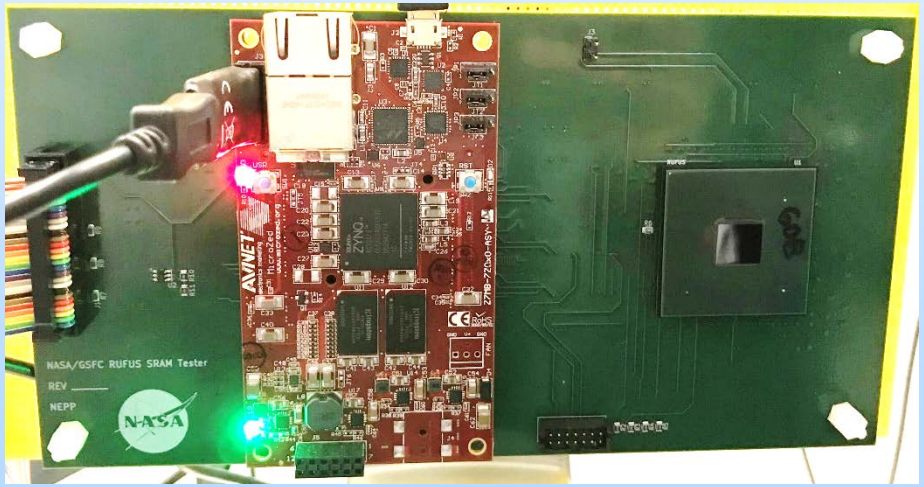
- 128-Mb SRAM fabricated in the GlobalFoundries 22FDX process
  - 22-nm FDSOI technology
  - Previous heavy-ion SEE data approximated the critical charge to be 0.06 fC
- SRAMs were packaged in a flip-chip package and the substrates were thinned to allow for particles to penetrate through the substrate and have sufficient energy/range to reach the SVs



Test Procedure

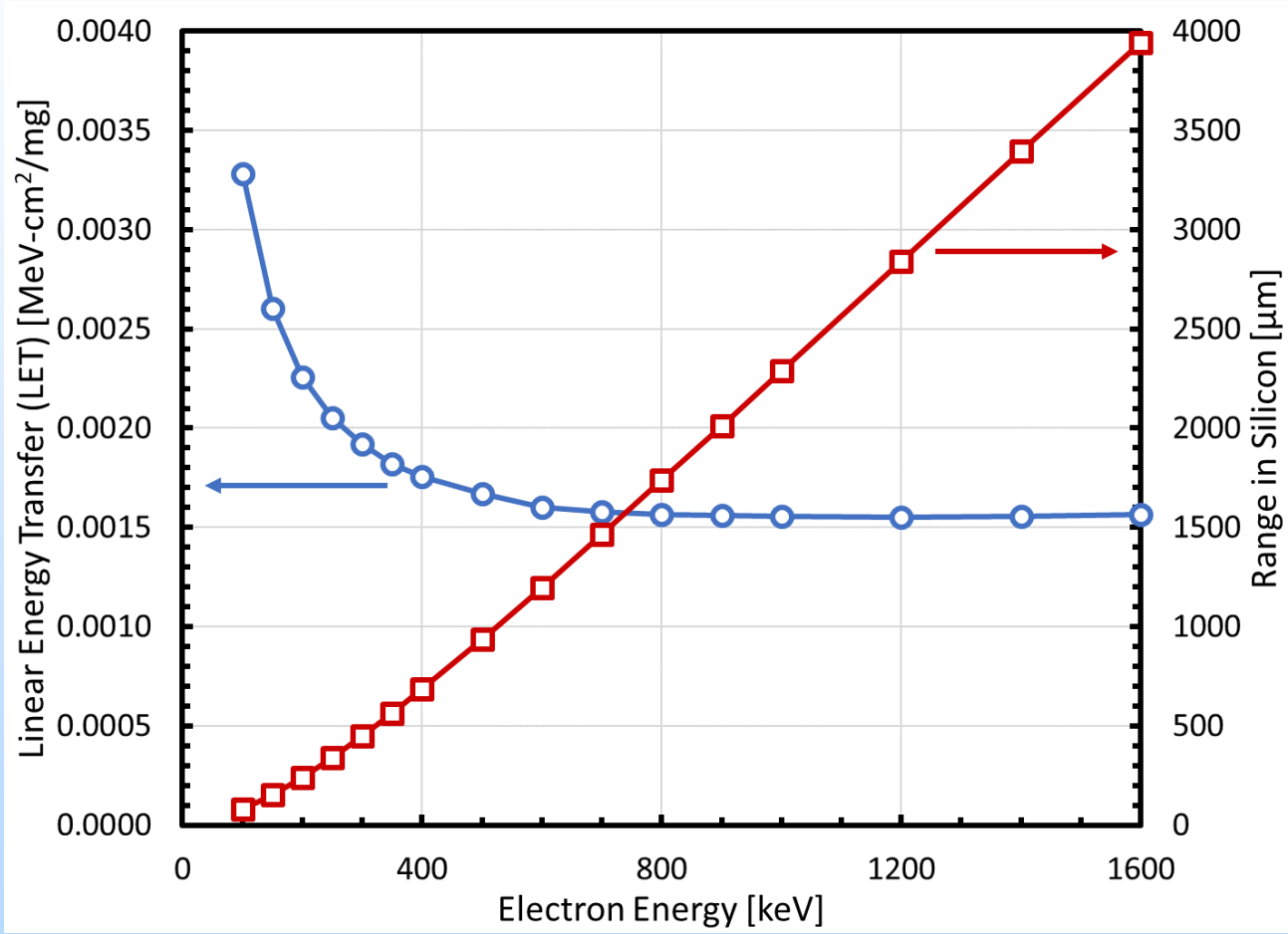
- Custom aluminum masking plate was built to protect board and external circuitry from electrical charging effects
- Before each run, SRAM was programmed and bits were read back
- Device was irradiated and SRAM was reread and number of upset bits was recorded
- Effect of input pattern, supply voltage, and electron energy was investigated





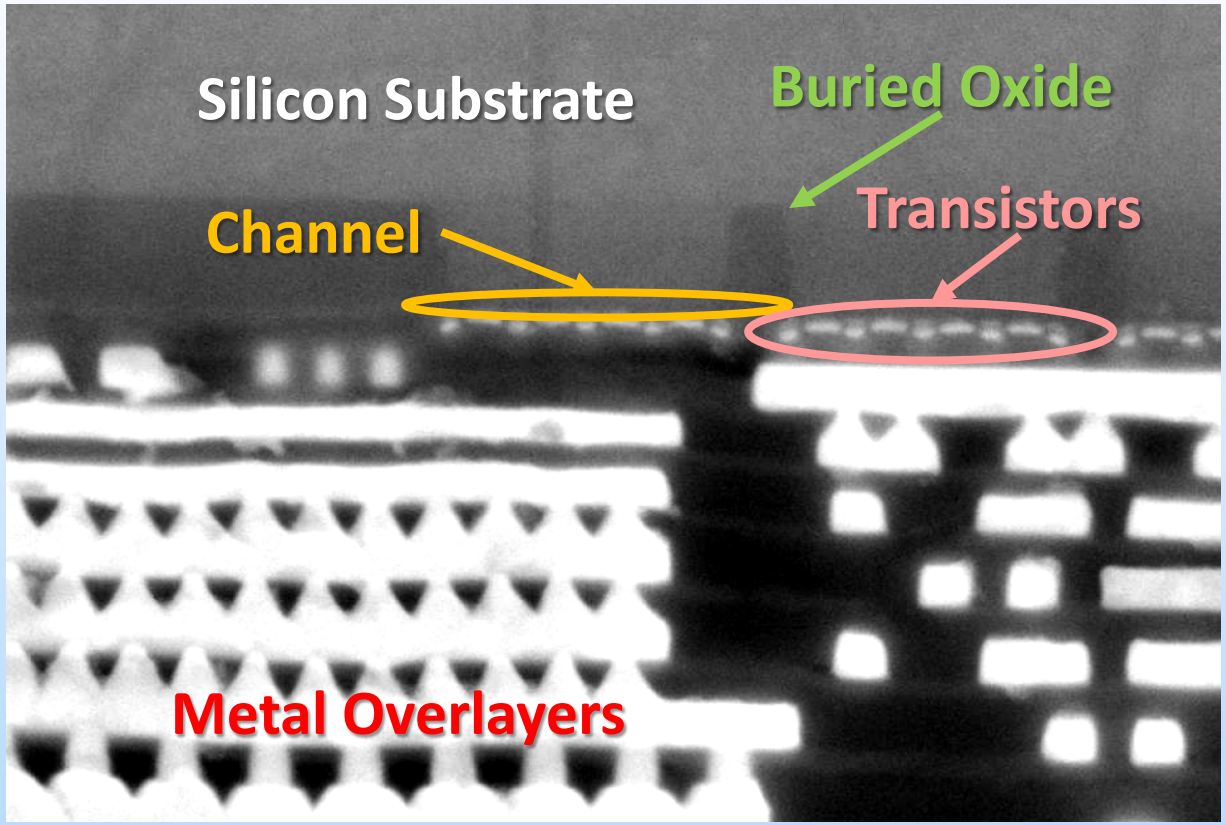
Test Facility

- All experiments were conducted using a 2-MeV Van de Graaff generator at NASA GSFC's REF
- The Van de Graaff generator is capable of supplying either protons or electrons with a mono-energetic beam ranging from approximately 100 keV to 2 MeV
  - In this work, electrons with energies from 130 keV to 1.4 MeV were used



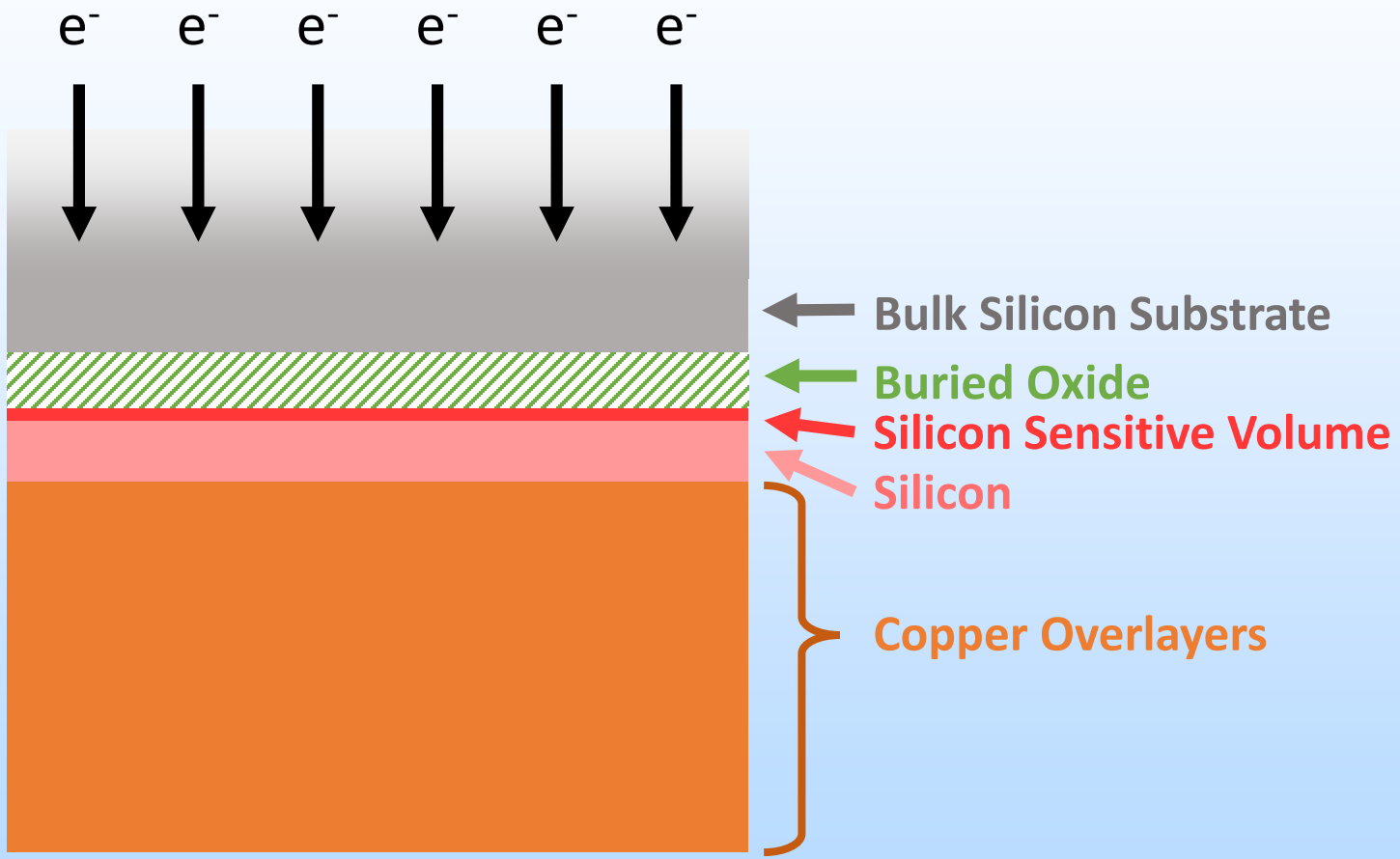
Device Cross-Section

- A single device was cross-sectioned and the thicknesses of the layers were measured
- The substrate is at the top of the image, followed by approximately 30 nm of buried oxide (BOX)
  - The devices are thinned, so the substrate thickness varies across the die as well as between devices
- There is approximately 40 nm of silicon which includes 7-nm deep channel
- Beyond the silicon is 200 nm of metal layers



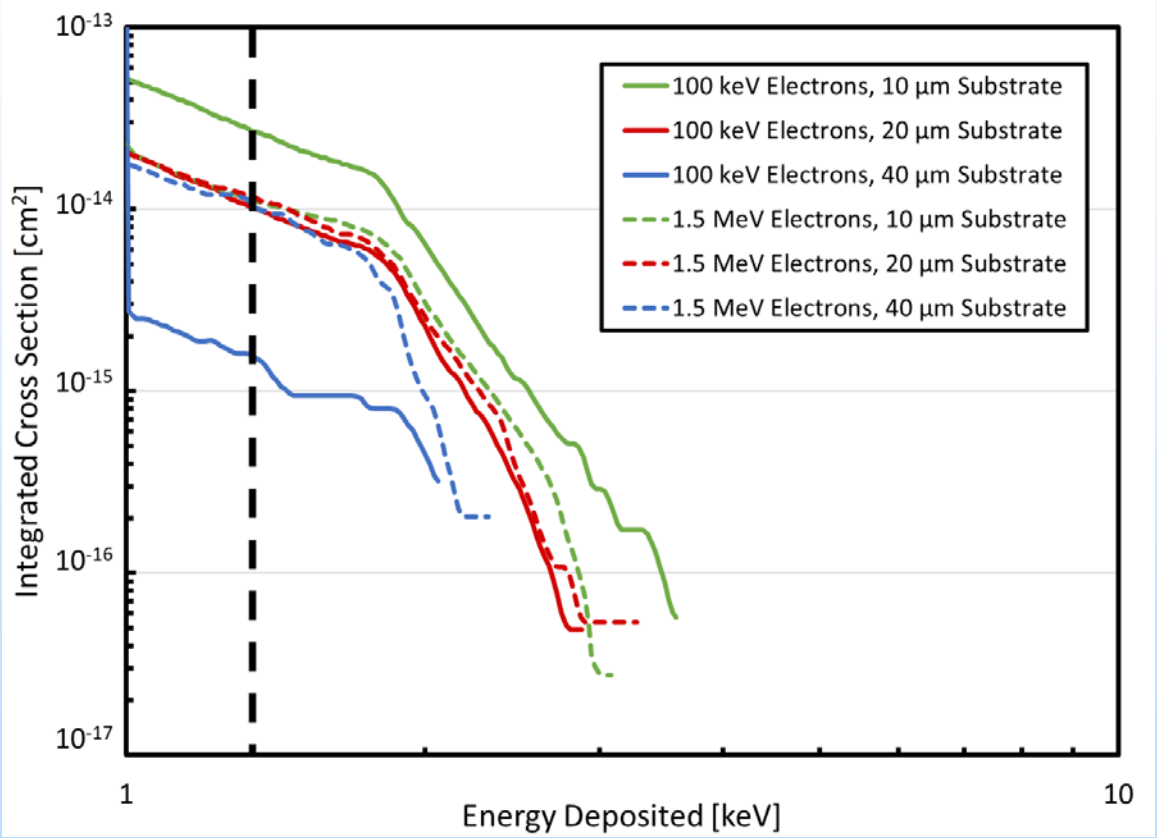
Modeling and Simulation

- Using the layer thicknesses measured in the cross-section, the device was modeled using the MRED code
- The DUTs have some variance in thickness across the surface of the substrate and each DUT has a different substrate thickness
  - Substrate thicknesses of 10, 20, 30, and 40 um were used in the simulations
  - Electron energies of 100 keV and 1.5 MeV were simulated to determine the energy that would be deposited in the sensitive volumes after traversing through the substrate



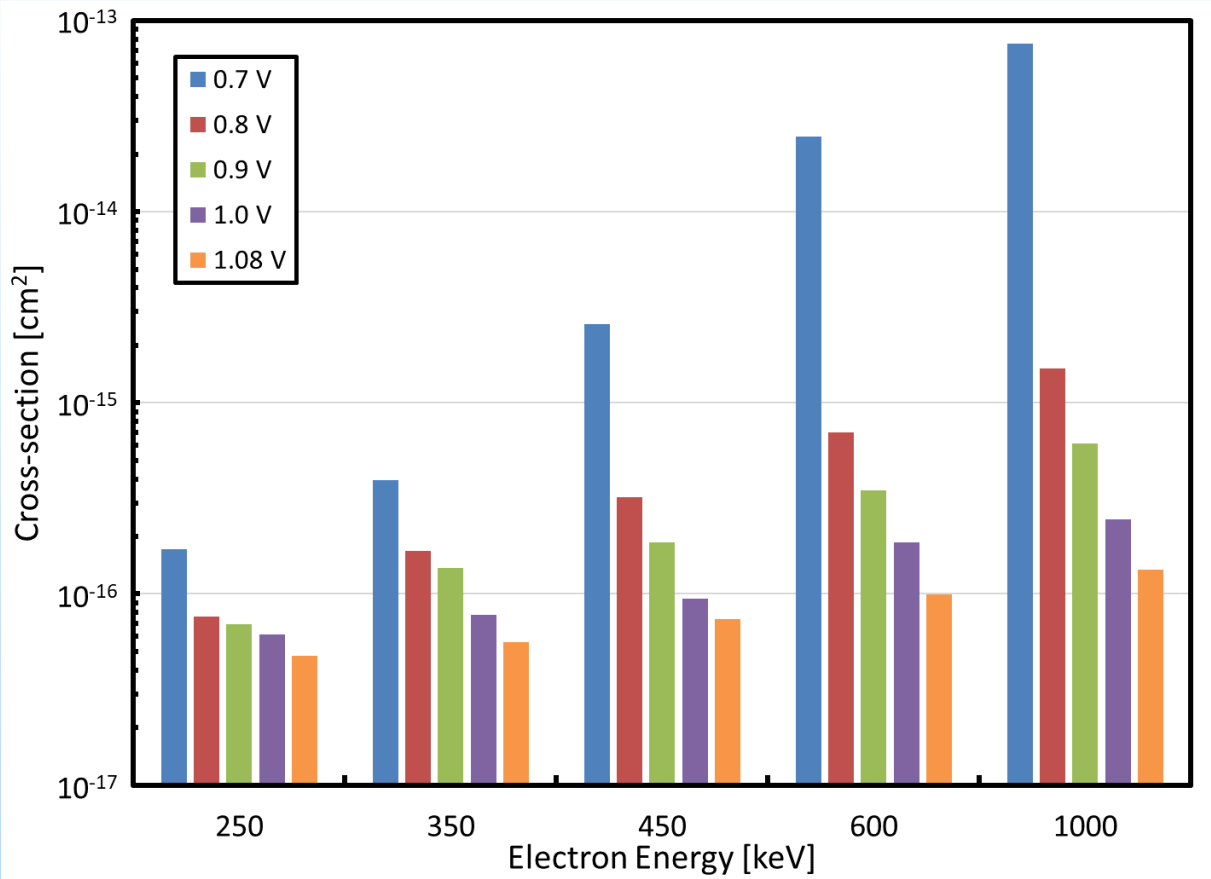
Modeling and Simulation

- Assuming critical charge is 0.06 fC and holes do not contribute to transient current, then critical deposited energy is 1.35 keV
- MRED results indicate enough charge/energy is deposited with low energy electrons to upset 22FDX SRAM bits
- These simulations were also used to estimate the fluence required to see statistically significant numbers of upsets bits

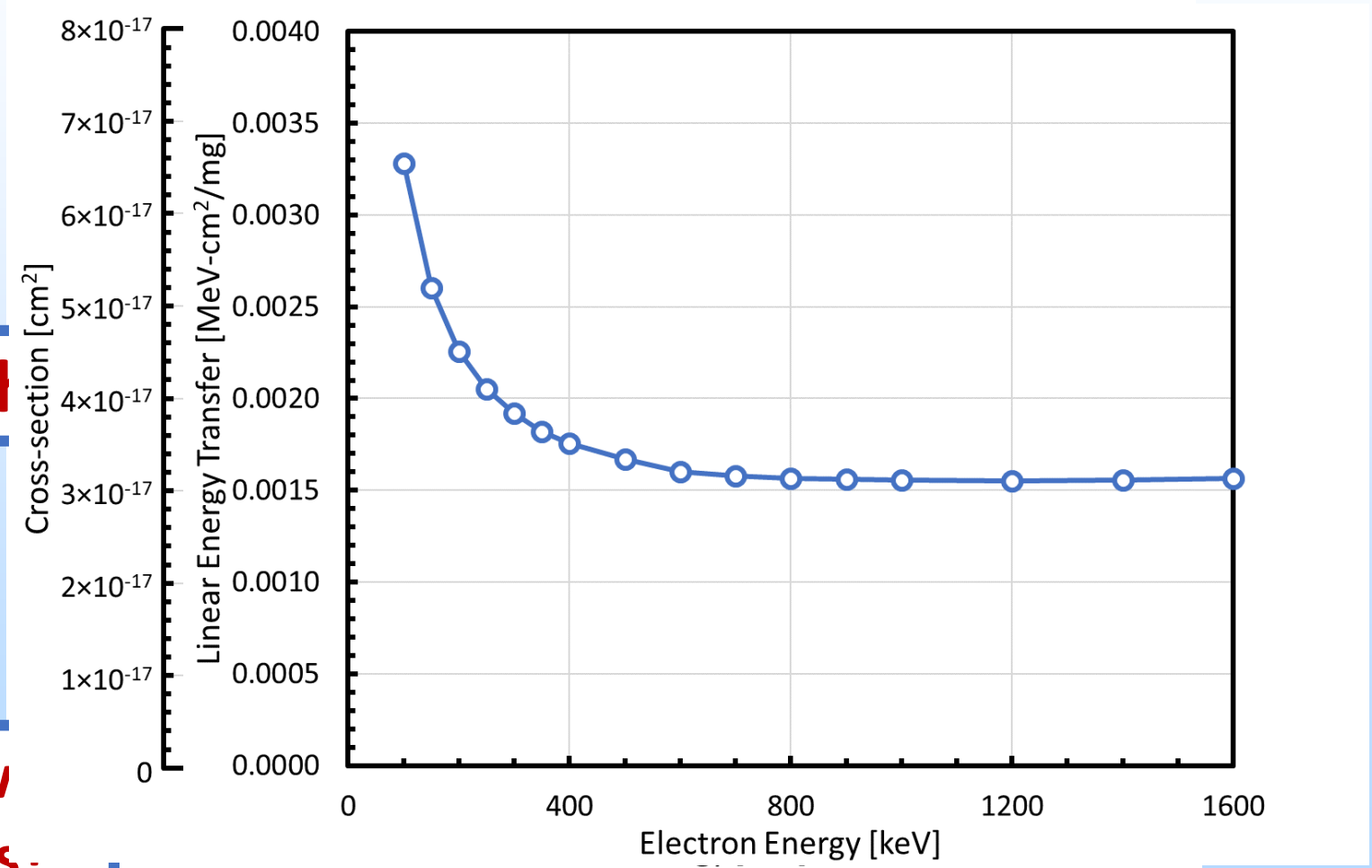


Low-Energy Electron Test Results

- In most of the previous testing, the irradiated devices were operated at voltages lower than nominal to increase the single-event sensitivity
- After several beam runs, the DUT seemed to experience dose effects such that the number of bits that were incorrect before irradiation were comparable with the number that were expected to upset during the run



Low-Energy Electron Test Results

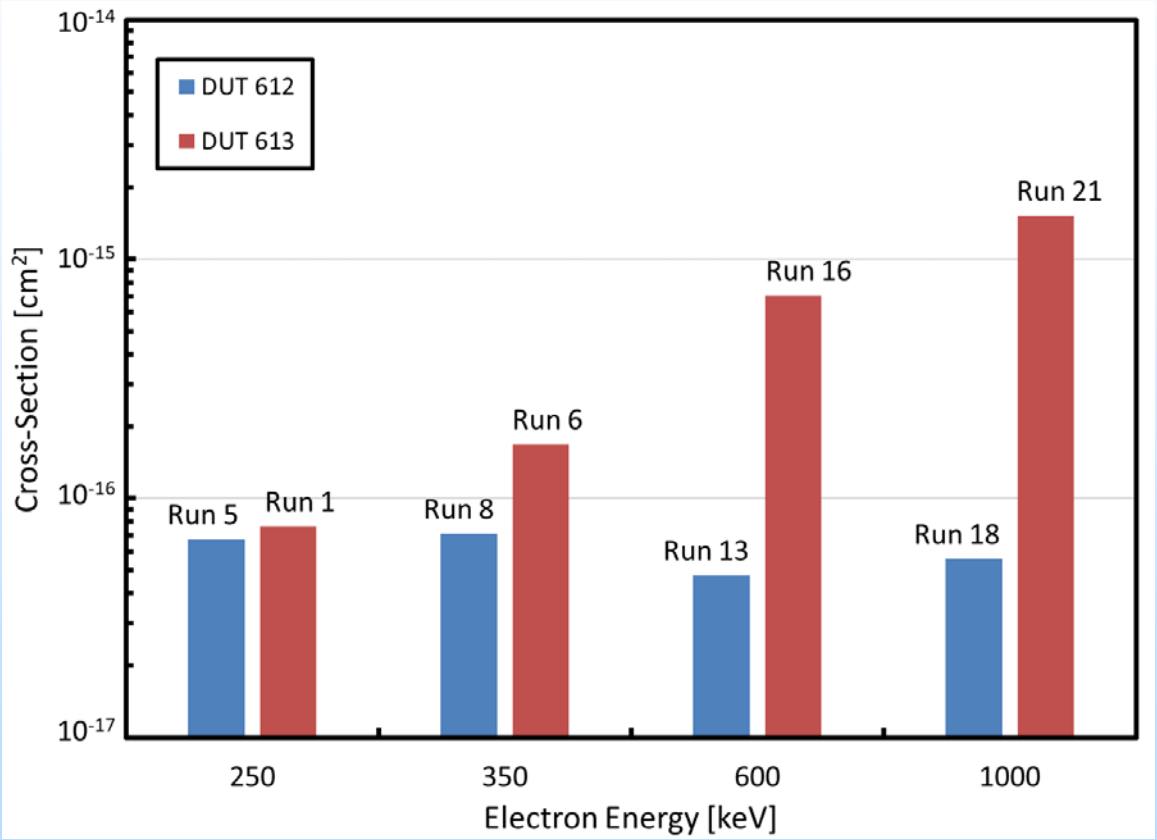


Th

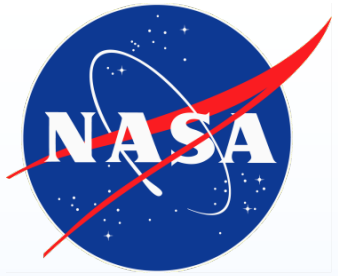
What's going on w these data points

Dose Enhancement

- Previously, other samples of these SRAMs were gamma-irradiated and stuck bits were observed first at 50 krad(Si)
- Stuck bits were observed beginning at a dose of less than 2 krad(Si)
- These results are consistent with research by Gadlage *et al.*, from 2017 where dose enhancement was observed in NAND flash memories irradiated with 20-100 keV electrons compared with gamma irradiations
  - The device with more runs at lower energy appeared to degrade significantly earlier than the device that had only one or two runs per energy



Conclusions



- Low-energy electron irradiations were performed and single-event upsets were observed in a 22 nm fully-depleted SOI process
- The upsets were observed at nominal and higher voltages
- Simulation data agree well with experimental cross-sections
- In addition, the irradiated devices also appeared to suffer dose enhancement similar to what has also been observed in NAND flash memories