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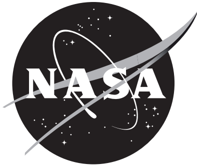

Practical SiC JFET-R Analog Integrated Circuit Design for Extreme Environment Applications

Michael J. Krasowski and Philip G. Neudeck
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May 2021

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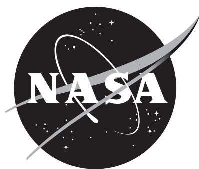

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Abstract

Silicon carbide (SiC) junction field effect transistor and SiC resistor (SiC JFET-R) integrated circuits (ICs) have uniquely demonstrated prolonged operation above 450 °C that promises significant operational improvements to a variety of NASA missions. However, the SiC epiwafers used to fabricate these ICs suffer from epi-growth process immaturity that imparts large and systematic spreads in JFET threshold voltages as a function of the device distance from the center on the wafer. Furthermore, the unprecedently wide range of intended application operating temperatures (in many cases over 600 °C wide) imparts as much as 5-fold change in JFET bias currents. This Technical Memorandum documents methods by which both temperature and radius associated JFET electrical parameter variances can be adequately eliminated, or even exploited in JFET-R circuit designs. Full analog circuit examples, including operational amplifiers, and SPICE simulations across experimentally documented SiC JFET parameter extremes are given to illustrate the efficacy of these methods. The reader may use the examples in this memorandum as either an end point, to get a desired analog signal conditioning design into hardware implemented in SiC JFET-R ICs, or as a basis point from which to derive further improvement.

1.0 Introduction and Background

A variety of aerospace, automotive, energy production, and other industrial systems are expected to benefit from expansion of the practical operating environment envelope of transistor integrated circuits (ICs) (Refs. 1 and 2). For useful infusion into most envisioned applications, it is a critical requirement that the IC function reliably for years in the harsh environment without degradation in functional circuit behavior. As of this writing in December 2020, the silicon carbide (SiC) junction field effect transistor + SiC resistor (SiC JFET-R) ICs fabricated at NASA Glenn Research Center have been the *first and only semiconductor devices reported as of this writing to demonstrate over a year of stable electrical operation at 500 °C (Refs. 3 and 4)*. These SiC JFET-R ICs have also been the first and only electronics ever to successfully operate for 60 days uncooled and unsheltered from a high-fidelity chamber simulation of the Venus surface environment (a highly reactive gas mixture at 460 °C and 9.4 MPa pressure) (Ref. 5). For Venus surface missions in particular, astonishingly improved mission metrics are enabled by the ability of SiC JFET-R ICs to operate without sheltering (compared to electronics that require environmental sheltering), including for example 60 days (compared to 1 day) of science data operations from a lander less than 20 kg in mass (compared to almost 700 kg) (Refs. 6 and 7).

As increasingly complex SiC JFET-R chips are being successively prototyped, correspondingly enhanced mission-relevant circuit capabilities (both digital and analog) can be realized. These SiC ICs are already surpassing chip complexities (in terms of transistors/chip) that successfully flew on Apollo and explored the solar system in the 1970s (e.g., Viking and Voyager) (Ref. 8). However, the relatively immaturity of SiC JFET-R IC fabrication technology compared to (many decades) more mature silicon

fabrication must be accommodated in order to obtain application-desired circuit functionalities. At the same time, SiC JFET-R ICs will be expected to function across temperature ranges 2 to 5 times wider than silicon ICs.

A major such issue effectively solved by this Technical Memorandum is the fact SiC IC JFETs and resistors experience large and systematic parametric changes, both as a function of temperature and also as a function of the radial distance from wafer center from which a device is harvested. It is well-known in the art of field-effect transistor (FET) IC design that threshold voltage V_T is a critical transistor electrical parameter greatly affecting the IC performance characteristics. Figure 1(a) plots a typical example of experimentally observed systematic change in SiC JFET threshold voltage V_T that correlates with how far from the center of the SiC wafer each particular SiC JFET physically resides. Such large (nearly 8V) variation in V_T was eliminated from silicon IC manufacturing many decades ago. The major physical reasons for the SiC JFET V_T variation is detailed in Reference 9, and it may take a number of years to shrink this variation down to sub-volt magnitude. In order for practical manufacturing of SiC JFET-R ICs to become viable within the nearer term, it is necessary that the majority of SiC ICs perform needed electrical functionality regardless of the location/region of the wafer they were harvested from.

In addition, many envisioned applications (especially in aerospace) will require "cold start" capability in addition to extreme high temperature operation. It is therefore vital that SiC JFET-R ICs perform their intended electronic functions across unprecedently large temperature spans (more than 600 °C span in some applications). Figure 1(b) illustrates the 25 to 500 °C temperature variation of another important field-effect transistor (FET) parameter, saturation drain current (I_{DSS}). Practical circuit design will have to accommodate large (>300 percent for I_{DSS}) JFET electrical parameters changes. Since this change is driven by fundamental SiC epilayer conduction behavior as a function of temperature (Ref. 10), advancing processing maturity will never significantly reduce the strong temperature dependence shown in Figure 1(b).

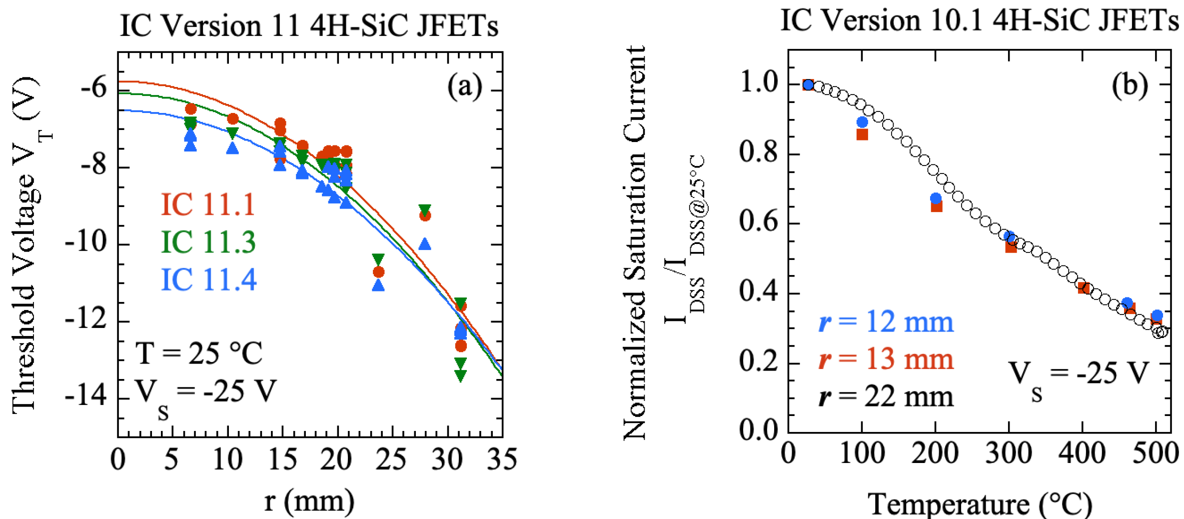


Figure 1.—Measured 4H-SiC JFET data illustrating *large but systematic* changes to key JFET electrical parameters typically observed in prototype SiC JFET-R fabrication runs. (a) JFET threshold voltage V_T change as a function of device radial position observed on prototype IC Version 11 devices. (b) JFET saturation current I_{DSS} change as a function of temperature observed on prototype IC Version 10.1 devices.

The circuit design techniques described in this Technical Memorandum enable desired electrical circuit functionality to be achieved despite the large systematic variations in JFET electrical parameters, which is critical to the practical design, manufacture and deployment SiC JFET-R ICs into desired harsh-environment applications. In particular, this memorandum provides methods by which both temperature- and radius-associated variances can be adequately eliminated, or even exploited. Further, full circuit examples with SPICE simulations are given to illustrate the efficacy of these methods. The reader may use the examples in this paper as either an end point, to get a desired signal conditioning design into hardware, or as a basis point from which to improve the designs. As NASA Glenn Research Center developmental device characteristics improve, the insights contained herein shall still apply.

1.1 SiC Device SPICE Models

The rest of this Technical Memorandum seeks to illustratively communicate the needed beneficial design techniques as applied to the design of actual SiC JFET-R integrated circuits that are presently undergoing fabrication as the NASA Glenn "IC Version 12" prototype run. In order to keep this Technical Memorandum focused on the primary intended subject matter of analog circuit design techniques, we now assume that the reader is already familiarized with the following online background information regarding the JFET-R IC Version 12 (ICv12) basic device structures and SPICE models summarized in the online "NASA Glenn SiC JFET IC Tech Guide" at https://sic.grc.nasa.gov/jfetictechguide/. The most technically relevant links referred to within this Tech Guide include:

IC Version 12 Mask Layout Primer, which details JFET and resistor device structures and layout rules: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190025716.pdf

IC Version 12 JFET SPICE Modeling Primer, which details the SPICE models used JFETs as function of T and *r*: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190026451.pdf

IC Version 12 Resistor SPICE Modeling Primer, which details the SPICE models used for resistors: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20190026452.pdf

Sufficient understanding of the above-referenced technical information is necessary background for understanding of this Technical Memorandum, in addition to electrical engineering understanding of semiconductor field-effect transistor electrical behavior, analog electronic circuits, schematic diagrams, SPICE computer electrical circuit simulation, and amplifiers.

While the experimental JFET parameter variations illustrated in Figure 1 are indeed substantial in magnitude, the variations exhibit (at least to first order) *systematic dependence* upon radial wafer position *r* (as seen in Figure 1(a)) and temperature T (as seen in Figure 1(b)). Instead of employing complicated parametric device equations and analysis, we instead chose to conduct simplified device modeling and circuit design based at benchmark values for both T and *r* that form 9 unique (T,*r*) combinations. In particular, we selected benchmark T values of 25, 460 (Venus surface), and 500 °C and benchmark *r* values of 10, 20, and 30 mm resulting in 9 device combinations of benchmark device electrical properties that effectively encompass the majority of anticipated operating temperatures and wafer surface area. In other words, if circuits are designed and SPICE-verified to perform desired operation across all 9 of these disparate combinations of electrical device parameters, there is confidence that ICs with electrical parameters therebetween (i.e., arising from *r* and T conditions therebetween) will also successfully function.

For reasons detailed in the above-referenced IC Version 12 JFET SPICE Modeling Primer, we employ baseline silicon NMOS device SPICE models to simulate the electrical behavior of our SiC JFETs. *Correspondingly, the silicon nMOSFET schematic symbol (and label that starts with "JFET…") is employed to represent SiC n-JFETs in schematic diagrams in this Technical Memorandum in lieu of using a traditional n-JFET schematic diagram symbol*. Table I (reproduced from page 12 of the IC Version 12 JFET SPICE Modeling Primer) shows the actual JFET SPICE models employed simulating the nine combinations of T and *r*. That the SPICE VTO parameter ranges from –9.4 to –15.7 V while the KP parameter spans 10.6 to 1.9 µA/V^2 exemplify the substantially large electrical parameter spreads that are being dealt with in these SiC JFET-R integrated circuit designs.

*The JFET models employed in SPICE simulations are displayed in all schematic diagrams of this Technical Memorandum as "JFET**TTT**C**RR**v12", where **TTT** is temperature in °C, and **RR** is device radial location on the wafer in mm*. These models are calculated estimations since the actual ICv12 devices have yet to be fabricated and electrically characterized as of this writing.

TABLE I.—ESTIMATED SPICE MODELS OF IC VERSION 12 JFETS VS. TEMPERATURE (T) AND RADIAL WAFER POSITION (*r*)

T	***r***	**Estimated SPICE Models for Unit Cell M = 1 W_G = 6 µm / L_G = 3 µm** **NASA Glenn IC Version 12 JFET**
25 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-9.443 KP=1.058E-5 GAMMA=0.9207 LAMBDA=0.0200 RSH=0.000E+0 CJ=6.856E-5 PB=2.870 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.435 RD=7799 RS=7799
25 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-11.401 KP=1.008E-5 GAMMA=0.9952 LAMBDA=0.0200 RSH=0.000E+0 CJ=6.856E-5 PB=2.870 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.435 RD=7799 RS=7799
25 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-14.979 KP=9.340E-6 GAMMA=1.1194 LAMBDA=0.0200 RSH=0.000E+0 CJ=6.856E-5 PB=2.870 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.435 RD=7799 RS=7799
460 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-10.088 KP=2.393E-6 GAMMA=0.9207 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.065E-5 PB=2.074 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.037 RD=11464 RS=11464
460 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-12.065 KP=2.277E-6 GAMMA=0.9952 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.065E-5 PB=2.074 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.037 RD=11464 RS=11464
460 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-15.674 KP=2.108E-6 GAMMA=1.1194 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.065E-5 PB=2.074 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=1.037 RD=11464 RS=11464
500 °C	10 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-10.155 KP=2.162E-6 GAMMA=0.9207 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.220E-5 PB=1.997 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=0.998 RD=12314 RS=12314
500 °C	20 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-12.134 KP=2.057E-6 GAMMA=0.9952 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.220E-5 PB=1.997 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=0.998 RD=12314 RS=12314
500 °C	30 mm	.MODEL JFETModel NMOS LEVEL=1 VTO=-15.747 KP=1.904E-6 GAMMA=1.1194 LAMBDA=0.0200 RSH=0.000E+0 CJ=8.220E-5 PB=1.997 CGDO=0.000E+0 CGSO=0.000E+0 JS=0.000000E+0 PHI=0.998 RD=12314 RS=12314

In addition to the "JFET***TTT***C***RR***v12" labels, each SiC JFET in the schematics also are labeled with an "M = **i**" label, where **I** is an integer that scales the gate width of the JFET measured in "number of paralleled W_G = 6µm/L_G = 3 µm unit-JFET layout cells" (as detailed on page 13 of the IC Version 12 JFET SPICE Modeling Primer). In simple terms, an "M = 2" SiC JFET conducts nearly twice as much current and has nearly twice the gate width as an "M = 1" SiC JFET (it is not exactly twice due to gate-end layout geometry). For IC Version 12, the physical JFET gate width $W_G \cong$ 6 µm x M, while all JFET gate lengths are constant at L_G = 3 µm. Because the SiC chip backside substrate bias impacts SiC JFET electrical characteristics, it is important to always connect the bulk terminal of the nMOSFET schematic diagram element (that SPICE-models the SiC n-JFET) to -VSS for consistency with the substrate biasing used to operate these SiC JFET-R ICs.

For reasons detailed in the IC Version 12 resistor SPICE Modeling Primer, we also employed silicon NMOS device SPICE models to simulate the electrical behavior of our SiC n-channel resistors. *Correspondingly, the silicon nMOSFET symbol (and label that starts with "RJFET…") is employed to represent SiC resistors in all schematic diagrams in this Technical Memorandum in lieu of using a traditional resistor schematic diagram symbol*. In an important distinction from SiC JFET behavior, the SiC resistors do NOT exhibit significant dependence on radial wafer position *r* (Ref. 10). This fundamental behavior difference arises from the fact that resistor channels are dominated by ion implantation doping that results in far more uniform sheet charge density than the SiC epitaxy that governs JFET conduction (Ref. 11). Table II (reproduced from page 10 of the IC Version 12 resistor SPICE Modeling Primer) shows the actual resistor models employed in this work that only depend upon temperature.

*The resistor models employed in SPICE simulations are annotated in all schematic diagrams of this Technical Memorandum as "RJFET**TTT**v12", where **TTT** is temperature in °C*. Furthermore, the effective number of resistance squares defined by the resistor layout (= length/width for a straight-rectangle resistor layout neglecting contact and end resistances) is also annotated by each resistor of schematic diagrams. Because the SiC chip backside substrate bias impacts SiC resistor I-V characteristics, it is important to always connect the bulk terminal of the nMOSFET schematic diagram element that SPICE-models the SiC resistor to -VSS for consistency with the substrate biasing used to operate these SiC JFET-R ICs.

TABLE II.—ESTIMATED SPICE MODELS FOR NASA GLENN IC VERSION 12 RESISTORS

T	SPICE Model for IC Resistors Including Substrate Body Bias Effect
25 °C	.MODEL RbodyBiasModel NMOS LEVEL=1 VTO=-151.256 KP=1.819E-6 CJ=6.856E-5 PB=2.870 PHI=1.435 RSH=0.000E+0 GAMMA=1E-12 RS=5073 RD=5073 JS=1.00E-25
460 °C	.MODEL RbodyBiasModel NMOS LEVEL=1 VTO=-136.774 KP=5.647E-7 CJ=8.065E-5 PB=2.074 PHI=1.037 RSH=0.000E+0 GAMMA=1.00E-12 RS=1753 RD=1753 JS=1.00E-25
500 °C	.MODEL RbodyBiasModel NMOS LEVEL=1 VTO=-135.480 KP=5.183E-7 CJ=8.220E-5 PB=1.997 PHI=0.998 RSH=0.000E+0 GAMMA=1.00E-12 RS=1634 RD=1634 JS=1.00E-25

2.0 Determination of Radius Dependent Drain Voltage Behaviors

LTSPICE (Ref. 12) schematic circuit drawing and simulations are henceforth used to illustrate the salient circuit design principles.

Figure 2(a) on the left shows a schematic circuit diagram of a SiC JFET-R common source circuit consisting of and SiC JFET (size M = 2 unit-cells) in series with a 300 square SiC resistor. Figure 2(b) on the right illustrates 10 alternate equivalent circuit representations (screen-captured from the LTSPICE schematic editor) of the Figure 2(a) common source circuit *wherein each of the 10 represents its own unique combination of SiC JFET and SiC resistor device models*. In other words, each circuit in Figure 2(b) is formed using different combinations of benchmark T and *r* SPICE models. The purpose of having the same circuit but with 10 unique combinations of device models is to simultaneously illustrate/plot what happens to the drain current (I_d) through the SiC JFET when sweeping of the gate to source voltage (V_{gs}) across various combinations of T and *r* circumstances. As can be deduced from the annotation labels of devices on the Figure 2(b) schematic, proceeding from left to right: The leftmost three common source circuits of Figure 2(b) reflect a 25 °C model at a radius of 10, 20, and 30 mm, respectively. The next two common source circuits of Figure 2(b) reflect a 300 °C model at a radius of 10, and 20 mm, respectively. The next two common source circuits of Figure 2(b) reflect a 460 °C model at a radius of 10 and 20 mm. The rightmost three common source circuits of Figure 2(b) reflect a 500 °C model at a radius of 10, 20, and 30 mm, respectively.

As introduced in the SPICE model section, Figure 2(b) replaces the 300 square resistor schematic diagram symbol seen in Figure 2(a) with a silicon nMOSFET schematic diagram symbol (with “300” annotations and bulk terminals tied to VSS2). Likewise, Figure 2(b) substitutes M = 2 silicon nMOSFET symbol for the Figure 2(a) SiC nJFET symbol. The 1 Ω current-sense resistors in Figure 2(b) merely facilitate simplified SPICE-simulated current plotting.

Figure 3 illustrates the SPICE simulation results when a linear ramp of voltage from –2 to –12 V (a sufficient voltage span to capture any interesting activity) is applied to all of the Vgate terminals of Figure 2(b). VDD2 is +25 V, corresponding to a standard supply voltage used in our SiC JFET ICs, and the SiC JFET source terminals are all grounded. Traces are labeled to show the current through the 1 Ω sense resistor in each circuit, named to reflect the corresponding temperature and radius combinations being tested. In particular, the label format is **I(R[temperature in °C]r[radius in millimeters])**. For example, I(R500r20) is the current through the sense resistor in the T = 500° C, r = 20 mm circuit that is 2nd to rightmost schematic in Figure 2(b). The four Figure 3 sub-plots are grouped by temperature: 25 °C on the bottom plot, increasing to 500 °C on the top plot.

As can be seen in the Figure 3 SPICE simulation result plots, as radius *r* in each instance increases, the threshold voltage of the transistor (reflected in the transition voltages between zero and non-zero currents) increases in negative magnitude. As temperature increases, the current through the circuit decreases to reflect increasing resistance proportional to temperature.

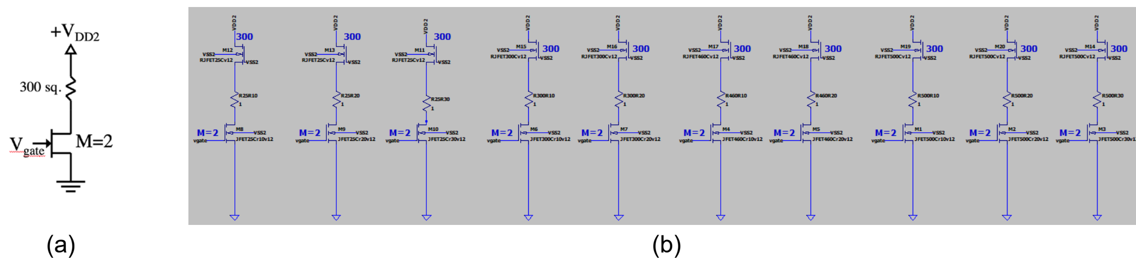


Figure 2.—Schematic diagrams of simple SiC JFET-R common-source circuits. (a) The basic circuit without specifying T or *r* conditions/models. (b) 10 of the same circuit, but each with unique combination of SPICE models corresponding to various benchmark T and *r* conditions (as annotated) and a 1 Ω current-sense resistor added.

Figure 4 to Figure 9 with annotated plot cursors included illustrate quantitative details of the Figure 3 plots. At each respective temperature, the threshold voltage changes by about 1.65 V between the r = 10 mm and r = 20 mm results. For those simulations where the r = 30 mm models exist (25 and 500 °C), the threshold voltage changes by about 3 V between r = 20 mm and r = 30 mm.

To create circuits which operate identically (enough) regardless of temperature or radius, it is intuitively obvious that suitable compensation for these threshold voltage shifts must be employed. The observation that from radius 10 to 20 mm, the change remains at about 1.64 V, and that from 20 to 30 mm, the change is around 3 V, suggests that this demonstrated stationarity is the basis of a solution.

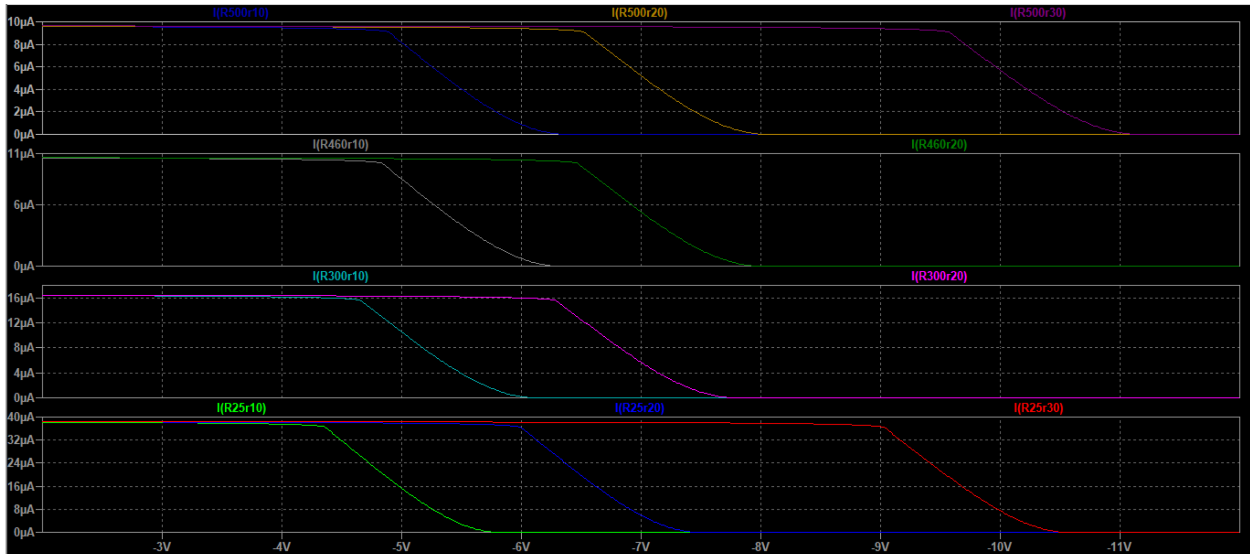


Figure 3.—SPICE simulation results of the common-source Figure 2 circuit current versus Vgate input voltage characteristics illustrating the differences arising from the 10 different combinations of T and r device models used in the simulations.

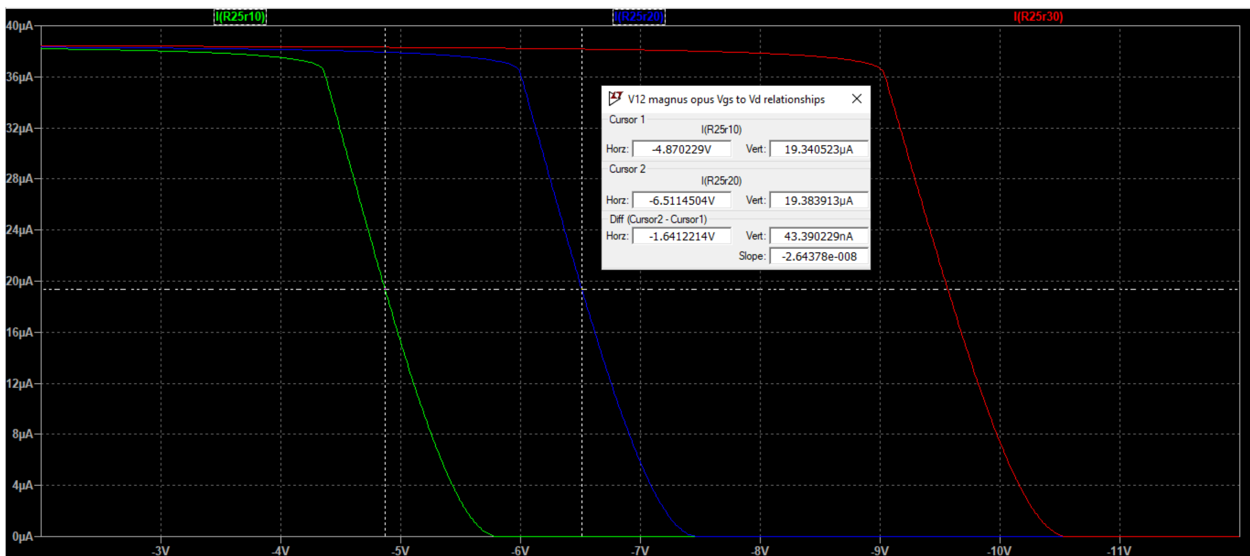


Figure 4.—The 25 °C SPICE simulation results (i.e., the bottom plot of Figure 3) enlarged with cursors highlighting the –1.64 V shift in characteristics between r = 10 mm (green trace) and r = 20 mm (blue trace).

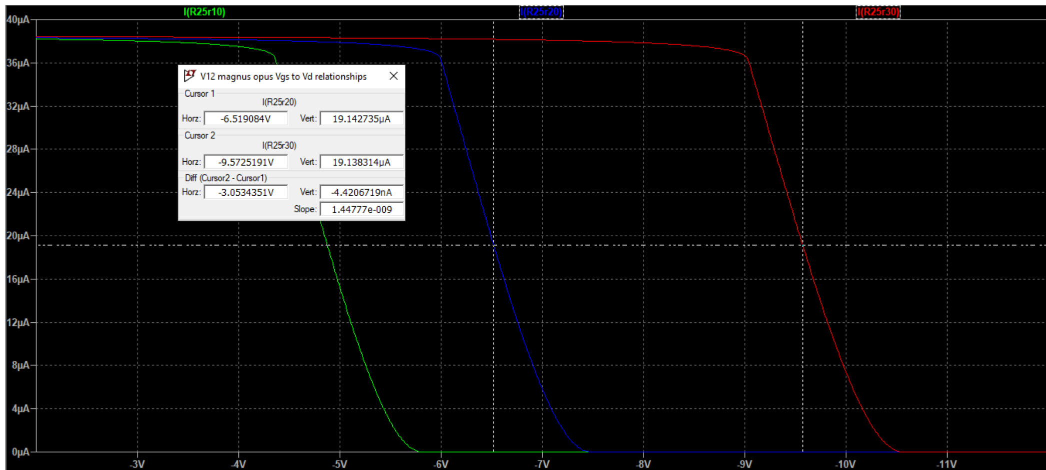


Figure 5.—The 25 °C SPICE simulation results (i.e., bottom plot of Figure 3) enlarged with cursors highlighting the –3.05 V shift in current versus voltage characteristics between r = 20 mm (blue trace) and r = 30 mm (red trace).

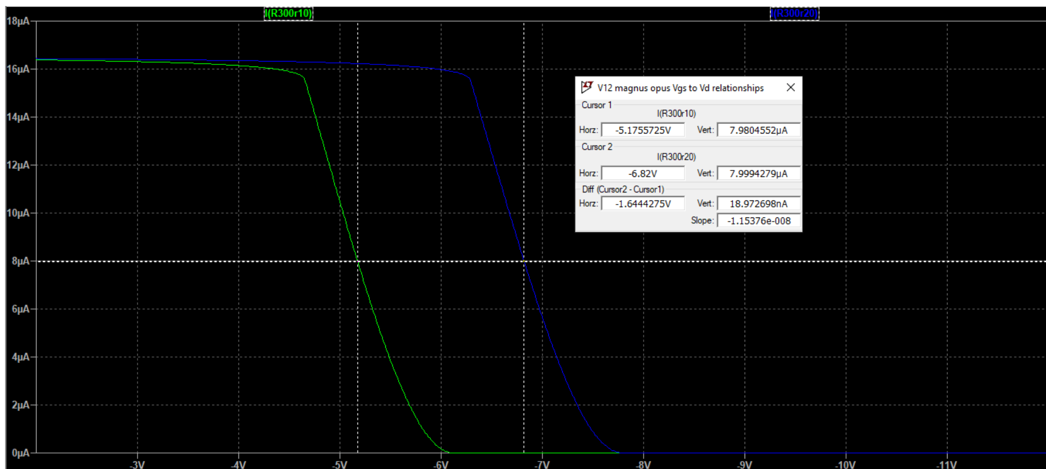


Figure 6.—The 300 °C SPICE simulation results (i.e., 3rd from top plot of Figure 3) enlarged with cursors highlighting the –1.64 V shift in characteristics between r = 10 mm (green trace) and r = 20 mm (blue trace).

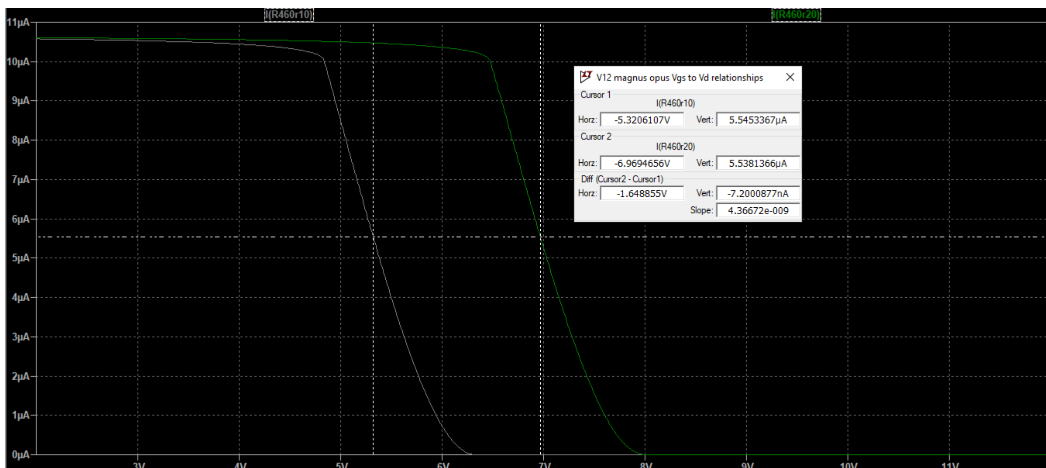


Figure 7.—The 460 °C SPICE simulation results (i.e., 2nd from top plot of Figure 3) enlarged with cursors highlighting the –1.64 V shift in characteristics between r = 10 mm (grey trace) and r = 20 mm (green trace).

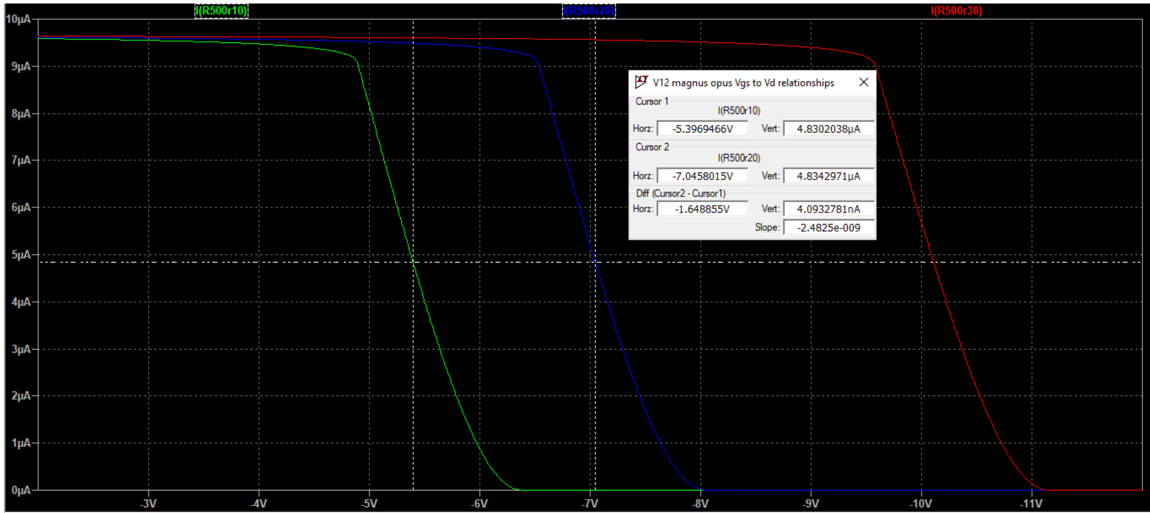


Figure 8.—The 500 °C SPICE simulation results (i.e., top plot of Figure 3) enlarged with cursors highlighting the –1.65 V shift in characteristics between r = 10 mm (green trace) and r = 20 mm (blue trace).

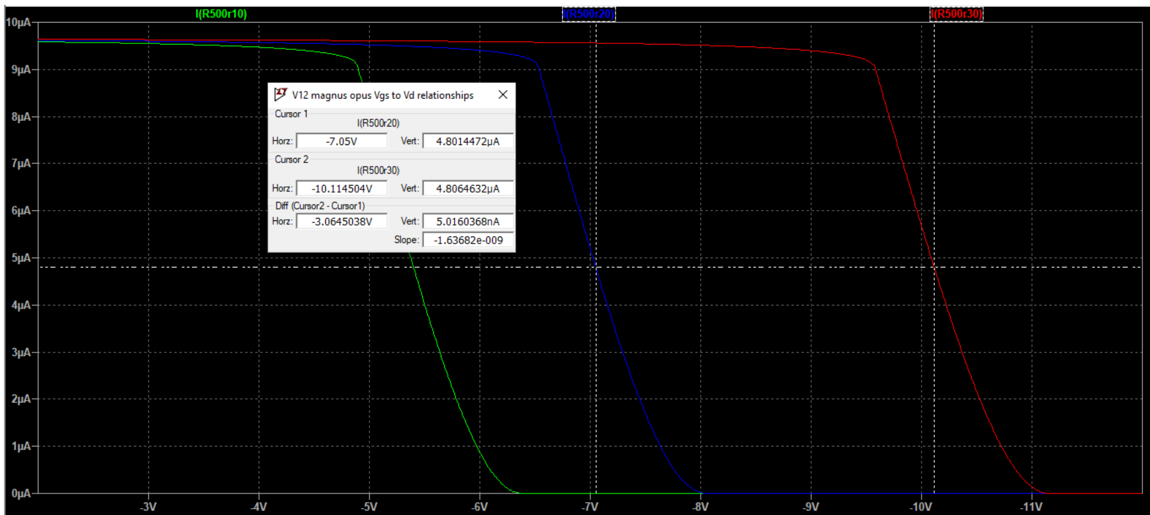


Figure 9.—The 500 °C SPICE simulation results (i.e., top plot of Figure 3) enlarged with cursors highlighting the –3.06 V shift in current versus voltage characteristics between r = 20 mm (blue trace) and r = 30 mm (red trace).

3.0 Current Sources

The previously demonstrated current-voltage characteristic imply that the output currents of current sources undesirably vary as a function each circuit's radial distance r from the SiC wafer center. For circuits to operate similarly regardless of from whence they did arise on the wafer, we must employ some form of self-regulation to make these circuits behave much more homogenously.

Figure 10 shows three **25 °C** circuits corresponding to (left-to-right) r = 10, 20, and 30 mm, wherein a "self-biased" (i.e., SiC JFET gate is shorted to VSS2 = –25 V) current source drives a 200-square SiC resistor drain circuit load connected to ground at the top of each circuit. Similarly, Figure 11 shows three identical-layout self-biased **500 °C** circuits (again, r = 10, 20, and 30 mm left-to-right). *For both Figure 10 and Figure 11, the resulting SPICE-simulated DC voltage and current at the drain node of the M = 2 SiC JFET is annotated*, as well as the "DIFF" difference in drain voltage between adjacent circuit diagrams. The 1 Ω current-sense resistors are negligible.

Note the relationship between the SiC JFET drain voltage changes and the source current changes with radius. In the case of the JFET drain voltage, the magnitude of the change from r = 10 mm to r = 20 mm, is about 1.57 V, fairly close to the 1.64 V change magnitude noted earlier in our Figure 4, Figure 6, and Figure 7 plots. Further, from r = 20 mm to r = 30 mm, the change magnitude is about 2.8 V at 25 °C, and about 2.5 V at 500 °C, also somewhat close to the previously observed 3 V magnitude changes shown in our Figure 5 and Figure 8 plots.

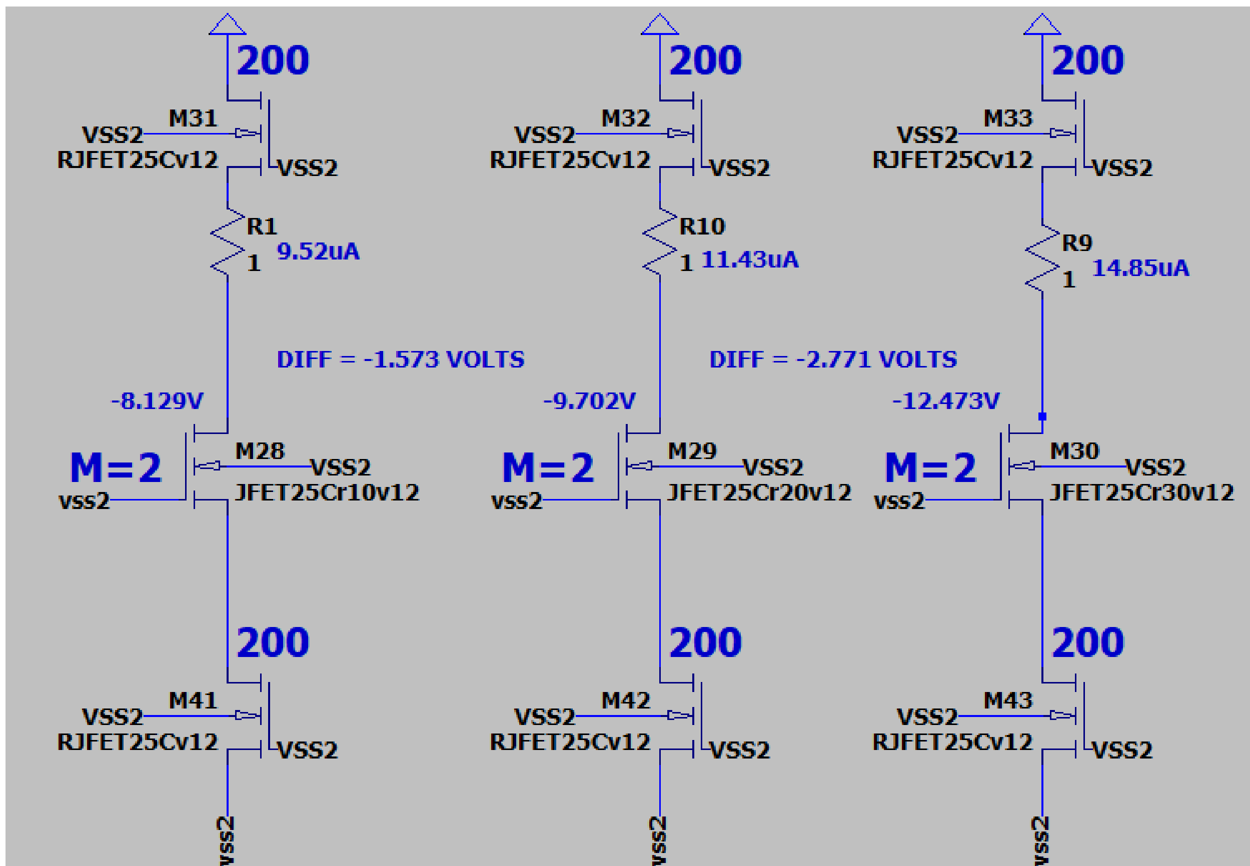


Figure 10.—Schematic diagram of current sources in series with 200 square drain resistors using (left to right) r = 10, 20, 30 mm 25 °C SiC JFET and SiC resistor models. SPICE-simulated voltages and currents of SiC JFET drain nodes are annotated, along with drain node voltage differences between adjacent cases.

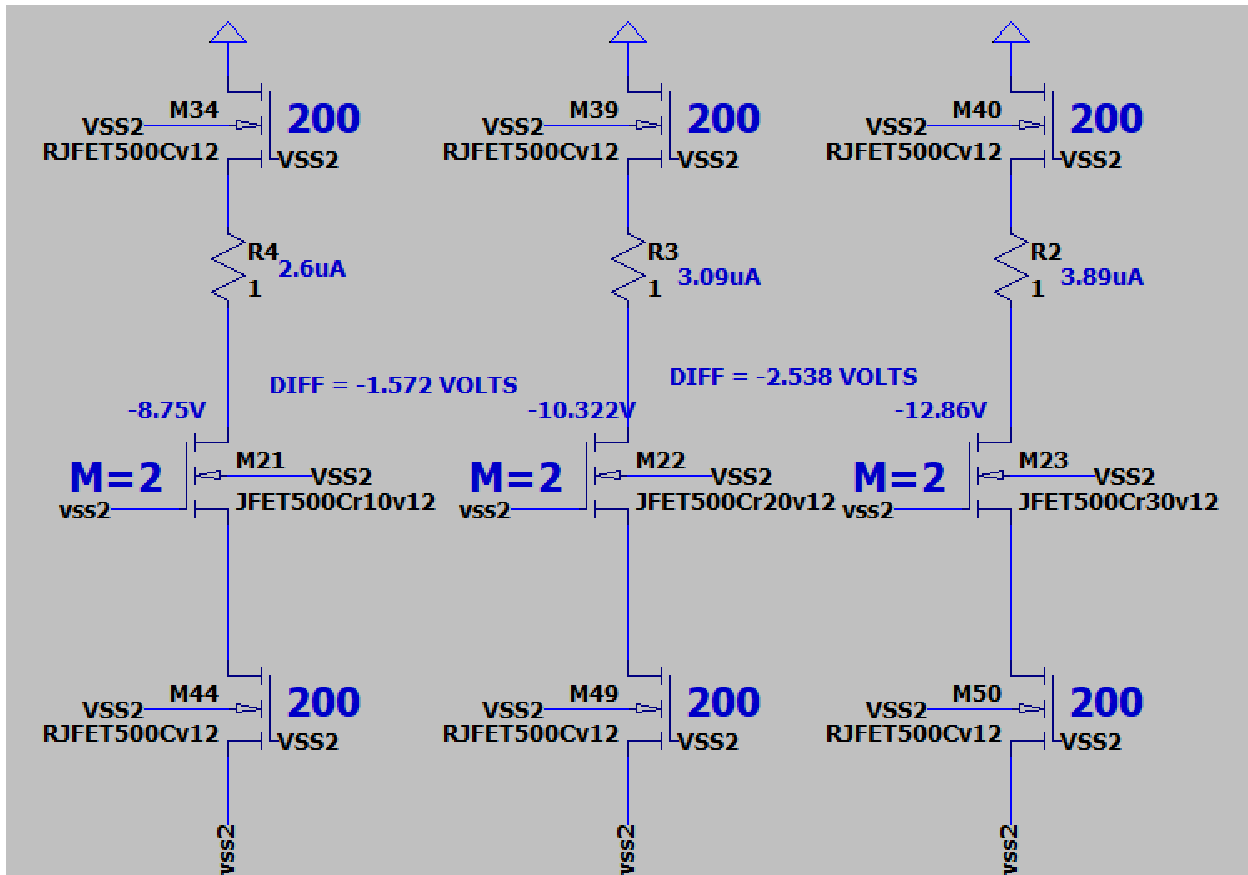


Figure 11.—Schematic diagram of current sources in series with 200 square drain resistors using (left to right) r = 10, 20, 30 mm 500 °C SiC JFET and SiC resistor models. SPICE-simulated voltages and currents of SiC JFET drain nodes are annotated, along with drain node voltage differences between adjacent cases.

Note that the drain currents at different radii do not match well in Figure 10 and Figure 11. For example, in the Figure 11 case of the 500 °C circuits at r = 10 and 20 mm, the change from 2.6 to 3.09 µA is 18.85 percent.

Figure 12 illustrates an attempt to bias SiC JFET drain node of the 500 °C Figure 11 circuit to around 10 V by generating a current source of around 5 µA using constant SPICE-applied JFET gate bias of –8.75 V. While the SPICE simulation of this approach gives the desired 5 µA for r = 20 mm case, it can be seen from the annotations in Figure 12 that the current matching is relatively poor (varying up to 14.5 percent) for the r = 10 mm to r = 30 mm cases.

Figure 13 illustrates nearly the same SPICE-simulated circuit as Figure 12, but instead of applying constant –8.75 V to the JFET gate at all three r values, the gate voltage set point is augmented by adding an additional –1.572 V to the r = 20 mm gate bias (for total V_G = –10.322 V), and an additional –2.538 V (i.e., –2.538 V + –1.572 V = –4.11 V) to the r = 30 bias (for total V_G = –12.860 V). Note that the changed gate biases greatly improve the SiC JFET drain current and voltage matching (JFET drain currents matched within 0.34 percent between r = 10 mm to r = 20 mm, 2.74 percent between r = 20 mm to r = 30 mm).

Figure 14 illustrates the same circuit with SPICE simulation results of the Figure 13 circuit, *except notice that the independent SPICE voltage sources that biased the SiC JFET gates in Figure 13* ***have each been replaced by the radius specific SiC JFET-R "self-biased" sources from Figure 11***. The SiC JFET-R "self-biased" sources act as radius dependent voltage sources to bias the current sources of Figure 13, resulting in a radius independent current source circuit.

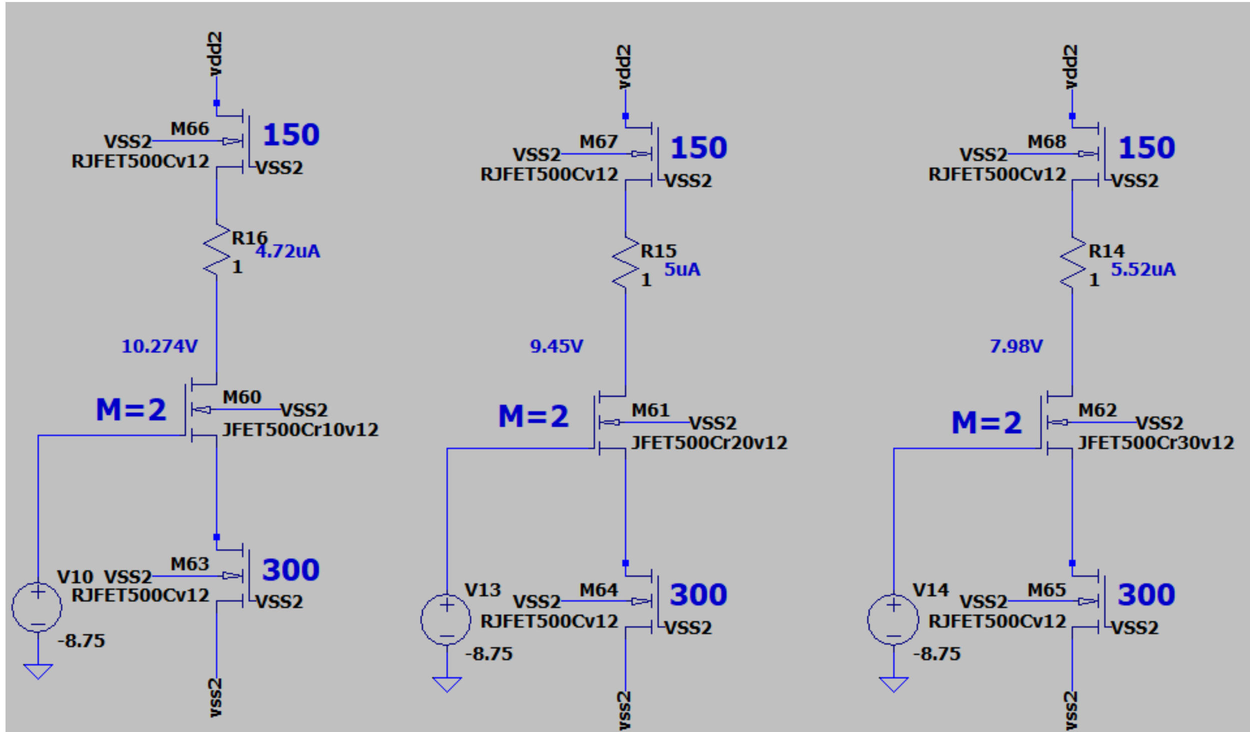


Figure 12.—Schematic diagram of current sources with load resistors using (left to right) *r* = 10, 20, 30 mm 500 °C SiC JFET and resistor models wherein constant –8.75 V bias is applied to each SiC JFET gate terminal. SPICE-simulated voltages and currents of SiC JFET drain nodes are annotated, showing that this constant-gate-voltage approach does not achieve good matching for the different benchmark radial locations. VDD2 = 25 V, VSS2 = –25 V.

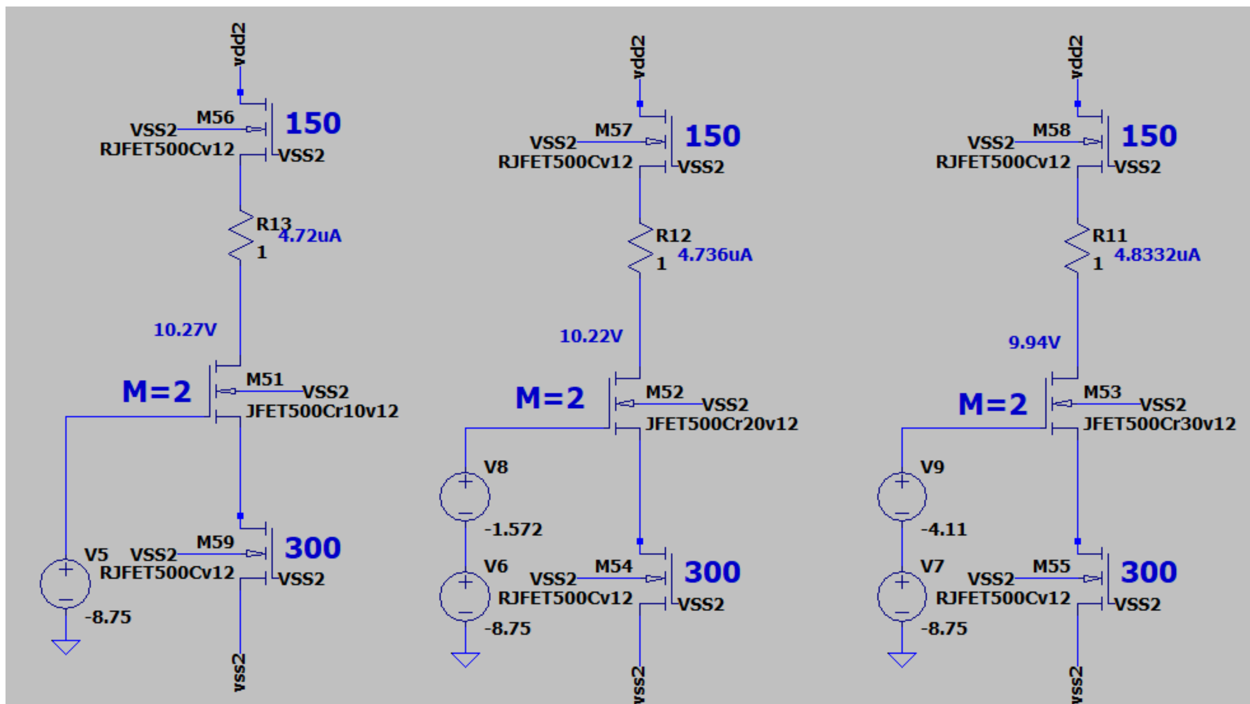


Figure 13.—Schematic diagram of current sources with load resistors using (left to right) *r* = 10, 20, 30 mm 500 °C SiC JFET and resistor models wherein adjusted biases are applied at each SiC JFET gate terminal. SPICE-simulated voltages and currents of SiC JFET drain nodes are annotated, showing that good matching for the different benchmark radial locations can be achieved using the adjusted gate biasing.

Figure 15 SPICE simulation of the *identical circuit layout as Figure 14* using 25 °C SPICE models illustrate that this drain voltage bias positioning is fairly accurate over temperature. Note that the bias voltage at the drain of SiC JFETs ("M87" for r = 10 mm), ("M90" for r = 20 mm), and ("M93" for r = 30 mm) are still within the ballpark, varying from 10.67 to 10.475 V across radius.

Figure 16 and Figure 17 show similar SPICE-simulation results for the 300 °C and the 460 °C r = 10 mm (left) and r = 20 mm (right) cases of *the identical circuit layout as Figure 14*.

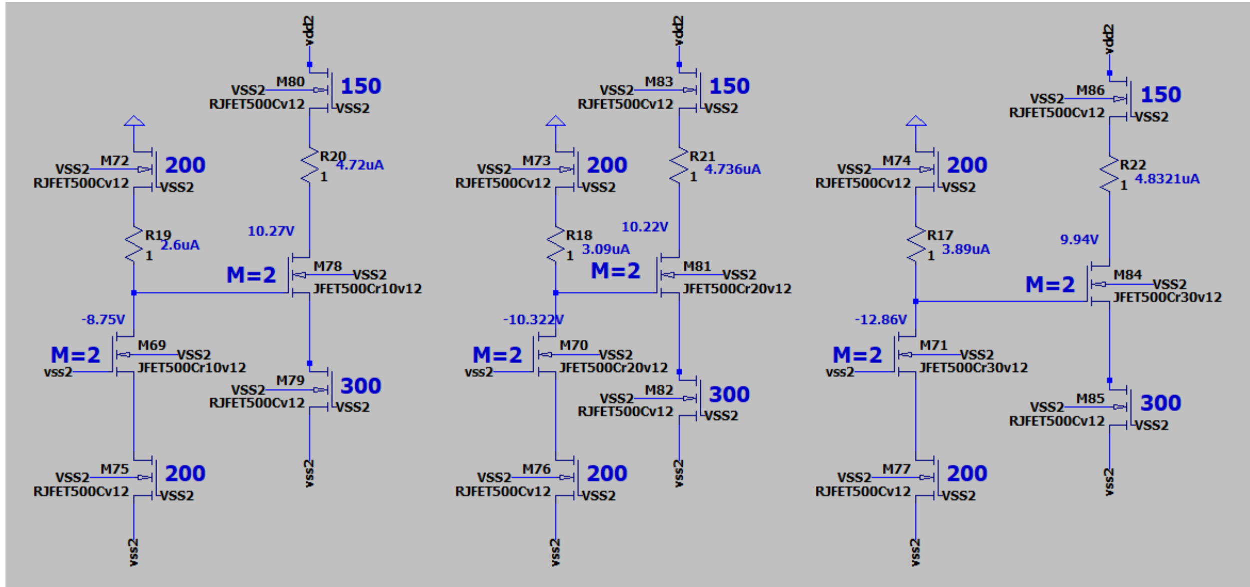


Figure 14.—Same 500 °C circuit schematic as Figure 13, except that the independent SPICE voltage sources that biased the SiC JFET gates of the current sources have each been replaced by the SiC JFET-R "self-biased" sources from Figure 11. SPICE-simulated voltage and current annotations show good matching is obtained between the r = 10, 20, and 30 mm cases.

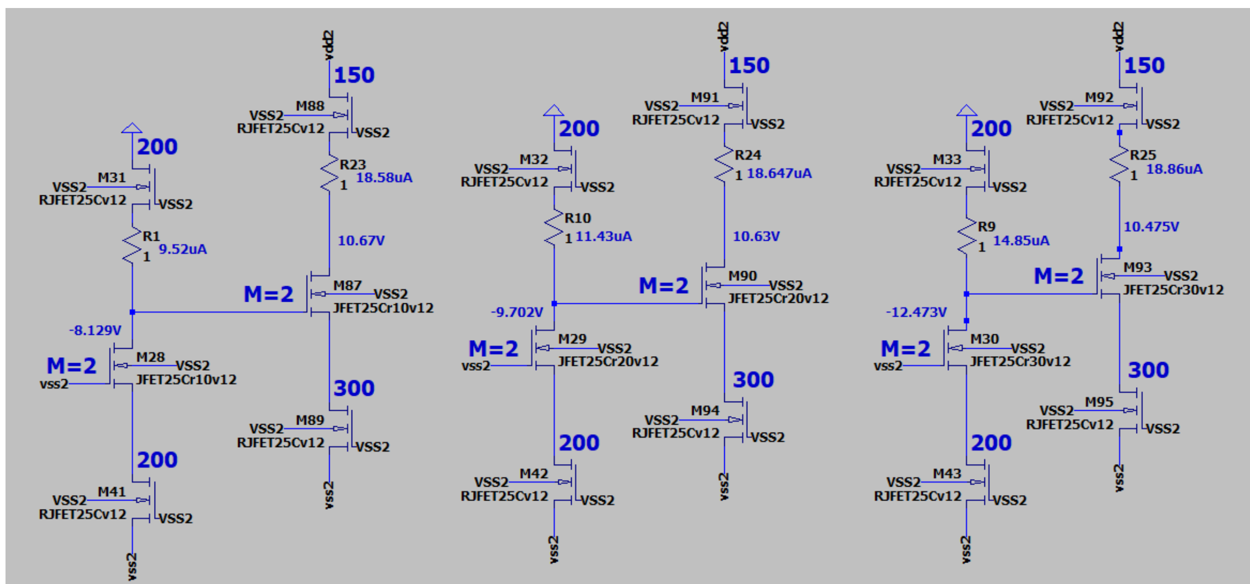


Figure 15.—Same circuit schematic as Figure 14, except that 25 °C SiC device models have replaced the 500 °C device models. SPICE-simulated voltage and current annotations show good matching is obtained between the r = 10, 20, and 30 mm cases. Furthermore, the 25 °C annotated drain voltages all fall within a volt of the 500 °C annotated drain voltages shown in Figure 14.

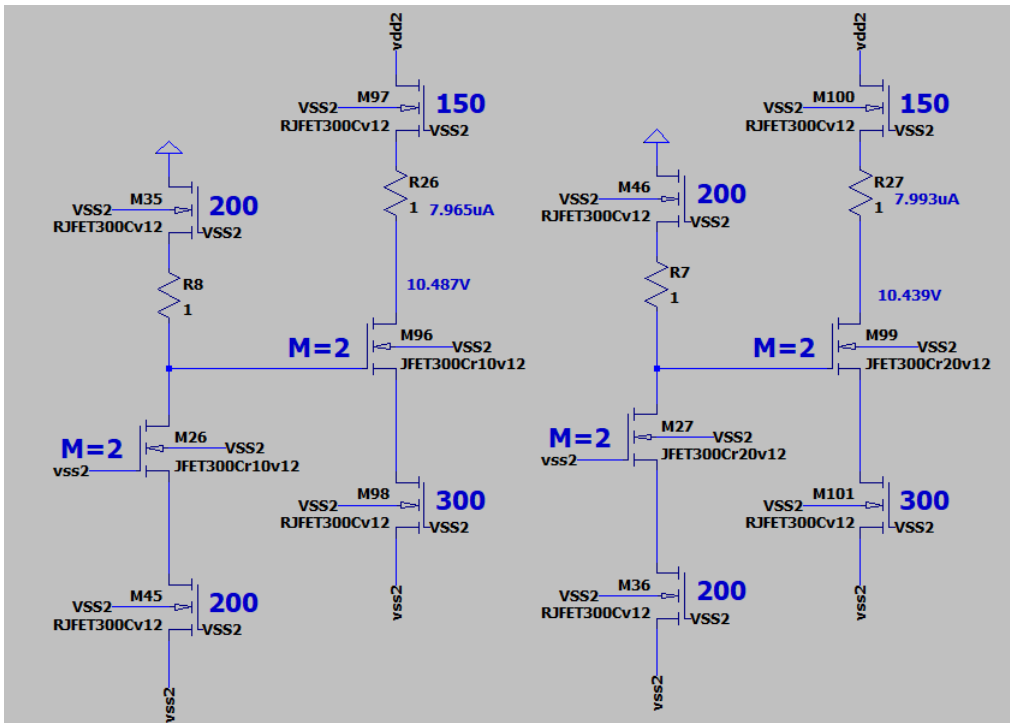


Figure 16.—Same circuit schematic as Figure 14, except that 300 °C SiC device models have replaced the 500 °C device models. SPICE-simulated voltage and current annotations show good voltage matching of the drain of the current-source SiC JFET is obtained between the two *r* values as well as compared to the Figure 14 (500 °C) and Figure 15 (25 °C).

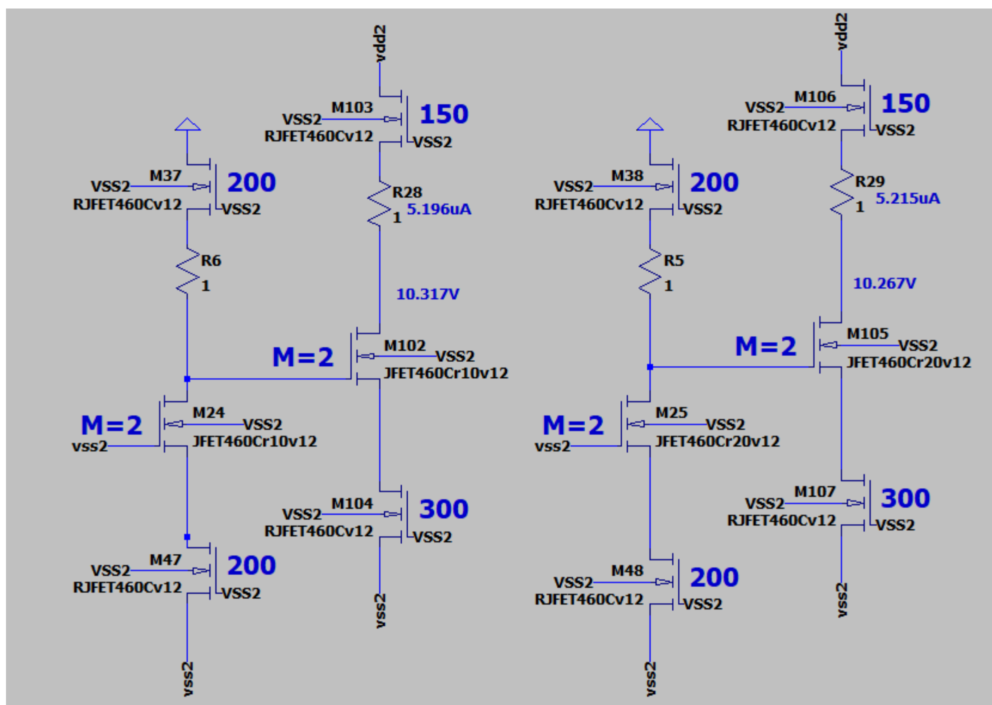


Figure 17.—Same circuit schematic as Figure 14, except that 460 °C SiC device models have replaced the 500 °C device models. SPICE-simulated voltage and current annotations show good voltage matching of the drain of the current-source SiC JFET is obtained between the two *r* values as well as compared to the 500, 25, and 300 °C results presented in Figure 14 to Figure 16.

4.0 Fine Tuning—The Impact of Body Bias Effect in The Circuit

The astute reader will have noted throughout the previous discussion that 1.648 V (change VT from r10 to r20 @ 25,460, 500C) ≠ 1.572V (Change in Output Voltage from self-biased current source from r10 to r20). When viewing the "self-biasing" current source as a common source amplifier, this change in VT at the input to the Output Voltage represents a gain of just about 0.95. In particular, the common source amplifier used to derive the gate bias voltage (left leg of each circuit) for the current source (right leg) circuit should nominally have a voltage gain of unity, given the source and drain resistors are identical in layout at 200 squares. *In reality however, the body bias effect (which is accounted for in these IC Version 12 SiC resistor SPICE models) causes the drain/upper 200-square SiC resistor to possess higher effective resistance than the source/lower 200-square SiC resistor*. As detailed in the IC Version 12 Resistor SPICE Modeling Primer and Reference 13, the current versus voltage characteristics of the SiC resistors are neither perfectly linear nor completely independent of the voltage difference between the substrate and the resistor n-channel.

An example of this circuit-relevant phenomenon is presented in the Figure 18 schematic that includes annotations of SPICE-simulated circuit results for 500 °C and r = 10 mm (left) and 20 mm (right). For both radii illustrated, the drain/upper resistor has (based upon Ohm's law) an effective resistance of 3.35 MΩ, while the identical-layout (i.e., identically 200 squares) source resistor exhibits an effective value of about 2.95 MΩ. This difference arises from the fact that the voltage difference between the drain/upper resistor's n-channel and VSS-biased substrate is larger than the voltage difference between the source resistor's n-channel and VSS-biased substrate, which renders a larger body bias effect to the otherwise physically identical drain resistor. Thus, the SiC resistor body bias effect causes the common source amplifier voltage gain to be less than unity, about 0.873 at r = 10 mm and 0.885 at r = 20 mm.

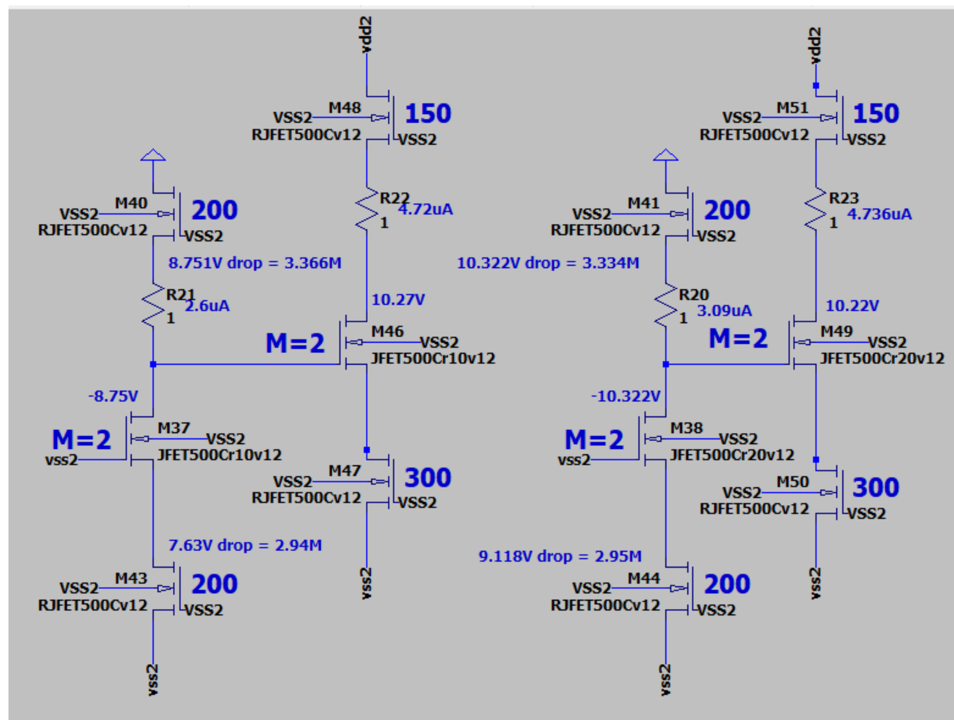


Figure 18.—Schematic diagrams with annotated 500 °C SPICE results for r = 10 mm (left) and r = 20 mm (right) showing differences in resistor voltage drop across physically identical 200-square drain resistors in the common-source biasing circuit that arise due to the body bias effect in SiC resistors.

Figure 19 illustrates the results of trimming the source resistor to 0.95 of its original value, down to at 190 squares. The difference between the r = 10 and 20 mm current source JFET gate bias voltages is now at (–9.172V) – (–10.8167) = 1.6447 V, right at the desired 1.64 V difference in VT seen in Figure 4. The quiescent operating points at the 150-square drain resistor load point now differs by 0.15 percent, compared to 0.49 percent for the circuit of Figure 14. So, with the removal of squares to compensate/offset resistance differences arising from body bias effects, the matching performance improved more than 3-fold. Note that the same results could also have been accomplished by increasing the size of the drain resistor.

Figure 20 additionally includes the r = 30 mm configuration. The change in bias voltage from the r = 20 mm to the r = 30 mm is about 2.4 V, a bit short of the 3 V which was what was wanted according to Figure 5. In fact, the performance compared to the Figure 14 case is actually worse, going from 2.74 percent match to 3.12 percent. Operation at r = 30 mm for analog circuits is contraindicated in that though still functional, the signal swing will be less than that of the matched swings at r = 10 and 20 mm. If an application is unaffected by this special case, or if higher power supply voltages are acceptable, then an op amp constructed from r = 30 mm SiC can be accomplished.

SPICE-simulation results annotated onto the schematics of Figure 21 (25 °C), Figure 22 (300 °C), and Figure 23 (460 °C), confined to r = 10 mm (left) and r = 20 mm (right), show similar improvements in matching at these temperatures.

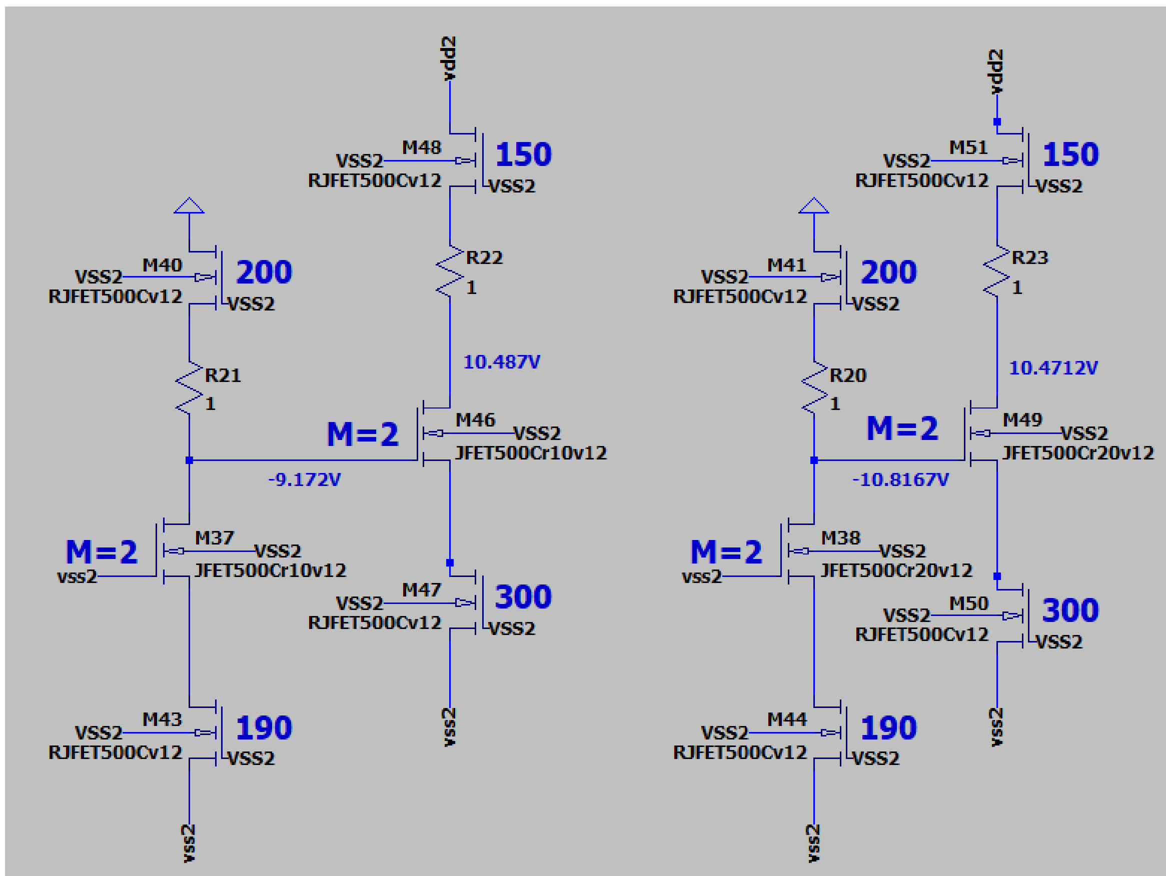


Figure 19.—Schematic diagrams with annotated 500 °C SPICE results for r = 10 mm (left) and r = 20 mm (right) showing how body bias effects can be offset by decreasing the source resistor layouts to 190 squares compared to 200 squares for the drain resistor layout. This offsetting of SiC resistor body bias effect enables better matching.

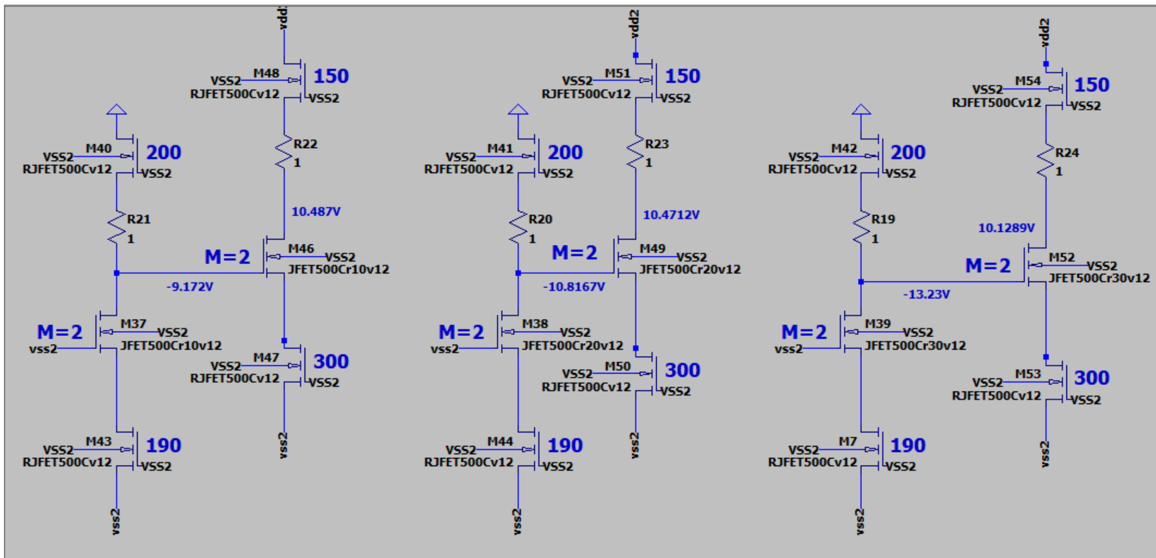


Figure 20.—Schematic diagrams with annotated 500 °C SPICE results with r = 30 mm added to the right for completeness. Matching is not as good for r = 30 mm, but could be improved if supply voltages VDD2 and VSS2 were increased in magnitude beyond 25 V.

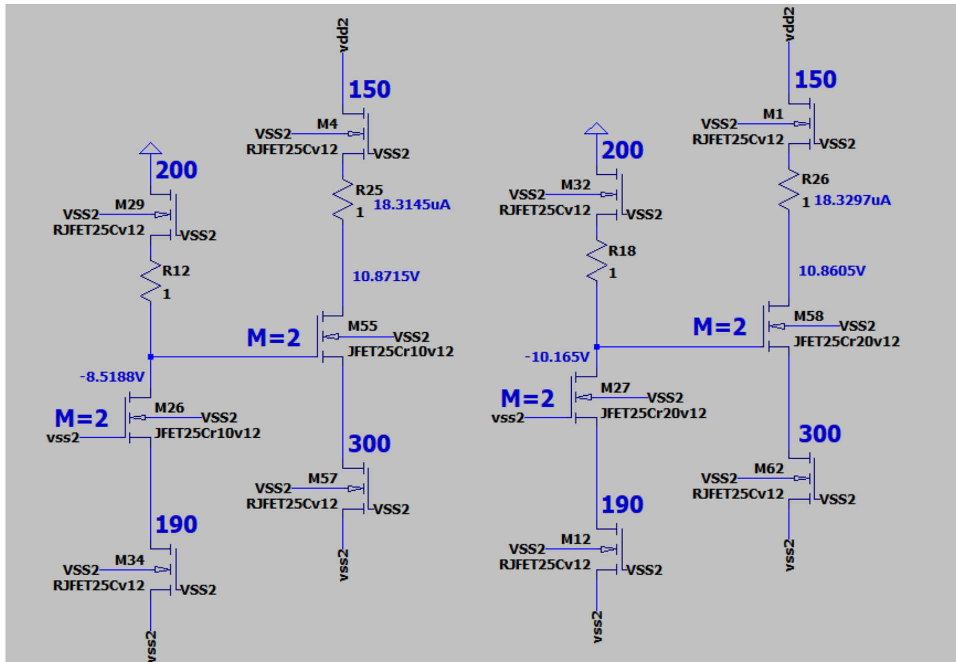


Figure 21.—Same r = 10 mm (left) and 20 mm (right) circuits as Figure 19 featuring 190 square source resistors simulated using 25 °C SPICE models.

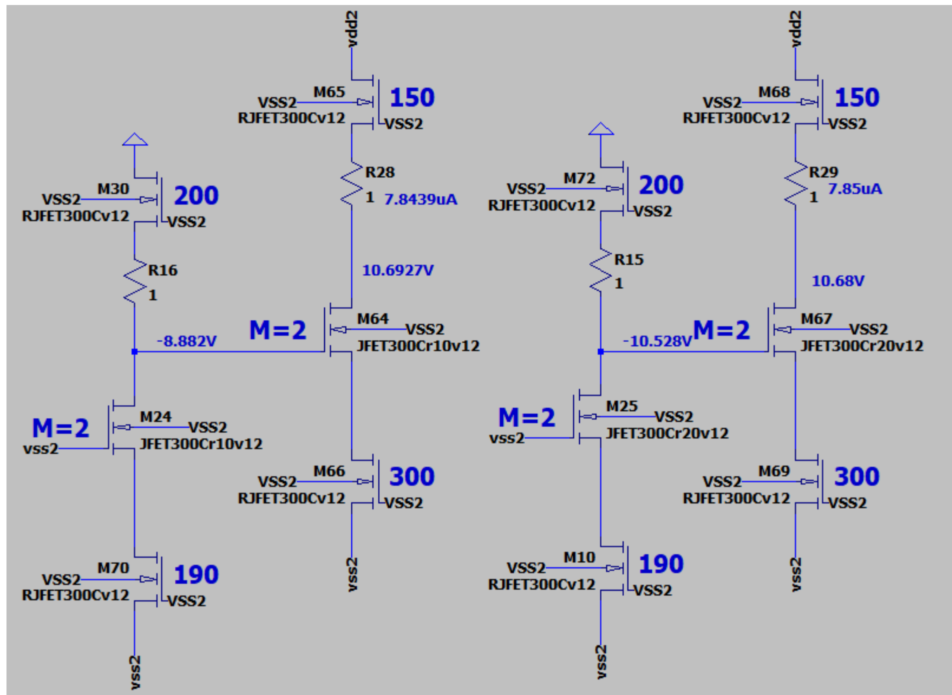


Figure 22.—Same r = 10 mm (left) and 20 mm (right) circuits as Figure 19 featuring 190 square source resistors simulated using 300 °C SiC JFET and resistor SPICE models.

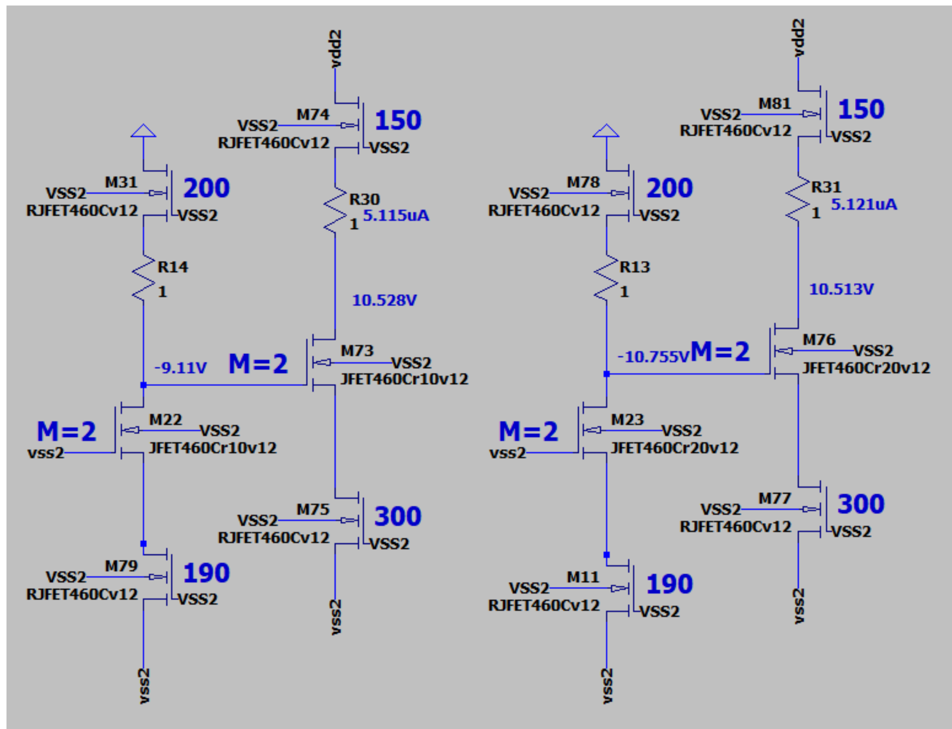


Figure 23.—Same r = 10 mm (left) and 20 mm (right) circuits as Figure 19 featuring 190 square source resistors simulated using 460 °C SiC JFET and resistor SPICE models.

A short note on an approximation of g_m

In the course of our studies, we have arrived at the following empirical approximation for the g_m of the NASA Glenn SiC IC Version 12 L_G = 3 µm SiC JFET as a function of temperature T, parallel-unit-cell M number, and radius r as follows:

$$g_m \approx \frac{\left(6.952mmho \cdot 1.45^{\log_2 M}\right)}{e^{0.0029 \cdot T}} \cdot (1.015 - 0.0025 \cdot r - 0.0125 \cdot r^2)$$

Where:

1. g_m is the JFET transconductance in millimhos
2. M is the transistor M number (= total gate finger width / 6 µm unit-cell JFET width)
3. 6.952 is the g_m of an M = 1 JFET, at radius r = 10 mm = 1 cm at 25 °C.
4. T is the temperature in °C.
5. r is the radius in **cm**.

As we see above, and as the M number of a FET structure increases, g_m increases logarithmically. However, there then is a point where returns diminish. The designer may make engineering decisions based on performance versus on-chip circuit layout space.

5.0 Amplifiers

In a common-source configuration, the voltage gain of a JFET amplifier is basically $-g_m$ R_d product, where g_m is the transconductance of the JFET, and R_d is the value of the drain resistor. In our IC Version 12 JFET-R circuit design, we have confined ourselves to maximum resistor topographies of 300 squares (to ensure bias currents through the resistors remain much larger at 500 °C than parasitic junction leakage currents), and a maximum transistor size of M = 96 (to ensure low 500 °C leakage junction leakage currents and negligible V_T changes across any single device).

The first amplifier circuit example is a single-output differential amplifier utilizing as their current sources the bias scheme of Figure 19. The transistor on the non-inverting branch has its gate tied to ground, with the transistor on the inverting leg receiving signal at its gate. Figure 24 shows the schematics with SPICE-simulated biasing outcomes annotated for r = 10 mm (left) and r = 20 mm (right) wherein the standard supply voltages of VDD2 = +25 V and VSS2 = –25 V are employed. The input signal to each amp is a 1 mV pk-pk sine wave imparted at “vsine” label of the “M28” (left) or “M45” (right) respective JFET gate terminals. The SPICE-simulated input and outputs of the two circuits are given with amplitude measurement plot cursors in Figure 25(a) (r = 10 mm) and Figure 25(b) (r = 20 mm). As seen by the plots in Figure 25, the gain of the r = 10 mm circuit is –137.7 V/V biased at 12.275 V, and the gain of the r = 20 mm circuit is –132.25 V/V biased at 12.29 V.

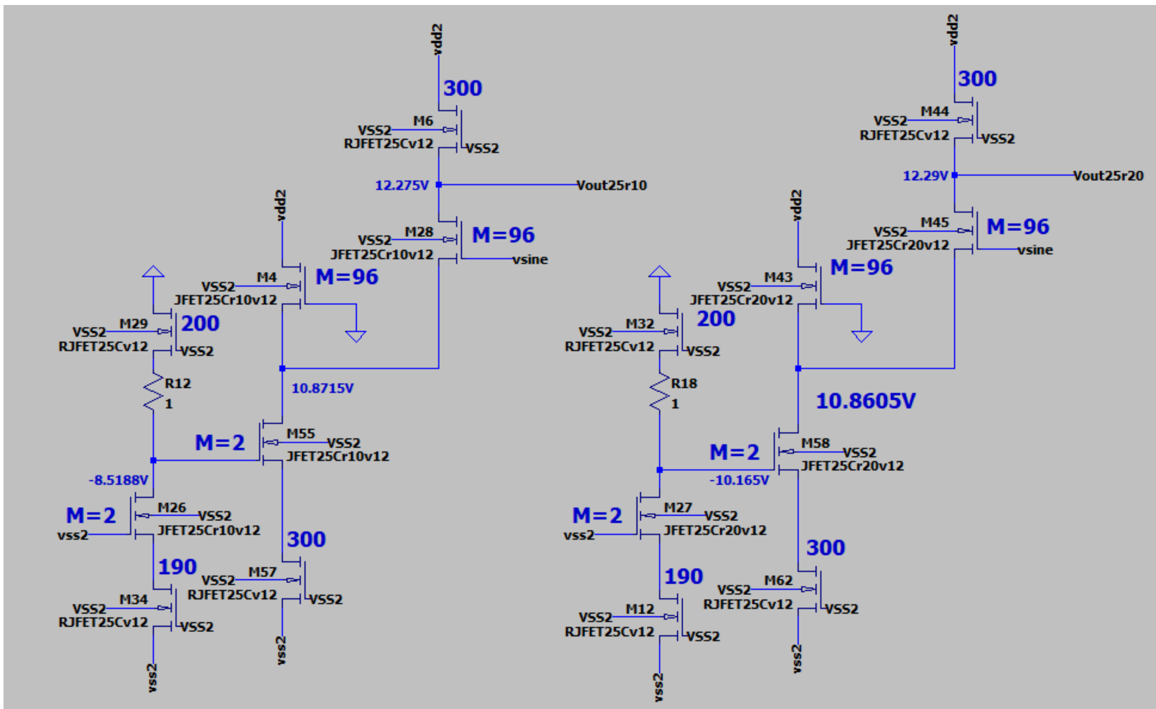
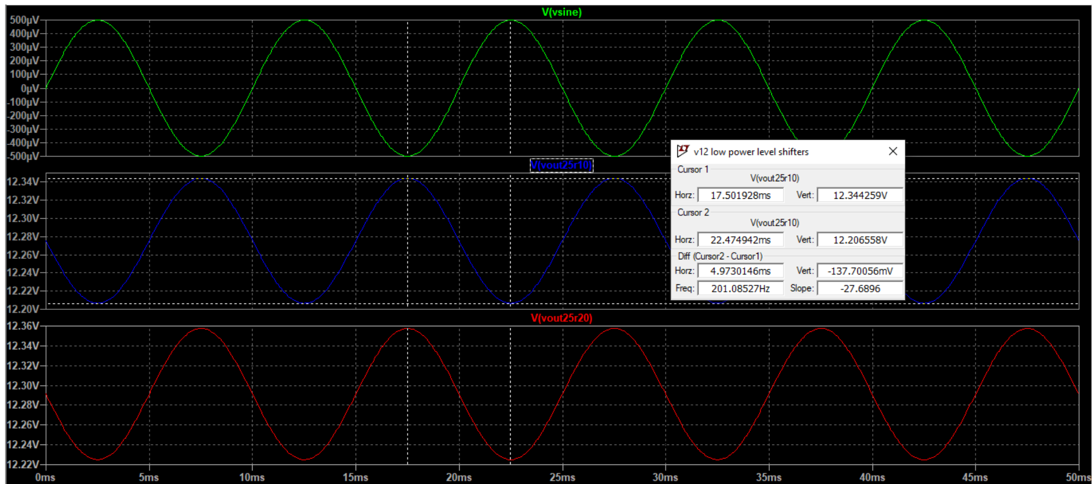
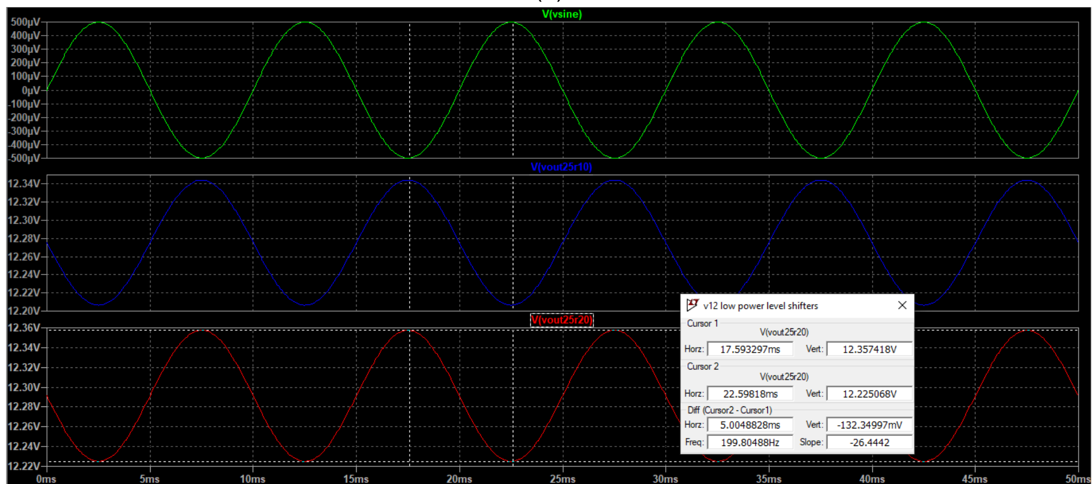


Figure 24.—Schematic diagrams with SPICE-simulated bias annotations of single-output differential amplifiers utilizing as their current sources the biasing scheme of Figure 19 at 25 °C using *r* = 10 mm (left) and 20 mm (right) SiC models.



(a)



(b)

Figure 25.—SPICE simulation waveforms demonstrating 25 °C operation and of the single-output differential amplifier circuits of Figure 24. Green trace is 1 mV peak-to-peak “vsine” input wave, blue trace wave is the *r* = 10 mm output wave, and red trace is the *r* = 20 mm output wave. The same waves but difference cursors are shown in (a) and (b).

Figure 26 is a schematic of what was wanted: *A complete SiC JFET-R op amp. Adding a parallel transistor in parallel with the input gives a differential amplifier.* The amplification section is leftmost and as above. To the right is a source follower level shifter with values picked to move the output signal of this amplifier to near ground, with minimal loss of amplitude.

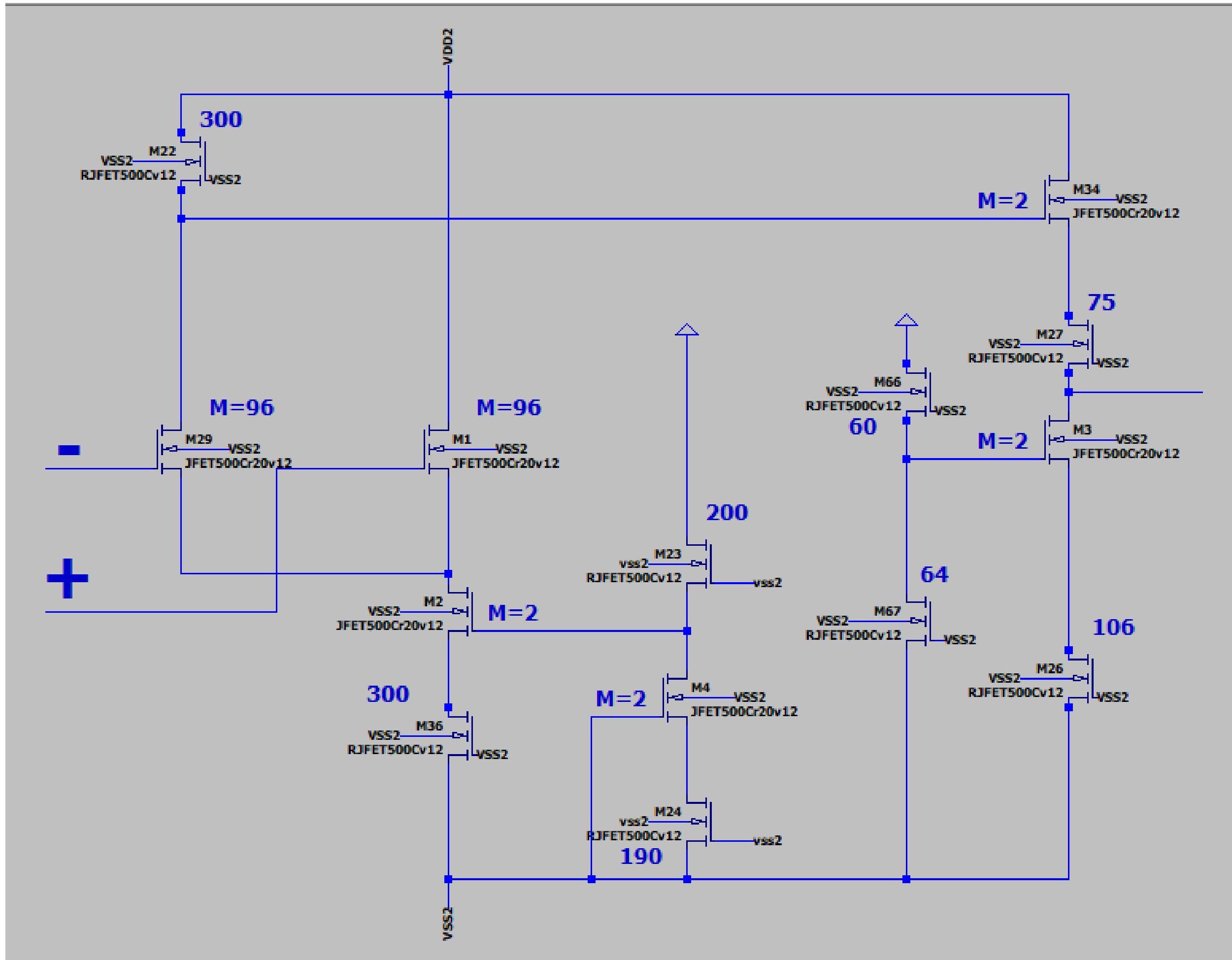


Figure 26.—Schematic diagram of NASA Glenn SiC IC Version 12 SiC JFET-R operational amplifier design depicted using T = 500 °C and *r* = 20 mm SiC device models.

The following sections are illustrative examples of the SiC IC Version 12 op amp functional characteristics SPICE-simulated under combinations of *r* and T and in various typical amplifier circuit configurations.

5.1 Op Amp Open Loop Voltage Gain (A_{vol})

Figure 27 presents a pair of schematic diagrams used for SPICE simulations of the Figure 26 SiC JFET-R op amp circuit layout at T = 500 °C, wherein the left schematic represents the *r* = 10 mm radial location while the right schematic represents the *r* = 20 mm case. The inverting input (denoted by the "–" sign) to each amplifier is tied to ground and the non-inverting input (denoted by the "+" sign) is driven by a sine wave.

Three different SPICE-simulated sinewave amplitudes (≈200 $\mu V_{(pk\text{-}pk)}$, ≈1 $mV_{(pk\text{-}pk)}$, and ≈20 $mV_{(pk\text{-}pk)}$) produced the respective results illustrated in Figure 28 to Figure 30. As seen from the plotted waves of Figure 28 to Figure 30, the SPICE-simulated open loop voltage gain A_{vol} did not change between the three simulated input signal amplitudes, remaining near 99.56 for all the *r* = 10 mm "*r*10" simulations and near 93.8 for all the *r* = 20 "*r*20" simulations.

5.2 Closed Loop, Unity Gain Configuration

The closed loop unity gain amplifier circuit is a well-known construct produced by tying the op amp output to the inverting "-" input and providing the input signal to the non-inverting "+" input which is illustrated in Figure 31 showing the left (*r* = 10 mm) and right (*r* = 20 mm) schematics. For these simulations, the non-inverting "+" input is driven by ≈2$V_{(pk\text{-}pk)}$ sinewave input, and the power supplies remain at VDD2 = +25 V and VSS2 = –25 V. As seen in the Figure 32 plotted SPICE simulation results, performance is adequate as shown for both radii where the theoretical gain of 1 (unity) is matched at 0.99.

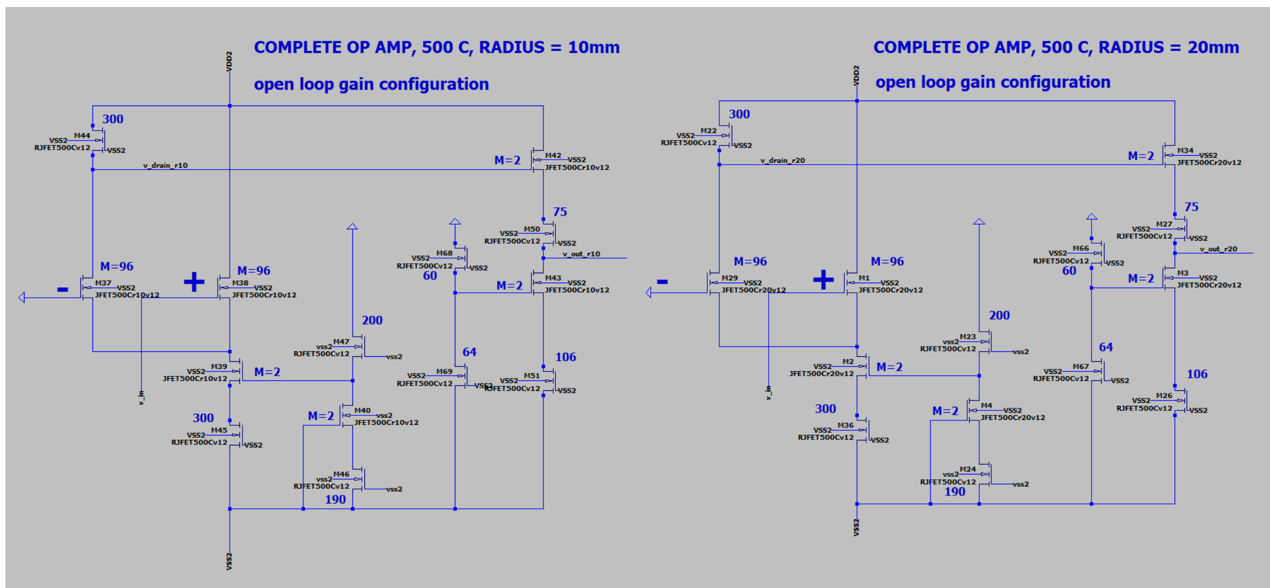


Figure 27.—Schematic diagrams of the Figure 26 op-amp configured open-loop for 500 °C simulation using *r* = 10 mm (left) and *r* = 20 mm (right) SiC JFET device models.

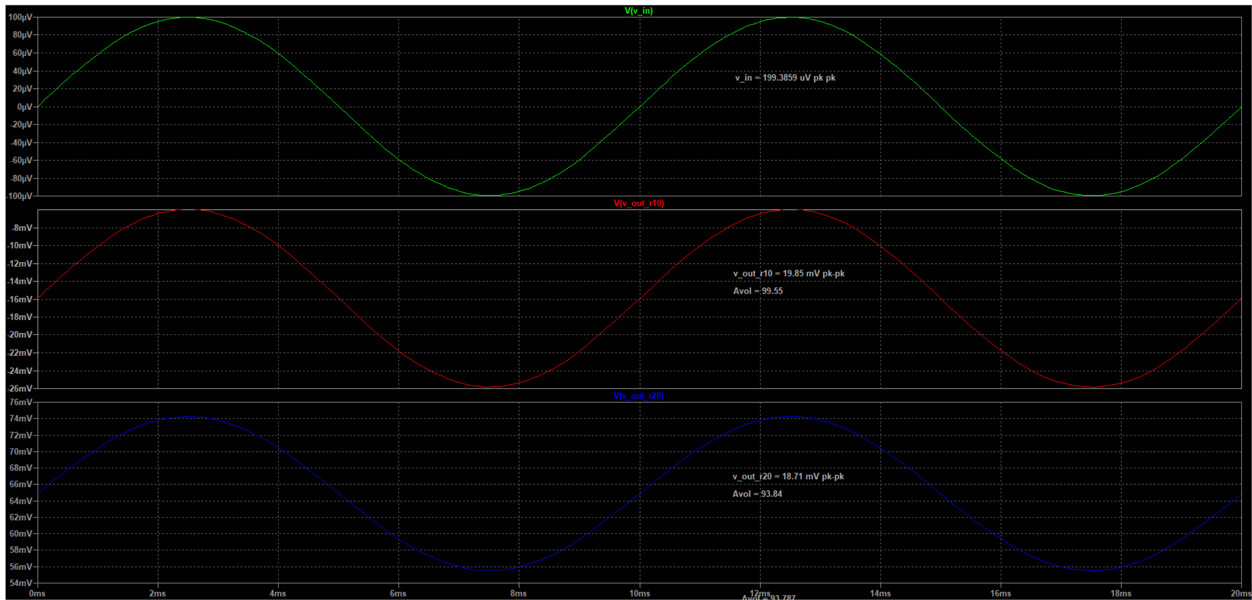


Figure 28.—SPICE simulation waveforms demonstrating open-loop performance of 500 °C Figure 27 op-amp circuits. Green trace is 200 µV Pk-Pk sinewave input, red trace is r = 10 mm simulation output with voltage gain of 99.55, and blue trace is r = 20 mm simulation output with voltage gain of 93.84.

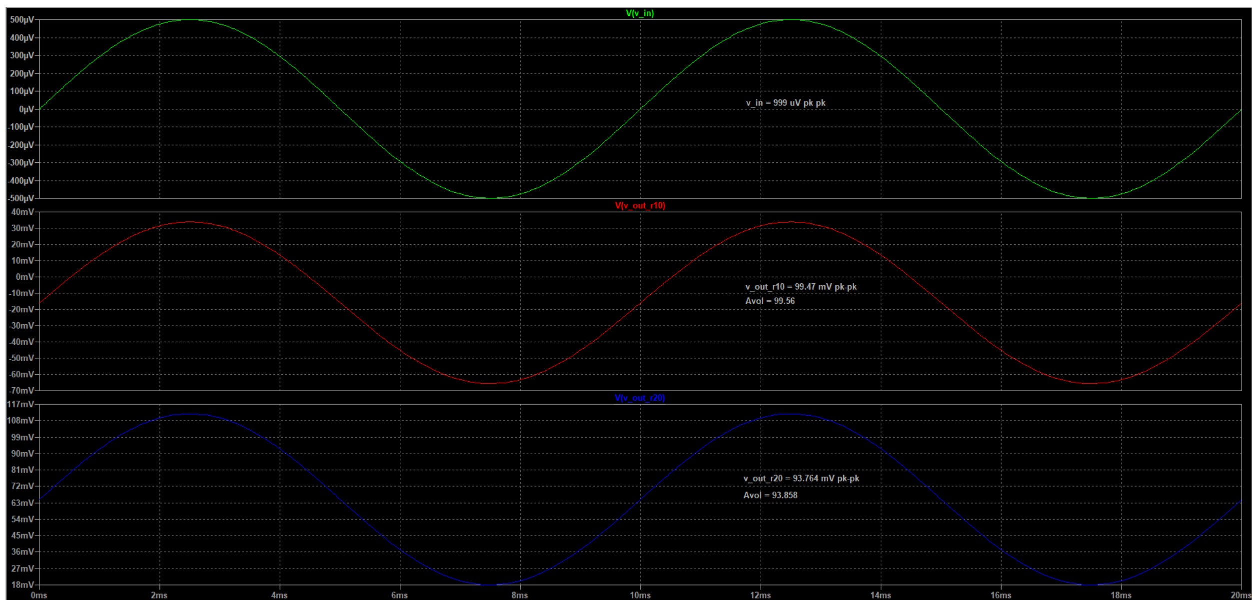


Figure 29.—SPICE simulation waveforms demonstrating open-loop performance of 500 °C Figure 27 op-amp circuits. Green trace is 1 mV Pk-Pk sinewave input, red trace is r = 10 mm simulation output with voltage gain of 99.56, and blue trace is r = 20 mm simulation output with voltage gain of 93.86.

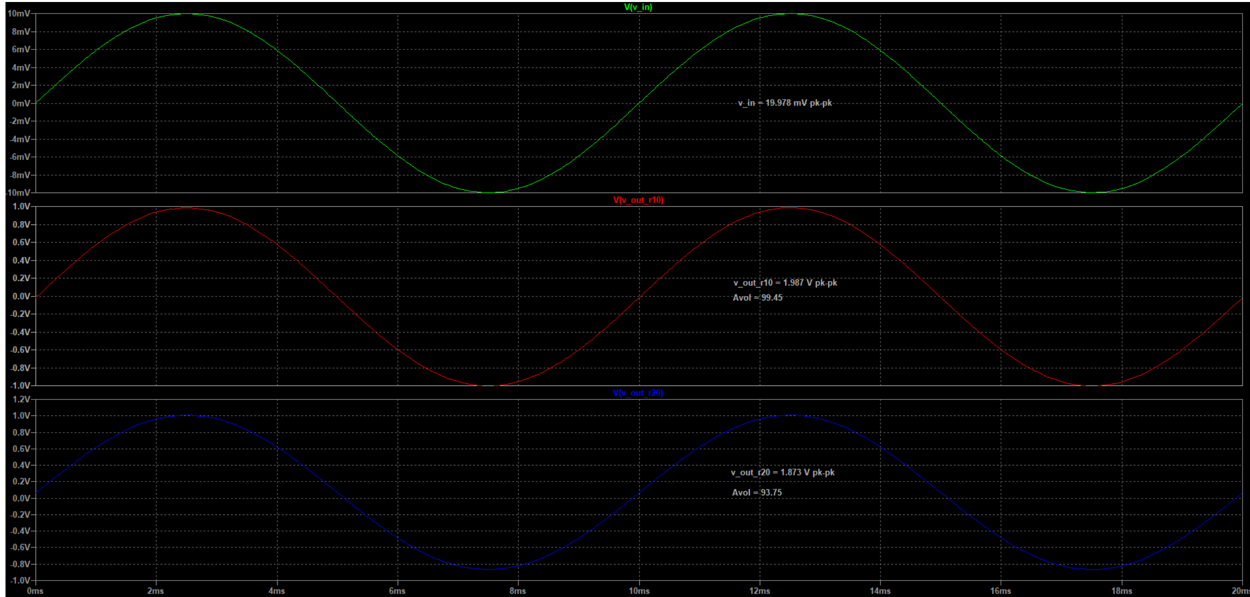


Figure 30.—SPICE simulation waveforms demonstrating open-loop performance of 500 °C Figure 27 op-amp circuits. Green trace is 20 mV Pk-Pk sinewave input, red trace is r = 10 mm simulation output with voltage gain of 99.45, and blue trace is r = 20 mm simulation output with voltage gain of 93.75.

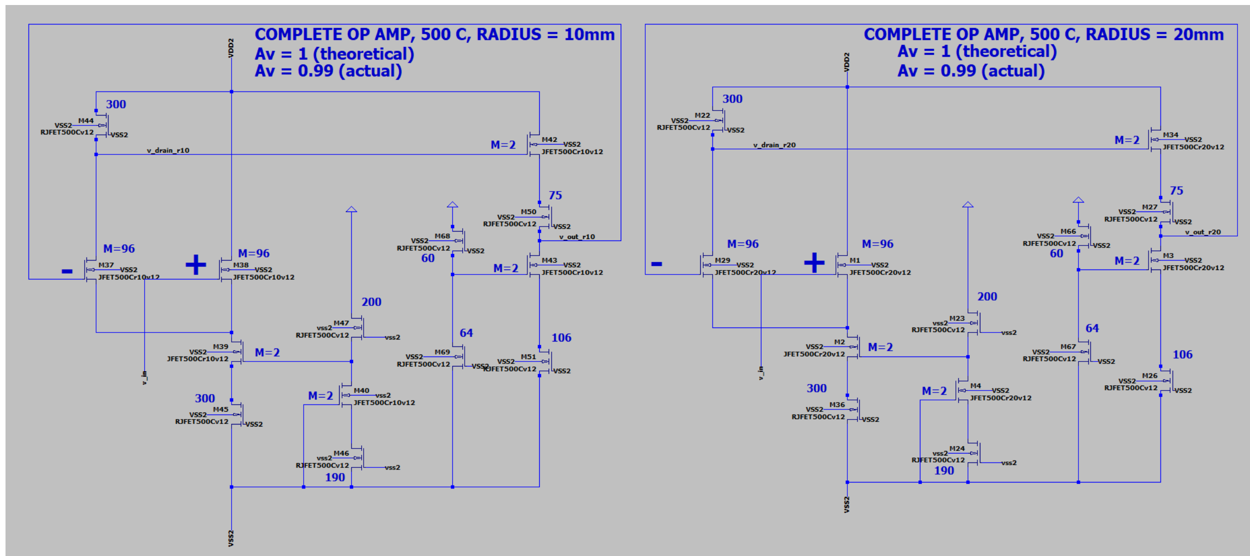


Figure 31.—Schematic diagrams of the Figure 26 op-amp configured for unity-gain closed 500 °C simulation using r = 10 mm (left) and r = 20 mm (right) SiC JFET device models.

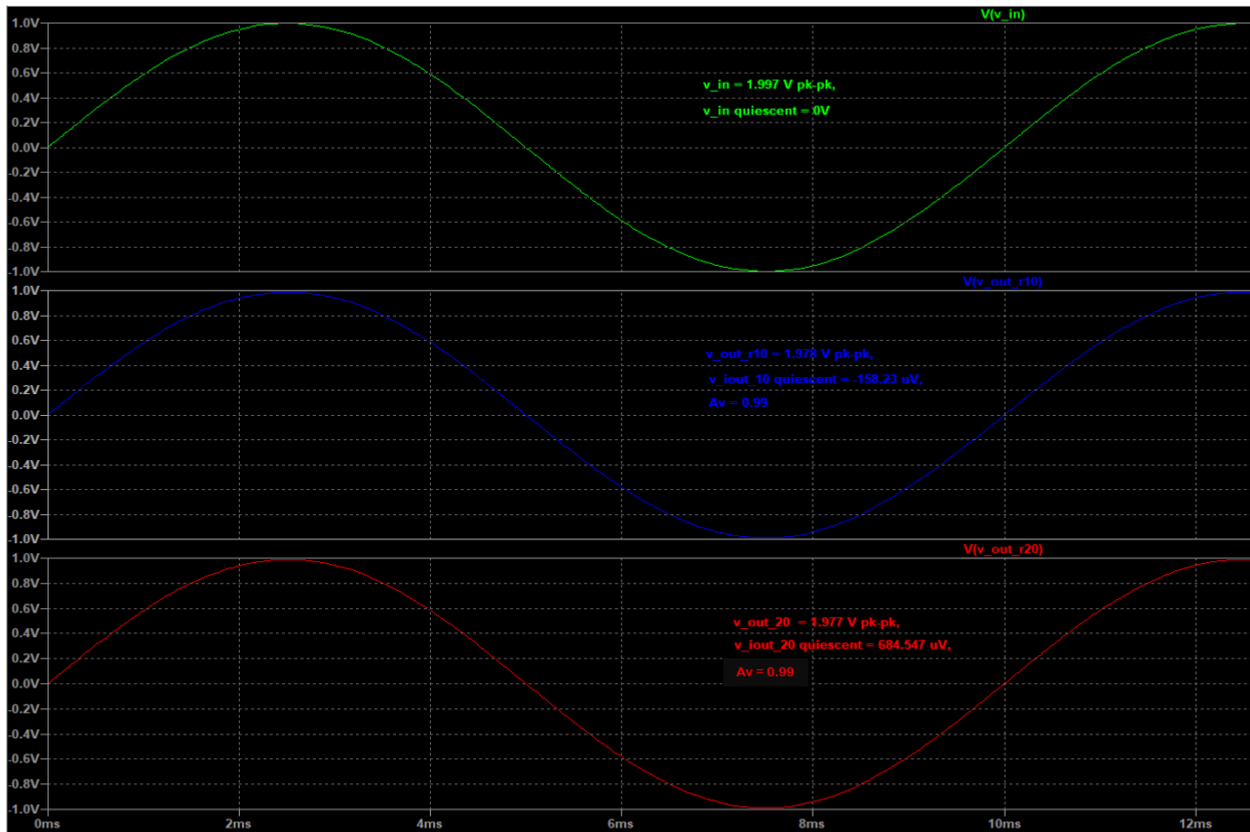


Figure 32.—SPICE simulation waveforms demonstrating closed-loop unity-gain performance of 500 °C Figure 31 op-amp circuits. Green trace is 2 V Pk-Pk sinewave input, red trace is r = 10 mm simulation output with voltage gain of 0.99, and blue trace is r = 20 mm simulation output with voltage gain of 0.99.

5.3 Closed Loop, Inverting Amplifier Configuration

The well-known closed-loop inverting amplifier circuit schematic is shown in Figure 33, which uses the classic op amp schematic symbol to condense the underlying SiC JFET-R op-amp circuit of Figure 26.

In an ideal op amp, one with huge open loop voltage gain α (= A_{vol}), an approximation for the voltage gain A_v of the above closed-loop circuit would be R2/R1. Common 25 °C α values for commercial silicon op amps are on the order of 100,000 to 1,000,000, and even orders of magnitude more than that for high-precision devices (Ref. 14).

With open-loop voltage gains in the 90's, our SiC JFET-R op amp is comparatively inferior in terms of α and as such we must account for it. This inferior open loop gain performance arises primarily from the limitation of M in transistor size due to layout constraints capping M at 96 that conservatively ensures 500 °C circuit functionality.

Figure 34 shows the Figure 33 circuit but with the internal SiC JFET-R circuitry of the op-amp explicitly illustrated (using *r* = 10 mm and T = 500 °C case SiC device models) and R1 = 30 square SiC resistor and and R2 = 300 square SiC resistor. At 500 °C and accounting for body bias effects, the effective resistance of R1 translated to ohms is R1 = 528.73 kΩ while R2 = 5.259 MΩ. Using well-known op-amp inverting amplifier equations, below is an analysis of the Figure 33 circuit if R1 = 528.73 kΩ and R2 = 5.259 MΩ and α ≈ 99.56 (i.e., A_{vol} seen in Figure 28 to Figure 30 *r* = 10 mm T = 500 °C simulation results):

β = the feedback ratio = R1/(R1 + R2)
α = open loop gain
α·β = K
GAIN = A_v = Vo / Vi = -R2/R1· K /(1+K)
β = 528.73 kΩ/(528.73 kΩ + 5.259 MΩ) = 0.09135
α ≈ 99.56
K = 9.0948
A_v = –R2/R1· K /(1+K)
= –9.946 · 9.0948/10.0948
= –8.96

Figure 35 shows the SPICE-simulated performance of the Figure 34 amplifier revealing an A_v of –8.73, reasonably close to the –8.96 obtained in the above equational analysis.

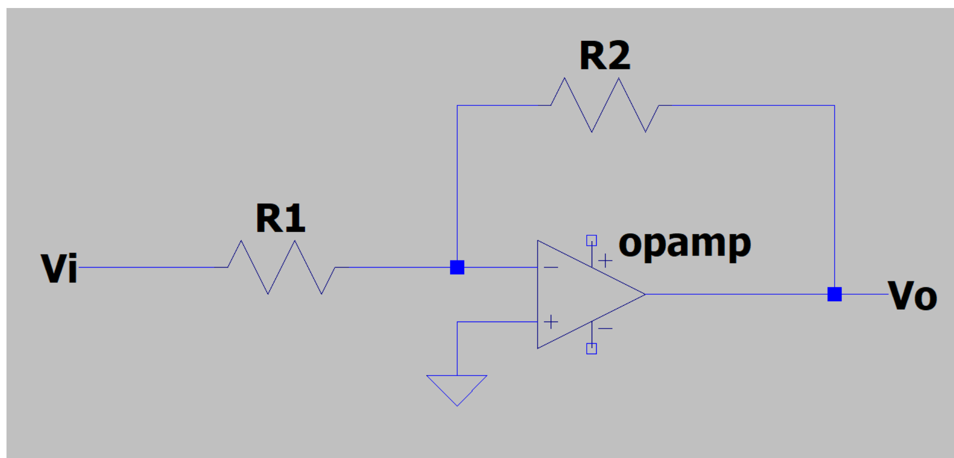


Figure 33.—Closed loop inverting amplifier circuit schematic, wherein the Vi/Vo gain nominally corresponds to -R2/R1.

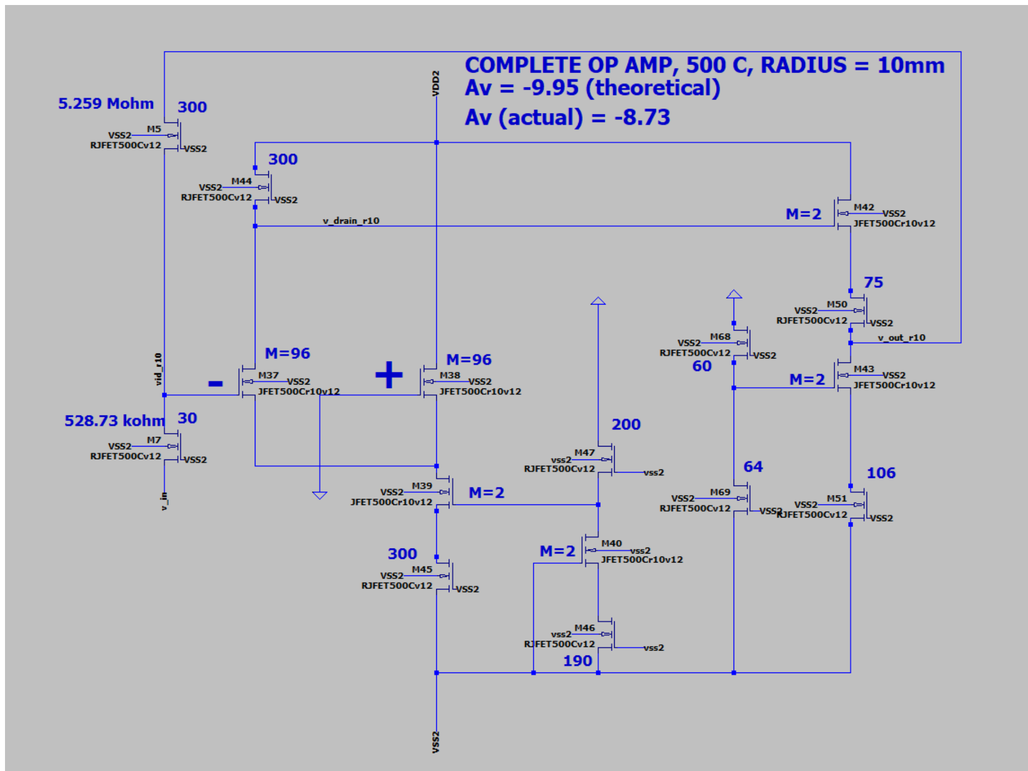


Figure 34.—Complete schematic diagram showing all internal components of a closed loop inverting amplifier circuit for *r* = 10 mm and T = 500 °C with R1 = 30 squares and R2 = 300 squares.

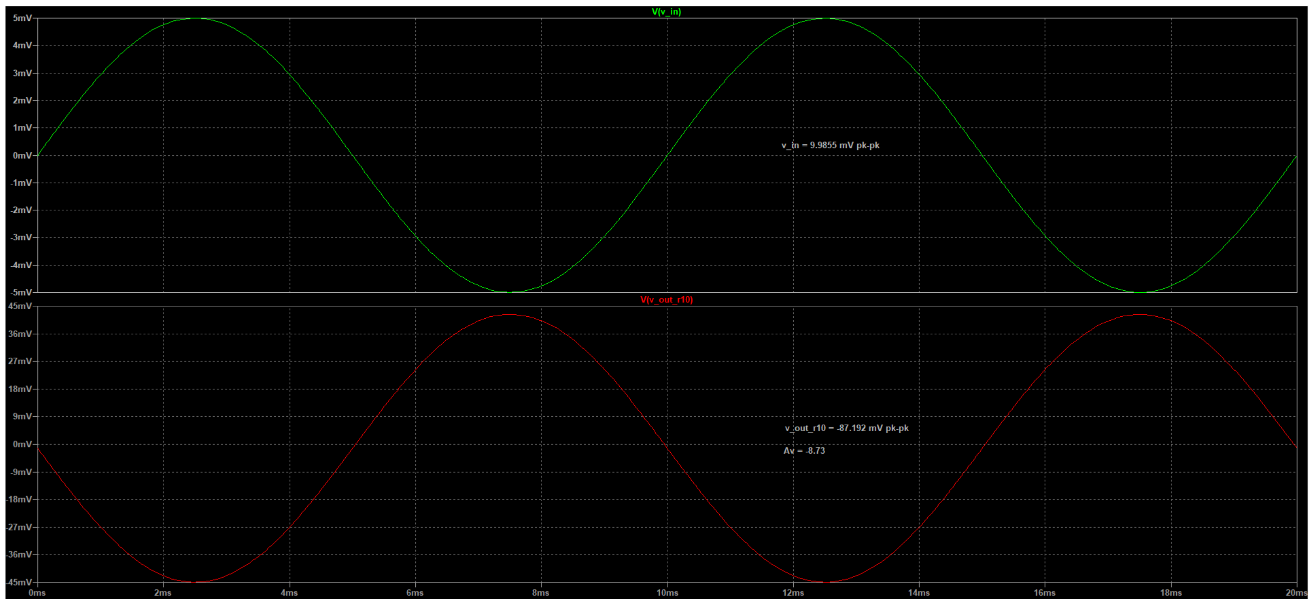


Figure 35.—SPICE simulation waveforms demonstrating performance of the Figure 34 closed loop inverting amplifier circuit. Green trace is 10 mV Pk-Pk sinewave input while the red trace is *r* = 10 mm output demonstrating voltage gain of –8.73.

5.4 Two Stage Op Amp (High A_{vol})

This section comparatively describes the performance of two-stage op amp with an A_{vol} of about 583 as well as a single-stage op amp with an A_{vol} of 93.8. The basis of this comparison is a non-inverting closed loop amplifier circuit configuration, wherein the voltage gain is ideally $1 + R_F/R_I$ with $R_F = 300$ squares and $R_I = 20$ squares corresponding to nominal $A_V = 16$. Figure 36 shows the v_in (green) versus v_out (red for single-stage, blue for two-stage) waveforms for both amplifiers. Note that the closed-loop circuit using the higher open-loop gain two-stage amp exhibits voltage gain closer to the nominal value of 16, as expected. Further, note the larger phase shift in the red waveform of the circuit that uses the single-stage amplifier.

Magnified plots in Figure 37 detail the SPICE-simulated DC offset corresponding to each amplifier. Note that the offset error is smaller for the two-stage amplifier (blue trace) than for that of the one-stage (red trace) amplifier.

However, Figure 38 illustrates that without high noise gain, the initial two-stage amplifier SPICE-simulates as unstable and eventually breaks into large-amplitude oscillation.

To address the instability problem seen in Figure 38, a resistor can be added across the amplifier input terminals resulting in stable amplifier characteristics seen in Figure 39 with the desired gain near 16.

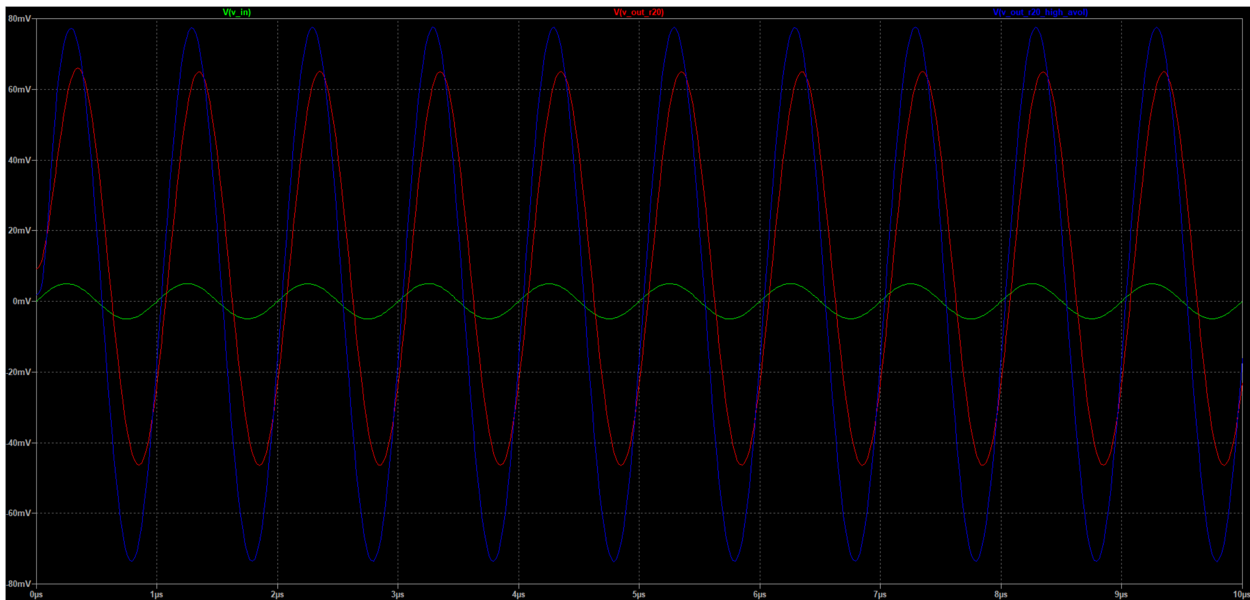


Figure 36.—SPICE simulation waveforms comparing the performance of closed loop non-inverting amplifier circuits configured with $R_I = 20$ squares and $R_F = 30$ squared that would ideally produce a voltage gain of 16. Green trace is 5 mV Pk-Pk sinewave input. The red trace is the output wave obtained using the single-stage op-amp design, while the blue trace illustrates closed loop gain closer to 16 obtained using a higher-gain two-stage op-amp.

Figure 37.—Magnified detail of Figure 36 SPICE simulation waveforms comparing the DC offset of the single-stage (red) and two-stage (blue) output waves.

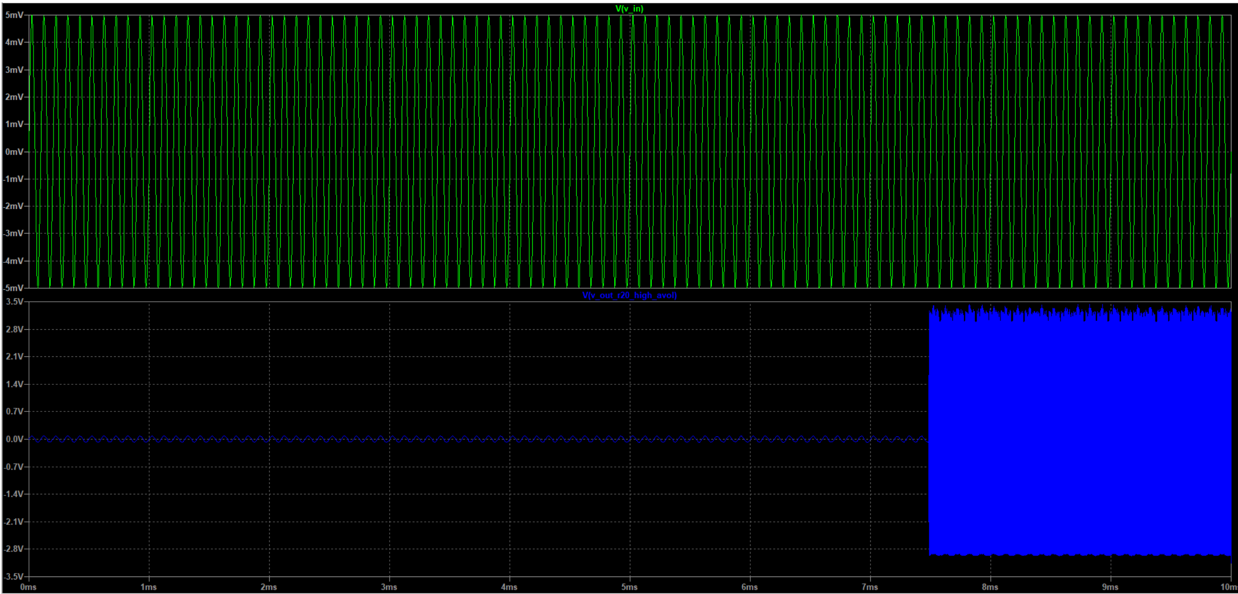


Figure 38.—SPICE Simulation waveforms of the non-inverting amplifier circuit showing unstable output observed for the version constructed with the two-stage op amp.

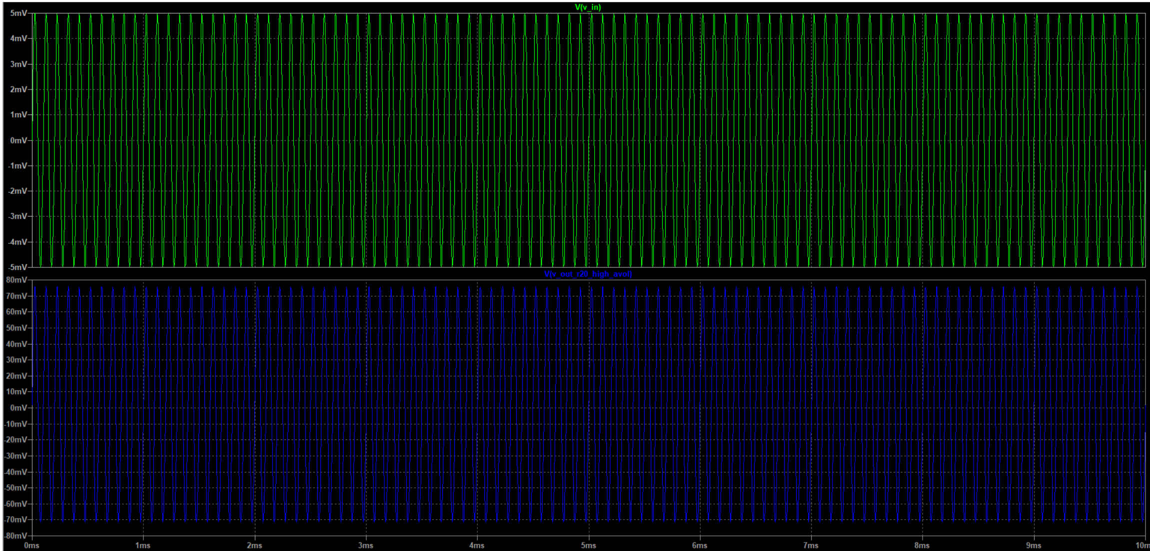


Figure 39.—SPICE Simulation waveforms of the non-inverting amplifier circuit showing stabilized output observed for the version constructed with the two-stage op amp following the addition of a 10-square compensation resistor as shown in Figure 40.

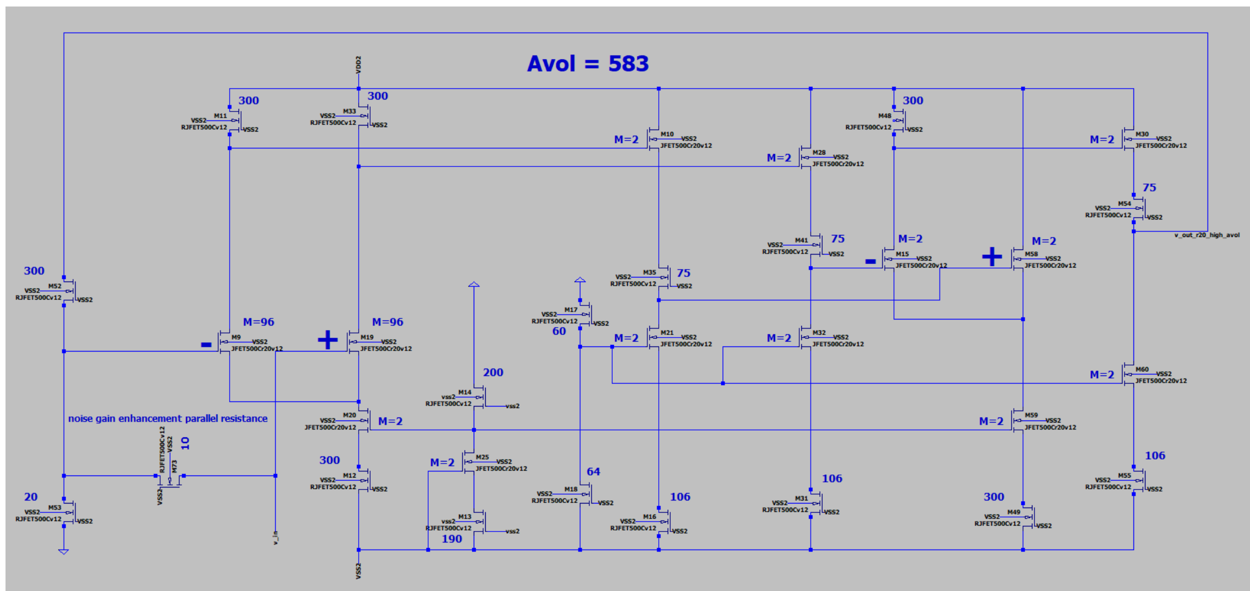


Figure 40.—The schematic diagram of the stabilized closed-loop amplifier circuit including all internal components of the high-gain two-stage op amp for T = 500 °C and ***r*** = 20 mm.

The schematic diagram of the stabilized closed-loop amplifier circuit including all internal components of the high-gain two-stage op amp is given in Figure 40. The 10-square compensation resistor M73 at the lower left of the schematic is used as a parallel resistance imparted upon the feedback ratio coefficient β and which increases the noise gain of the amplifier to a value greater than the gain realized by the R_F = 300 sq. / R_I = 20 sq. resistor ratio and thus stabilizes the closed-loop amplifier. The open-loop gain of the two-stage op-amp is actually set by transistors M15 and M58 the differential amplifier pair in the 2nd stage. Making these transistors larger (i.e., increasing and integer M above 2) will increase the open-loop gain of this two-stage op-amp design.

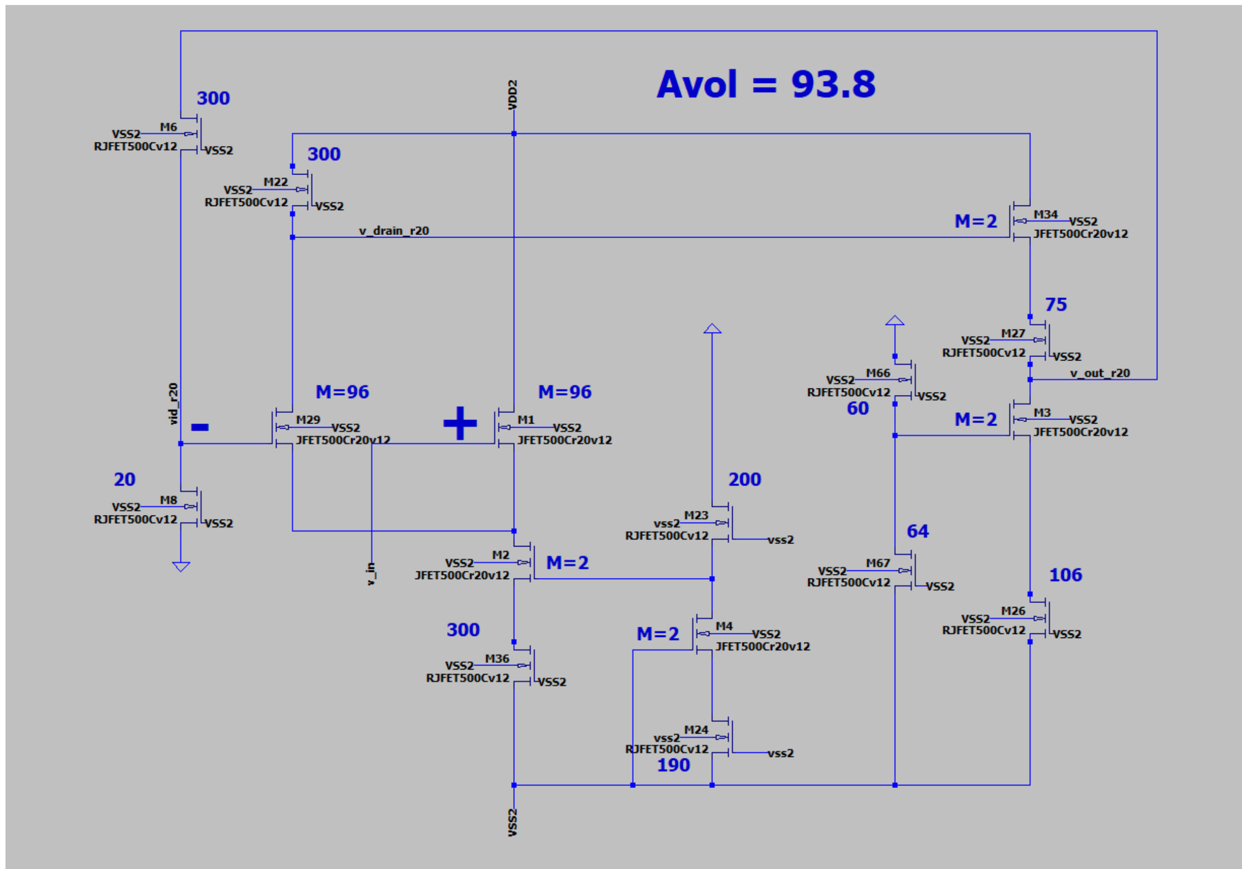


Figure 41.—Schematic diagram of the non-inverting closed loop amplifier based on the one-stage op-amp including the internal makeup of the one-stage op-amp for T = 500 °C and *r* = 20 mm.

For completeness of this discussion, the schematic diagram of the non-inverting closed loop amplifier based on the one-stage op-amp is illustrated in Figure 41 including internal makeup of the one-stage op-amp.

5.5 Adjusting the Op Amp Level Shifter Resistors to Trim Output Operating Point

Resistor Rs highlighted in Figure 42 schematic diagram is the quiescent point positioning circuit element in the op amp's output stage. The value of Rs = 75 squares was inferred after performing numerous SPICE simulations to tradeoff a compromise between mission-desired low amplifier power draw versus DC output accuracy. In Figure 42, the entire output stage is comprised of the M68 and M69 gate bias resistive voltage divider, JFET M43 and resistor M51 comprising a tail current source, M50 as Rs, and the source amplification JFET, M42. The tail current is at about 11 µA for the 500 °C, *r* = 10 mm case. At Rs = 75 squares, the amplifier open-loop output signal is relatively well positioned near ground (about 2 mV) for a 0 V differential input. The available output signal swing in this design is from about +6 V to about –3.85 V.

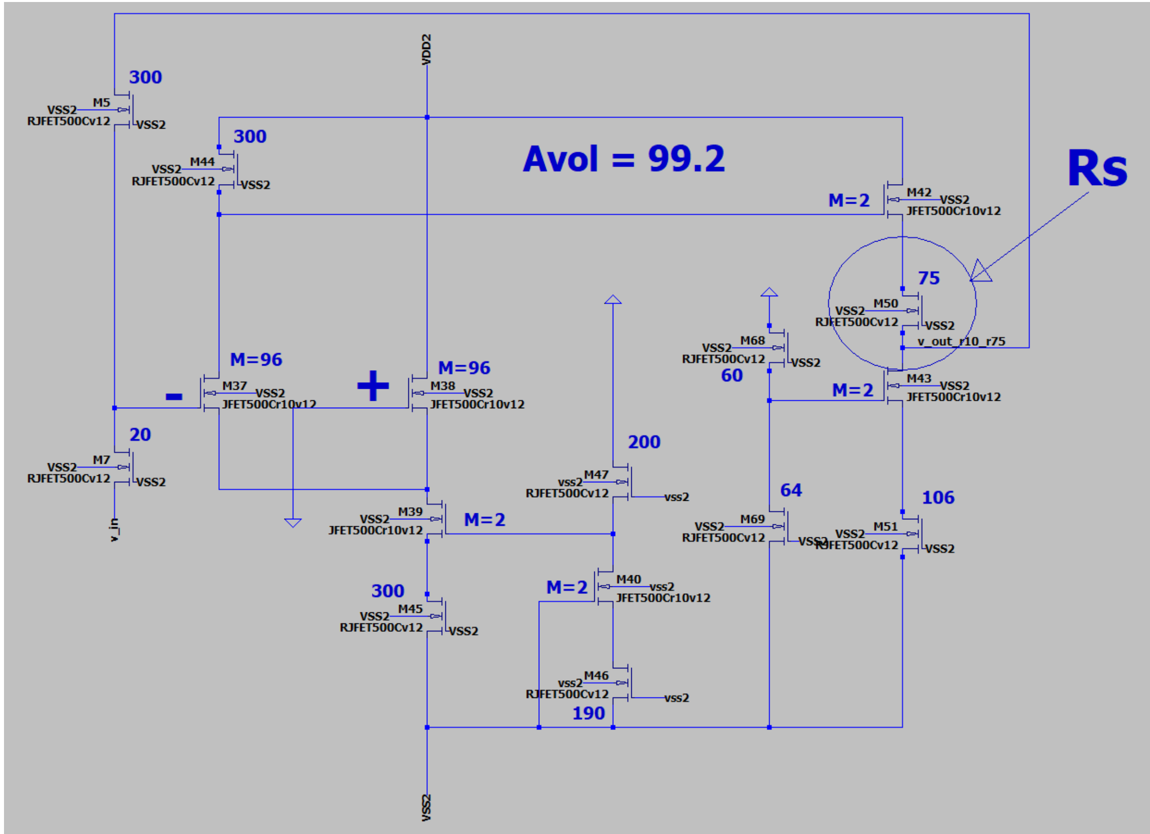


Figure 42.—Schematic diagram of the non-inverting closed loop amplifier based on the one-stage op-amp including the internal makeup of the one-stage op-amp for T = 500 °C and *r* = 10 mm. The 75-square resistor Rs highlighted is the quiescent point positioning circuit element in the op amp's output stage. Note this circuit is the same mask layout design as the Figure 41 schematic (that depicts the T = 500 °C and *r* = 20 mm case).

In our studies, instances have arisen where it has been useful to trim the accumulated DC error by trimming Rs in order to reposition the level of an output signal. For example, if at some stage of a multi-stage circuit design the accumulated error becomes too positively large due to the prior stages, Rs can be increased to trim the DC output level back closer to 0 V. This may be likened to laser-trimming of resistors on die to achieve enhanced accuracy.

Results from SPICE simulations of the closed loop inverting amplifier Vout versus Vin transfer characteristics for various Rs values of 70, 75, 80, 85, and 90 squares at *r* = 10 mm and T = 500 °C are shown in Figure 43. The gain of the various closed-loop amplifiers is at about –12.5. The DC accuracy of the Rs = 75 squares (blue trace) is closest to 0 V, as illustrated by the annotations in the plots.

The Figure 44 schematic diagram is an example of a customized sensor bridge instrumentation amplifier signal conditioning circuit where Rs was increased to 85 squares at the final output stage in order to remove a positive DC error value.

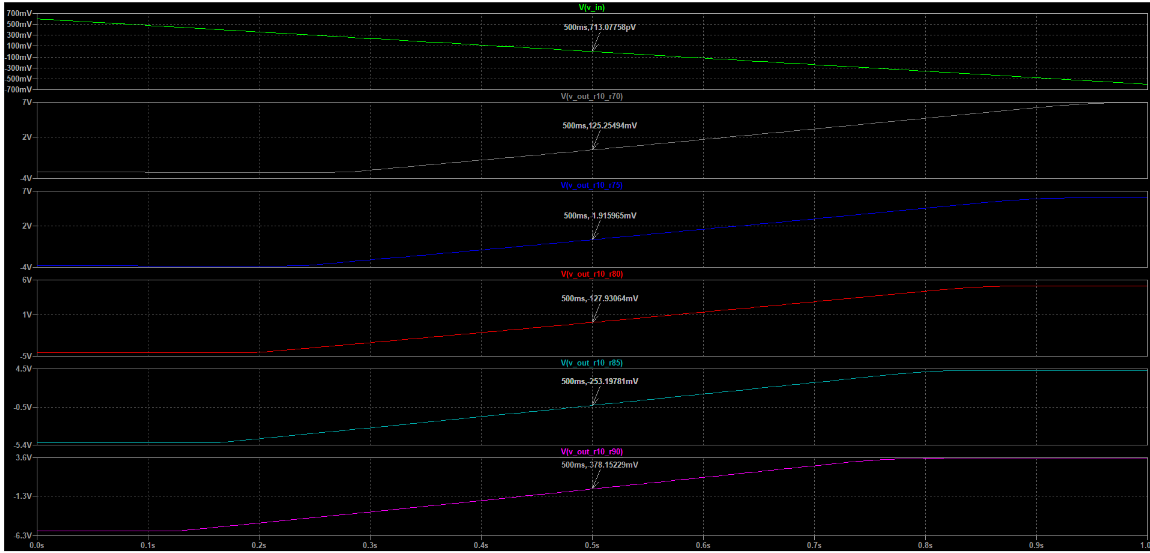


Figure 43.—Results from SPICE simulations of the Figure 42 closed loop inverting amplifier Vout versus Vin transfer characteristics for various Rs values of 70, 75, 80, 85, and 90 squares at *r* = 10 mm and T = 500 °C. The green trace of the top plot shows the Vin ramp, while the plots beneath show the amplifier output Vout for the respective values of Rs. While the voltage gain for the various Rs values remains near –12.5, the DC accuracy of the Rs = 75 squares (blue trace) is closest to 0 V as illustrated by the annotations.

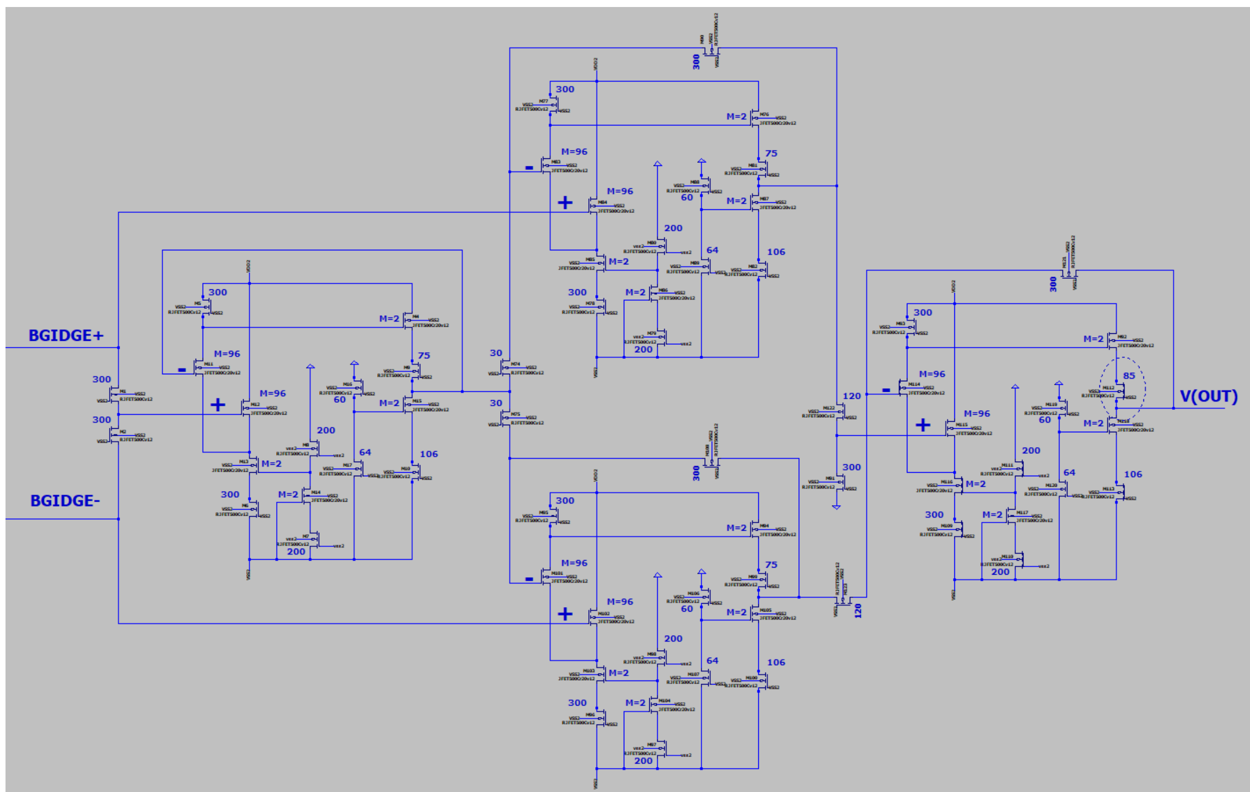


Figure 44.—A sensor bridge instrumentation amplifier with final-stage Rs increased to 85 squares to remove DC error.

6.0 Application Circuit Examples

This section will detail a number of fundamentally important circuits made practical by the techniques described in the previous sections of this report.

6.1 Voltage Reference

The schematic diagram for a –3 V reference voltage circuit that is effectively independent of radius and temperature is illustrated in Figure 45.

The Figure 45 circuit's SPICE-simulated dependence upon VSS2 supply voltage change is shown in Figure 46.

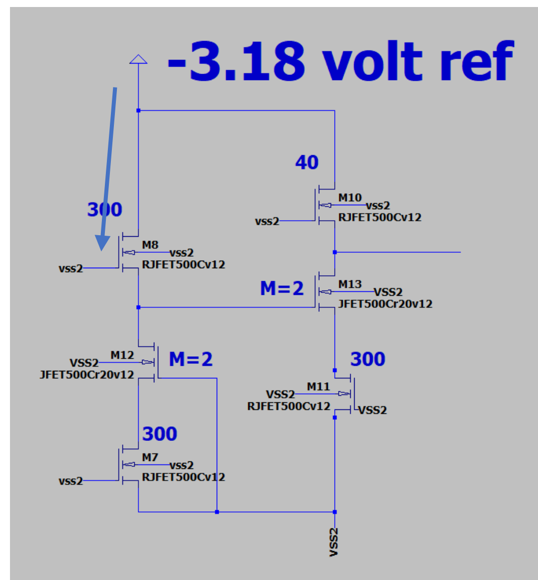


Figure 45.—Schematic diagram for –3 V voltage reference circuit.

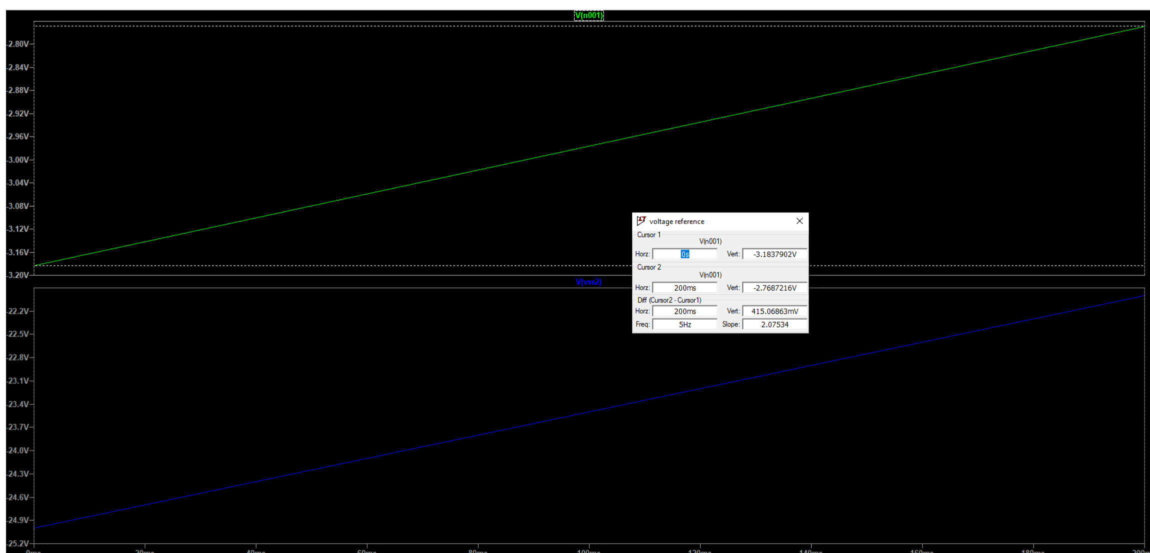


Figure 46.—SPICE simulation of Figure 45 voltage reference circuit output (top green trace) as a function of VSS2 power supply voltage (bottom blue trace).

Voltages other than –3 V may be readily obtained by changing the value of SiC resistor M10. Similarly, other reference output voltages may also be accomplished by adding parallel resistors, or also by changing resistor M10 and adding parallel componentry. For example, the Figure 47 schematic diagram illustrates a –1.24 V reference obtained by parallel and series additional resistors.

As shown in Figure 48, the Thevenin equivalent of M60, M64, and M74 may be used as the input into a closed loop inverting amplifier to create a positive voltage reference.

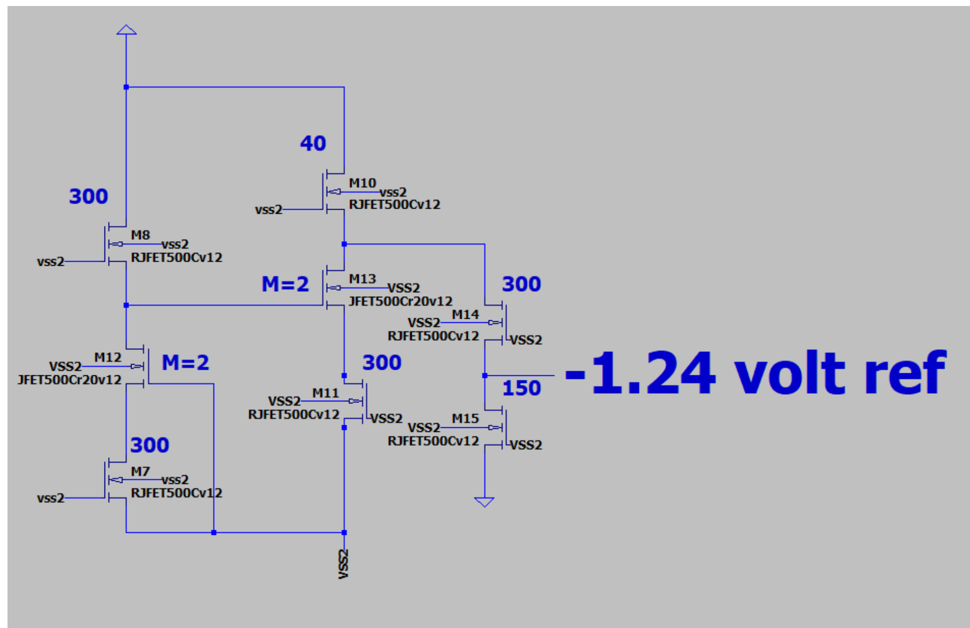


Figure 47.—Schematic diagram of a –1.24 V reference obtained by adding parallel and series resistors to the Figure 45 circuit.

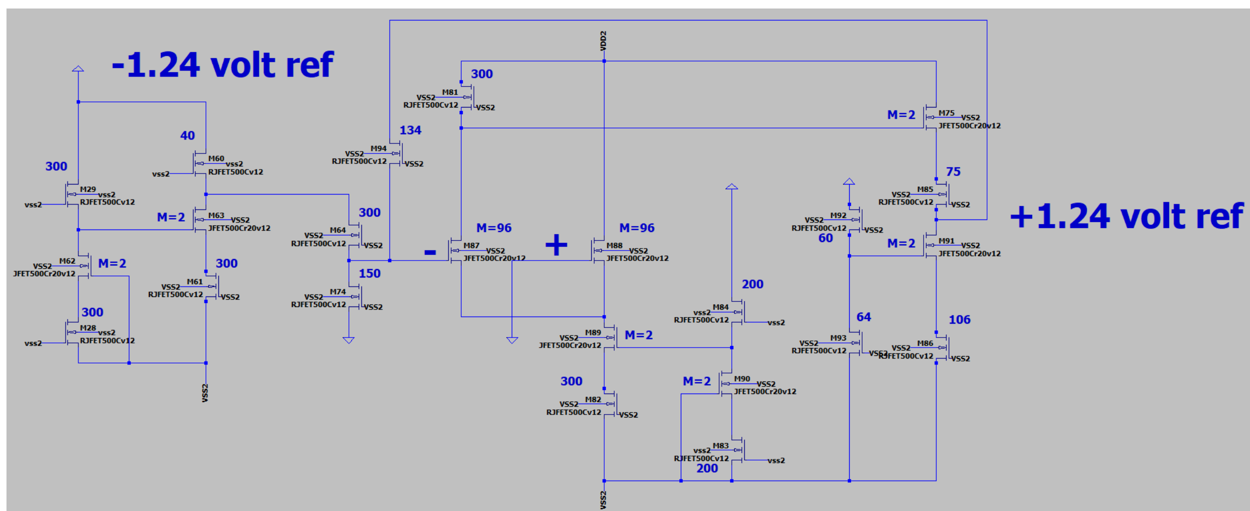


Figure 48.—Schematic diagram of +1.24 V reference obtained by adding an inverting amplifier to the Figure 47 circuit.

6.2 Analog Comparator

A comparator circuit schematic diagram is shown in Figure 49. This circuit compares the input voltages at the “+” and “-“ inputs (–3 to +3 V range) to output a SiC digital logic level depending on which input has the higher voltage.

Figure 50 details the two stage cascade of open loop op amp structures at the input, followed by a level shifter that performs initial translation to SiC logic output levels.

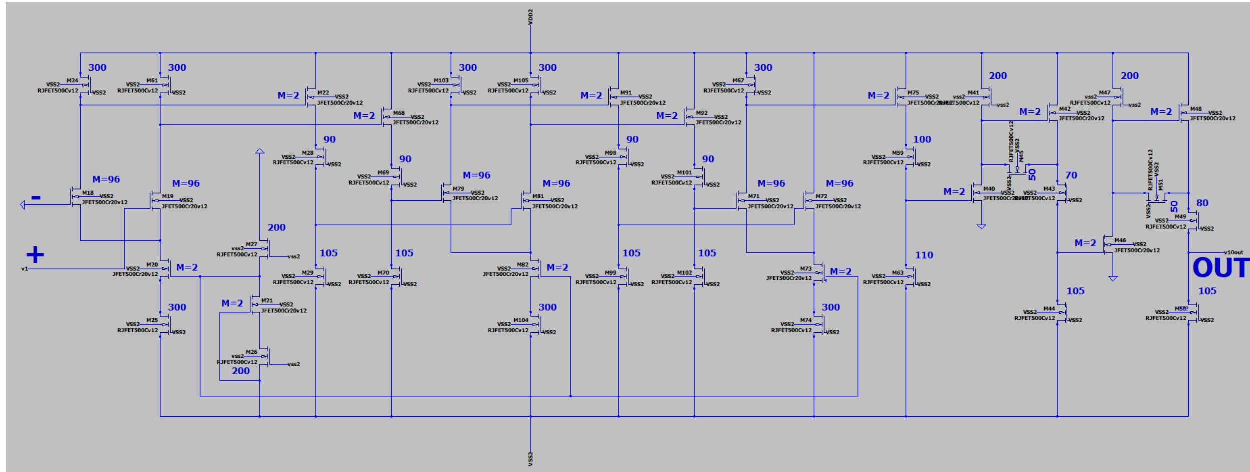


Figure 49.—Overall schematic diagram of a SiC JFET-R analog comparator circuit. The left and right sides of this schematic are respectively detaild in Figure 50 and Figure 51.

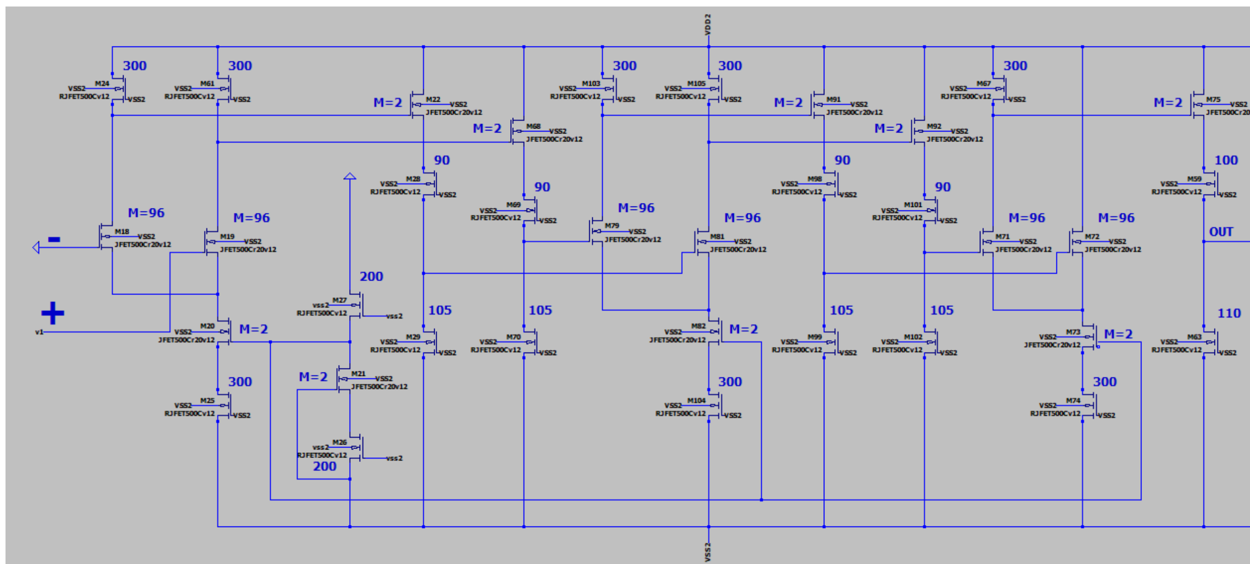


Figure 50.—Enlarged schematic of the left side of the Figure 49 comparator circuit.

Figure 51 details the output buffer section of the comparator, wherein two SiC inverters are cascaded to sharpen the output of the SiC logic signal.

SPICE simulation waveforms shown in Figure 52 to Figure 54 illustrate the comparator response to a bipolar (0 V reference) 1 mV input sine wave. The magnified view of a positive-slope equal-voltage crossing (i.e., zero-volt crossing) is shown in Figure 53, while Figure 54 details negative-slope equal (zero) cross. As seen in these plots, the ciruit is capable of resolving with sharp transition voltage comparisons (differences) on the order of microvolts.

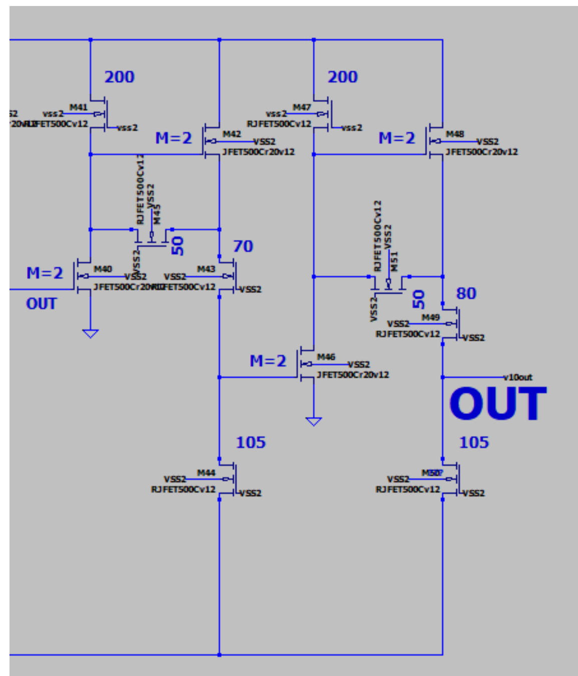


Figure 51.—Enlarged schematic of the right side of the Figure 49 comparator circuit.

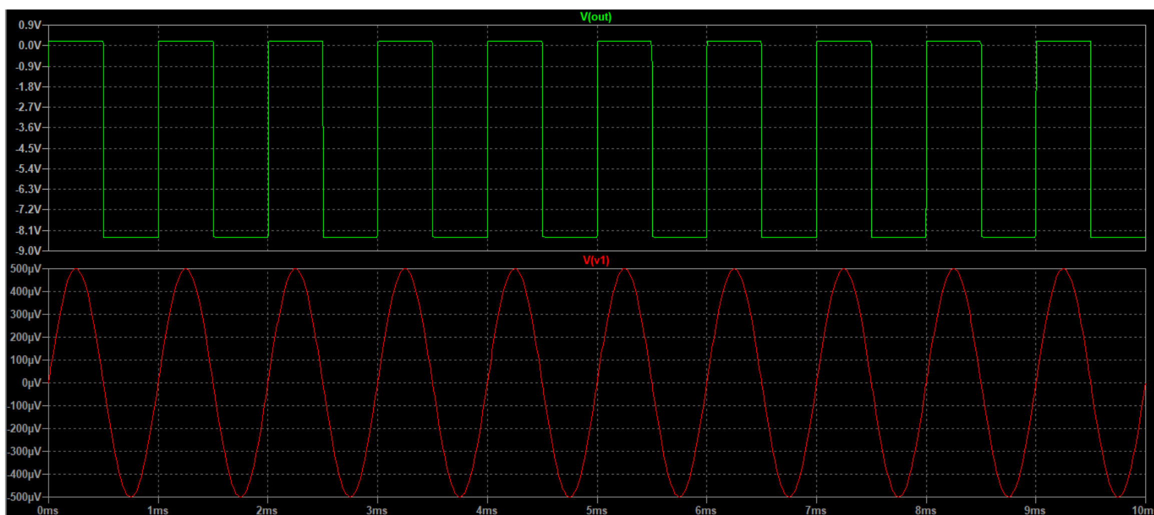


Figure 52.—SPICE simulation waveforms illustrating the response of the Figure 49 comparator circuit to a bipolar (0 V reference) 1 mV input sine wave.

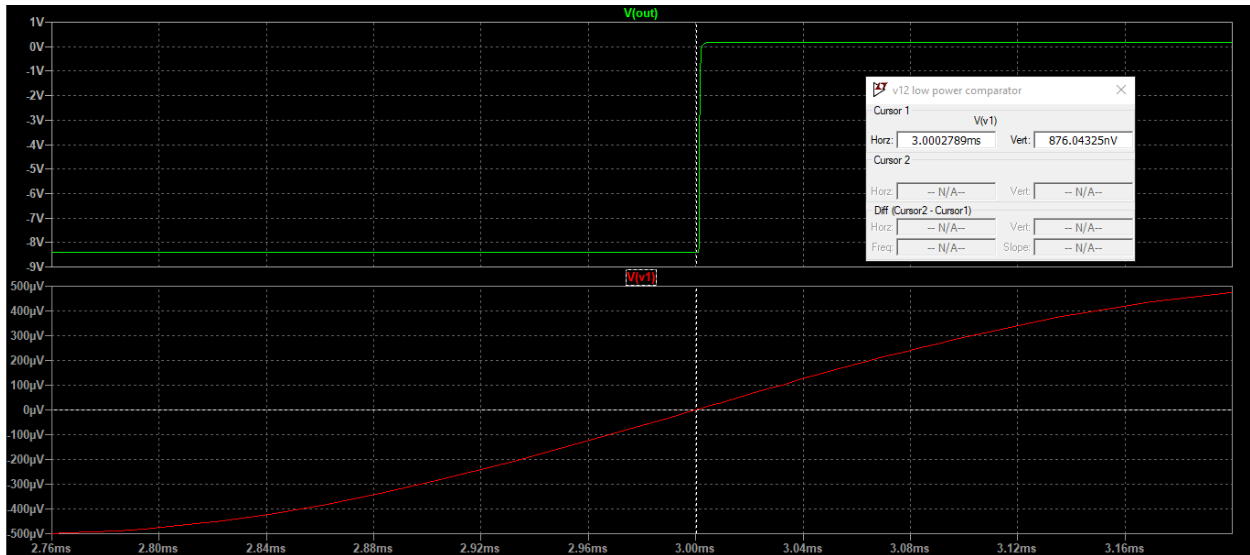


Figure 53.—Annotated magnified view of Figure 52 SPICE simulation detailing the positive-slope equal-voltage crossing.

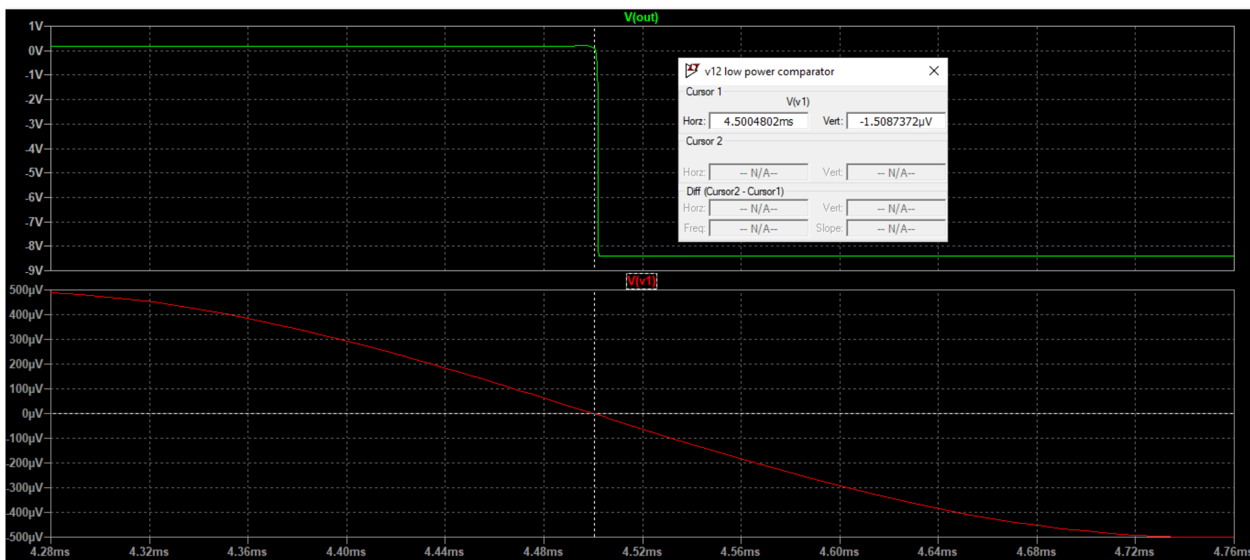


Figure 54.—Annotated magnified view of Figure 52 SPICE simulation detailing the negative-slope equal-voltage crossing.

6.3 Sense Amp and Squarer for RAM

A single-stage open-loop op amp can also be used as a comparator that consumes less chip-area at some expense to signal resolution. For example, a small-layout-area comparator is particularly useful for maximizing the number of storage bits that can be fit into a single SiC random access memory (RAM) chip. The Figure 55 illustrates the schematic diagram of a sense amp and squarer circuit that effectively reads the stored contents of a single addressed memory cell by resolving the voltage difference the single cell imposes on complementary bitlines DATA and /DATA running down a column of an array of RAM data storage cells on a SiC JFET-R memory chip.

Figure 56 is an illustrative example schematic of a complete 4-bit (i.e., 4-row) data column circuit on a RAM IC, along with a "digital waverform machine" (in the left box) that generates the test signals needed for the SPICE simulation of RAM IC operation. A practical RAM IC will of course have many more rows, columns, and storage cells than this illustrative simple example.

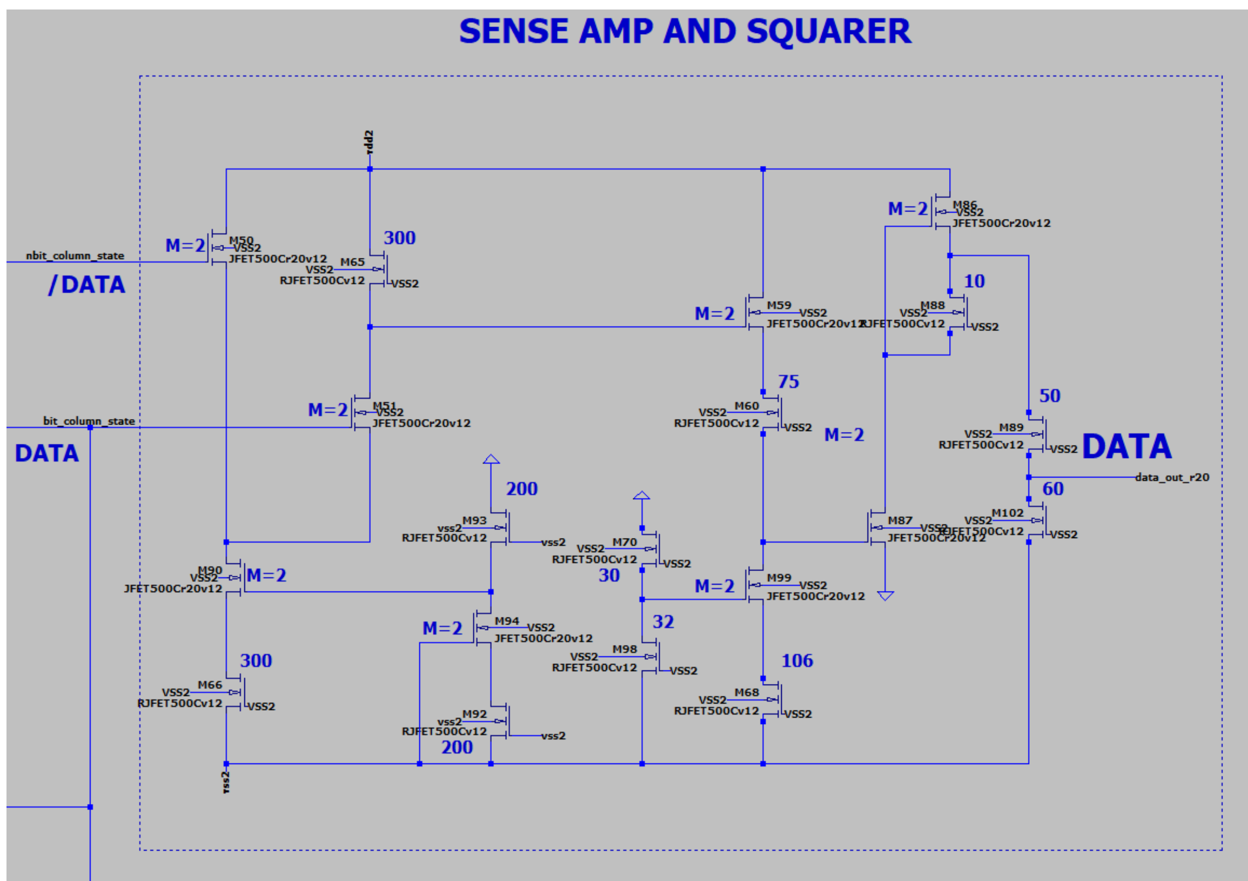


Figure 55.—Schematic diagram of a sense amp and squarer circuit for reading the voltage difference imposed upon bitlines DATA and /DATA by the stored contents of an addressed/accessed RAM cell.

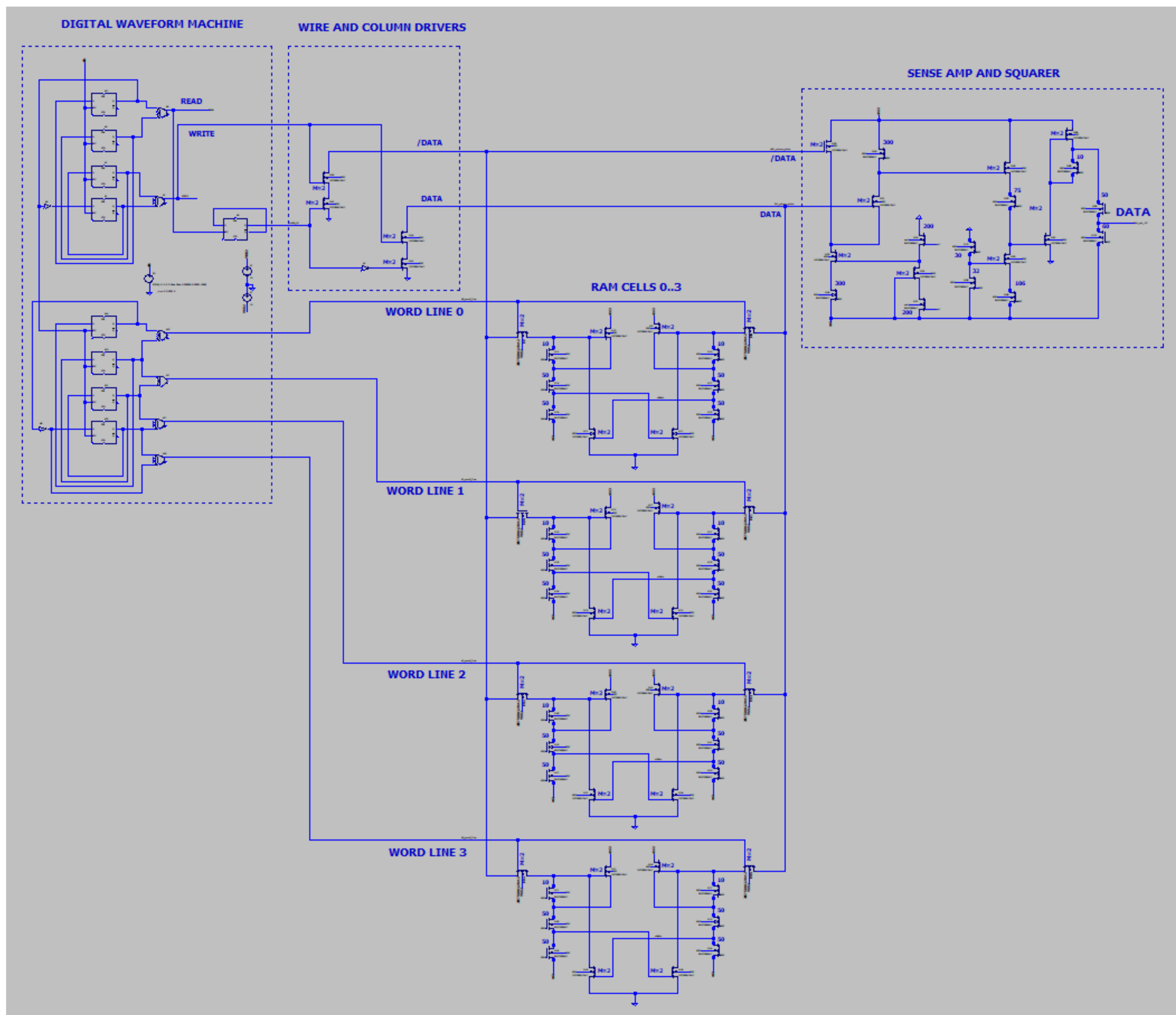


Figure 56.—Schematic diagram of a 4-bit (i.e., 4-row) data column circuit on a RAM IC, along with a “digital waveform machine” (in the top left dashed box) that generates the test signals needed for the SPICE simulation of RAM IC operation and “sense amp and squarer” circuit shown in Figure 55 (in the top right dashed box).

Figure 57 details one of the repeated RAM cells as well as the column drive (with complementary bit/column lines DATA and /DATA) and row address logic that uses pass transistors (M7 and M8) to control storage cell (i.e., cross-coupled regenerative logic) access to the bit lines. It is important to note that the bit lines function at positively shifted logic levels whereas the word lines operate at negative (standard for SiC JFET-R) voltages, which is needed in order to achieve adequate isolation of unaddressed cells from the bit lines as bit lines are driven to write data into the addressed cell. This shifted logic level approach is evident in the SPICE-simulated waveforms of bit line (i.e., column) activity during a test sequence of writing and reading an alternating pattern 0’s and 1’s given in Figure 58. In other words, a high (logic 1) on the blue “bit line” = “bit_column_state” and a low on the green “not bit line” = “nbit_column_state” results in a high output from the addressed RAM device (data_outr20), after which the opposite (write 0 and subsequent read 0) functionality is also illustrated.

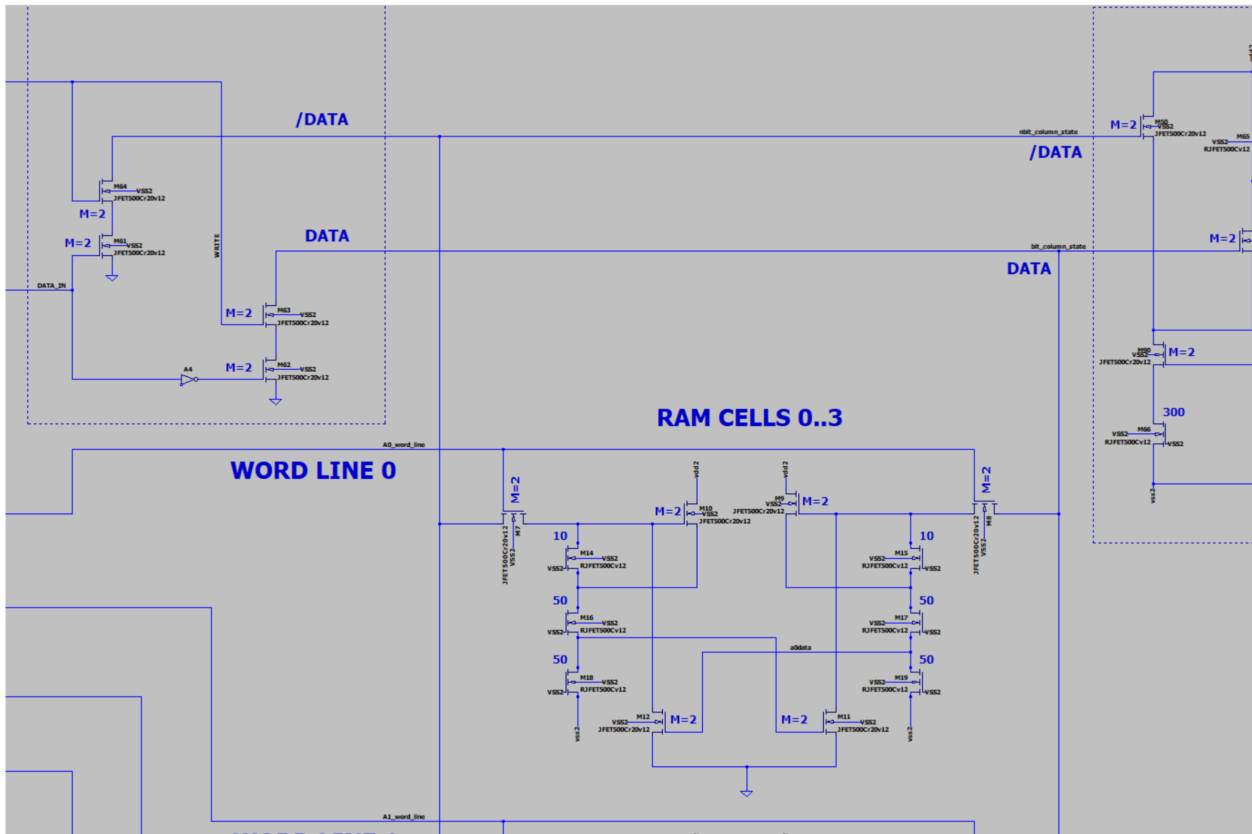


Figure 57.—Magnified detail of Figure 56 schematic illustrating RAM cell 0 as well as the column drive (with complementary bit/column lines DATA and /DATA) and RAM cell access transistors (M7 and M8) to memory cell (i.e., cross-coupled regenerative logic) access to the bit lines.

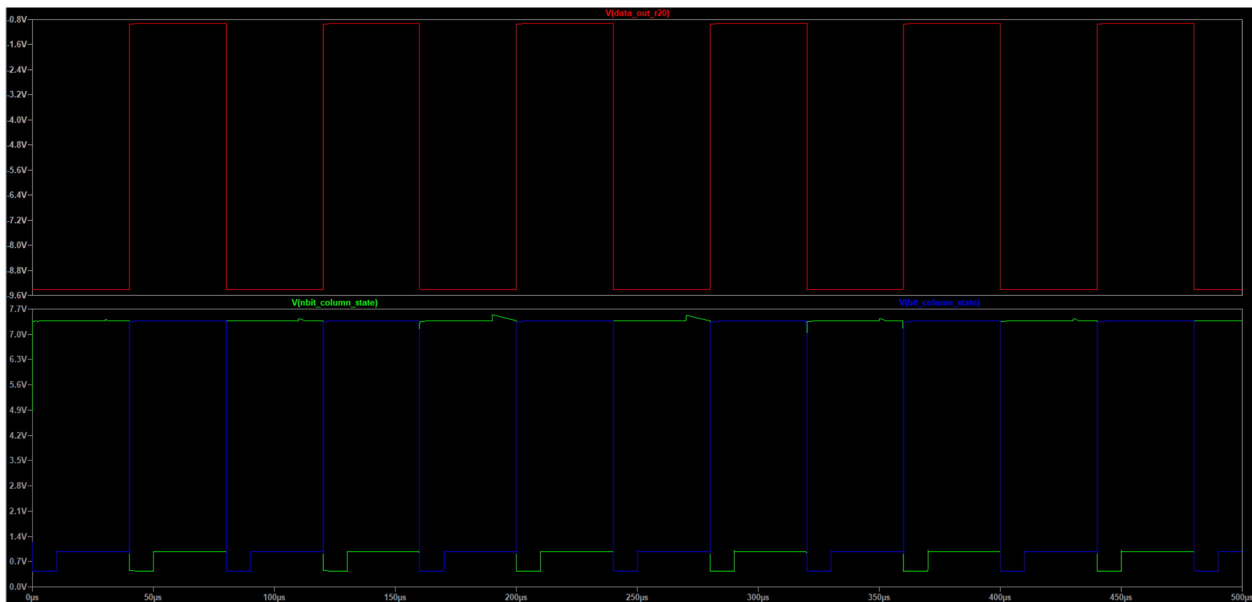


Figure 58.—SPICE-simulated waveforms of sense amp and squarer output (upper red plot) and bit line DATA and /DATA voltages (lower plot) during a test sequence of writing and reading an alternating pattern 0's and 1's for the circuit schematic shown in Figure 56.

6.4 Analog Switch

The SiC JFET may be used as an analog switch as long as care is taken to not forward bias the gate-source transistor pn junction and further to allow for sufficient voltage swing on the gate to take the gate-to-source voltage V_{gs} from full on (zero volts) to full off (below VT.)

The SiC logic gates can be designed to exhibit binary output voltage levels of around 0 V (ground) and –10.5 V. For a SiC JFET analog switch whose source is held at or near 0 Volts, this logic swing is sufficient to turn on (0 V) and turn off (≥ –10.5 V) the switch.

An obvious technique to keep the source of the JFET close to 0 V is to either tie it to a small resistance or to connect it to an op amp summing junction which is referenced to ground. Schematic diagrams of Figure 59 and Figure 60 illustrate examples of the op amp summing junction approach.

If the Input Voltage in Figure 59 has positive voltage components only, the SiC analog switch circuit will work as desired. While the circuit will also function for small negative-voltage signals, larger-amplitude negative-voltage signals can undesirably forward bias the JFET (i.e., SiC Analog Switch) gate-to-source junction when the Control Voltage is high near 0 V. It is therefore best to stick with positive Input Voltage signals.

Of course, multiple input channels each with a SiC JFET may be paralleled to create an analog multiplexer as illustrated in the Figure 60 schematic diagram. The on-state channel impedance for the JFETs must be accounted for (i.e., summed with its input corresponding resistor) when designing the signal voltage gain of this analog multiplexor circuit.

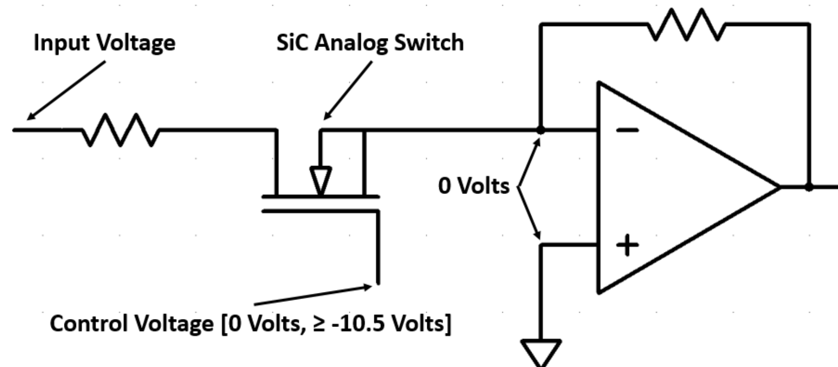


Figure 59.—Schematic diagram of single-channel SiC JFET-R analog switch circuit

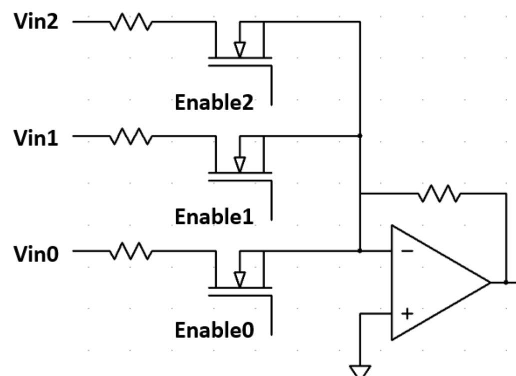


Figure 60.—Schematic diagram of 3-channel SiC JFET-R analog multiplexer.

Waveform generation, such as a sine wave approximation, can be achieved using obvious modifications of the circuit of Figure 60 through proper choice of input resistors each tied to the same voltage. Sine waves are often used to exicte sensors such as a capacitive seismometry sensor whose capacitance value changes relative to seismic activity. Tracking the variations in peak sine wave value passed by the sensor (envelope) provides a time series of seismic activity.

The Figure 61 schematic diagram illustrates an op amp configuration using an analog switch to select the polarity of a unity gain amplifier. With the control signal at logic 1 (near 0 V), the amplifer has a gain of –1. With the control signal at logic 0 (near –10 V), the amplifier has a gain of +1. One application for this circuit is in waveform generation as mentioned in the previous paragraph. If one were to produce the first 180° of a sine wave using the circuit of Figure 60 and a reciprocal up/down counter with data selector, the circuit of Figure 61 could be used to create the second 180° at opposite polarity to the first. With a comparator, the circuit of Figure 61 could be used for asynchronous rectification. With a clock signal, it can be used for synchronous rectification.

As shown by the Figure 62 schematic diagram, gain selection may be achieved through the introduction of the switches into the feedback loop, referenced to the summing junction. Choosing individual feedback resistors RfN individually or in parallel allows for variable gain selection. Again, it is important that the JFET channel impedances be considered (i.e., summed with respectived series RfN) in gain calculations.

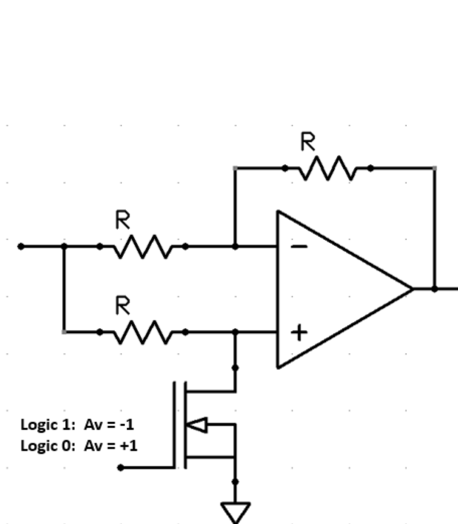


Figure 61.—Schematic diagram of analog switch circuit to select a unity gain output polarity.

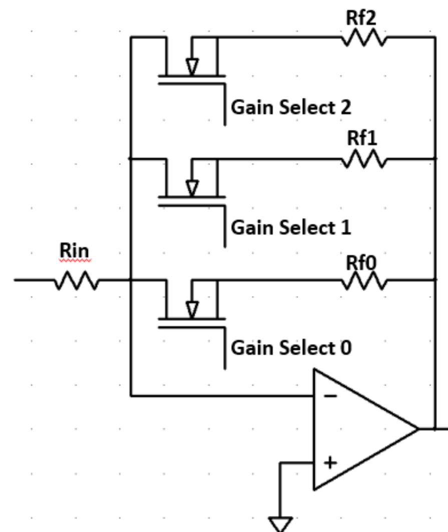


Figure 62.—Schematic diagram of inverting amplifier with selectable gain via three digital Gain Select input signals.

The classic R2R ladder circuit construct (shown in 4-bit configuration) is adapted to our requirements in the schematic diagram illustrated in Figure 63. Recall that the output impedance of the R2R ladder is equal to R.

For small INPUT VOLTAGE values, relying on the op amp to add gain, this circuit can be used as a digital to analog (D/A) converter. However, the input voltage source must have an output impedance << 2R. An op amp conditioning a voltage value is one option. A low impedance sensor output is another. Clever combinations of individual voltage sources each associated with a digital signal are also possible. Though Figure 63 shows the R2R ladder driving a summing junction, the output of the ladder, if left open circuit, is a voltage and may be used as such, into any impedance that suits the designer's needs.

6.5 Analog-to-Digital Converter

The schematic diagrams of Figure 64 and Figure 65 respectively illustrate two forms of analog-to-digital (A/D) converter circuit topologies. The R2R ladder-based D/A, when combined with the voltage comparator is an integral part of most analog to digital (A/D) converter topologies, including for example the Successive Approximation Register (SAR) and tracking A/D approaches.

SAR logic is well documented and certainly constructable from SiC JFET-R logic circuitry. A basic block-diagram SAR configuration is illustrated in Figure 64. An *n* Bit Word A/D conversion of the Input Voltage occurs in *n* Clock cycles.

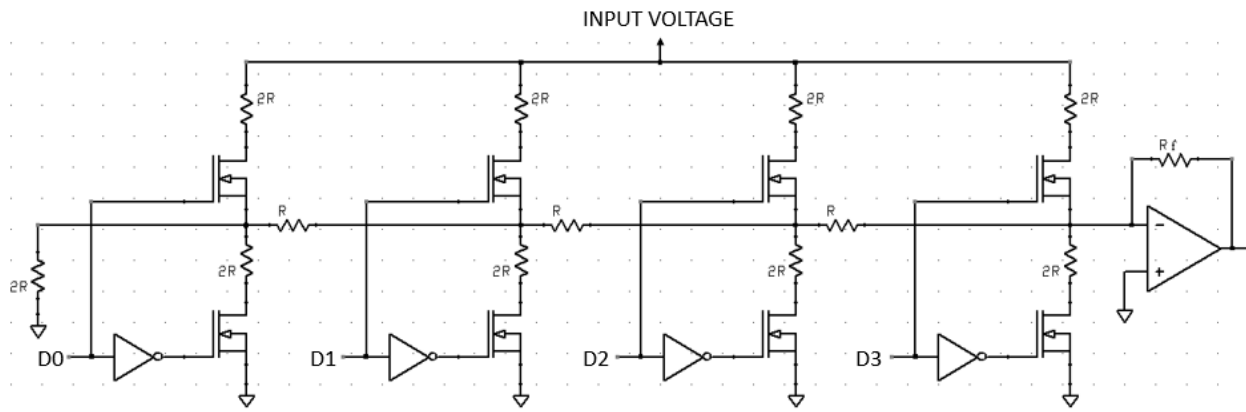


Figure 63.—Schematic diagram of 4-bit selectable gain R2R ladder inverting amplifier circuit.

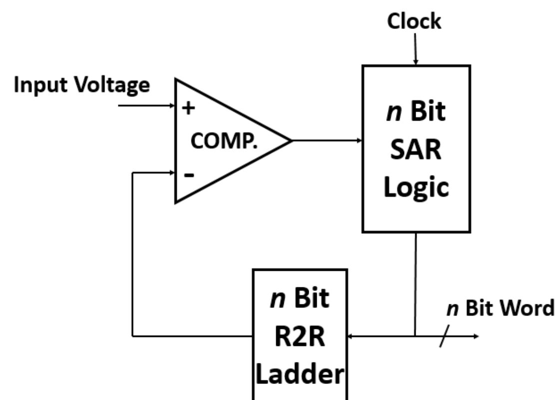


Figure 64.—Block diagram of Successive Approximation Register (SAR) A/D converter circuit topology.

The circuit topology for a tracking (also referred to as delta-sigma = ΔΣ) A/D converter (using an Up/Down Counter rather than an op amp integrator) is illustrated in the block diagram of Figure 65. Given a free running, Continuous Clock, this converter tracks an Input Voltage signal producing an updated *n* Bit Word at each clock cycle while at the same time producing a 1-bit conversion signal stream.

The Up/Down Counter counts up when the Input Voltage exceeds the output of the R2R ladder (i.e. counter-determined D/A signal) and counts down when the Input Voltage is below. At 100 percent convergence to a DC signal, the 1 bit ΔΣ stream has a 50 percent duty cycle representing 1 LSB ± ½ LSB of uncertainty (LSB = Least Significant Bit).

An improvement to the Figure 65 circuit topology is illustrated in Figure 66, wherein an edge-triggered Flip/Flop is used to synchronize the output of the comparator to the Continuous Clock, thus suppressing jitter from the 1-bit ΔΣ conversion stream.

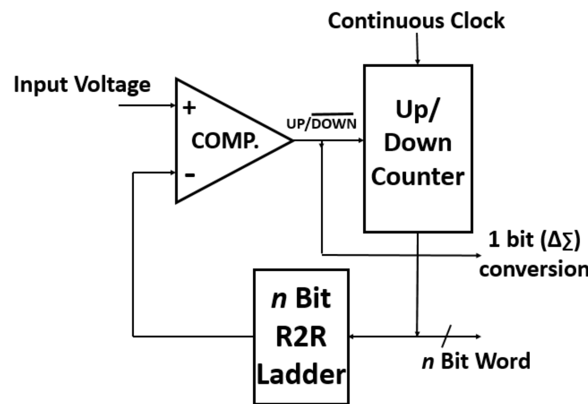


Figure 65.—Block diagram of the tracking (also referred to as delta-sigma = ΔΣ) A/D converter circuit topology.

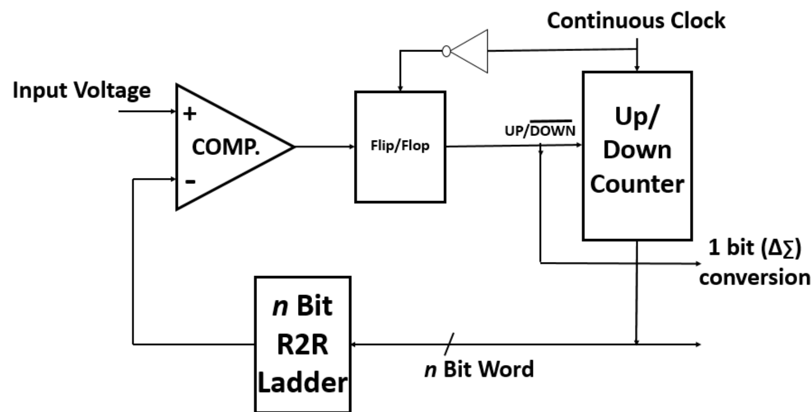


Figure 66.—Block diagram of the ΔΣ A/D converter circuit topology with Flip-Flop added to suppress jitter.

Obviously, the slew rate of the input signal must be within the volts-per-bit amplitude of the R2R ladder for high precision. If this is the case, the n Bit Word digital output will track the Input Voltage signal exactly. The application and the designer will determine the level of tracking accuracy necessary.

A 1-bit ΔΣ stream is also produced which may be transmitted to a similar *n* bit Up/Down Counter and R2R ladder at a receiving location running from a clock at the same frequency to reproduce the converted signal. A three-wire interface for any sized *n* bit conversion is thus possible comprised of the ΔΣ stream, the clock, and ground.

Such an output can also be combined with the clock, using various communications techniques such as Manchester coding to produce a single channel, suitable for radio transmission or upon any other linear combining medium.

7.0 Conclusion

This Technical Memorandum has presented methods by which both temperature and radius associated SiC JFET electrical parameter variances can be adequately eliminated, or even exploited in JFET-R circuit designs. Full analog circuit examples, including operational amplifiers and A/D converters, and SPICE simulations across experimentally documented SiC JFET parameter extremes have been presented to illustrate the effectiveness and usefulness of these methods. These circuits and methods were developed and illustrated using the NASA Glenn JFET-R IC Generation 12 process technology. With straightforward adjustments accounting for updated SPICE models of future JFET-R IC process generations (e.g., Generation 13 and above), the circuit engineering principles communicated here will remain generally applicable. The reader may use the examples in this memorandum as either an end point, to get a desired analog signal conditioning design into hardware implemented in SiC JFET-R ICs, or as a basis point from which to derive further improvement.

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