Nuclear and Emerging Technologies for Space
Sponsored by Oak Ridge National Laboratory, April 26th-30th, 2021.
Available online at https://nets2021.ornl.gov

DESIGN OF 1 KW SIMPLIFIED STIRLING CONTROLLER USING CAPACITOR-BASED POWER FACTOR CORRECTION

Christopher B Barth, Donguk Max Yang, and Max F Chaiken

[1]*NASA Glenn Research Center, Cleveland, Ohio, 44111*

Primary Author Contact Information: Christopher.b.barth@nasa.gov, 216-433-2678

Free-piston Stirling convertors provide efficient, reliable thermal to electric power conversion, provided they are paired with a robust controller. This paper outlines work underway on a system-level optimization of a 1 kW controller. Using passive power factor correction (PFC) this design explores the possibility of reducing programmatic risk through system simplification. Efficiency is improved through incorporating wide-bandgap gallium nitride (GaN) switches, and PFC volume is minimized through the use of polymer multi-layer capacitors. This work is aimed at exploring new approaches for future Stirling space power concepts.

I. Project Background and State of the Art

Free-piston Stirling convertors are valuable tools for thermal to electric power conversion as they are capable of converting heat energy into electricity with 3-4 times higher efficiency than radioisotope thermoelectric generator (RTG) systems and have a higher power density than Brayton systems in the 1 to 10 kW power range.

I.A. Stirling and Controller Optimization

The NASA Glenn Research Center (GRC) has made steady progress with corporate partners on the development of both Stirling convertors and controllers for Dynamic Radioisotope Power Systems (DRPS). Specifications have been guided by historical precedent in the design of 80 W convertors and the needs of 28 V spacecraft power buses. The development of 1 kW space-qualified Stirling convertors and controllers for the Fission Surface Power (FSP) project will benefit from a system-level optimization of the Stirling alternator and controller.

There are a few key differences between Stirling control for FSP and prior DRPS systems. The most prominent is that DRPS systems are required to remain operational from fueling through end of mission, necessitating that the Stirling control system operate through launch. FSP mission concepts call for the system to be activated after landing on the moon alleviating the launch requirements. Another simplification of the FSP system arises from the introduction of centering springs into most of the candidate Stirling engine concepts. This change will likely make the engines self-starting and eliminate the need for extended motoring at startup.

I.B. Power Factor Correction

The control of free-piston Stirling convertors has historically been complicated by high winding inductance in the alternator. This inductance, and the resulting reactive impedance, limits the flow of power from the Stirling alternator and prevents an energy balance between thermal energy flowing into the convertor and electrical energy leaving the alternator. The difference between the thermal energy input and the electrical load results in excess mechanical energy in the piston, causing over-stroke and damaging the convertor. In order to maintain control of the engine, the winding inductance must be negated using power factor correction (PFC).

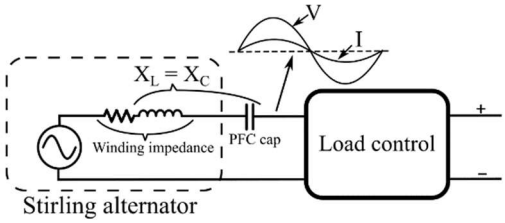

Figure 1: Capacitor-based PFC

PFC can be accomplished actively using an H-bridge to emulate a capacitive reactance by enforcing a phase shift between the Stirling alternator current and voltage. H-bridge control can be implemented using a digital controller. The Dual Convertor Controller and Advanced Stirling Convertor Control Unit, are two flight-like designs developed with oversight from GRC to control 80 W, low voltage Stirling convertors. Both systems employed an FPGA with relatively complex control for PFC functionality. H-bridge control has also been implemented using analog control strategies to replace the FPGA.

An alternative to active PFC is the use of a series-connected capacitor. The capacitor-based PFC controller approach as shown Figure 1 has been demonstrated in breadboard-form as the NASA Analog Controller (NAC) at GRC controlling a single 80 W Stirling convertor. Historically, the use of power factor correction capacitors has been avoided because of their large size and unverified reliability. Polypropylene capacitors following the MIL-PRF-83421/2 specification are the most appropriate legacy devices for this application, and 1 kW class Stirling convertors anticipated for FSP will require approximately 36 parallel devices resulting in a volume of 1.2 L, and 1.5

lbs. for each convertor. This volume is challenging for large arrays of 8 or more engines in fission applications, and more so when redundancy is considered.

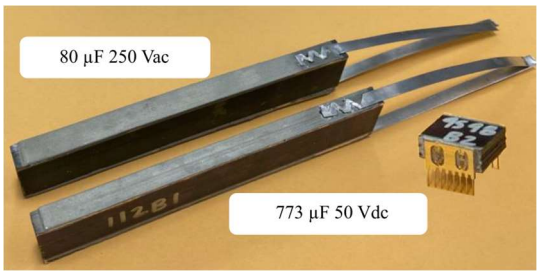

Figure 2: Unencapsulated NanoLam capacitors

II. System design methodology and core strategy

The high radiation environment and high engine count (8, 12 or 24) required for the FSP project motivates the consideration of a simplified controller which is robust, reasonably compact, and minimizes development risks in cost and schedule. All electronic components, the circuit topology, and thermal management demonstrated in this research are selected to have a path to flight within the timeframe of the FSP project.

II.A High-density NanoLam capacitors

To address the need for high-density capacitors for Stirling controllers, NASA has awarded an FY21 Small Business and Innovation and Research (SBIR) Phase I contract to Sigma Technologies/Polycharge of Tuscon, AZ, to adapt their polymer nanolaminate or "NanoLam" capacitors for use in Stirling controllers. NanoLam capacitors are formed via vacuum deposition and comprised of 1000s of nano-capacitors formed from polymer dielectrics and aluminum electrodes. The nano-laminate material is formed in sheets then cut and stacked to form capacitors with voltage ratings from 10-10,000 V.

The NanoLam technology replaces the process of film extrusion, metallization, and winding used in film capacitors with a simplified process in which aluminum wire and a monomer liquid are introduced into a machine that converts them into a large "mother capacitor" of nanolaminate material. This manufacturing simplification combined with the use of low-cost radiation-cured monomers used to form the cross-linked dielectrics makes NanoLam technology highly cost competitive when compared to film and multi-layer ceramic capacitors (MLC). Additionally, NanoLam devices have demonstrated an energy density (J/cc) 4X higher and a specific energy density (J/kg) 10X higher than the dc multilayer ceramic MLC capacitors frequently used in Stirling control dc link applications. NanoLam capacitors also do not exhibit voltage bias derating but do offer self-healing, open-mode failure, and superior radiation hardness to polypropylene devices. Figure 2 shows two of the prototype NanoLam capacitors developed by Sigma Technologies/Polycharge.

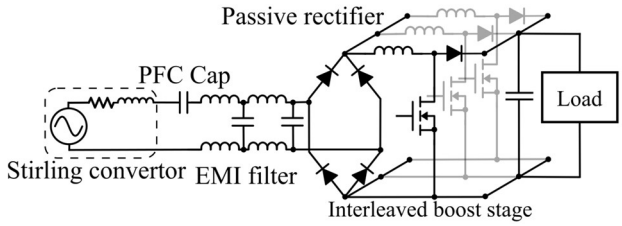

Figure 3: Schematic of controller with interleaved boost stage. The "Load" block includes voltage regulation and a backup power dissipating shunt.

II.B Active Device Selection

Wide bandgap devices such as GaN and SiC have promised advances in space power for some time because of their general resilience to ionization, however challenges related to device quality and single event effects (SEEs) have limited their use in space power to commercial applications in near-earth orbit. To motivate further adoption of these devices in space power, this work is evaluating the use of GaN devices from two suppliers of high-reliability devices targeting the space market. While these devices do not have flight heritage with NASA, discussions with industry representatives and NASA radiation and quality experts have indicated that they are representative of GaN devices which could feasibly be brought to flight within the timeframe of the FSP project.

II.C. Stirling control strategy

Achieving high power factor requires minimal phase shift between line current and voltage as well as minimal distortion in the current waveform. With the challenge of phase shift being handled directly by a capacitor, the remaining functionality of the Stirling controller is to provide a low THD, unity power factor load to the Stirling. Fortunately this functionality is common in terrestrial applications with the most common topology being the boost PFC converter as shown Figure 3. The boost converter draws current in phase with the input voltage and boosts the rectified ac input voltage up to a dc link voltage which is higher than the peak ac input voltage.

While continuous conduction mode (CCM) is historically the most frequent strategy for boost PFC control, hardware and control can be simplified through the use of boundary conduction mode (BCM) or discontinuous conduction mode (DCM). In these approaches the inductor current either instantaneously reaches zero each switching cycle (BCM) or returns to zero for a percentage of each switching cycle (DCM). Neither BCM nor DCM require the accurate measurement of inductor current required for CCM operation. Under BCM conditions it is sufficient to sense the inductor current zero crossing by means of a sense winding on the boost-inductor coil and no sensing is

required for DCM operation. A comparison of the inductor current waveforms for CCM and DCM is shown in Figure 4.

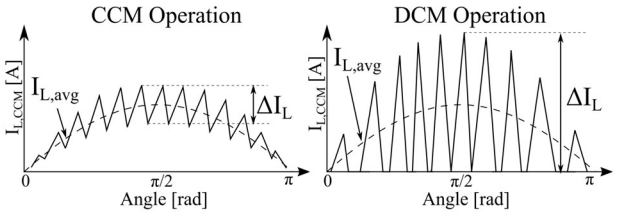

Figure 4: Comparison of CCM and DCM waveforms

Historically, Stirling control has been implemented using CCM-type control accomplished via the modulation of H-bridge switches. Given the complexity of the overall controller, the measurement of inductor current was inconsequential. However in an effort to explore a radically simplified control system, this work has pursued the use of DCM control. Under DCM the high-frequency control loop regulating the inductor current amplitude is eliminated and the boost converter runs at a constant frequency and duty ratio with the system designed to ensure that the inductor current returns to zero each switching cycle [1]. The average line current flowing into the boost circuit stays in phase with the line voltage simply due to the changing volt-second balance on the inductor resulting from the changing input voltage. A properly designed DCM boost stage can maintain efficiency on par with CCM control despite the higher RMS inductor current under DCM as shown in Figure 4. This is partially due to the elimination of switching losses in the diode during DCM operation [1].

Using the DCM approach there is no control needed at the switching frequency and only minimal changes in duty ratio over the line cycle to optimize power factor and control the Stirling stroke to the proper amplitude. Flyback, Cuk, and SEPIC converters can produce unity power factor as PFC circuits operating in DCM, however a simple boost converter will exhibit distortion in the current waveform as the peak line voltage approaches the dc link voltage [2] [3]. For this reason the design is constrained such that a minimum boost ratio of 15% is required between the peak ac amplitude and the dc link voltage.

During CCM operation the boost converter raises voltage between input and output as a function of duty ratio (d) according to the relationship,

$$V_{out} = \frac{1}{1-d} V_{in}. \quad (1)$$

In DCM operation the voltage conversion ratio is more complex. The approximate duty ratio needed to load the Stirling may be calculated based on the impedance conversion which must take place between the Stirling and the dc link at the output of the controller. The input and output impedance of the boost stage is simply calculated as,

$$R_{in} = \frac{V_{Stirling}}{I_{Stirling}} \ \ and \ \ R_{out} = \frac{V_{dc\,link}^2}{P_{dc\,link}}. \quad (2)$$

The required gain (M) between the input and output voltage can be stated in terms of impedance as,

$$R_{in} * M^2 = R_{out} \quad \rightarrow \quad M = \sqrt{\frac{R_{out}}{R_{in}}}. \quad (3)$$

The dimensionless parameter K is an indication of the range of conditions over which a boost converter will operate in DCM. For $K > K_{crit}$ the converter will run in CCM and for $K<K_{crit}$ the converter will run in DCM [4]. K and K_{crit} are calculated in terms of the boost inductance (L), the switching frequency (f_{switch}) and the duty ratio for the boost converter as,

$$K = \frac{2\,L\,f_{switch}}{R_{out}} \ \ and \ K_{crit} = d(1-d)^2. \quad (4)$$

The gain for a boost converter in DCM is [4],

$$M = \frac{1+\sqrt{1+\frac{4d^2}{K}}}{2}. \quad (5)$$

Constraining the system to operate in DCM, the duty ratio required to load the Stirling can be calculated as,

$$d = \sqrt{K * (M^2 - M)}. \quad (6)$$

The boost duty is tuned at low bandwidth to maintain the appropriate alternator loading and voltage amplitude.

II.D. System-level optimization

Mass minimization and efficiency maximization are important for flight applications, but a tradeoff often exists between these two design goals. Additionally, circuit components for flight are limited by reliability and radiation hardness requirements, and semiconductor switches, inductors and capacitors are available with discrete values and limitations. This makes solving a continuous optimization for the best trade between efficiency and power density very challenging and minimally beneficial. Instead of a continuous optimization, a random process can be used to develop a Pareto design front indicating the optimized trade space [5]. The optimization is accomplished using a script to generate a large number of feasible circuit designs based on an available parts library and acceptable limitations for variables such as alternator current/voltage, switching frequency, and conducted EMI [6].

In this work a script has been created in Matlab to generate and evaluate the performance of a large number of plausible circuit designs. After each selection, following selections were restricted to ensure the system would function as designed. The selections made for each design iteration include:

- Number of parallel interleaved boost stages
- Primary switch
- DC link voltage
- Diode
- Stirling alternator voltage and resulting impedance

- DC link capacitor size
- PFC capacitor size
- Switching frequency
- Inductor selection
- DCM duty ratio
- Input differential mode filter stage count and sizing

After the design is formulated, linear loss and mass models (objective functions) are used to evaluate the design performance. Simplified linear loss estimates are used for the Pareto optimization because the ability to quickly iterate over a large number of candidate designs and calculate their relative merit is more important than knowing the precise efficiency. After analysis, the efficiency and mass of each design is then plotted as shown in Figure 5. In this example the trade front is relatively sharp, and choosing the design closest to the lower left corner will result in the best trade between efficiency and power density.

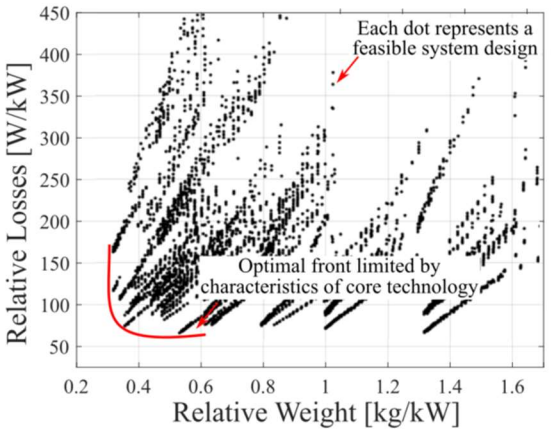

Figure 5: Pareto plot of feasible system designs showing relative weight and losses

III. Control simulation results

Simulations have been conducted using LT Spice with a Stirling model to validate the concept of DCM boost control of a Stirling engine. Assuming the use of self-centering engines in the FSP application, the engine temperature and piston amplitude will rise with reactor start-up. During this interval the controller will present a small constant impedance load to the engine. As the piston amplitude increases the controller PI control will adjust the boost duty ratio to limit engine voltage and piston motion to the designed amplitude.

Figure 6 shows the plot of regulated engine operation with the PI control nearly constant throughout the ac cycle of the engine. This is the only dynamic control required for the DCM boost controller strategy and is implemented using simple analog operational amplifiers widely available as high-reliability, SEE tolerant devices.

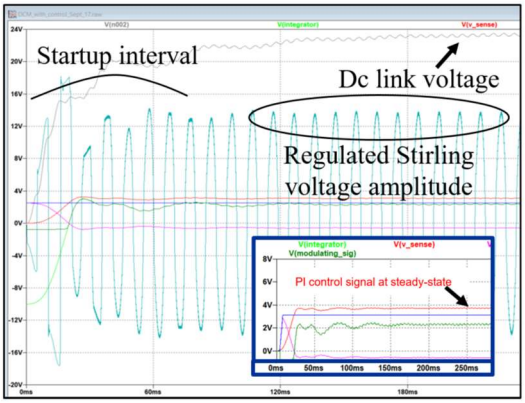

Figure 6: Plot of simulated Stirling and controller waveforms

III. Conclusions and next steps

This work has motivated a simplified Stirling control strategy focused on multi-engine fission applications. The development of NanoLam PFC capacitors was discussed as well as the active devices and DCM control strategy being used. The design optimization strategy is outlined as well as preliminary simulation results showing control functionality. Hardware and experimental results will be presented in future work.

ACKNOWLEDGMENTS

Special thanks to Dr. Tomas Modeer of SCiBreak, Stockholm, Sweden for the use of his Pareto front template script.

References

[1] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela and J. Kolar, "Comprehensive Design and Optimization of a High-Power-Density Single-Phase Boost PFC," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 7, pp. 2574-2587, 2009.

[2] L. Rossetto, G. Spiazzi and P. Tenti, "Control Techniques for Power Factor Correction Converters," in *Power Electronics, Motion Control and associated applications (PEMC)*, Warzawa, Poland, 1994.

[3] K.-H. Liu and Y.-L. Lin, "Current Waveform Distortion in Power Factor Correction Circuits Employing Discontinuous-mode Boost Converters," in *20th Annual IEEE Power Electronics Specialist Conference*, Milwaukee, WI, 1989.

[4] P. T. Krein, Elements of Power Electronics, New York: Oxford University Press, 1998, pages 117-124.

[5] J. Kolar, J. Biela, S. Waffler, T. Friedli and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *6th International Conference on Integrated Power Electronics Systems*, Nuremberg, Germany, 2010.

[6] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth and R. C. N. Pilawa-Podgurski, "Design of a GaN-Based Interleaved Nine-Level Flying Capacitor Multilevel Inverter for Electric Aircraft Applications," *IEEE Transactions on Power Electronics,* vol. 35, no. 11, pp. 12153-12165, 2020.

[7] T. Nussbaumer, K. Raggi and J. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 7, pp. 2559-2573, 2009.