Space Radiation Effects on SiC Power Device Reliability

Jean-Marie Lauenstein, Megan C. Casey, and Ray L. Ladbury
Flight Data Systems and Radiation Effects Branch
NASA Goddard Space Flight Center
Greenbelt, MD, USA
jean.m.lauenstein@nasa.gov

Alyson D. Topper, Anthony M. Phan, and Hak S. Kim
Science Systems and Applications, Inc. (work performed for NASA GSFC)
Lanham, MD, USA

***Abstract*—Heavy-ion radiation can result in silicon carbide power device degradation and/or catastrophic failure. Test procedures and data interpretation must consider the impact that heavy-ion induced off-state leakage current increases will have on subsequent single-event effect susceptibility and testability. On orbit, reliable performance in the presence of increased off-state leakage currents due to cumulative ion-induced non-catastrophic single-event effects must be assured over the mission lifetime. This work presents a large body of heavy-ion test data for different diode, power MOSFET, and JFET devices. Susceptibility to single-event effects is compared between SiC and Si power devices. Initial recommendations on heavy-ion radiation test methods for silicon carbide power devices are made and radiation hardness assurance is discussed with the goal of moving one step closer to reliably getting this technology off the ground into a broad array of spacecraft and instruments that will benefit from its unique capabilities.**

***Index Terms*—diode, heavy ion, JFET, power MOSFET, radiation, Schottky diode, silicon carbide, single-event burnout, single-event effects.**

I. Introduction

Next generation aerospace power systems demand high-efficiency power technologies to achieve lower cost and expanded capability. SiC power devices are considered inherently more radiation tolerant than silicon devices [1],[2]. Both the ionization energy and threshold energy for defect formation (atomic bond strength) exceed that for Si. Despite this tolerance to radiation dose [3-8], adoption into space applications is hindered in part by susceptibility to damage from galactic cosmic ray heavy ions [9-17]. Heavy-ion irradiation of SiC power devices in the biased off state results in either catastrophic failure, or at lower voltage, single-event leakage current (SELC) whereby the ion causes thermal damage resulting in a permanent increase in the device leakage current. SELC differs from displacement damage in that it requires ionized charge in a high electric field (e.g., conditions for Joule heating) [9],[10],[18]. The term SELC was introduced by Martinella in [19].

Recently, substantial progress has been made in understanding heavy-ion effects on SiC power devices. The modes of damage will be examined with reference to the underlying mechanisms. Results will be contrasted with effects in silicon power devices under heavy-ion exposure. The impact of these differences on radiation test methodology and reliability will be discussed.

II. Experimental Methods

Heavy-ion test data were taken at the Texas A&M University Cyclotron Facility (TAMU) in air or at Lawrence Berkeley National Laboratory (LBNL) in vacuum. Sample size was typically 2-3 devices per data point. Samples were delidded or decapsulated and a controlled, uniform 1-mil layer of parylene-C was deposited to prevent electrical arcing of the device. Ion beam properties are reported in Table I and account for energy loss to the parylene. Test fluxes ranged from under 10 $cm^{-2}s^{-1}$ to capture effects from individual ion strikes, up to 5×10^{3} $cm^{-2}s^{-1}$. Ion fluence varied based upon the presence and rate of degradation of device leakage currents. When establishing the absence of measurable effects, the beam was shuttered after a fluence of 5×10^{5} $cm^{-2}s^{-1}$.

The irradiation test circuit was compliant with MIL-STD-750 TM1080 [20]. Six DUTs can be mounted on the NASA/GSFC high-voltage power device test board with daughter cards, and individually accessed via dry Reed relays controlled by an Agilent 34907A data acquisition/switch unit. All terminals of the devices not under test are then floating. Parts were electrically characterized at the test facility. In addition, immediately prior to the first and following each irradiation run, either a gate stress test was performed in which the gate leakage current (I_{GSS}) was measured as a function of gate voltage at zero drain-source (V_{DS}) voltage, and the drain-source breakdown voltage (BV_{DSS}) was measured on the transistors, or the DC peak reverse voltage (V_{RRM}) was measured on the diodes. Measurement equipment included a Keithley 2400 current-voltage sourcing and

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measurement instrument (SMU) for gate voltage supply and current measurement (< 1 nA accuracy) and two Keithley 2410 SMUs in series for the drain or cathode voltage supply and current measurement. Breakdown voltages exceeding 1350 V could therefore not be measured. More recent test data were obtained using a Keithley 2635A SMU and Keithley 2657A SMU, thereby raising the upper voltage limit to 3000 V.

Samples were irradiated in air at TAMU or in vacuum at LBNL at normal incidence unless otherwise indicated. For each transistor, the gate-source bias (V_{GS}) was held in its nominal off state; diodes were reverse-biased during irradiation.

TABLE I. HEAVY-ION BEAM PROPERTIES AT DIE SURFACE

Facility	Ion	Energy (*MeV*)	LET (SiC) (*MeV-cm²/mg*)	Range (SiC) (*μm*)
TAMU	Ne	267	2.9	177
	Ar	499	8.9	121
	Ag	1110	49	66
	Xe	1137	64	56
	Xe	1214	62	60
LBNL	B	104	1	198
	Ar	361	11	77
	Cu	566	24	61
	Kr	763	34	63
	Xe	996	66	50

III. SiC DIODE RESULTS

As described by Kuboyama, *et al.*, [10] and shown in Fig. 1, three behaviors can be measured during irradiation of SiC Schottky diodes depending upon the heavy-ion beam conditions, device reverse voltage (V_R), and prior beam exposure: no permanent effects, a permanent increase in leakage current (I_R) or catastrophic single-event burnout (SEB). The threshold for SEB is therefore difficult to identify due to the increasing I_R during irradiation. SELC becomes larger with higher V_R and with heavier ions [21]. The device will reach prohibitively large I_R from cumulative SELCs before adequate sampling of the die for SEB sensitivity can occur—that is, before an acceptable minimum fluence can be reached. Compounding this issue is the impact the prior degradation may have on the threshold V_R at which SEB can occur. An example of prior degradation from heavy ions resulting in a higher measured threshold V_R for SEB can be found in [10].

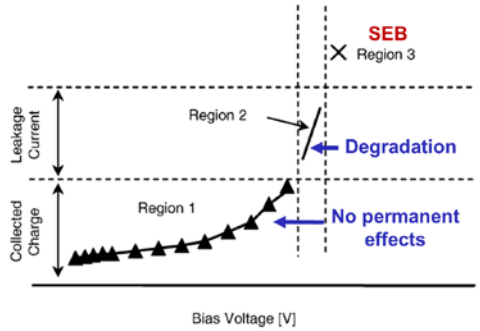

Figure 1. SiC Schottky diode responses to heavy-ion irradiation range from no permanent effect to leakage current degradation to sudden catastrophic single-event burnout (SEB) depending on the reverse bias voltage (V_R) during irradiation. After [10]. © IEEE, 2006.

In the work presented here, three Schottky diodes, each from a different manufacturer and with V_R ratings from 650 V to 1700 V, as well as two PiN diodes with V_R ratings of 1200 V and 3300 V from a fourth manufacturer, were irradiated.

A. SELC

Fig. 2 shows as a function of ion LET the lowest V_R at which I_R measurably degraded during irradiation; error bars indicate uncertainty due to the discrete voltage increment between the highest V_R at which no degradation was measured and the onset of degradation. From Fig. 2, the following conclusions can be made: 1) Onset V_R for degradation is higher for PiN diodes; 2) Onset V_R for degradation is similar for 650 V – 1700 V Schottky diodes or 1200 V and 3300 V PiN diodes; and 3) There is no difference between the Schottky barrier diode (SBD) (D1) and junction barrier Schottky (JBS) diode designs (D2 – D4) in this study.

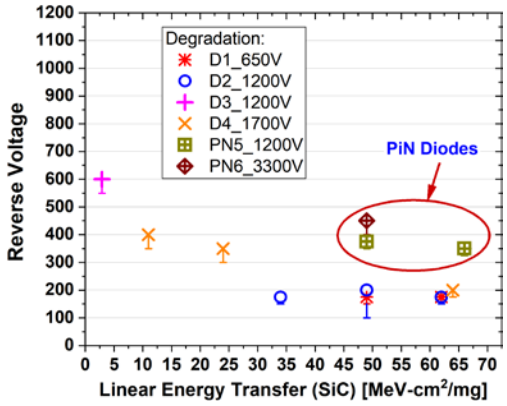

Figure 2. SiC diode V_R at which SELC is measured during irradiation, as a function of LET. Error bars extend to highest V_R at which no degradation was measured.

1) Impact of diode design on SELC

The Schottky contact may contribute an additional mechanism for I_R degradation, as has been suggested in [22-24]. Previous charge collection measurements during irradiation at biases above the threshold for damage indicate charge enhancement that is unaccounted for by the ionization from the heavy ion [9]. In this study, Kamezawa hypothesized that this anomalous charge collection is due to the heat generated by the ionized charge causing additional current across the Schottky contact by charge tunneling and barrier height lowering. This theory is supported by work in [10]. Numerical simulations comparing the heavy-ion response of a JBS diode to that of a PiN diode demonstrate a shift of the peak temperature from the Schottky contact to the p+/n- junction in absence of the Schottky contact, despite the peak electric field occurring at the Ohmic contact [24]. Based

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on these studies, no difference in onset V_R for degradation would be expected between SBD and JBS designs; instead, future analyses should compare SELC cross sections.

2) Independence of SELC onset from voltage rating

The similarity of susceptibility across diodes with different voltage ratings suggests that the electric field strength does not play a primary role in the onset of degradation. Johnson, *et al.*, studied this phenomenon in [25]. Working with Kuboyama's concept of peak power used to normalize the threshold voltage for damage from different ion beams [10], Johnson demonstrates through numerical simulations that the diode active layer may no longer factor into the total instantaneous power. Instead, because of the redistribution of the electric field during an ion strike at a given bias, this total instantaneous power becomes a constant. Johnson's analysis suggests that the threshold voltage for leakage current degradation is only a function of the diode voltage bias, material properties (density, ionization energy, and ambipolar carrier mobility of the ionized charge during the ion strike event), and the ion LET.

B. SEB

Both the Schottky and PiN diodes with different voltage ratings and from different manufacturers experienced immediate SEB at similar fractions of their rated voltages, indicating a strong dependence on the electric field. In Fig. 3, this threshold is plotted as a function of LET; the SEB voltages have been normalized to the measured breakdown voltage as opposed to the rated voltage with the exception of the 650 V Schottky diode, where in the absence of measured data, a conservative 700 V breakdown is assumed. Immediate failure occurs between 30% and 47% of measured breakdown voltage, even at the lowest LET (2.9 MeV·cm^2/mg with 13.4 MeV/u neon). The similarity in SEB susceptibility across SiC diodes with different breakdown voltages has also been shown with neutron-induced failures-in-time studies [26].

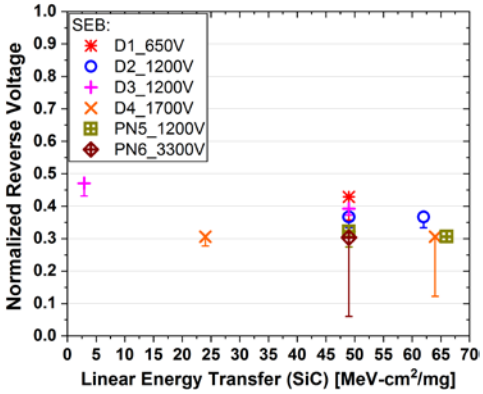

Figure 3. SiC diode V_R at which immediate SEB occurs, normalized to measured breakdown voltage, as a function of LET. Error bars extend down to the highest voltage evaluated at which immediate SEB did not occur.

IV. SiC Power MOSFETs

MOSFETs are susceptible to additional heavy-ion damage effects. The presence of a gate oxide introduces a latent-damage mechanism revealed only on the post-irradiation gate stress (PIGS) test [27-29]. During irradiation under higher drain-source voltage (V_{DS}), two leakage current pathways can degrade: a drain-gate path where the change in drain and gate currents with fluence is equal, and a drain-source leakage current (I_{DS}) pathway [19, 27, 29]. Rather than occurring arbitrarily with V_{DS}, drain-gate leakage current (I_{DG}) degradation always occurs at lower V_{DS} than does I_{DS} degradation, in parts that exhibit both effects. The drain-gate leakage pathway involves the drain neck (JFET) region, and the drain-source pathway involves the body-drain p-n junction [16]. Martinella's MOSFET version of Fig. 1 showing the different regions of response types is given in Fig. 4 [30].

Eight different MOSFETs coming from four different manufacturers and ranging from 900 V to 3300 V were

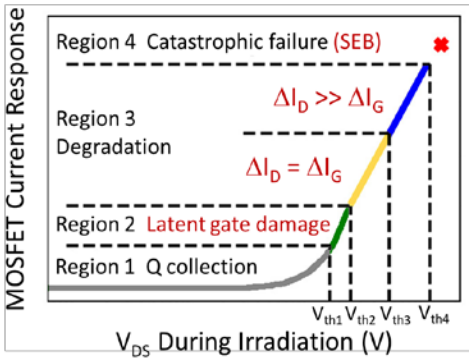

Figure 4. Heavy-ion radiation effects in SiC power MOSFETs as a function of V_{DS} during irradiation include two types of single-event leakage current (SELC), in addition to catastrophic failure. I_D=drain current; I_G=gate current; Q=charge; V_{th}=threshold voltage. Modified from [30] (region labeling changed). Used under CC BY.

evaluated under several beam conditions. Fig. 5 shows a stacked column plot of responses for different ion beam conditions. This figure is described in more detail in the following sections.

A. Latent gate damage

All MOSFETs evaluated exhibited latent damage to the gate oxide at a very low fraction of the rated breakdown voltage (BV_{DSS}), from ions with LET greater than ~10 MeV·cm^2/mg. Although no measurable change in leakage currents is detected during irradiation at 0 V_{GS}, PIGS testing reveals increased gate oxide leakage current (I_{GSS}).

In Fig. 5, the grey bottom portion of the columns indicates V_{DS} regions of no permanent heavy-ion effects; green shows the threshold V_{DS} and range over which only latent gate damage was measured. Color gradients span between known V_{DS} for the given response types. As can be seen, latent damage is 1) dependent on LET, and 2) at higher LETs the threshold becomes independent of device voltage rating and manufacturer. With copper (LET = 24 MeV·cm^2/mg), the difference in onset of latent gate damage for 900 V and 1200 V MOSFETs could be related to voltage rating or to manufacturer differences.

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Not obvious in Fig. 5 but important to bear in mind is that gate damage continues to occur at all voltages higher than the threshold for this latent damage, even as other effects become measurable [27]. Gate rupture can occur during the PIGS test with sufficient fluence.

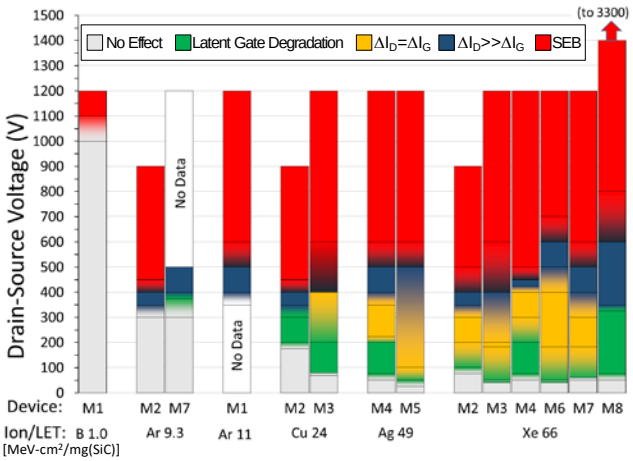

Figure 5. Column plot of SiC MOSFET responses to different ion beams. Solid colored areas indicate V_{DS} ranges for which the following occur: Grey – no permanent effects; Green – only latent gate damage; Yellow – I_{DG} degradation; Blue – I_{DS}-dominated degradation; and Red – catastrophic SEE. Color gradients span between known V_{DS} for given response types.

B. SELC

1) Drain-gate leakage current

Shown by yellow regions of the columns in Fig. 5, irradiation at a higher V_{DS} can result in increasing I_{DG} measurable during the beam run. The damage, although non-catastrophic during the run, can result in a failed PIGS test (typically soft breakdown until the full standard test fluence is delivered; see [31],[32] for detailed analyses of soft vs. hard gate breakdown in silicon MOSFETs). This PIGS failure constitutes single-event gate rupture (SEGR). The I_{DG} leakage degradation mode is not dominant under irradiation with lighter ions – that is, when degradation occurs at lower LETs, the change in drain current exceeds the change in gate current, similar to Mizuta, *et al.*'s findings [16]. Importantly, not all MOSFETs exhibit pronounced I_{DG} degradation even at higher LET, suggesting this mechanism can be mitigated by design.

Evaluation of two generations of SiC power MOSFETs found that the threshold V_{DS} for I_{DG} degradation was higher in the newer generation [30], known to have a smaller cell pitch and thus narrower drain neck region [33]. Narrowing of this region results in a lower gate oxide electric field due to pinch-off of the neck region by the parasitic JFET depletion regions [34]. In addition, this neck width narrowing has been shown in simulations of silicon power MOSFETs to reduce susceptibility to SEGR by facilitating faster charge removal from the oxide interface at the center of the drain neck region [35]. Variability to susceptibility of ion-induced increase in I_{DG} leakage is thus likely to be related to differences in the drain neck width.

2) Drain-source leakage current

At still higher V_{DS} all devices exhibit increasing I_{DS} leakage degradation (Fig. 5, blue regions). This effect can result in degradation of the breakdown voltage (BV_{DSS}) and increased off-state drain leakage current (I_{DSS}). The threshold for this form of SELC was least influenced by device breakdown voltage rating and ion LET, suggesting it may involve material properties of SiC. With the exception of irradiation with the lightest ion (boron), all MOSFETs regardless of voltage rating exhibited this damage at a threshold V_{DS} of around 350 V – 400 V, which is the about the same threshold found for PiN diode leakage current degradation (see Fig. 2). This same voltage threshold was independently identified by Martinella, *et al.* and Abbate, *et al.* in 1200-V SiC MOSFETs [19],[36], where they found a tight distribution between parts of 50 V or less. This tight distribution indicates a mechanism involving device characteristics having minimal variability during fabrication. Microbeam studies demonstrated that the sensitive region for I_{DS} SELC is the p-n junction region formed by the p-body implant and the drain region [30].

C. SEB

As shown by the red regions in Fig. 5, vulnerability to immediate catastrophic failure was present at an LET as low as 1 MeV·cm^2/mg. The threshold voltage for immediate catastrophic SEB saturates quickly with LET; for most MOSFETs, the saturated V_{DS} is only 50% of the rated voltage. As with SEB in the other device types, the mechanism is strongly electric-field dependent.

V. SiC JFETs

Very limited heavy-ion SEE data are available for junction field-effect transistors. We have reported single-event effects on four different trench gate vertical JFETs from two manufacturers [29]. Data are limited to device exposures to argon with an LET of either 5.9 MeV-cm^2/mg or 11 MeV-cm^2/mg. At the higher LET, two enhancement mode designs in which gate and source were grounded during irradiation, and one normally-on design irradiated with V_{GS} = -15 V, exhibited drain-gate leakage current degradation (Fig. 6). Only one of the JFETs showed evidence of possible drain-source leakage current degradation, including I_{DS} current spikes recorded during irradiation (Fig. 7). At the lower LET, there was no measurable leakage current degradation prior to catastrophic failure in the enhancement-mode JFET samples evaluated.

The catastrophic failure mode is less clear. In all failures, both the drain and gate currents hit the power supply compliance; an oscilloscope would be required to identify whether the events occurred simultaneously (SEB between drain and gate nodes), or if a drain-source SEB event damaged the gate. A typical vertical JFET cross section is illustrated in Fig. 8; in the off state, the region between adjacent p+ gate implants becomes fully depleted to pinch off the vertical channel. The pinch-off is asymmetrical because of the contribution from the high drain voltage as compared to the grounded source. Single-event burnout involving the gate/drain p-n junction thus would be favored, although

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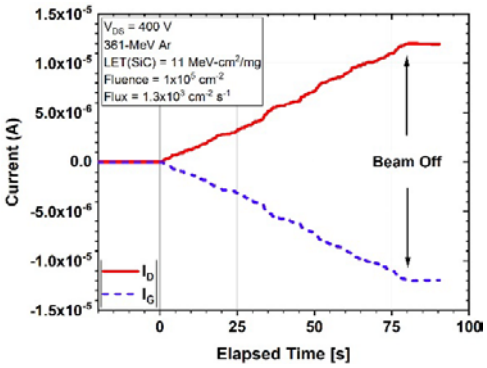

Figure 6. Example striptape data showing increasing I_{DG} leakage in a JFET during heavy-ion irradiation.

drain-source current spikes could be possible when the ion strikes the center of the source, passing between the gates.

Power JFETs exhibit similar responses to heavy-ion irradiation as diodes. One normally-on and three normally-off JFETs were evaluated in this study. The normally-off behavior of the three JFETs is accomplished by device design as opposed to a cascoded configuration. Devices came from two different manufacturers. For these tests, the gate-source voltage (V_{GS}) was held at 0 V for the normally-off devices and at -15 V for the normally-on JFET.

A. SELC

The leakage current degradation thresholds for the four

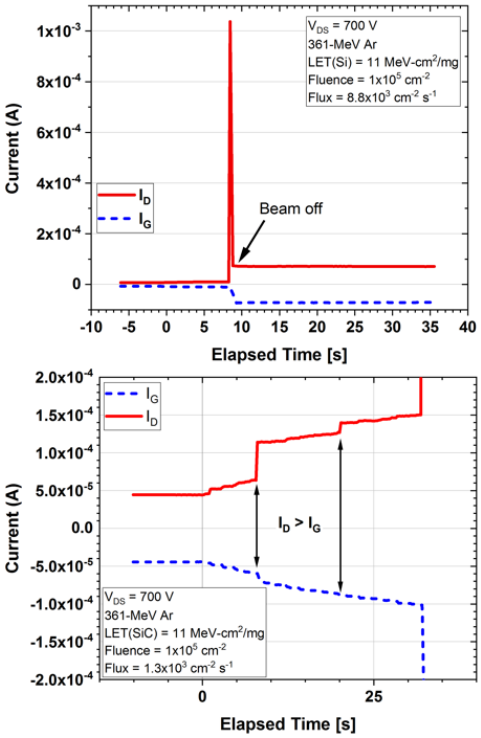

Figure 8. Top: I_{DS} spike during irradiation of 1700 V JFET. At this same bias, this sample catastrophically failed when the beam was turned on again. Bottom: 1700 V JFET sample exhibiting non-catastrophic I_{DS} degradation events prior to failure. Failures in both samples resulted in drain and gate currents hitting supply compliance levels.

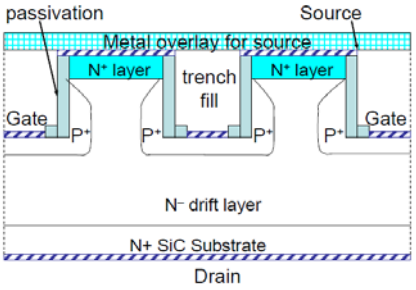

Figure 9. Illustration of a vertical JFET cross section. From [37]. © IEEE, 2005.

JFETs are plotted in Fig. 9, where the columns indicate the voltage range at which no SELC occurred (green and light-grey columns), and the error bars extend to the next step in voltage at which SELC was measured. In the left panel of the plot, thresholds are given in terms of the applied drain-source voltage; the right panel shows these same data normalized to the device voltage rating. From these results, the following conclusions can be made: 1) the threshold V_{DS} for degradation is similar for normally-on and normally-off JFETs evaluated in this study; and 2) there is a greater electric-field dependence of the SELC mechanism than was found for the diodes or for MOSFET drain-source current degradation (I_{DS}), possibly due to the involvement of the gate. However, this difference may also be due to the lower LET used to evaluate the JFET SELC response.

Normally-off devices can have a narrower region between gate trenches and relatively lower doping to enable depletion region overlap at 0 V_{GS} [38], however, these factors would not be expected to influence SEE susceptibility because both normally-on and -off devices are biased to achieve channel pinch-off during irradiation.

Interestingly, in contrast to the diode SELC threshold data in Fig. 2, the 1700 V JFET SELC threshold is higher than that of the 1200 V JFETs; normalization reveals the onset for degradation in all JFET devices evaluated is between 30% and 35% of rated voltage. Data are limited, but if this pattern

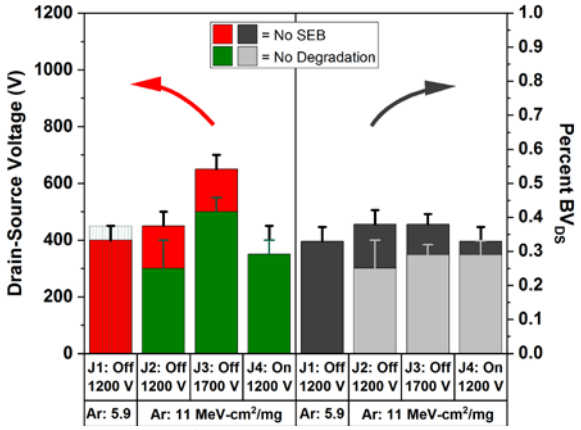

Figure 7. Column plot of SiC JFET maximum V_{DS} at which no leakage current degradation (green and grey columns) or SEB (red and black columns) occurred. No degradation occurred in J1, likely due to the lower LET. Data plotted for absolute V_{DS} (left) and normalized to the device rated breakdown voltage (BV_{DS}, right).

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holds across LETs and other JFET devices, electric field (and epilayer thickness) may be more important in the damage mechanism in this device type.

B. SEB

Fig. 9 shows the voltage range at which no SEB occurs (red and dark grey columns), with error bars extending to the next voltage step at which SEB was detected. SEB occurs at ~40% of the rated voltage for the four JFETs; however, at the relatively low LETs evaluated, JFET SEB was not always immediate and prior current degradation did not seem to impact the susceptibility (Fig. 7). Additional tests are needed at higher LETs typical of device qualification requirements – it is expected that more significant degradation will become a bigger interference with SEB onset evaluation just as with diodes and MOSFETs.

VI. Silicon vs. Silicon Carbide SEE Susceptibility

A. Diodes

SiC Shottky and PiN diode susceptibility to SEB occurs at <50% of avalanche V_R regardless of manufacturer and voltage rating assessed in this work. In contrast, a screen of 45 silicon SBDs from 10 manufacturers using 59 MeV-cm^2/mg Xe found no SEEs when derated to 50% [39]. Almost half of the silicon SBDs passed at 100% of their rated voltage.

SiC power diodes universally exhibit non-catastrophic SELC [9, 10, 14, 17, 21, 29]. In comparison, SELC in silicon SBDs is less common and typically much less severe [39].

B. MOSFETs

Except possibly at lower LETs, SiC power MOSFETs may be less susceptible to SEB than lower-voltage, unhardened, commercial silicon power MOSFETs, as shown in Fig. 10. In this figure, Si data are for MOSFETs rated 50 V to 200 V; higher-voltage Si MOSFET data can be unreliable due to insufficient ion energy (penetration range into the active region). In addition, the silicon data are true SEB thresholds, whereas for SiC, the data are for the threshold at maximum SEB cross section, due to SELC interference in SEB determination at the true V_{DS} threshold [10].

SELC has not been reported in silicon power MOSFETs (leakage in silicon trench MOSFETs is a result of total ionizing dose effects in the gate oxide rather than damage to the silicon crystal). Latent gate oxide damage is found in silicon power MOSFETs. An important distinction between heavy-ion induced gate degradation in Si and SiC MOSFETs is the extremely low V_{DS} necessary for SiC latent damage (≤ 10% of rated BV_{DSS}). Wide bandgap materials can support a much higher electric field than can silicon but the gate SiO_2 maximum field strength is comparable between the two technologies. Per Gauss' law, the oxide field is about three times the field in the semiconductor [40]; therefore, because the field in SiC is typically 10x higher than that in Si, the oxide of the SiC MOSFET can easily exceed its breakdown field strength when a portion of the drain voltage is coupled to the oxide upon a heavy-ion strike [40], [41]. Furthermore, despite the high field that the gate oxide must withstand, the thickness of the oxide is typically thinner than that in a silicon MOSFET in order to maintain capacitive control of the channel.

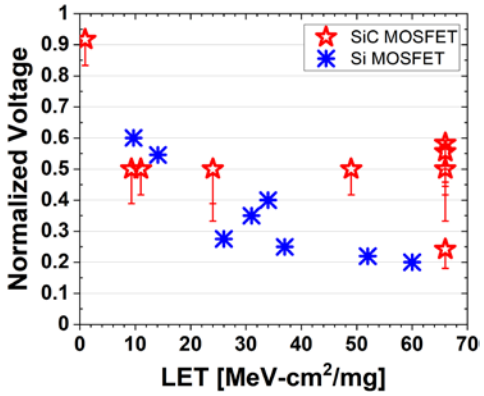

Figure 10. SiC vs. unhardened (commercial) power MOSFET normalized V_{DS} for SEB as a function of LET.

C. JFETs

To date, no single-event effects have been publicly reported in silicon power JFETs, to the best of our knowledge.

VII. Radiation Hardness Assurance

A. Heavy-Ion Radiation Test Method Recommendations

1) Test standards for silicon power devices

Silicon power device test methods such as [20],[42] are based on decades of test data and research into the mechanisms of failure. An overview of key elements is provided for context. In Si MOSFET testing, ion beam angle and energy are chosen for worst-case response – typically at normal incidence to the die surface with an energy that places the ion Bragg peak at the epitaxial layer/substrate interface. Standard heavy-ion test fluence is between 10^5 cm^{-2} and 10^7 cm^{-2}. Test data define an SEB or SEGR response curve for the device that delineates a safe operating voltage area for the given ion beam conditions. For SEB in silicon MOSFETs, protective-mode testing can be used to obtain statistically significant cross-section curves for rate estimation. As indicated in the test methods, colder temperature typically increases susceptibility to SEB due to increased impact ionization; SEGR is not sensitive to temperature to first order.

2) Recommended SiC test practices

a) Beam selection

In addition to mission requirement ion beam conditions, consider lighter ion/lower LET tests to aid on-orbit risk assessments and reveal differences between parts. Normal incidence is likely the worst case [43], [29].

b) Fluence

Ion fluence should be dictated by test goals and the degradation response of the device. Non-catastrophic damage can *increase* the threshold voltage of SEB. Identification of the threshold voltage yielding the maximum cross section for SEB will likely be identified instead of the threshold defining a true SEB safe operating area for the device. In contrast, the

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rate of degradation of leakage current is not dependent on prior history until the rate is no longer constant with fluence.

c) Temperature

The susceptibility of SEB with temperature is unknown for SiC power devices. Unlike in silicon, impact ionization is hole driven. Some data suggest the non-catastrophic degradation rate increases with temperature [28]. For applications intending to operate at high or low temperature, SEE tests should be performed at several temperatures to identify trends in the effects.

B. SEE Risk Assessment

1) Failure rate prediction

Failure rate prediction methods developed (but unvalidated) for Si and SiC power devices may provide an upper bound for on-orbit SEEs. Additional margin should be given for uncertainty of SiC SEB voltage threshold. In addition, the steradian window of vulnerability may change with voltage (see [43]). For applications whose risk posture allows early adoption of this new technology, derating margin and unpowered redundancy is advisable.

2) Reliability uncertainty

Radiation hardness assurance must go beyond calculations of SEB likelihood, due to heavy ion induced permanent degradation effects. Latent gate damage and SELC are cumulative and depend upon both the device bias condition and the properties of the ions striking the device. Estimations of leakage current degradation can be determined experimentally or modeled (*e.g.* [22]), and the impact on device power loss and system efficiency evaluated. The most important unanswered question is how heavy ion induced non-catastrophic damage will affect overall risk of flying SiC power devices in space. This uncertainty includes the impact of degradation on device lifetime, and on subsequent heavy ion induced catastrophic failure. For example, although prior degradation can increase the threshold voltage necessary for SEB [10], electrical aging of a SiC MOSFET can increase susceptibility to ion-induced failure [44]. Application temperature and functional lifetime requirements should be considered. Life tests of damaged parts may reveal higher-likelihood failure modes but sample size will limit discovery of rarer modes.

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REFERENCES

[1] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Trans Electron Devices*, vol. 36, pp. 1811-1823, 1989.

[2] C. Zetterling, "Present and future applications of Silicon Carbide devices and circuits," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, 2012, pp. 1-8.

[3] J. M. McGarrity, F. B. McLean, W. M. DeLancey, J. Palmour, C. Carter, J. Edmond, *et al.*, "Silicon carbide JFET radiation response," *IEEE Trans Nucl Sci*, vol. 39, pp. 1974-1981, 1992.

[4] S. K. Dixit, S. Dhar, J. Rozen, S. Wang, R. D. Schrimpf, D. M. Fleetwood, *et al.*, "Total Dose Radiation Response of Nitrided and Non-nitrided SiO_2/4H-SiC MOS Capacitors," *IEEE Trans Nucl Sci*, vol. 53, pp. 3687-3692, 2006.

[5] R. D. Harris, "SiC vs. Si for High Radiation Environments," in *2007 IEEE Radiation Effects Data Workshop*, 2007, pp. 63-67.

[6] Z. Cher Xuan, Z. En Xia, D. M. Fleetwood, R. D. Schrimpf, S. Dhar, R. Sei-Hyung, *et al.*, "Effects of Bias on the Irradiation and Annealing Responses of 4H-SiC MOS Devices," *IEEE Trans Nucl Sci*, vol. 58, pp. 2925-2929, 2011.

[7] A. Akturk, J. M. McGarrity, S. Potbhare, and N. Goldsman, "Radiation Effects in Commercial 1200 V 24 A Silicon Carbide Power MOSFETs," *IEEE Trans Nucl Sci*, vol. 59, pp. 3258-3264, 2012.

[8] P. Hazdra and S. Popelka, "Radiation resistance of wide-bandgap semiconductor power transistors," *physica status solidi (a)*, vol. 214, p. 1600447, 2017.

[9] C. Kamezawa, H. Sindou, T. Hirao, H. Ohyama, and S. Kuboyama, "Heavy ion-induced damage in SiC Schottky barrier diode," *Physica B: Condensed Matter*, vol. 376–377, pp. 362-366, 4/1/ 2006.

[10] S. Kuboyama, C. Kamezawa, N. Ikeda, T. Hirao, and H. Ohyama, "Anomalous Charge Collection in Silicon Carbide Schottky Barrier Diodes and Resulting Permanent Damage and Single-Event Burnout," *IEEE Trans Nucl Sci*, vol. 53, pp. 3343-3348, 2006.

[11] S. Kuboyama, C. Kamezawa, Y. Satoh, T. Hirao, and H. Ohyama, "Single-Event Burnout of Silicon Carbide Schottky Barrier Diodes Caused by High Energy Protons," *IEEE Trans Nucl Sci*, vol. 54, pp. 2379-2383, 2007.

[12] S. Onoda, T. Makino, N. Iwamoto, G. Vizkelethy, K. Kojima, S. Nozaki, *et al.*, "Charge Enhancement Effects in 6H-SiC MOSFETs Induced by Heavy Ion Strike," *IEEE Trans Nucl Sci*, vol. 57, pp. 3373-3379, 2010.

[13] T. Makino, M. Deki, N. Iwamoto, S. Onoda, N. Hoshino, H. Tsuchida, *et al.*, "Heavy-Ion Induced Anomalous Charge Collection From 4H-SiC Schottky Barrier Diodes," *IEEE Trans Nucl Sci*, vol. 60, pp. 2647-2650, 2013.

[14] C. Abbate, G. Busatto, P. Cova, N. Delmonte, F. Giuliani, F. Iannuzzo, *et al.*, "Thermal damage in SiC Schottky diodes induced by SE heavy ions," *Microelectron Reliab*, vol. 54, pp. 2200-2206, 2014.

[15] M. Deki, T. Makino, N. Iwamoto, S. Onoda, K. Kojima, T. Tomita, *et al.*, "Linear energy transfer dependence of single event gate rupture in SiC MOS capacitors," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 319, pp. 75-78, 2014.

[16] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of Single-Event Damages on Silicon Carbide (SiC) Power MOSFETs," *IEEE Trans Nucl Sci*, vol. 61, pp. 1924-1928, 2014.

[17] C. Abbate, G. Busatto, P. Cova, N. Delmonte, F. Giuliani, F. Iannuzzo, *et al.*, "Analysis of Heavy Ion Irradiation Induced Thermal Damage in SiC Schottky Diodes," *IEEE Trans Nucl Sci*, vol. 62, pp. 202-209, 2015.

[18] E. C. Auden, R. A. Weller, R. D. Schrimpf, M. H. Mendenhall, R. A. Reed, N. C. Hooten, *et al.*, "Effects of High Electric Fields on the Magnitudes of Current Steps Produced by Single Particle Displacement Damage," *IEEE Trans Nucl Sci*, vol. 60, pp. 4094-4102, 2013.

[19] C. Martinella, R. Stark, T. Ziemann, R. G. Alia, Y. Kadi, U. Grossner, *et al.*, "Current Transport Mechanism for Heavy-Ion Degraded SiC MOSFETs," *IEEE Trans Nucl Sci*, vol. 66, pp. 1702-1709, 2019.

[20] "MIL-STD-750: Test Methods for Semiconductor Devices: TM1080: Single-Event Burnout and Single-Event Gate Rupture," Nov 2019

[21] A. Javanainen, K. F. Galloway, C. Nicklaw, A. L. Bosser, V. Ferlet-Cavrois, J.-M. Lauenstein, *et al.*, "Heavy Ion Induced Degradation in SiC Schottky Diodes: Bias and Energy Deposition Dependence," *IEEE Trans Nucl Sci*, vol. 64, pp. 415-420, 2017.

[22] A. Javanainen, K. F. Galloway, V. Ferlet-Cavrois, J.-M. Lauenstein, F. Pintacuda, R. D. Schrimpf, *et al.*, "Charge Transport Mechanisms in Heavy-Ion Driven Leakage Current in Silicon Carbide Schottky Power Diodes," *IEEE Trans Dev Mater Rel*, vol. 16, pp. 208-212, 2016.

[23] A. F. Witulski, R. D. Schrimpf, A. L. Sternberg, K. F. Galloway, A. Raman, R. Arslanbekov, *et al.*, "Single Event Burnout of High-Voltage SiC Junction Barrier Schottky Diodes," *Submitted to IEEE Transactions on Nuclear Science*, 2017.

[24] S. Kuboyama, E. Mizuta, Y. Nakada, H. Shindou, A. Michez, J. Boch, *et al.*, "Thermal Runaway in SiC Schottky Barrier Diodes Caused by Heavy Ions," *IEEE Trans Nucl Sci*, vol. 66, pp. 1688-1693, 2019.
[25] R. A. Johnson, A. F. Witulski, D. R. Ball, K. F. Galloway, A. L. Sternberg, E. Zhang, *et al.*, "Enhanced Charge Collection in SiC Power MOSFETs Demonstrated by Pulse-Laser Two-Photon Absorption SEE Experiments," *IEEE Trans Nucl Sci*, vol. 66, pp. 1694-1701, 2019.
[26] A. Akturk, J. M. McGarrity, N. Goldsman, D. Lichtenwalner, B. Hull, D. Grider, *et al.*, "Terrestrial Neutron-Induced Failures in Silicon Carbide Power MOSFETs and Diodes," *IEEE Trans Nucl Sci*, vol. 65, pp. 1248-1254, 2018.
[27] C. Abbate, G. Busatto, D. Tedesco, A. Sanseverino, L. Silvestrin, F. Velardi, *et al.*, "Gate Damages Induced in SiC Power MOSFETs During Heavy-Ion Irradiation--Part I," *IEEE Trans Electron Devices*, vol. 66, pp. 4235-4242, 2019.
[28] S. A. Ikpe, J. M. Lauenstein, G. A. Carr, D. Hunter, L. L. Ludwig, W. Wood, *et al.*, "Long-term reliability of a hard-switched boost power processing unit utilizing SiC power MOSFETs," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, pp. ES-1-1-ES-1-8.
[29] J.-M. Lauenstein, "Getting SiC Power Devices Off the Ground: Design, Testing, and Overcoming Radiation Threats," in *Microelectronics Reliability and Qualification Workshop (MRQW)*, El Segundo, CA, 2018. Available at: https://aerospace.org/MRQW.
[30] C. Martinella, T. Ziemann, R. Stark, A. Tsibizov, K. O. Voss, R. G. Alia, *et al.*, "Heavy-Ion Microbeam Studies of Single-Event Leakage Current Mechanism in SiC VD-MOSFETs," *IEEE Trans Nucl Sci*, vol. 67, pp. 1381-1389, 2020.
[31] N. Ikeda, S. Kuboyama, Y. Satoh, and T. Tamura, "Study of Latent Damage in Power MOSFETs Caused by Heavy Ion Irradiation," *IEEE Trans Nucl Sci*, vol. 55, pp. 3388-3393, 2008.
[32] S. Kuboyama, E. Mizuta, Y. Nakada, and H. Shindou, "Physical Analysis of Damage Sites Introduced by SEGR in Silicon Vertical Power MOSFETs and Implications for Postirradiation Gate-Stress Test," *IEEE Trans Nucl Sci*, vol. 66, pp. 1710-1714, 2019.
[33] D. Grider, "Recent Advances in 900 V to 10 kV SiC MOSFET Technology," presented at the NEPP Electron Technol Workshop Greenbelt, MD, Jun 15, 2016. Online: https://nepp.nasa.gov/workshops/etw2016/talks.cfm.
[34] B. J. Baliga, *Silicon Carbide Power Devices*. New Jersey: World Scientific, 2005.
[35] J. L. Titus, S. Yen-Sheng, M. W. Savage, R. V. Mickevicius, and C. F. Wheatley, "Simulation study of single-event gate rupture using radiation-hardened stripe cell power MOSFET structures," *IEEE Trans Nucl Sci*, vol. 50, pp. 2256-2264, 2003.
[36] C. Abbate, G. Busatto, S. Mattiazzo, A. Sanseverino, L. Silvestrin, D. Tedesco, *et al.*, "Progressive drain damage in SiC power MOSFETs exposed to ionizing radiation," *Microelectron Reliab*, vol. 88-90, pp. 941-945, 2018/09/01/ 2018.
[37] J. Lai, H. Yu, J. Zhang, P. Alexandrov, Y. Li, J. H. Zhao, *et al.*, "Characterization of normally-off SiC vertical JFET devices and inverter circuits," in *Fourtieth IAS Annual Meeting Conference Record of the 2005 Industry Applications Conference, 2005.*, 2005, pp. 404-409 Vol. 1.
[38] M. Bakowski, "Prospects and Development of Vertical Normally-off JFETs in SiC," *Journal of telecommunications and information technology*, pp. 25-36, 2009.
[39] M. C. Casey, J. M. Lauenstein, R. L. Ladbury, E. P. Wilcox, A. D. Topper, and K. A. LaBel, "Schottky Diode Derating for Survivability in a Heavy Ion Environment," *IEEE Trans Nucl Sci*, vol. 62, pp. 2482-2489, 2015.
[40] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed. New York: Springer International Publishing AG, 2019.
[41] C. Abbate, G. Busatto, D. Tedesco, A. Sanseverino, F. Velardi, and J. Wyss, "Gate Damages Induced in SiC Power MOSFETs During Heavy-Ion Irradiation--Part II," *IEEE Trans Electron Devices*, vol. 66, pp. 4243-4250, 2019.
[42] JESD57A, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation." Arlington, VA: JEDEC Solid State Technology Association, 2017.
[43] A. Javanainen, M. Turowski, K. F. Galloway, C. Nicklaw, V. Ferlet-Cavrois, A. Bosser, *et al.*, "Heavy-Ion-Induced Degradation in SiC Schottky Diodes: Incident Angle and Energy Deposition Dependence," *IEEE Trans Nucl Sci*, vol. 64, pp. 2031-2037, 2017.
[44] K. Niskanen, A. D. Touboul, R. C. Germanicus, A. Michez, A. Javanainen, F. Wrobel, *et al.*, "Impact of Electrical Stress and Neutron Irradiation on Reliability of Silicon Carbide Power MOSFET," *IEEE Trans Nucl Sci*, vol. 67, pp. 1365-1373, 2020.