Jet Propulsion Laboratory
California Institute of Technology

Oh, The Shape We're In

Module 10:

The Future of Electronics Single Event Effects (SEE) Testing

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SSAI, Inc., work performed for NASA-GSFC

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Acronyms

Three Dimensional (3D)
Aluminium (Al)
Atomic Layer Deposition (ALD)
Aluminium Gallium Nitride (AlGaN)
Berkeley Accelerator for Space Effects (BASE)
Berkeley National Laboratories (BNL)
Bump Plating Photoresist (BPR)
Complementary Metal Oxide Semiconductor (CMOS)
Chemical Mechanical Polishing (CMP)
Commercial Off The Shelf (COTS)
Central Processing Unit (CPU)
Chip to Wafer (CtW)
Double Data Rate (DDR)
Dual Inline Packages (DIPs)
Dynamic Random Access Memory (DRAM)
Design Technology Co-Optimization/Synthesis Technology Co-Optimization (DTCO/STCO)
European Union (E.U.)
Electron Cyclotron Resonance Ion Source (ECRIS)
Electromagnetic (EM)
Extreme Ultraviolet Lithography (EUV)
Ferroelectric Field Effect Transistor (FeFET)
Field Effect Transistors (FETs)
Fin Field-Effect Transistor (FinFET)
Fully Self Aligned Via (FSAV)
Ferroelectric Tunnel Junction (FTJ)
Gate All Around (GAA)
Gallium Arsenide (GaAs)
Gallium Nitride (GaN)
Gallium Oxide (GaO)
Germanium (Ge)
High Bandwidth Memory (HBM)
High-Electron-Mobility Transistor (HEMT)
Hybrid Memory Cube (HMC)
Integrated Circuit (IC)
Indium Gallium Arsenide Phosphide (InGaAsP)
Indium phosphide (InP)
Internet Protocol (IP)
Vanderbilt-ISDE (ISDE)
Jyvaskyla Accelerator Laboratory (JYFL)
Josephson Junction (JJ)
University of Jyvaskala (Jyvaskala)
Lawrence Berkeley National Laboratories (LBNL)
Light-Emitting Diodes (LEDs)
Linear Energy Transfer (LET)
Layered Lithium Niobium Oxide (LiNbO2)
LASER Ion Source (LIS)
Low Normalized Pressure Thermoconductivity (Low po (lamda)) Metals
Low-Voltage Differential Signaling (LVDS)
Modeling And Simulation (M&S)
Magnetic Shielding (Mag.)
Mixed Axial and Radial field System (MARS)
Model Based Mission Assurance (MBMA)
Microelectromechanical Structure (MEMS)
Mott-Insulator Based Field Effect Transistor (Mott FET)
Multiplexer/Demultiplexer (MUX/DEMUX)
National Aeronautics and Space Administration (NASA)
Negative Capacitance Field Effect Transistor (NCFET)
Nanoelectromechanical Systems (NEMS)
Nuclear and Space Radiation Effects Conference (NSREC)
NASA Space Radiation Lab (NSRL)
Optical Input/Output (I/O)
Peripheral Component Interconnect Express (PCIe)
Phase Change Memory (PCM)
Photonic Integrated Circuit (PIC)
Phase-Locked Loop (PLL)
Packaging Research Center (PRC) at Georgia Tech
Random Access Memory (RAM)
Redistribution Layer (RDL) Scaling and Mold
Resistive Random Access Memory (ReRAM)
Radio Frequency (RF)
Rad hard by design (RHBD)
Self-Aligned Gate Contact (SAGC)
Single Diffusion Break (SDB)
Single Event Burnout (SEB)
Single Event Effects (SEE)
Single Event Effect Criticality Analysis (SEECA)
Single Event Functional Interrupt (SEFI)
Single Event Gate Rupture (SEGR)
Soft Error Rate (SER)
Single-Electron Transistor (SET)
Single Event Upset (SEU)
Single-Flux-Quantum (SFQ) Interconnect
Silicon (Si)
Silicon Carbide (SiC)
Silicon-Germanium (SiGe)
Silicon Nitride (SiN)
silicon dioxide (SiO2)
System On A Chip (SOC)
Silicon-on-Insulator (SOI)
Silicon On Sapphire (SOS)
Single-Photon Absorption (SPA)
Static Random-Access Memory (SRAM)
Super-steep Slope (SS)
Steep Switching (SS) Devices
Michigan State University, Superconducting Cyclotron Laboratory (SUSSI)
Shortening vs Voltage (SV)
Size, Weight, and Power (SWaP)
Texas A&M University (TAMU)
Tunnel Field Effect Transistor (TFET)
Two-Photon Absorption (TPA)
Through Silicon Via/Through Mold Via/Through Die Via (TSV/TMV/TDV)
Under Secretary General (USG)
Wafer-To-Wafer (WTW) Stack

Outline

- Then and Now and Wow!
  - What's Changed Since SEE Testing Started
- The Future of Semiconductor Technology
- The Future of Semiconductor Packaging and Device Integration
- But Wait a Minute!
- Space Systems of Tomorrow
- Heavy Ions and Supply Side Economics
- The Future of Heavy Ion Facilities
- Reducing the Demand: Protons as a Screen (and not a Surrogate)
- The Future of Alternate Test Facilities – Lasers and X-Rays
- Optimizing SEE Testing via Model Based Mission Assurance (MBMA)
- Improving Test Efficiency and Performance
- System Testing
- The Future of Modeling for SEE Testing
- And a Few More…

BLUF: We'll Still Need TAMU ☺

Back Then…

- Devices were simple
  - Transistors
  - Memory Arrays (4 kb SRAM!),8 bit CPUs, and so forth…
  - High speed was 10 MHz operation
- Technologies were large and mostly silicon
  - >0.5 um (some >2.0um) CMOS feature size
  - GaAs was emerging; RH was silicon on sapphire (SOS)
- Device packaging
  - Planar
  - Ceramic and a little plastic
  - Through-hole packages (i.e. Dual Inline Packages (DIPs))…

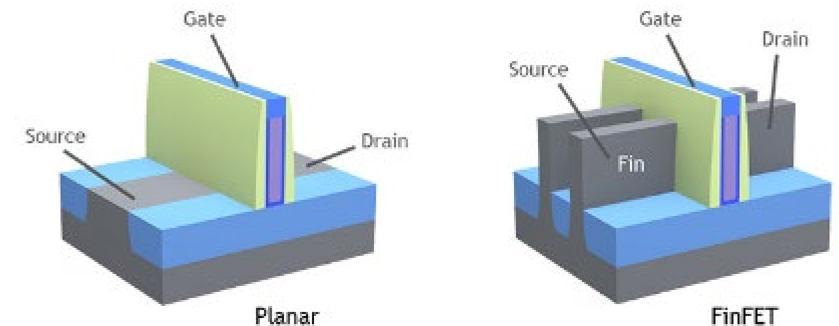
650x Processor
8 um feature size (not a typo) – ~1975
» 8-bit CPU
» Up to 14 MHz
» 64 KB RAM
» 256 bytes stack
» No I/O ports
» 28 or 40-pin DIP

Ken's first CPU!

For SEE testing – it was easy to access to the die (delidding) with limited SEE signatures (homogeneous devices)

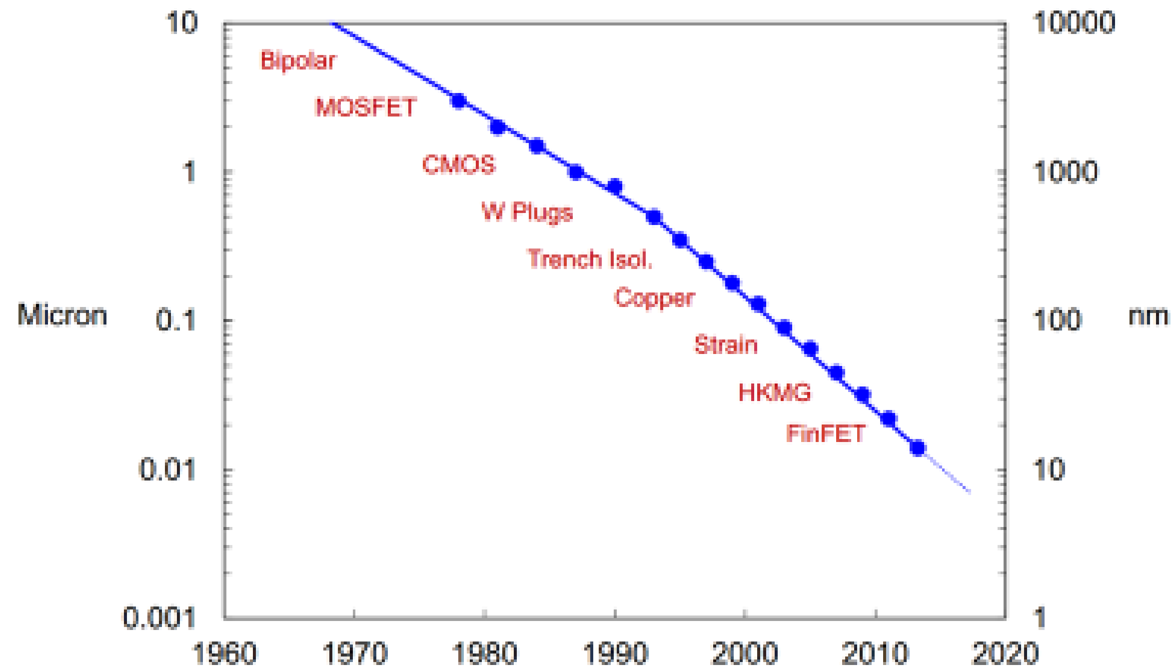
And Now

- Devices are not simple (though “glue” is still needed)
  - FPGAs, Multi-core SOCs
  - >>Gbit Memories (with built-in voltage conversion and microcontrollers)
  - Extreme resolution or operating speeds and integration (single devices replacing a whole card of devices from a decade or two earlier)
- Technologies are
  - <10nm CMOS feature size
  - Proliferation of widebandgap (power, RF)
  - Fins and silicon-on-insulator (SOI) are in!
    - » Rad hard = by design (RHBD)
- Device packaging
  - Mix of planar (old school) and multi-dimensional (2/5/3D) packaging



Courtesy Lam Research Corp.
https://blog.lamresearch.com/tech-brief-finfet-fundamentals/

(EP1) Moore's Law Challenges Below 10nm: Technology, Design and Economic Implications



Process/device innovation has always been an indispensable part of scaling

www.intel.com

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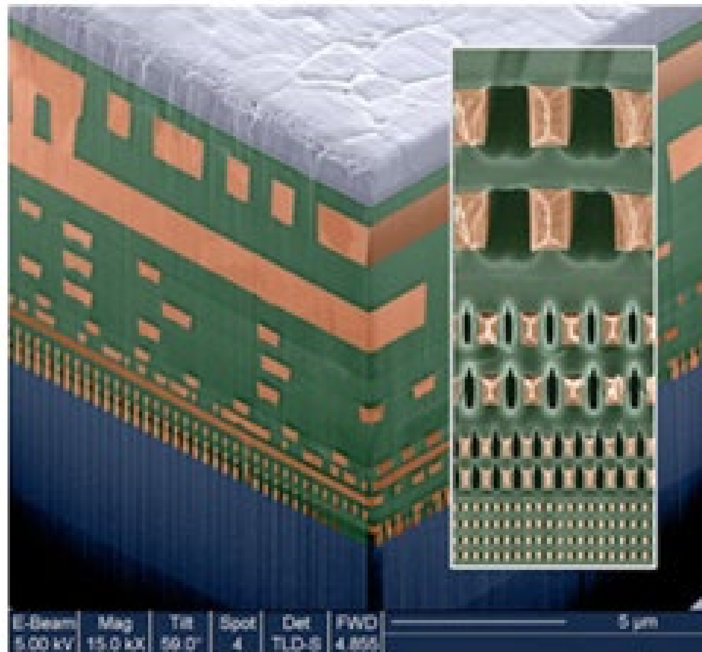
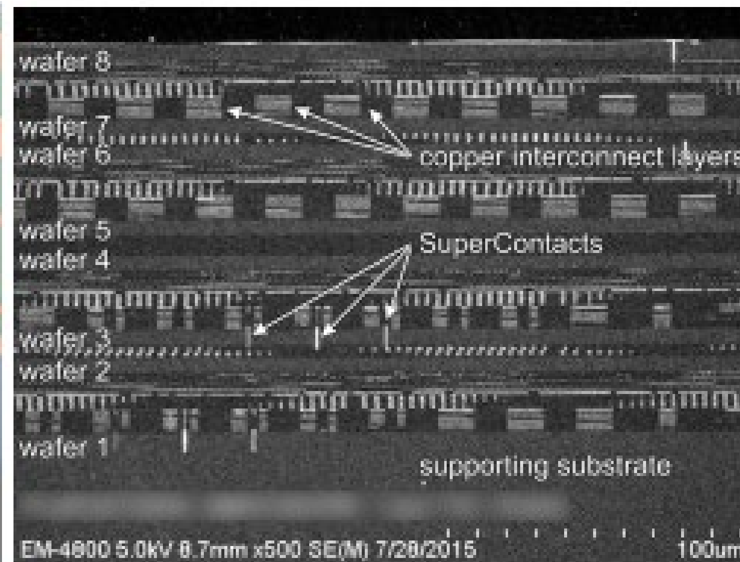
Material and topology changes are part of the "process"

Courtesy of Daniel Fleetwood, IEEE NSREC 2020 Short Course

Devices in 2020 are more 3-dimensional, more complex, and include more kinds of materials than devices before ~2000



http://images.dailytech.com/nimage/4621_21476.jpg



https://tezzaron.com/tezzaron-announces-worlds-first-eight-layer-active-wafer-stack/

Dimensionality issues make it harder to get the ion to the sensitive areas, provide challenges for fault isolation, and complicate data analyses

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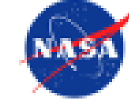
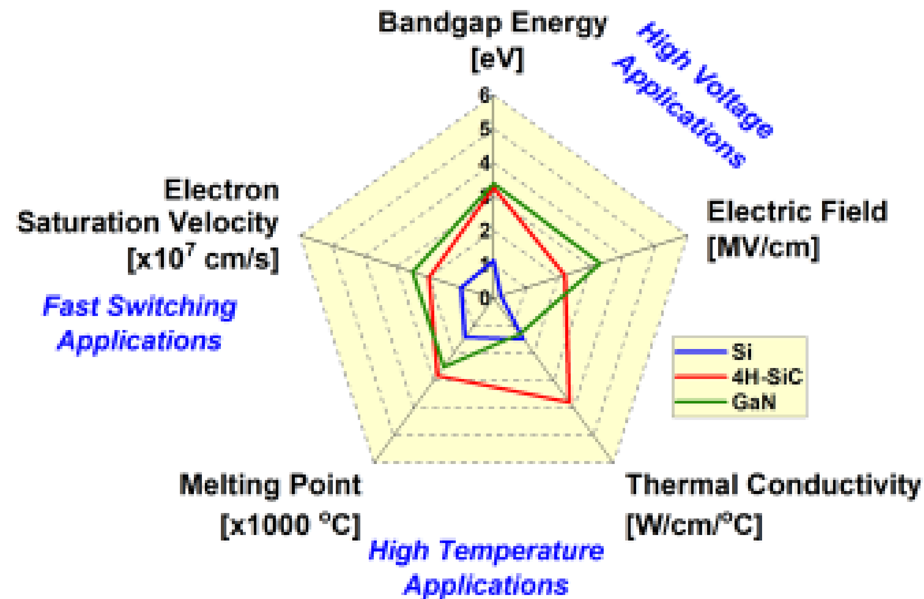
Courtesy of Daniel Fleetwood, IEEE NSREC 2020 Short Course

Widebandgap

A Closer Look: GaN vs. SiC vs. Si





To date, GaN's upper limit on voltage rating is dictated primarily by device reliability issues

To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020

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Widebandgap is now widely used in applications like automotive power and RF: improving efficiency and performance

Courtesy of Jean Marie Lauenstein, IEEE NSREC 2020 Short Course

THE FUTURE OF SEMICONDUCTOR TECHNOLOGY

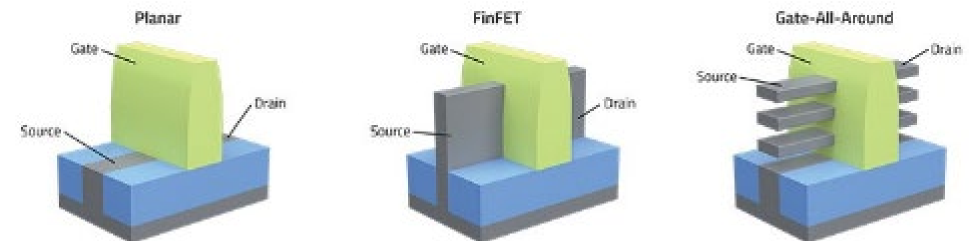
Beyond Tomorrow

- Devices are
  - Multi-technology (e.g., integrated optics)
  - New architectures (gate all around – GAA, nanowires,…)
  - Will increased integration ever stop? AI, robotics,…
    - Keyword: heterogeneous
- Technologies silicon and ?
  - A few electrons only needed to switch states
  - Use of SiGe, graphene, carbon nanotubes
- Device packaging
  - Integration, integration, integration

The crystal ball gets fuzzy (logic)!

- "The Cerebras Wafer-Scale Engine is massive any way you slice it. The chip is 8.5 inches to a side and houses 1.2 trillion transistors."
- "This wafer-scale chip contains almost 400,000 processing cores. Each core is connected to its own dedicated memory and its four neighboring cores."

https://singularityhub.com/2020/11/22/the-trillion-transistor-chip-that-just-left-a-supercomputer-in-the-dust/



Courtesy Lam Research Corp.
https://blog.lamresearch.com/tech-brief-finfet-fundamentals/

Sub 10nm CMOS

- CMOS scaling is focusing more and more on low voltages, cost-effective processes, and high performance to meet the requirements of high-end mobile applications.
  - Materials: Pure silicon-based channels are being replaced with silicon-germanium (SiGe) or germanium (Ge), and III-V materials, because they have better mobility
  - Device shape: Changing, from simple fin-like structures to alternates like GAA, fully depleted on insulator fins, or nanowire FETs

SEE Testing implications:

- **Material interactions/charging/track structure**
- **Continued angular concerns**
- **Increased speed (SETs) and lower critical charges**

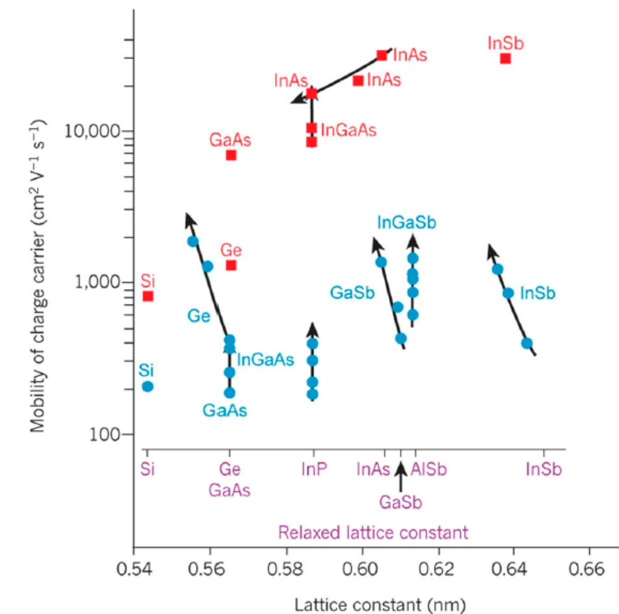


Figure 3. Carrier mobility in inversion layers and quantum wells in Si, Ge, and III-V compounds. Red symbols represent electron mobility and blue ones are marked for hole mobility. The electron mobility in the compounds shown in the plots are much higher than that in Si and Ge [50].

State of the Art and Future Perspectives in Advanced CMOS Technology, Radamson, et al Nanomaterials 2020, 10, 1555; doi:10.3390/nano10081555

Semiconductor Future in One Slide

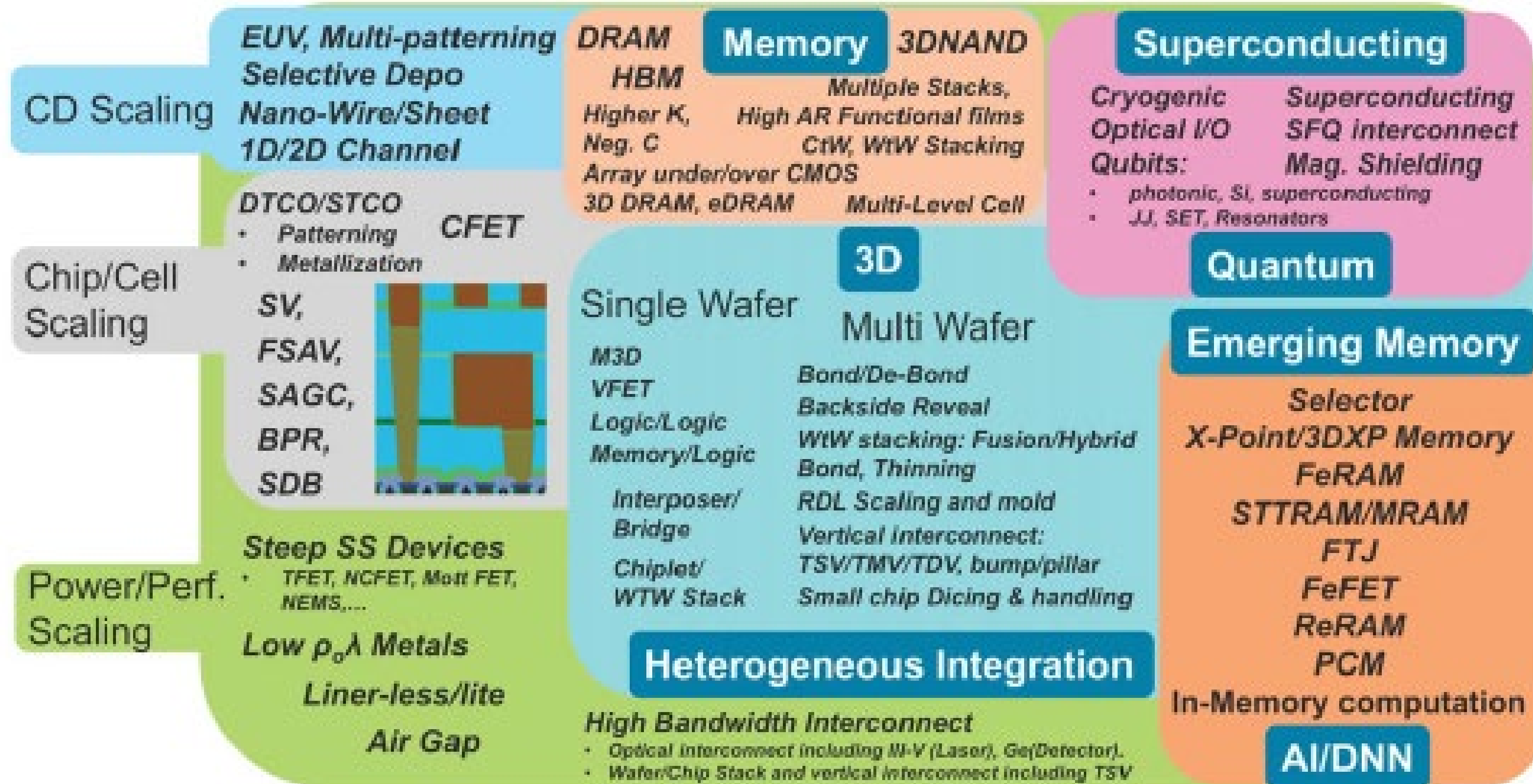


Figure 5.9: Drivers and technologies for better power, performance, area, and cost Scaling[SM] (courtesy of Robert Clark, Tokyo Electron)

https://www.src.org/about/decadal-plan/ Full Report

Changing materials, transistor topologies, and mechanisms: How will they react to heavy ion charge generation and interactions?

Heterogeneous Devices

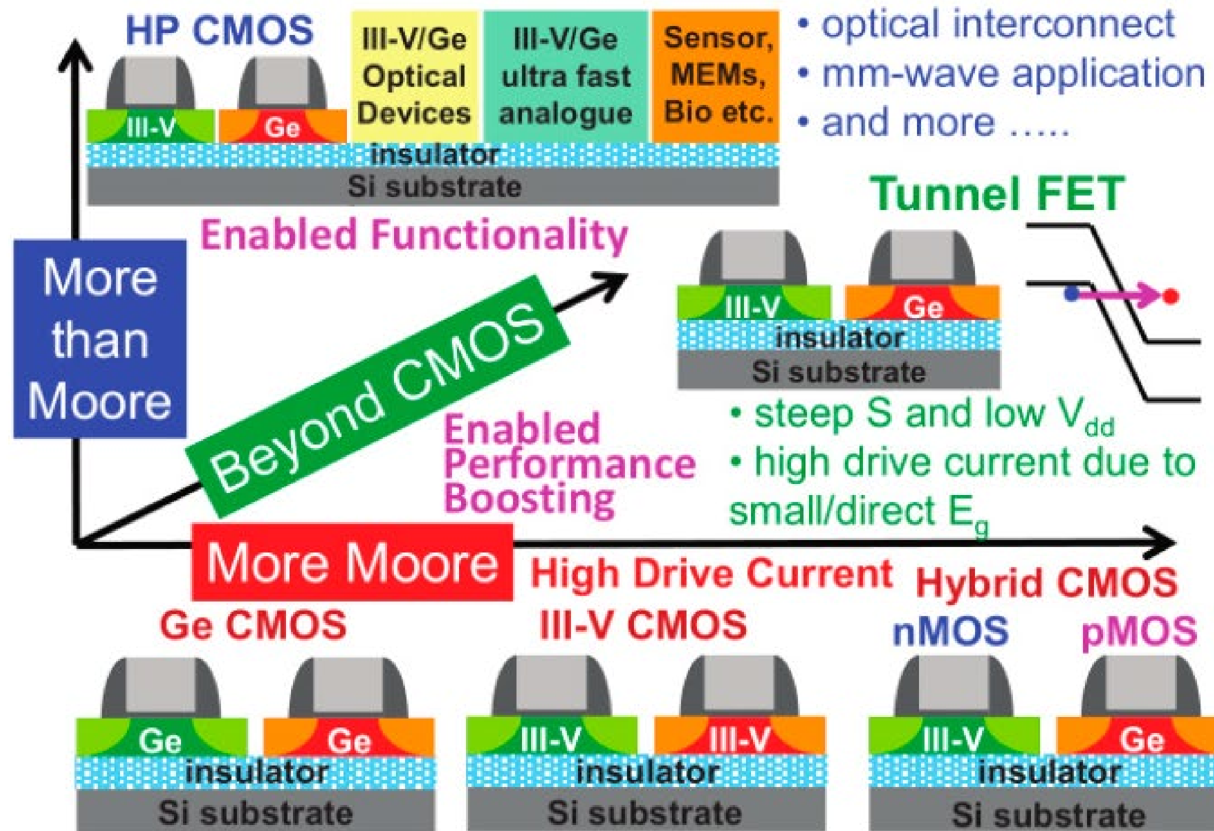


Figure 49. Possible evolution scenario for III–V/Ge devices on Si platform through heterogeneous integration [343].

State of the Art and Future Perspectives in Advanced CMOS Technology, Radamson, et al
Nanomaterials 2020, 10, 1555; doi:10.3390/nano10081555

Convergence of technologies, topologies, speed, power, and integration

Transistor Pathway

n22, n14 → **Si FinFET**

n10, n7 → **Si/Ge FinFET**

n5, n3

Si/Ge Gate All Around (GAA) Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET

Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

Vertical TFET

Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP

Gate, Fin, STI Oxide, Silicon Substrate, New Fin Material, Ge Fin, SiGe SRB, III/V Fin, III/V SRB

Borrowed from Applied Materials

APPLIED MATERIALS

3 External Use

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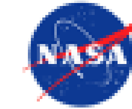
http://www.extremetech.com/computing/162376-7nm-5nm-3nm-the-new-materials-and-transistors-that-will-take-us-to-the-limits-of-moores-law

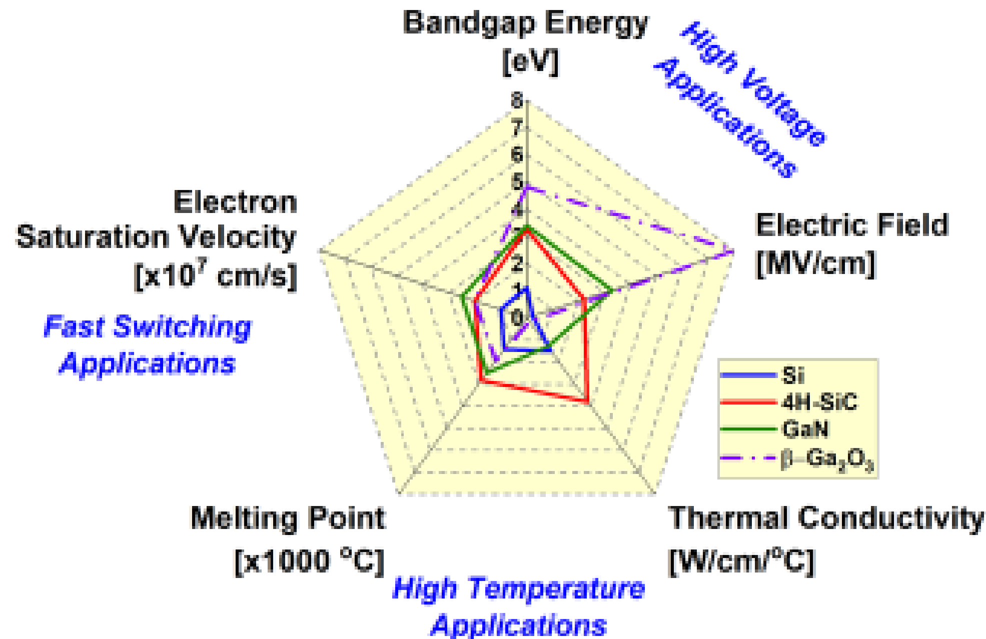
Courtesy of Daniel Fleetwood, IEEE NSREC 2020 Short Course

Changing transistor topologies

Widebandgap

Overview: Ga_2O_3 vs. Si, GaN, and SiC





New materials for power and RF devices – higher performance and efficiency

Ga_2O_3 offers a breakdown electric field over 2x larger than that of SiC or GaN – for high-voltage, low-loss applications

To be presented by J.-M. Lauenstein at the IEEE Nuclear and Space Radiation Effects Conference, Santa Fe, November 30, 2020

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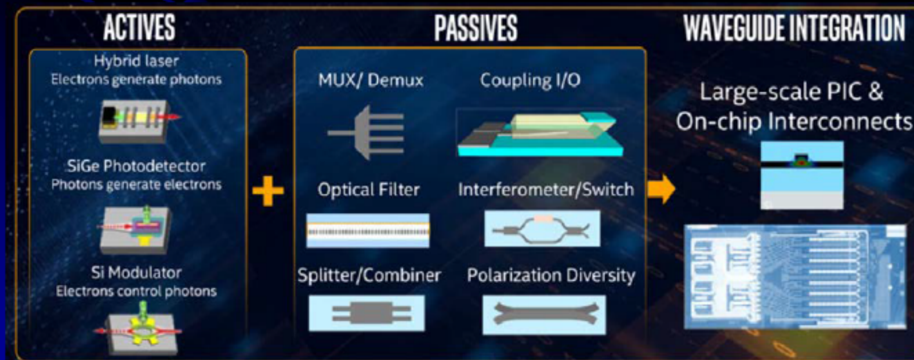
Courtesy of Jean Marie Lauenstein, IEEE NSREC 2020 Short Course

Integrated Photonics

Jet Propulsion Laboratory
California Institute of Technology

What is a Photonic Integrated Circuit (PIC)?

- PICs are advanced systems-on-a-chip, enabling transmission of data at high speeds, using optical carriers. Operate in visible and near infrared of EM spectrum (350–1650 nm).
- Feature highly-scaled integration of multiple optical components on single compact chip (micron to mm-size), enabling complex functions analogous to electronic ICs. Future integration with electronic circuits (drivers, logic) will further extend PIC functionality for wider market applications.
- Common PIC components: optical amplifiers, MUX/DEMUX, lasers, modulators, LEDs, photodetectors, planar optical waveguides, optical fiber, lenses, attenuators, filters, switches.
- Available PIC platform materials: **Si (SOI)**, $LiNbO_2$, GaAs, InGaAsP, **SiN**, **InP**, SiO_2.
- Integrated photonics is next generation disruptive technology critical to meeting size, weight, power (SWaP) as well as performance goals for many diverse applications.
- *Key benefits of PICs: >50% less mass and power, 100X size reduction, higher bandwidth and data rate, no-cost redundancy, aperture-independent (fiber-coupled), transparent to modulation format, versatile, and scalable. Offering improvements in performance and reliability.*



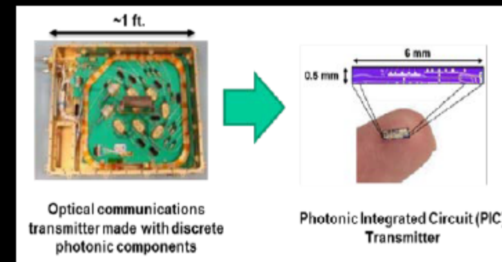


Photo Credit: Patrick Kennedy, "Intel Silicon Photonics Update at Interconnect Day 2019", https://www.servethehome.com/intel-silicon-photonics-update-at-interconnect-day-2019/

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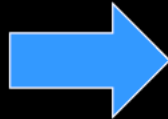
PICs are not just one technology, but multiple materials each with differing pros and cons

Courtesy of Amanda Bozovich
NASA Electronic Parts and Packaging (NEPP) Program Electronics Technology Workshop

Integrated Photonics - Now

THE PRESENT: Integrated Photonics

Discrete optical components not easily scaled and integrated into complex systems. Growth of network interconnects to meet data demand slowed by implementation of complex discrete optical designs.



Containing over 100s of optical components on a single Tx or Rx chip, photonic integrated circuits (PICs) offer more functionality, reliability, and scalability than discrete systems.

- Monolithic InP-based PICs (first introduced in 2004) established commercial viability for large-scale production of integrated photonics for telecom networks.
- PICs are technology of present and future for data centers and cloud computing, enabling simpler, more reliable, and cost effective higher bandwidth communications (overcoming limitations of discrete optical designs and electronic comm systems).

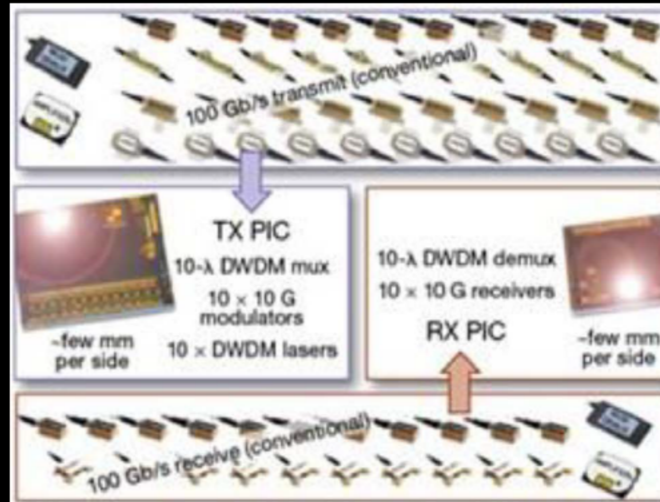


Photo Credit: Erik Pennings, "PIC Component Tutorial", 7Pennies PIC training, Dec 2019

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PICs provide a means of increasing communication and processing performance

Courtesy of Amanda Bozovich
NASA Electronic Parts and Packaging (NEPP) Program Electronics Technology Workshop

Integrated Photonics - Potential

Jet Propulsion Laboratory
California Institute of Technology

Comparison of Integrated Photonics Technology Platforms

Material	Optical Components	Refractive Index Contrast	Propagation Loss	Thermo-optic coefficient	Compatibility with CMOS electronics	Reliability
III-V Semicon-ductors (InP, GaAs)	Lasers, optical amplifiers, modulators, detectors	Low	Relatively high	High	No	High
Silicon	Filters, modulators, switches	High	Relatively high	High	Yes	High
Silica on silicon	Filters, modulators, switches, splitters	Low	Very low	Low	Yes	High
Polymer	Modulators, attenuators	Low	Low	High	Yes	Low

Comparison of material and waveguide characteristics for popular PIC technology platforms.

Photo Credit: VLC Photonics, "Interfacing with the Photonic Ecosystem in a Fabless World", 7Pennies PIC training, Dec 2019

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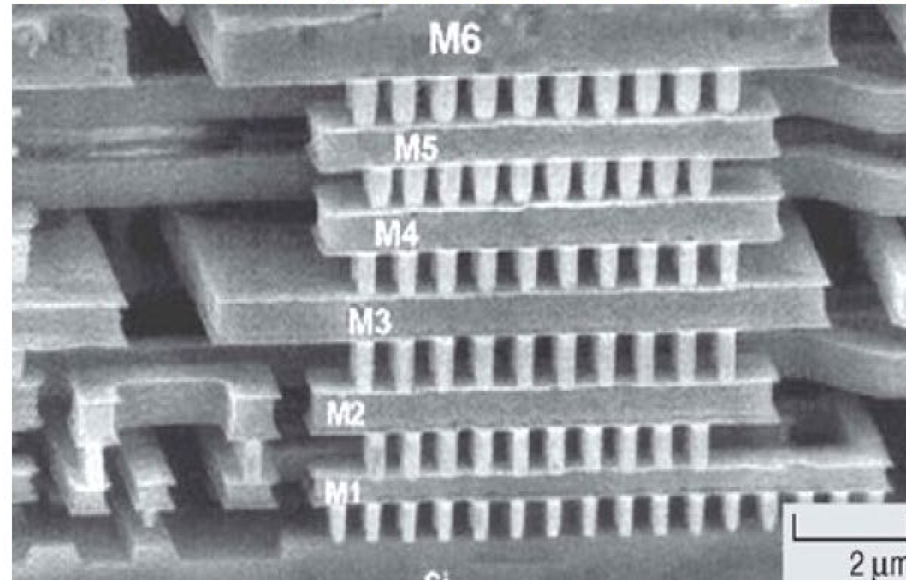
Examples of characteristics of some PIC materials that enable performance for the future

Courtesy of Amanda Bozovich
NASA Electronic Parts and Packaging (NEPP) Program Electronics Technology Workshop

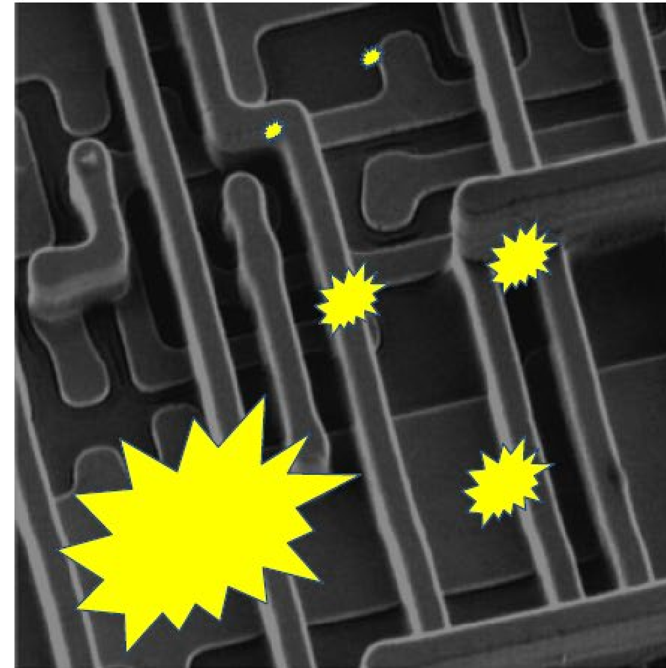
Variability in Manufacturing *= Variability in SEE response*

Making Manufacturable ICs

L.J. Chen, "Metal Silicides: An Integral Part of Microelectronics" J. of Materials, Vol. 57, No.9, pp. 24-31



Typical IC takes several dozen masks, with 10-20 steps/mask => Finished product = 100 – 500 steps



https://www.samcointl.com/featured-solutions/failure-analysis/

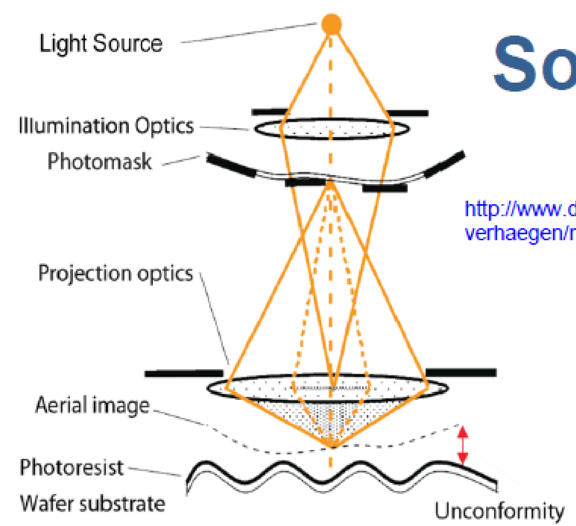
Mass-produced ≠ Identical

Robert Baumann Slide 17 of 34

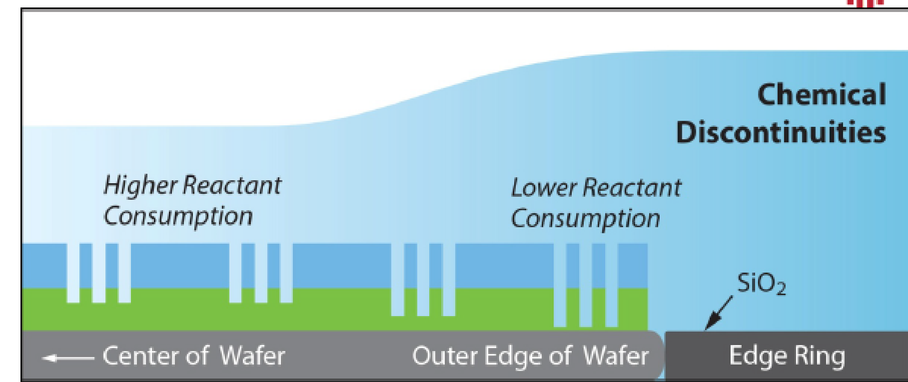
Courtesy of Robert Baumann, IEEE NSREC 2020 Short Course

Yield is "king/queen" in the manufacturing world

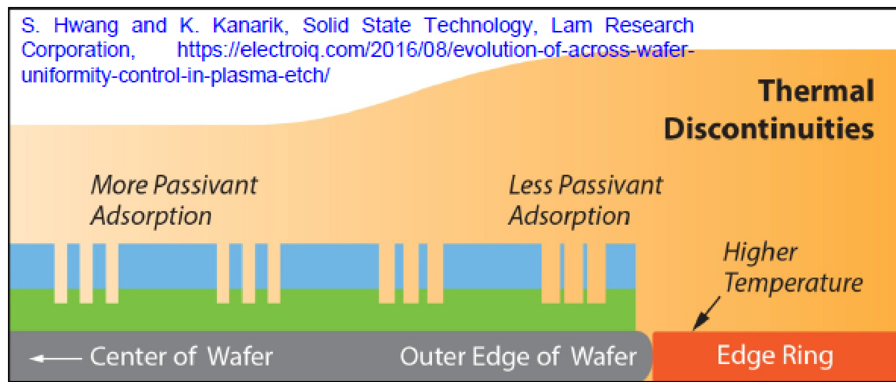
Sources of IC Variation

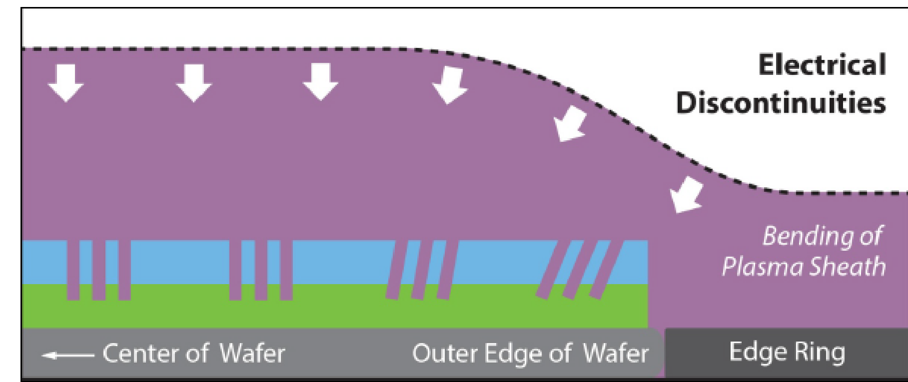


http://www.dcsc.tudelft.nl/~mverhaegen/n4ci/imwacol.htm



S. Hwang and K. Kanarik, Solid State Technology, Lam Research Corporation, https://electroiq.com/2016/08/evolution-of-across-wafer-uniformity-control-in-plasma-etch/





Robert Baumann Slide 18 of 34

NSREC 2020 SHORT COURSE - PART IV

Courtesy of Robert Baumann, IEEE NSREC 2020 Short Course

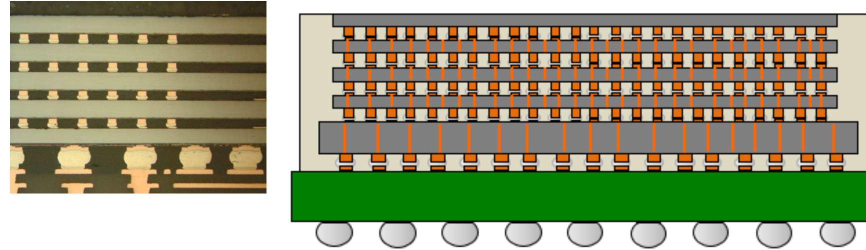
Problem increases as manufacturing complexity increases. Reduction in “electrons needed” reduces design margins. For SEE testing, sample to sample inconsistencies may require larger sample sizes and challenges for repeatability of results.

THE FUTURE OF SEMICONDUCTOR PACKAGING AND DEVICE INTEGRATION

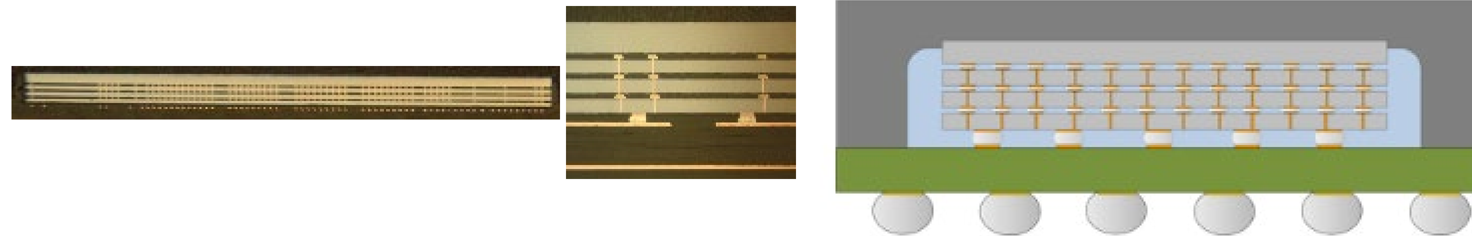
Note: the following 2 charts on packaging were graciously provided by Doug Sheldon and Eric Suh of JPL

Where we are today - Complex

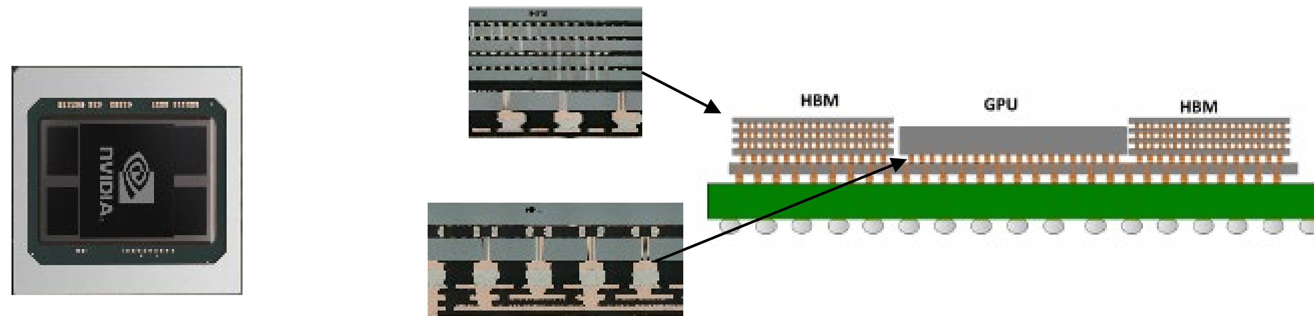
HMC



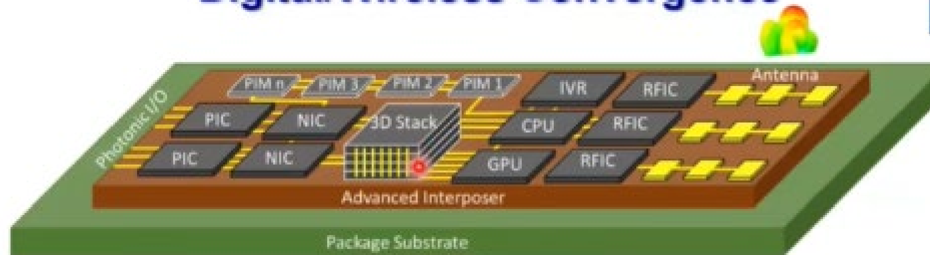
3D DDR4

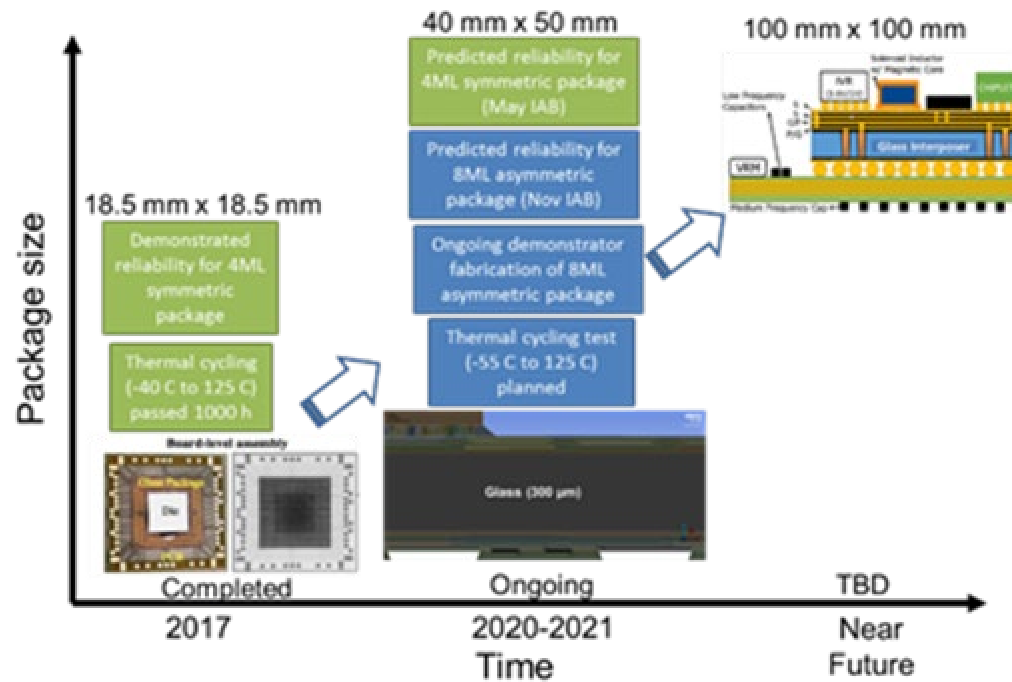


Nvidia P100



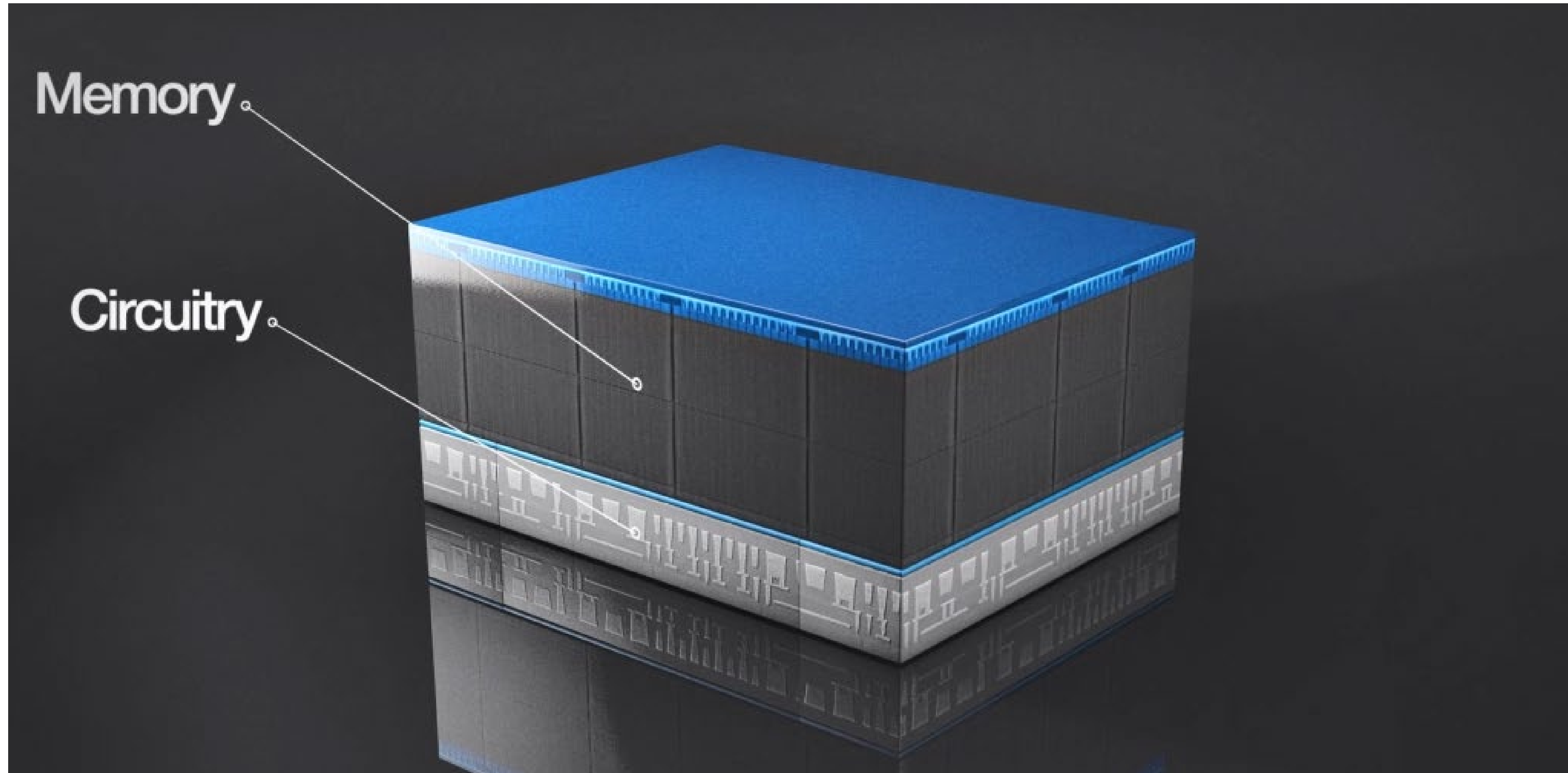
Georgia Tech visions (packaging)





The more complex devices/packages become, the bigger the challenge for SEE testing: ***Complexities for event capture and observability, sufficient ion beam penetration and device preparation, fault isolation, etc…***

And new 176 layer FLASH memory!



Micron's proprietary CMOS-under-Array technique constructs the multilayered stack over the chip's logic, packing more memory into a tighter space and shrinking 176-layer NAND's die size, yielding more gigabytes per wafer. (Image source: Micron)

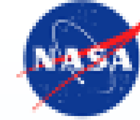
Courtesy of Micron , https://www.eetimes.com/micron-leapfrogs-to-176-layer-3d-nand-flash-memory/#

BUT WAIT A MINUTE!

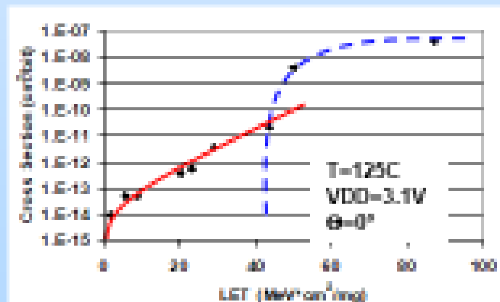
Some Things Haven't Changed!

Where we are –

Test methods and what has changed in the world



- Existing test methods
  - SEE
    - JEDEC JSD 57
    - ASTM, F1192-00
  - TID
    - MIL-STD-883B, Test Method 1019.7
    - ASTM, F1892-06
- All had prime development in the mid-90s with some updates since, however, many new issues have been discovered that may not be covered adequately



Courtesy ISDE, Vanderbilt University

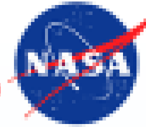
- Examples: Recent SEE Phenomena
  - Angular effects in SOI technologies
  - Role of single event transients (SETs) and commensurate speed-related issues in both analog and digital circuits
  - Ion penetration and range issues in power and packaged components
  - Approaches to die access
  - Impact of application and reconfigurable approaches to SEE performance
  - Role of nuclear reactions from heavy ion particle interactions

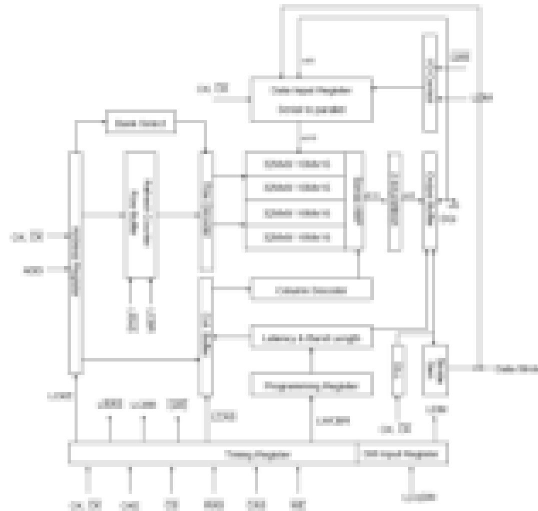
Scaled CMOS Test Challenges – Presented by Kenneth A. LaBel, GOMAC Conference, Orlando, Fl 3/22/07 6

2007!

We've been dealing with many of these issues for decades, however, evolving technologies exacerbate and create new ones! Consider that low energy protons (LEP), electrons, and muons are now part of the SEE risk equation.

Can we test anything completely?





Commercial 1 Gb SDRAM
68 operating modes
operates to >500 MHz
Vdd 1.8V external, 1.25V internal

Sample Single Event Effect Test Matrix

full generic testing

Amount	*Item*
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096	Hours
2754	Days
7.54	Years

and this didn't include temperature variations!!!

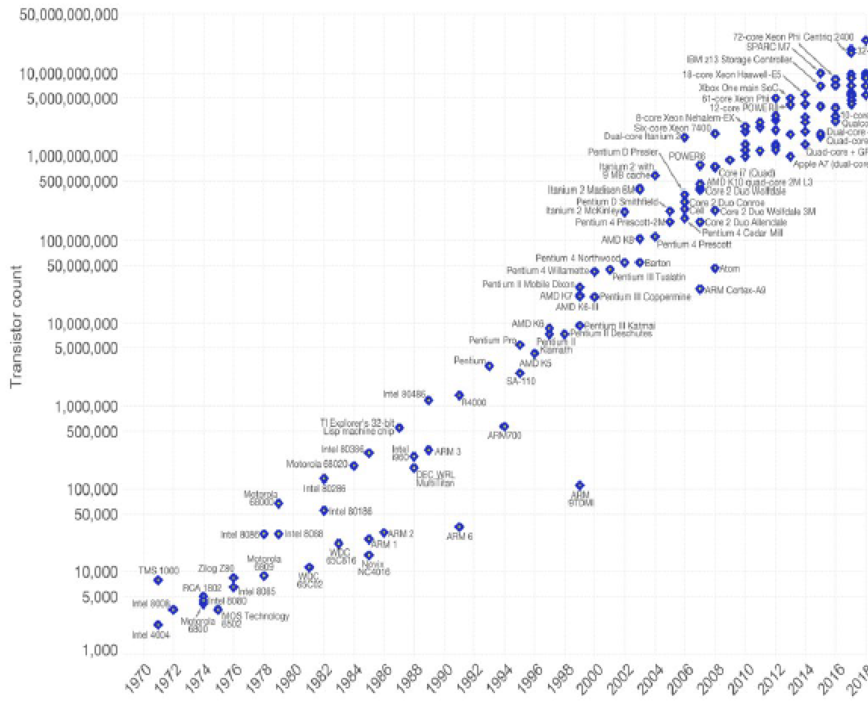
Test planning requires much more thought in the modern age
as does understanding of data collected (be wary of databases).
Only so much can be done in a 12 hour beam run – application-oriented

Scaled CMOS Test Challenges – Presented by Kenneth A. LaBel, GOMAC Conference, Orlando, Fl 3/22/07 11

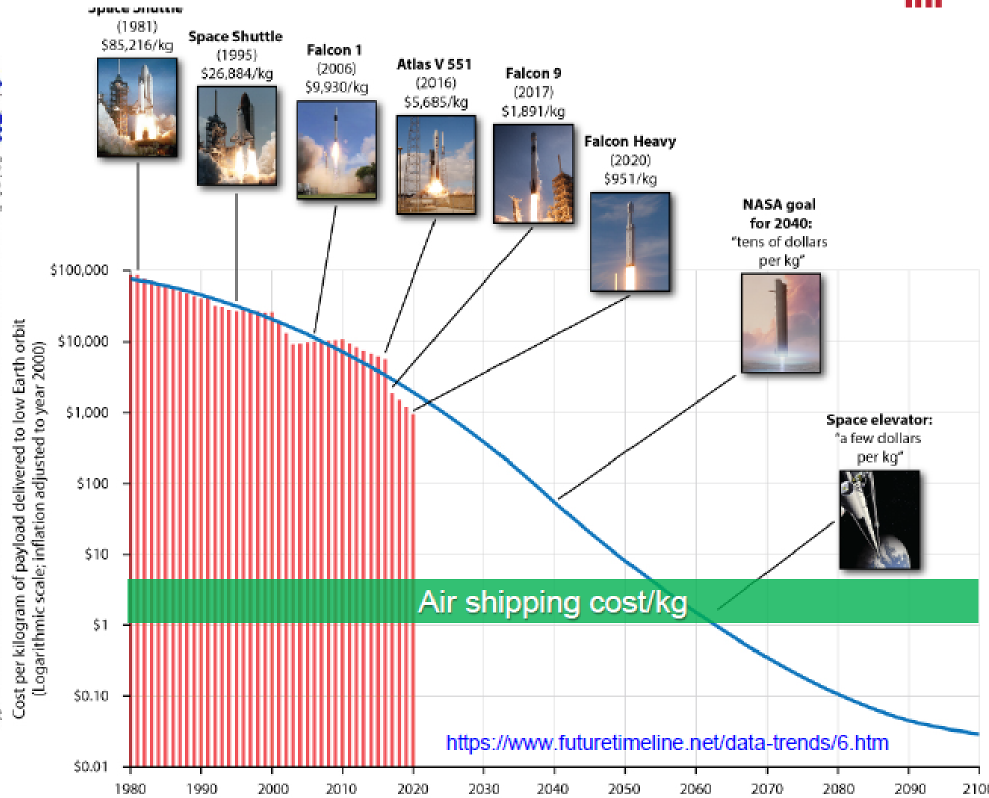
"Complete" SEE testing: is it a fallacy?
Two thoughts:
- **Good enough set of "generic" data for device selection?**
- **Additional testing for actual application?**

SPACE SYSTEMS OF TOMORROW

What is Driving New Space Growth?



By Max Roser - https://ourworldindata.org/uploads/2019/05/Transistor-Count-over-time-to-2018.



RADIOSITY SOLUTIONS

Robert Baumann — Slide 10 of 34

NSREC 2020 SHORT COURSE - PART IV

SMU LYLE SCHOOL OF ENGINEERING

Courtesy of Robert Baumann, IEEE NSREC 2020 Short Course

No argument:
COTS semiconductors are generations ahead of radiation hardened alternatives.
Integration drives lower power and higher performance.

- **Launch costs have also declined rapidly making space reachable for even the small "guy/gal". This also makes the business model for space more attractive overall.**

HEAVY IONS AND SUPPLY-SIDE ECONOMICS

Meeting the Demand and…

- Right now, there are 4 facilities within the U.S. typically used for heavy ion testing
    - TAMU K500/K150
    - LBNL 88 in
    - BNL NSRL
    - BNL Tandem
- Studies such as National Academies' "Testing at the Speed of Light" have predicted several things:
    - An increasing demand that exceeds capacity of these 4 facilities,
    - Frailty of the infrastructure (highlighted recently by the downtime at LBNL related to equipment failure), and,
    - Need for higher energy facilities (increased penetration range of ions).
- Personally, I believe there's one other trend that increases:
    - System/assembly level tests

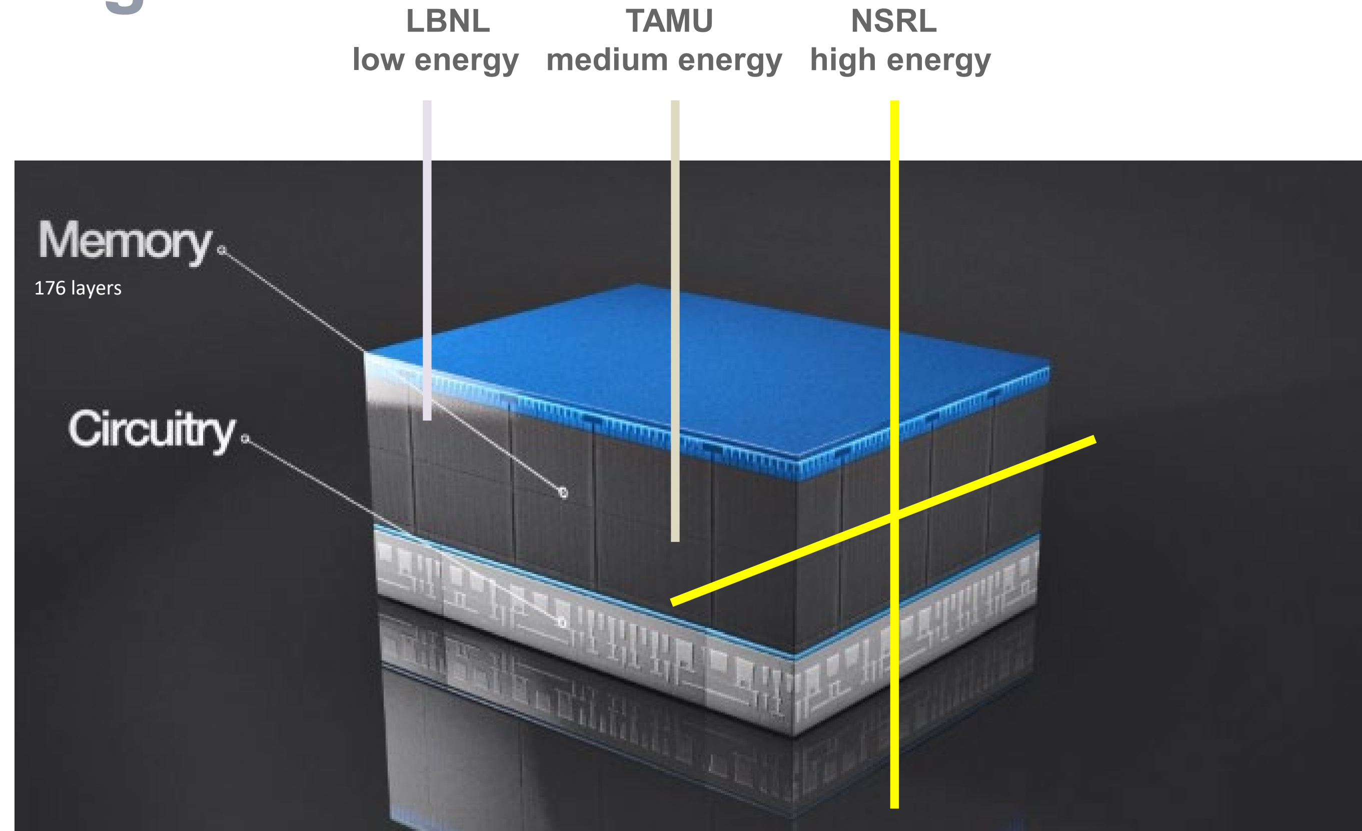
While 2020 was an unusual year, a recent survey of heavy ion SEE users showed over a 3500 beam-hour shortfall in available time. ***New USG programs, commercial space, and further use of COTS are expected to increase the capacity shortfall total.***

Notional ion energy and device testability- penetration range

LBNL
low energy

TAMU
medium energy

NSRL
high energy



Micron's proprietary CMOS-under-Array technique constructs the multilayered stack over the chip's logic, packing more memory into a tighter space and shrinking 176-layer NAND's die size, yielding more gigabytes per wafer.

Courtesy of Micron , https://www.eetimes.com/micron-leapfrogs-to-176-layer-3d-nand-flash-memory/#

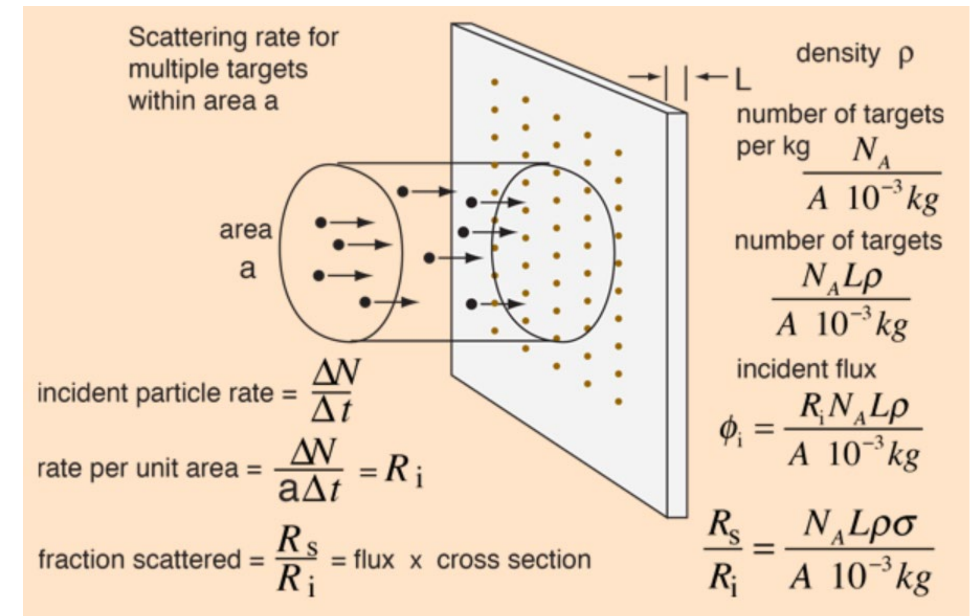
Note that non-3D devices are not disappearing from space systems and the energies at LBNL and TAMU will still be needed as well.

High energy ions are needed to ensure penetration to all radiation sensitive portions of modern 3D devices. These are the state-of-the art devices that have enabling properties for space applications.

THE FUTURE OF HEAVY ION FACILITIES

Improving Existing Facilities

- The accelerators themselves are “minimally” improvable, however, there are other areas that can either add capacity or capability
- Higher energy ions, improved intensity, and reduction of “ion/energy” switching
  - New ion source (Jyvaskala, MARS, LASER sources)
  - Improved vacuum systems (for the machine, not the user end station)
- Time saving/efficiency measures
  - Multiple target rooms
  - Increased automation and control



This is a figure depicting ion beam particle interaction with a target at a cyclotron

Courtesy of Rod Nave

http://hyperphysics.phyastr.gsu.edu/hbase/nuclear/imgnuc/crosec.gif

Higher Reliability and Intensity – Heavy Ion Ion Source Injector (HIISI)

- The typical ion source used in SEE testing accelerators is cryogenic magnetic based
- New designs such as the HIISI at University of Jyvaskyla use room-temperature magnets
  - ***This improves reliability (i.e., less down time) and beam intensity at ions of interest to SEE***
- The figure at the right compares the new HIISI at two kinetic energy tunes versus two cryogenic sources
  - Existing Jyvaskyla (JYFL), and
  - Existing Michigan State University (SUSSI)
  - The results are favorable for SEE test improvements without building a new cyclotron

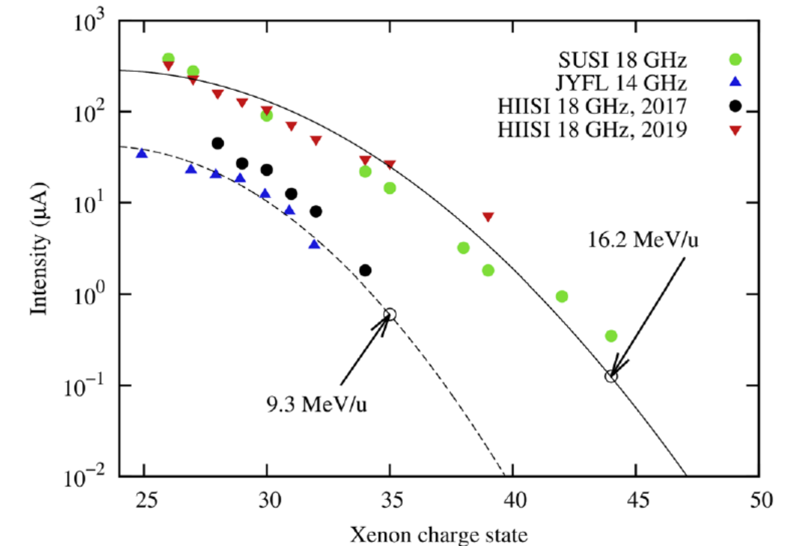


FIG. 3. Intensities of Xe ion beams produced by different ECR ion sources: JYFL 14 GHz ECRIS, SUSI at 18 GHz (4 kW), and HIISI in 2017 (14.5 GHz + 18 GHz/2.3 kW) and 2019 (14.5 GHz + 17.4 GHz + 18 GHz/3 kW). The xenon charge states of 35+ and 44+ required for the currently used 9.3 MeV/u and proposed 16.2 MeV/u beam cocktails are marked on the fitting curves.

"A new 18 GHz room temperature electron cyclotron resonance ion source for highly charged ion beams", Rev. Sci. Instrum. 91, 023303 (2020)

Next Generation Electron Cyclotron Resonance Ion Source (ECRIS)

- A 4th generation ECRIS, MARS-D, capable of operation at 45 GHz is under continuing development at Lawrence Berkeley National Laboratories (LBNL)
- For the Berkeley Accelerator for Space Effects (BASE), multiple ion sources are available pending the user needs
- ***The MARS-D (under planning) would provide a higher charge state allowing ions with a greater penetration range***

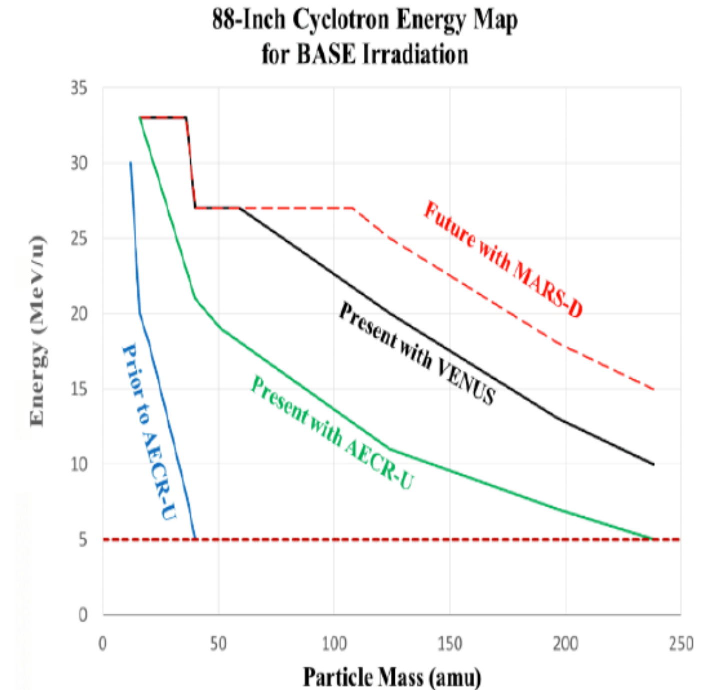


Figure 2: This plot shows the energy-mass curves achieved by the 88-Inch Cyclotron with the existing ECRISs and extrapolation with a future ECRIS for the BASE Facility.

"A PATHWAY TO ACCELERATE ION BEAMS TO 3 GeV WITH A K140 CYCLOTRON", Rev. Sci. Instrum. 91, 023303 (2020)

LASER Ion Source (LIS)

- While not yet mainstream, LASER ion sources are under development worldwide and a prototype is in use at NSRL
  - ***Allowed vast improvement in ion change times at NSRL for SEE testing***
  - Light to heavy ions have all been demonstrated
  - Intensity of beam improved
  - LIS is used an injector into the Electron Beam Ion Source (EBIS)

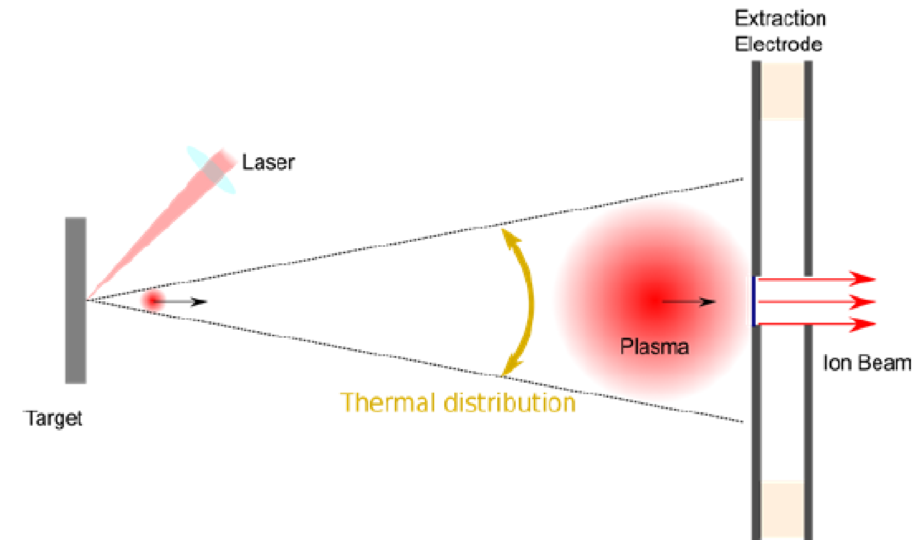


Figure 1: Expanding plasma and extracted ion beam.

"PERFORMANCE OF THE LOW CHARGE STATE LASER ION SOURCE IN BNL", ISBN 978-3-95450-180-9 Proceedings of NAPAC2016, Chicago, IL, USA MOA4IO01

Other Heavy Ion Facility Thoughts

- There are other ways of either increasing capacity, capability, or test efficiency with improvements at heavy ion sites
  - Improving accelerator vacuum systems
    - Increases ion intensity and possibly ion selection options
  - Spare accelerator equipment such as power supplies, ion sources, etc…
    - Significantly reduces unplanned maintenance time
  - In air testing
    - Reduces SEE test set complications (thermal, cabling, etc…)
    - Increases beam time efficiency (no lost time to break vacuum to change devices)
  - Higher energy ions >20 MeV/amu
    - Reduces risk of deprocessing test devices
  - Improved beam control and telemetry
    - Better ways of coupling the test set with the beam control/dosimetry system

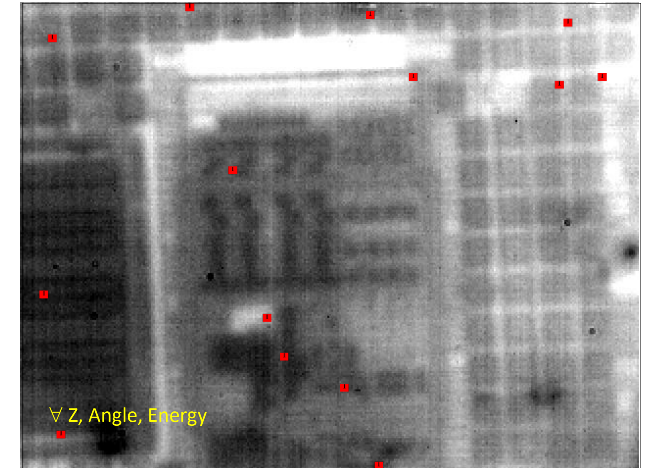
REDUCING THE DEMAND: PROTONS AS A SCREEN (NOT A SURROGATE)

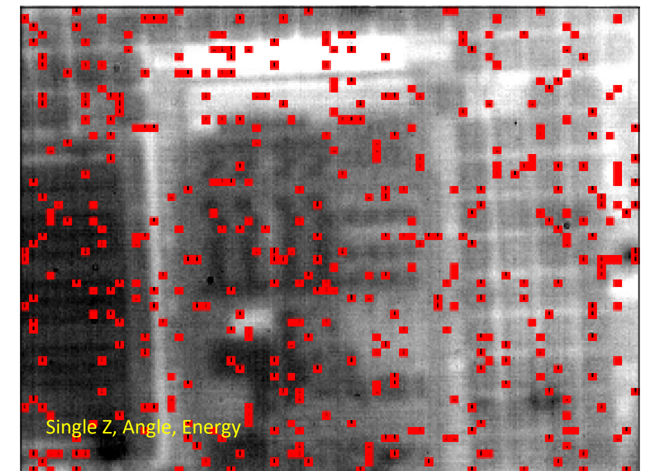
Heavy Ions vs. Protons – Proton facilities are much more readily available but insufficient to qualify hardware for deep space environments

SEE Proton testing relies on proton nuclear interactions and spallation effects to generate secondary heavy ions. This secondary environment presents the following limitations:

- Reduced feature coverage
  - Infrared micrograph of a portion of a 512 Mb SDRAM ~60x70 μm^2
  - Shows both memory cells and control logic (10 yr. old tech.); Red spots are simulated ion hits
- Maximum theoretical LET of 14 MeV-cm^2/mg
  - 8 MeV-cm^2/mg more realistic
  - SMC-S-010 requires 75 MeV-cm^2/mg
- Limited penetration (range)
  - Insufficient to cause some destructive effects that would occur in space
- Caveats include dose during testing and material activation

Coverage from1E11 200 MeV protons/cm^2





Coverage from1E7 heavy ions/cm^2

After Ladbury, TNS-2017-TN35833

So Why Mention Protons?

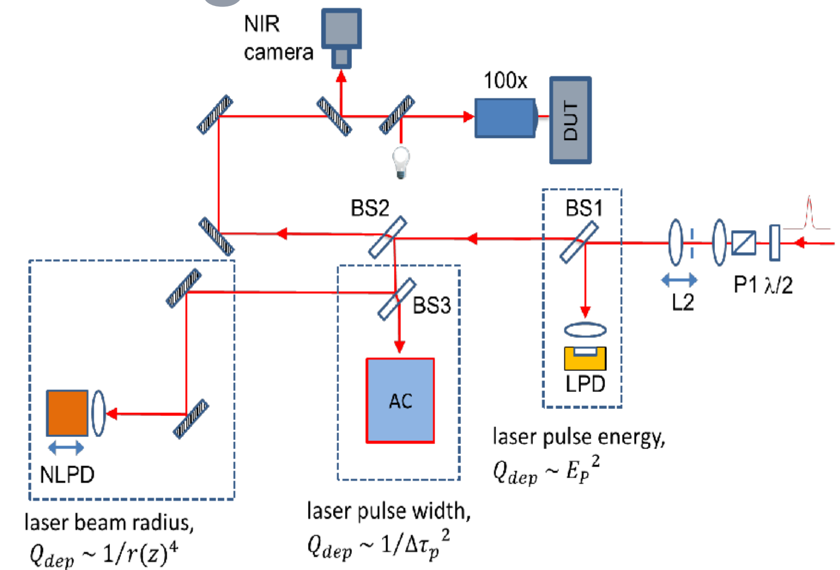
- They do have some utility and are very readily available
- Utility features that may reduce heavy ion demand
  - Validate test set prior to heavy ion test (eliminates wasted time at heavy ion site)
  - Use as a pre-screen in parts selection
    - If SEE observed with protons, they will be sensitive to heavy ions
    - Test multiple vendors of the same/similar device
      - Eliminate those that are most proton sensitive
  - Large spot size: Use as a system validation test (i.e., protons as a “fault injector) for mitigated designs
  - Typical tested proton energies such as 200 MeV have inches of penetration range for complex 3D packaging that provide a challenge at most heavy ion accelerators (including cost!)

THE FUTURE FOR ALTERNATE TEST FACILITIES – LASERS AND PULSED X-RAYS

Note: the following 3 charts on LASER testing were graciously provided by Dr. Stephen Buchner/NRL

Using a Pulsed Laser for SEE Testing

- **Focused, pulsed** laser-light may be used to inject charge into a semiconductor device to produce SEEs.
- The charge track characteristics, such as spatial and temporal extent, approximate those produced by ions.
- The track of charge has radial dimensions (~1 um) determined by the optics of the focusing system and by the wavelength of the light.
- The pulse duration is in the range of hundreds of femtoseconds, which is faster than the response time of most circuits and comparable to that of an ion, necessary for accurately determining SEE sensitivity.
- Both Single-Photon Absorption (SPA) and Two-Photon Absorption (TPA) may be used for SEE testing. SPA is used when the top-side of the chip is accessible. Otherwise TPA is used for backside illumination



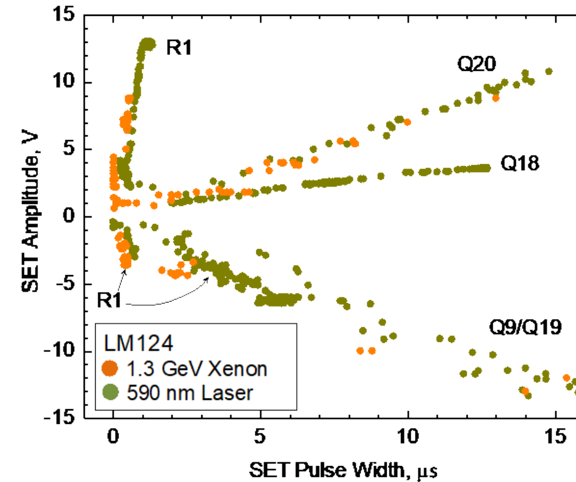
Experimental Setup for doing Two-Photon-Absorption

Microscope Lens used to Focus Light on the DUT

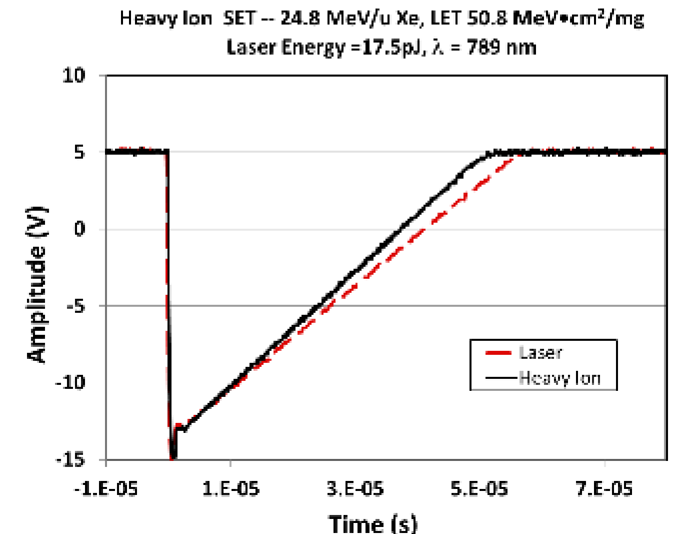
Uses of a Pulsed Laser for SEE Testing

Pulsed laser can be used to:

- Determine whether a part is sensitive to single-event latchup (SEL) as well as its location
- Test for SEL as a rapid screen to avoid time and expense of doing heavy ion testing
- Bound the amplitudes and widths of single-event transients in linear bipolar circuits
- Inject charge to produce an SEE to determine whether a mitigation approach is necessary and after implementation, whether it is effective
- Investigate the fundamental mechanisms involved in charge collection
- Identify the spatial location of destructive SETs without actually destroying the device
- Validate a test set prior to heavy ion test



SET Amplitude vs Width for LM124 showing good comparison between laser-light-induced and ion-induced SET shapes



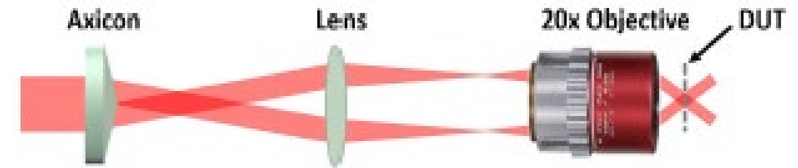
Comparison of SET for LM124 showing good comparison between laser-light-induced and ion-induced SET shapes

Future of LASER SEE Testing

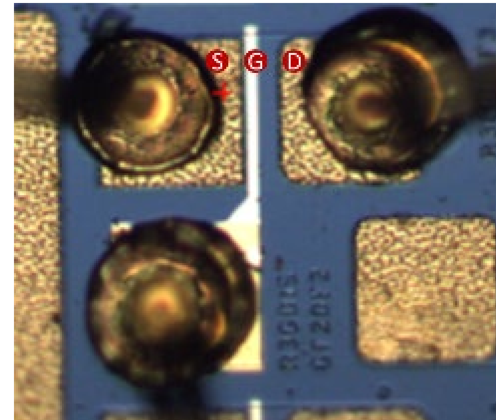
Future efforts for SEE Testing

- Apply the technique to other semiconductor systems with large electronic energy bandgaps, GaO, AlGaN, SiC etc.
- Investigate the fundamental mechanisms contributing to SETs, including charge deposition, charge collection, charge enhancement and circuit response
- Write a Guidelines Document for SEE Testing
- Pursue the Axicon approach for producing a focused beam of light that more closely resembles an ion track
- Correlate ion LET with laser pulse energy

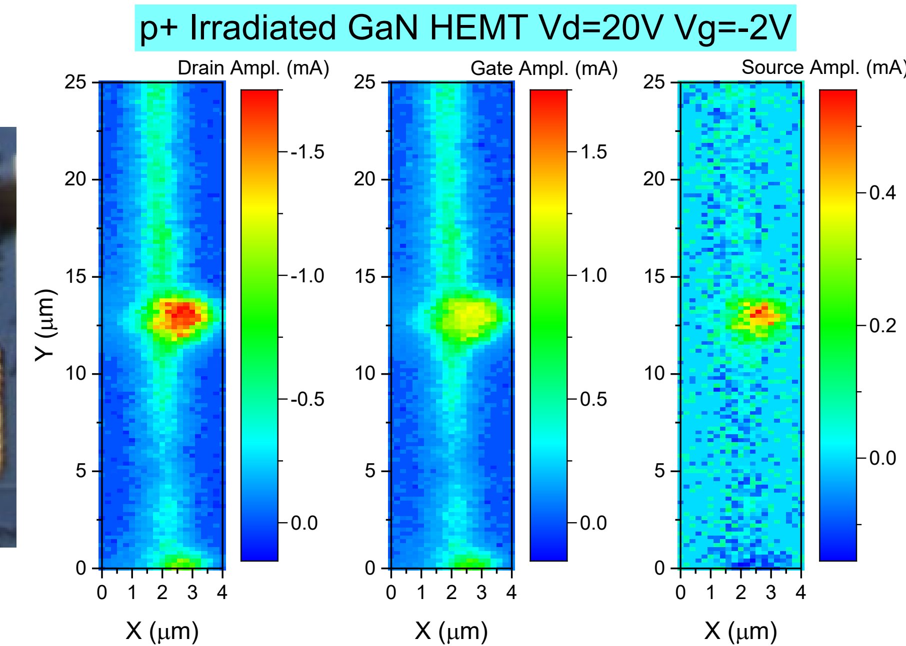
Note: At least 3 commercial SEE LASER test vendors are selling systems



Addition of two optical elements converts typical TPA test setup into an Axicon focusing geometry



AlGaN HEMT



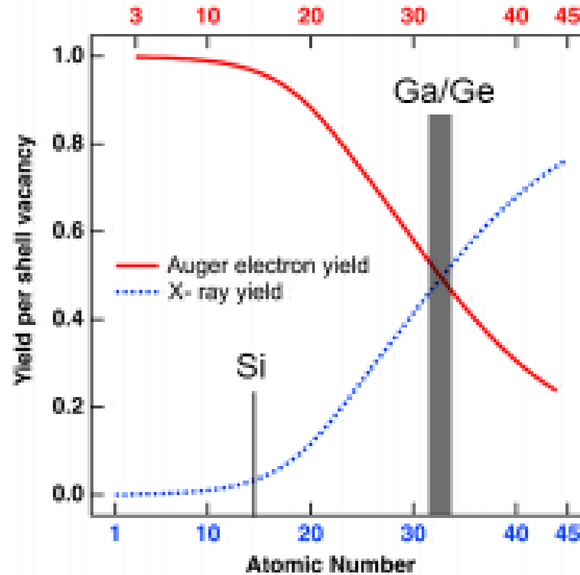
Scan of the region between the gate (G) and drain (D) of the AlGaN HEMT. The colors are proportional to the SET amplitudes

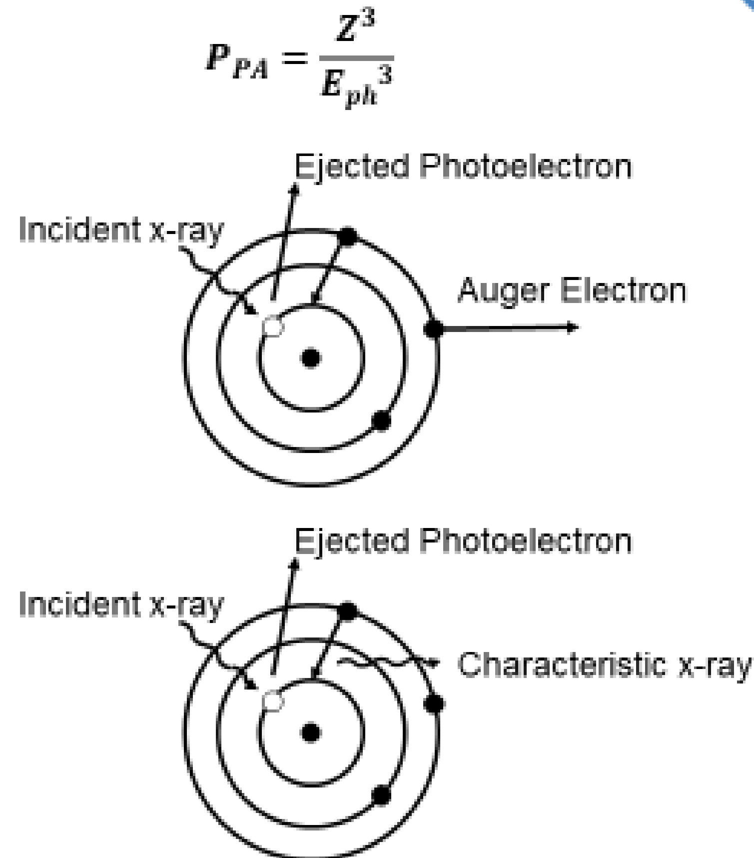
Ken's Comment:
The Holy Grail
(and how will material/topology changes affect this?

X-Rays for SEE Testing

X-ray Interaction – The Photoelectric Effect (E_{ph} < 20 keV)

- Interaction depends on Atomic Number (Z) and E_{ph}
- X-ray interacts with tightly bound electrons
- Photoelectron ejected – atom relaxes
  - *Low Z: dominated by Auger process*
  - *Hi Z: dominated by fluorescence process*
- $N_{ehp} = E_{ph} / \omega$ (ω = 3.62 eV/ehp for silicon)





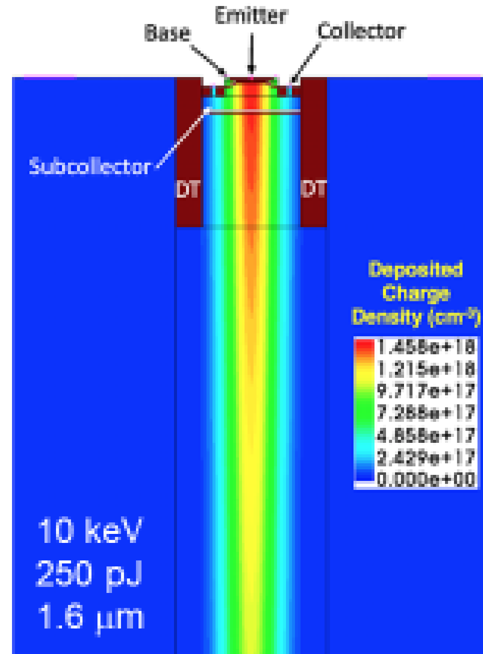
Courtesy of Stephen LaLumondiere, G-Rad 2020

Ken's Comments: X-Rays are an interesting complement to heavy ion and LASER testing. They provide a pulsed, focused beam that penetrates metallization and creates an ion track similar to an ion.
However, research in utility is still in the early stages.

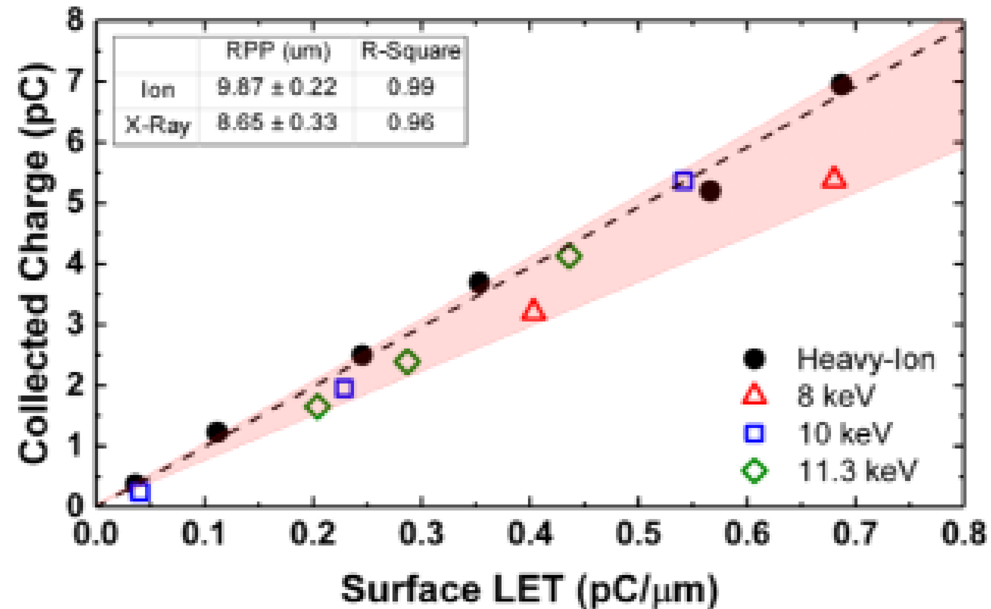
Example Data of X-Ray SEE Testing

Single Event Upset Measurements in Silicon Germanium Technologies

Collaboration with Georgia Institute of Technology



- TCAD Simulation deposited charge in SiGe Heterojunction Bipolar Transistor



D. Nergui *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 91-98, Jan. 2020,

Good agreement is observed between x-rays and heavy ions for higher energy x-ray photons.

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Courtesy of Stephen LaLumondiere, G-Rad 2020

Where's X-Ray Going

Concluding Remarks

- **Pulsed X-rays are a relatively new technique for SEE testing**
  - *Current prospects are good*
    - Able to reproduce SEU, SEL, SEB, SEFIs, SETs from energetic particles
    - More work to come on SEB and SEGR
- **Future benefits and challenges from synchrotron upgrades**
  - *Increased brightness is advantageous*
    - Higher effective LETs (more photons in focused spot)
  - *Fill formats could change to higher repetition rates*
    - Mechanically challenging
    - Need new pulse selection technique (MEMs devices?)
- **Aerospace/APS X-ray microprobe station is under development (Partner User Proposal)**
  - *Expect to commission in summer of 2021*
  - *Open to ideas for collaborations*
  - *Always available to talk with others who are interested*
- **Work together to increase community awareness of need/benefit of advanced techniques**

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Ken's Note:
Both U.S. and E.U. have pulsed x-ray sources where SEE testing utility is being investigated

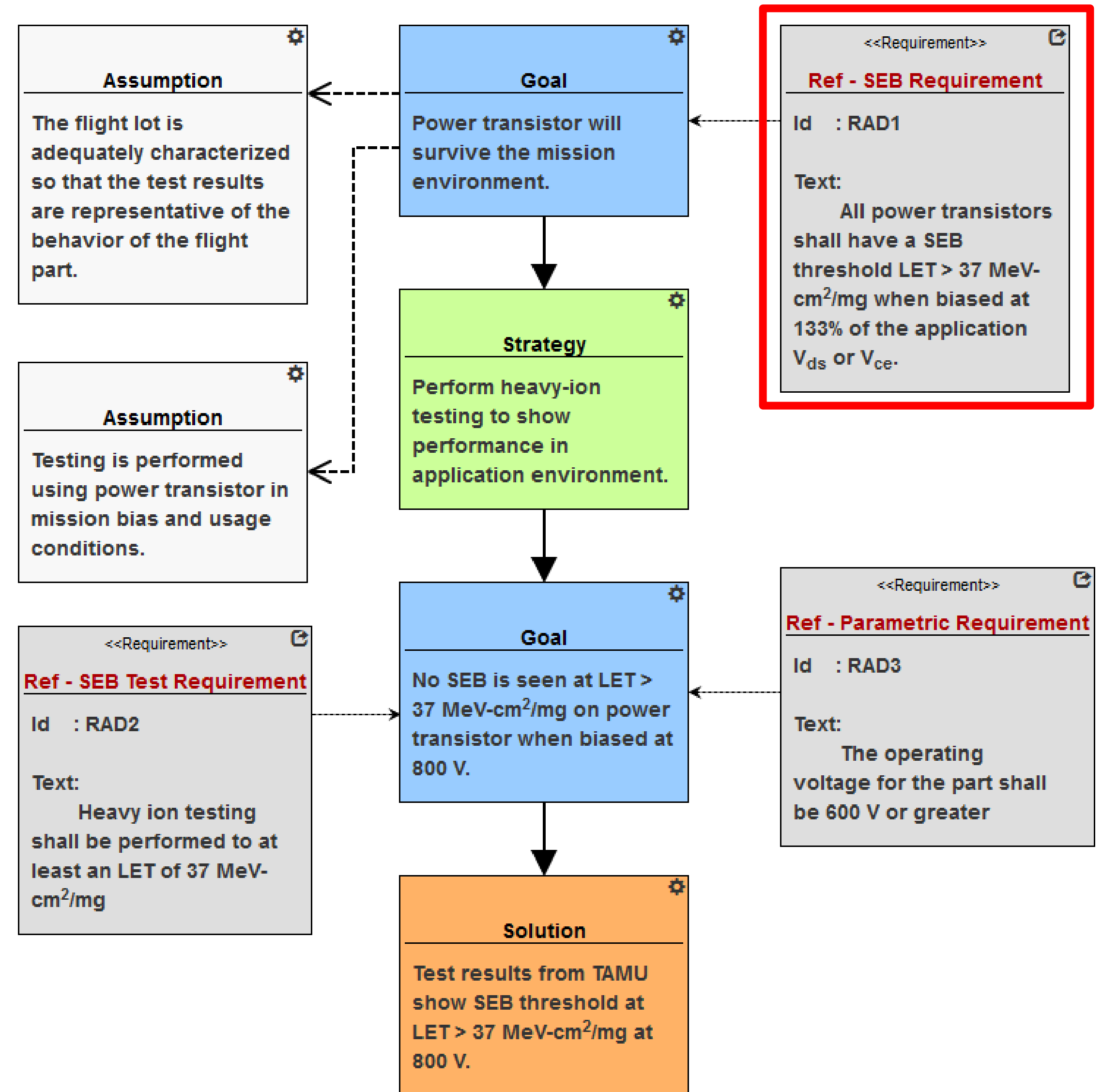
Courtesy of Stephen LaLumondiere, G-Rad 2020

OPTIMIZING SEE TESTING VIA MODEL BASED MISSION ASSURANCE (MBMA)

Note: the following 6 charts on MBMA were graciously provided by Rebekah Austin/NASA-GSFC.
MBMA is course unto itself, but moves engineering assurance from the unconnected paper domain to the connected digital domain.

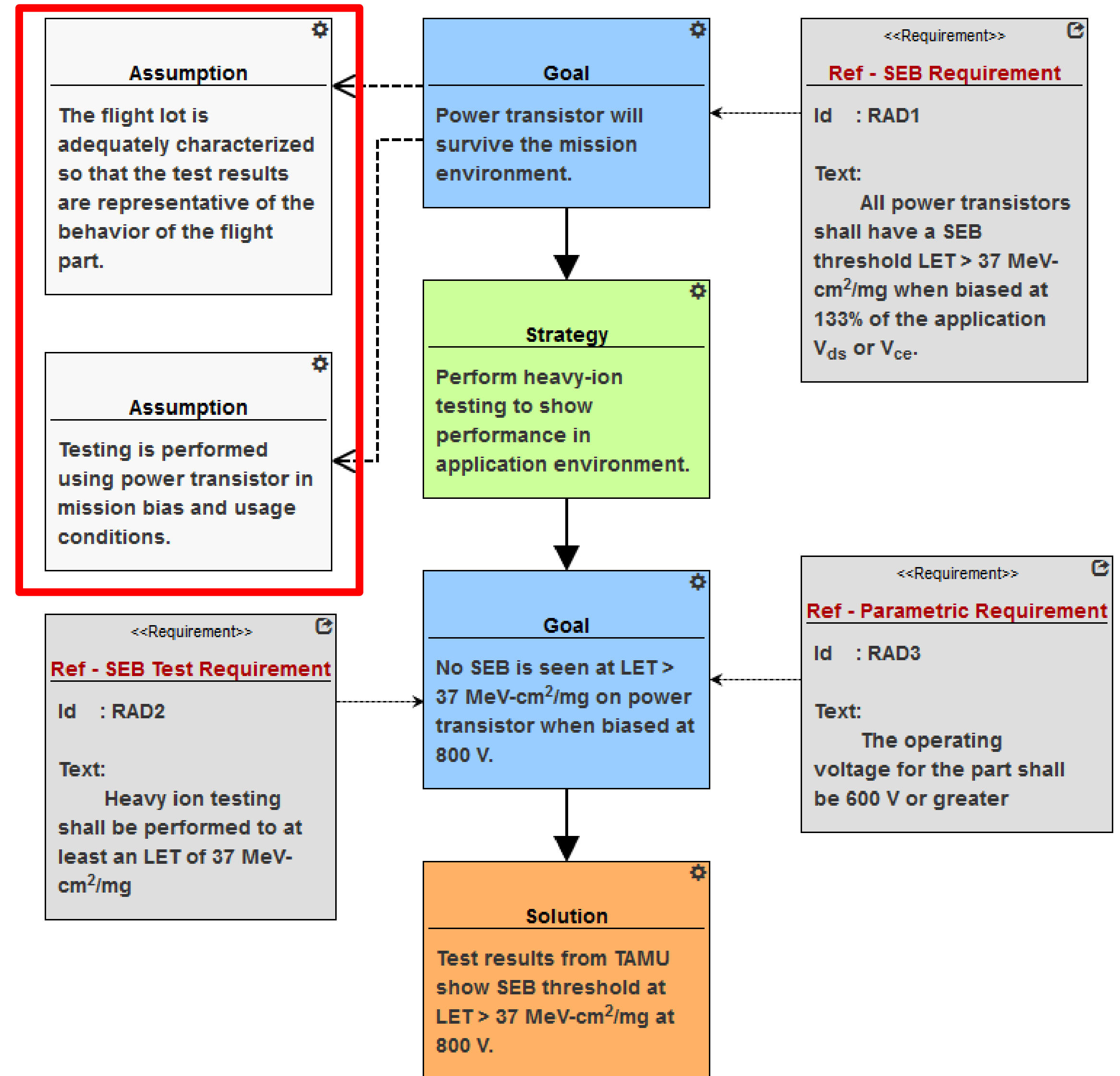
Example 1: Verify Requirements with SEE Test data

- Standard requirement verified through heavy-ion testing



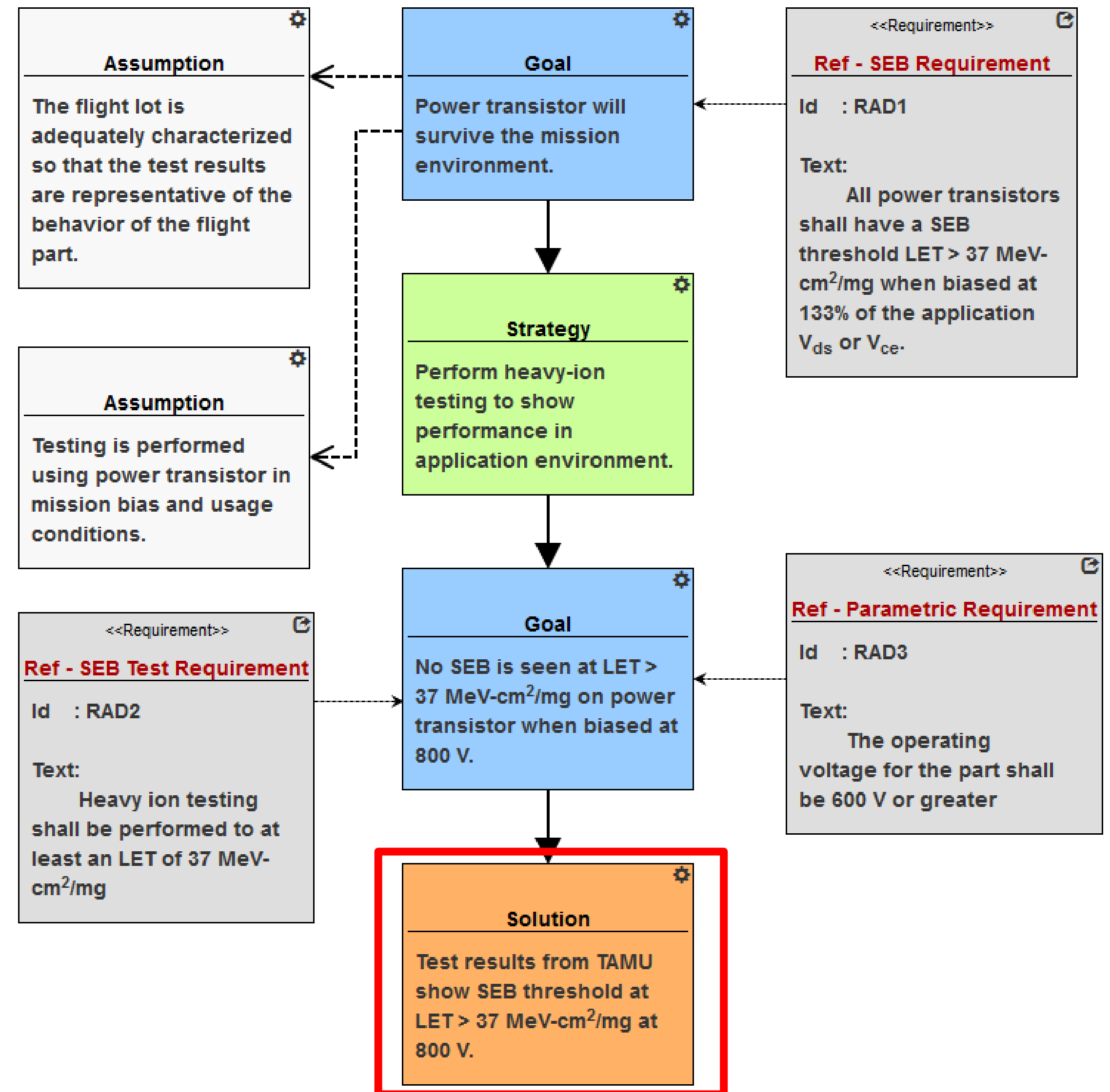
Example 1: Verify Requirements with SEE Test data

- Standard requirement verified through heavy-ion testing
- Assumptions explicitly stated



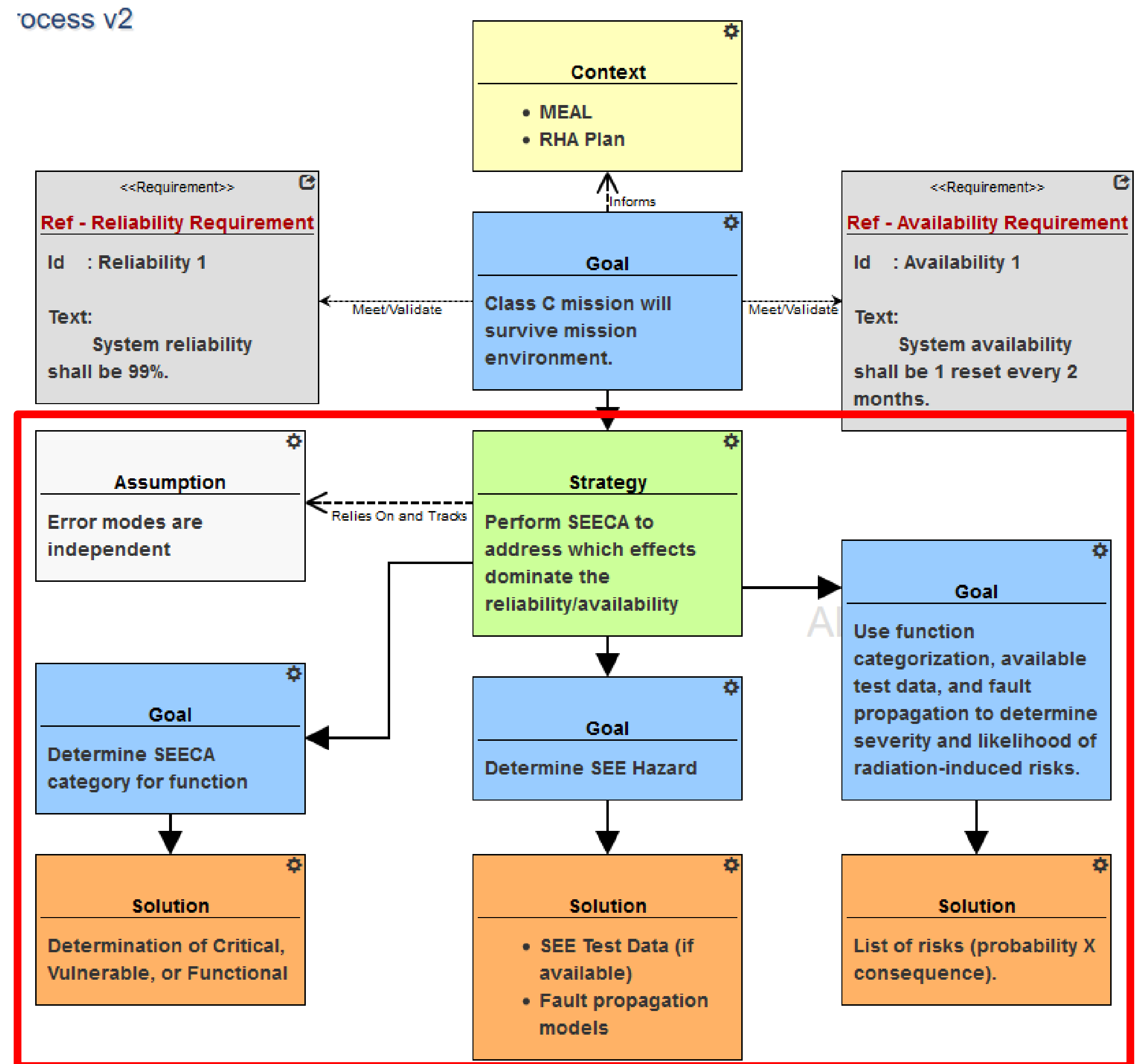
Example 1: Verify Requirements with SEE Test data

- Standard requirement verified through heavy-ion testing
- Assumptions explicitly stated
- Verification of requirement is backed by the graphical argument AND the test data



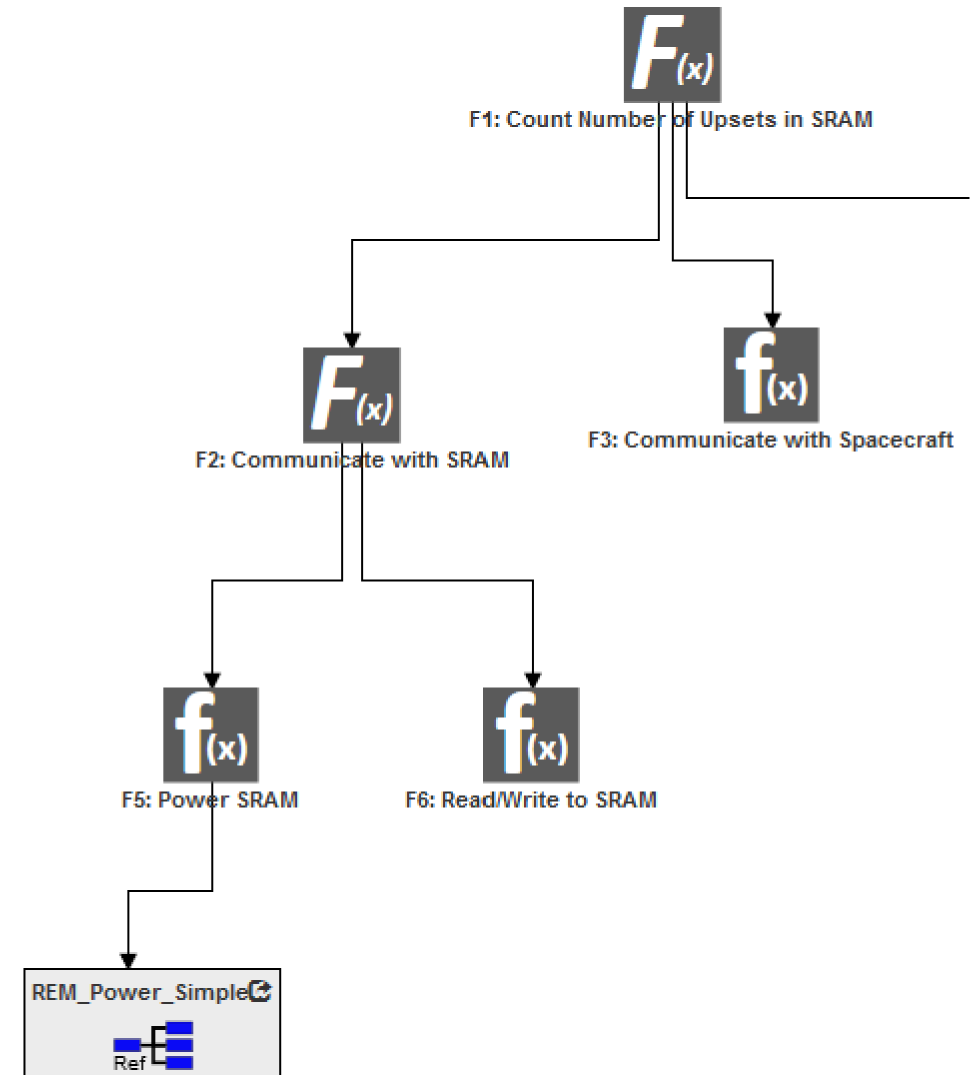
Example 2: Prioritization of SEE Testing for Maximum Risk Reduction

- The SEECA process can be documented and supplemented using MBMA
  - Graphical argument links together steps and logic



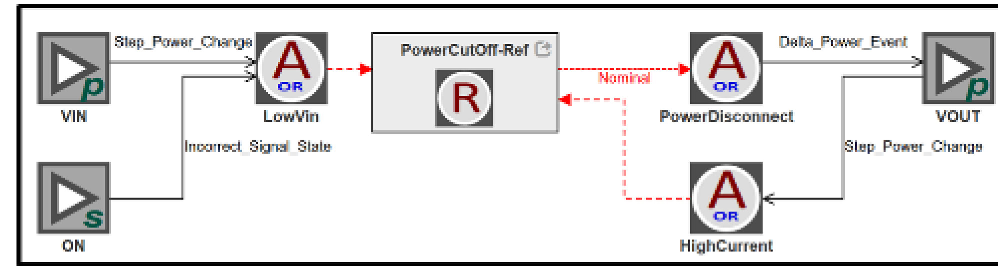
Example 2: Prioritization of SEE Testing for Maximum Risk Reduction

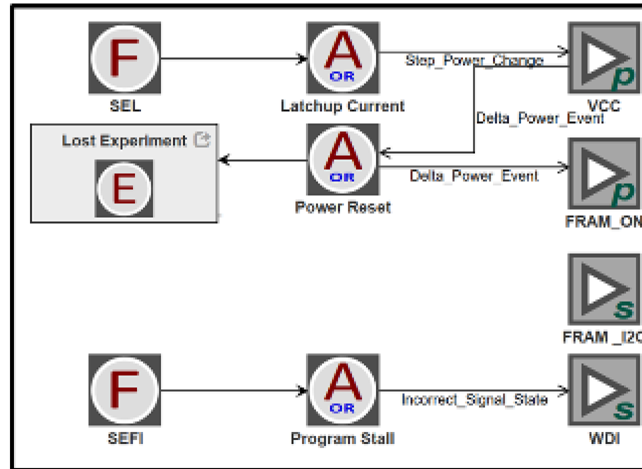
- The SEECA process can be documented and supplemented using MBMA
  - Graphical argument links together steps and logic
  - Functional decomposition can be used to determine SEECA categories

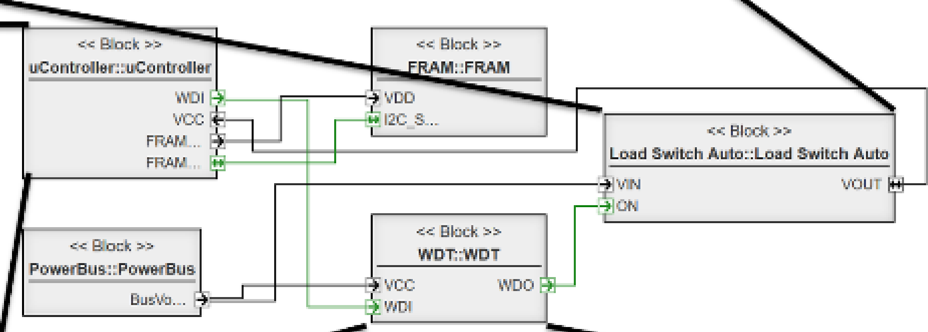


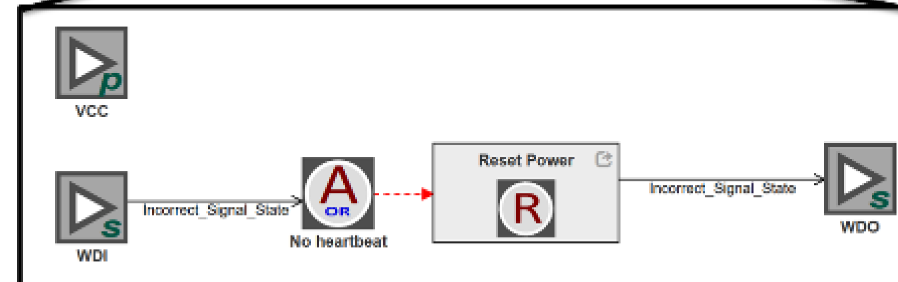
Example 2: Prioritization of SEE Testing for Maximum Risk Reduction

- The SEECA process can be documented and supplemented using MBMA
  - Graphical argument links together steps and logic
  - Functional decomposition can be used to determine SEECA categories
  - Fault propagation models can be used to determine consequence of SEE hazard









Ken’s MBMA Thoughts

- One of the great things surrounding MBMA is the efficiency it brings to the process of connecting requirements to engineering processes/methods to validation and documentation
  - This enhances the ability to optimize test time by connecting results to requirements in a manner that is easy to document
- To put it simply, MBMA as applied to SEE testing provides opportunities to
  - Verify requirements with SEE test data
  - Determine best bang for the buck SEE tests for risk reduction
  - Make test decisions during a SEE test campaign

It’s all about being more efficient!

IMPROVING TEST EFFICIENCY AND PERFORMANCE

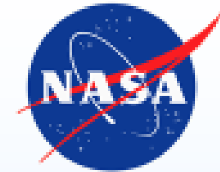
Be Clear on Test Objectives

- While test requirements were discussed in an earlier module, it is important to emphasize that objectives for a test need to be well defined.
- Examples include:
  - Go/No-go: do you see an event at a given LET or not?
  - Product qualification
    - Test at specific operational levels such as low, medium, and high device utilization/performance. Don't try to get data for ALL applications, just sufficient amounts for device selection purposes.
  - Mission specific
    - Will discuss during "system testing" later
  - Technology or architecture research

This isn't new, but with test time being a premium…

Create Your Own Checklist

- Create a priority approach of test objectives based on:
  - Device operating modes, voltage levels, frequencies, …
  - Device physics
    - Angles, ions, energies, …
    - Beam characteristics
- An early description of the checklist approach



Are Current SEE Test Procedures Adequate for Modern Devices and Electronics Technologies?

Kenneth A. LaBel
Co- Manager,
NASA Electronic Parts and Packaging (NEPP) Program
NASA/GSFC
ken.label@nasa.gov
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Lewis M. Cohn, Defense Threat Reduction Agency
Ray Ladbury, NASA/GSFC

https://radhome.gsfc.nasa.gov/radhome/papers/HEART08_LaBel_pres.pdf

Measured Data on Complex Device - Caveat

Modeling Empirical Cross-Sections from Beam Experiments

$$P_{upset} = P_{gen} \times P_{Effect} \times P_{observe}$$

- **Empirical cross sections are not pure:**
  - P_{gen}: physics, sensitive region, basic mechanisms. Generally what our models target. Probability that an ion strike will generate an SET/SEU
  - P_{Effect}: design, operation, frequency: Incorporates design dependent topology and frequency as a transfer function (H(s)). Given P_{gen}, what is the probability that the system will be disturbed?
  - $P_{observe}$: test system and test conductor. Probability that the system disturbance is observed. Goal is to capture and observe every event with $P_{observe}$=1
- **What is the goal of the experiment?**
  - If attempting to measure P_{gen} (perhaps to compare to a model or perform basic mechanism research): P_{Effect} and $P_{observe}$ must approach 1.
  - If attempting to apply mitigation and measure its efficacy: P_{Effect} should approach 0 and $P_{observe}$ must approach 1.
  - **No one test-type and analysis fits all.**

Courtesy of Melanie Berg, SPACER2

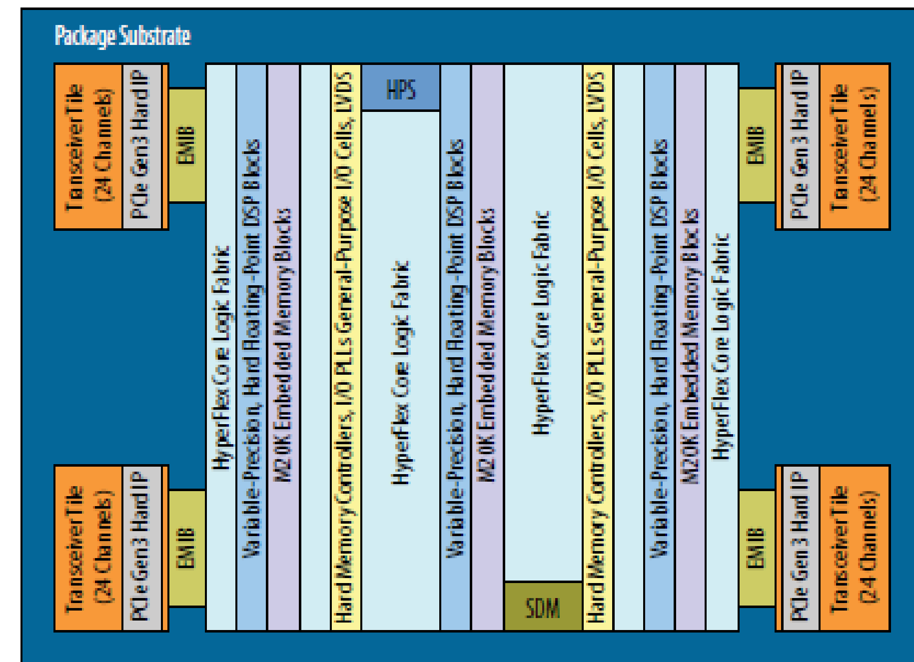
Space R² LLC Proprietary Information Presented by Melanie Berg

Ken's key takeaway:
The capabilities of the test system need to be included in the interpretation of complex data sets.
This is especially true for those test devices with a large number of operational states and IP blocks (processors, FPGAs, SOCs) and cases where some events are missed due to another event "crashing" the device.
Remember flux(ground test) >> flux(space).

Observability and Capture –

- Start with a complex modern multi-million transistor, multiple embedded and soft IP device like at the right
- Ions are randomly impacting across entire device (unless localization is done)
  - Any area may be “hit” at any time
- Operationally, not all areas of the device are active at one time nor are able to be interrogated “instantaneously” by a test system
- The “lag time” between the test system observability and when the particle actually impacted the device may cause either
  - Incorrect measurements of fluence to event or
  - Masked events
    - Area 1 has an ion event but has not yet been interrogated by the test system
    - Area 2 has an event that crashes the device and area 1 event never observed

Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram



HPS: Quad ARM Cortex-A53 Hard Processor System
SDM: Secure Device Manager
EMIB: Embedded Multi-Die Interconnect Bridge

Intel Stratix 10 GX/SX Device Overview Data Sheet
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10-overview.pdf

Test Levels

- One of the difficult challenges in testing any modern complex device (processor, FPGA, SOC,…) is:
  - Events that “crash” the device occur so readily that providing “traditional” 1E7 SEL fluence levels can be a challenge
  - In other words, if SEFIs keep crashing the device, will we be able to:
    - Obtain sufficient fluence levels for confidence?
    - Mask potential SEL events
  - The higher the blue screen of death rate, the harder it is to get to achievable SEL test levels
- Diatribe: high current <> SEL…
  - Be aware that there are a myriad of reasons (mostly circuit related SEUs) that can show increases in current consumption

Will it take ~100 test runs to get to an effective fluence of 1E7 if each SEFI crashes the device?

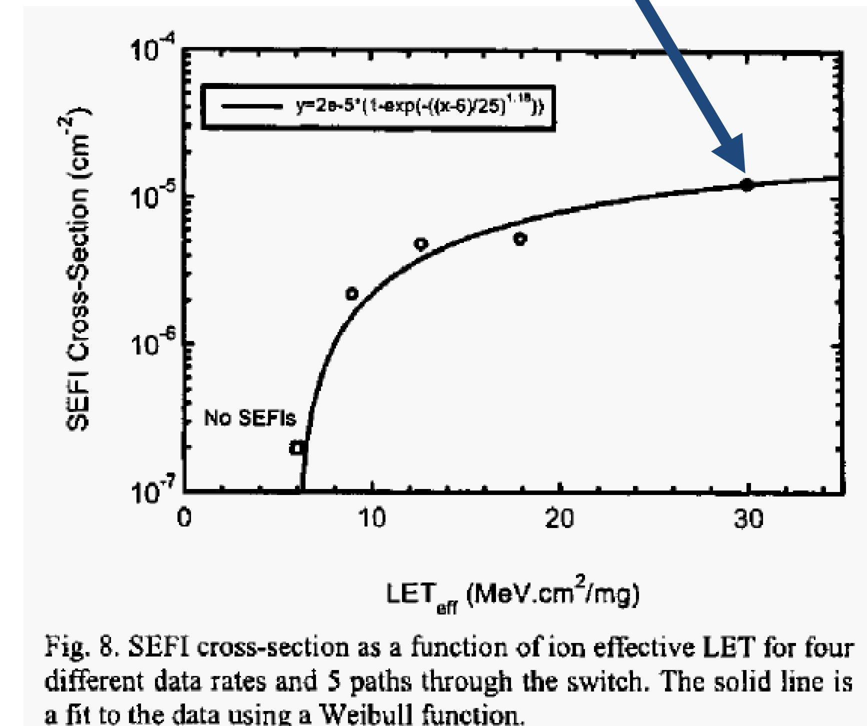


Fig. 8. SEFI cross-section as a function of ion effective LET for four different data rates and 5 paths through the switch. The solid line is a fit to the data using a Weibull function.

Stephen Buchner, et al, "Characteristics of Single-Event Upsets in a Fabric Switch (ADS151)“ https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1442463

Lessons Learned from Pandemic

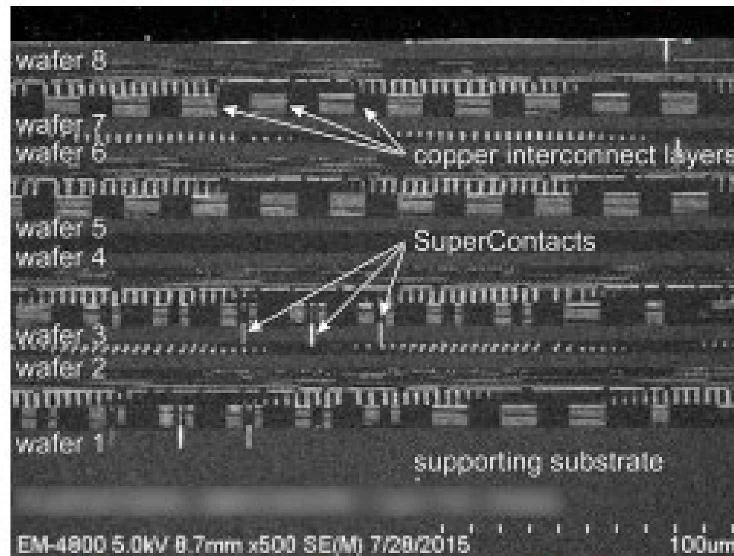
- Minimization of personnel on-site (reduced travel)
- Automation (and also for data analysis)
  - Increasing automation of test sets (reduces on-site personnel needs)
- Virtual testing
  - Remote data/control
    - IT security is a potential concern
  - Virtual reality options
  - Robotics?
- Flexibility counts
  - Beam time has become preciousssssss
  - Always have a backup plan if a test set doesn’t work

SYSTEM TESTING

A System is Much More Complicated (and Smaller) Than It Used To Be

Qualification of Complex Systems

How to Qualify ICs/Systems Like These for Space?



https://tezzaron.com/tezzaron-announces-worlds-first-eight-layer-active-wafer-stack/

One option:

Fly in economical, non-system-critical assessment vehicle, e.g., CubeSat

VU 2012 RadFxSat#1 team
EECE Senior Design

Space data
Workforce Development

B. D. Sierawski, et al., "CubeSats and crowd-sourced monitoring for single event effects hardness assurance," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 293-300, Jan. 2017.

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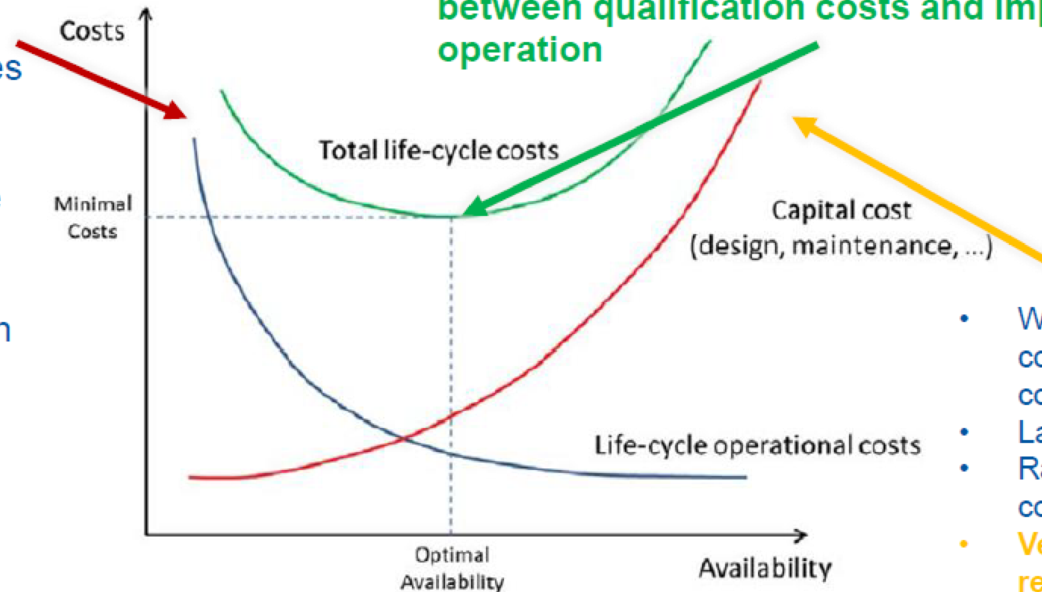
Courtesy of Daniel Fleetwood, IEEE NSREC 2020 Short Course

Changing Philosophies

R2E: from mitigation to prevention

- Components not qualified for radiation
- No radiation level estimates (monitoring, calculation)
- **Low system reliability/availability** due to radiation effects
- **High costs** associated to need of mitigating radiation effects once system is in operation
- (Situation in early LHC days)

- System level testing, common developments, monitoring and calculation
- **Rad-tol design targeting optimal compromise between qualification costs and impact on operation**



- Worst-case condition testing at component level
- Large margins
- Rad-hard components
- Very large system reliability at very high cost

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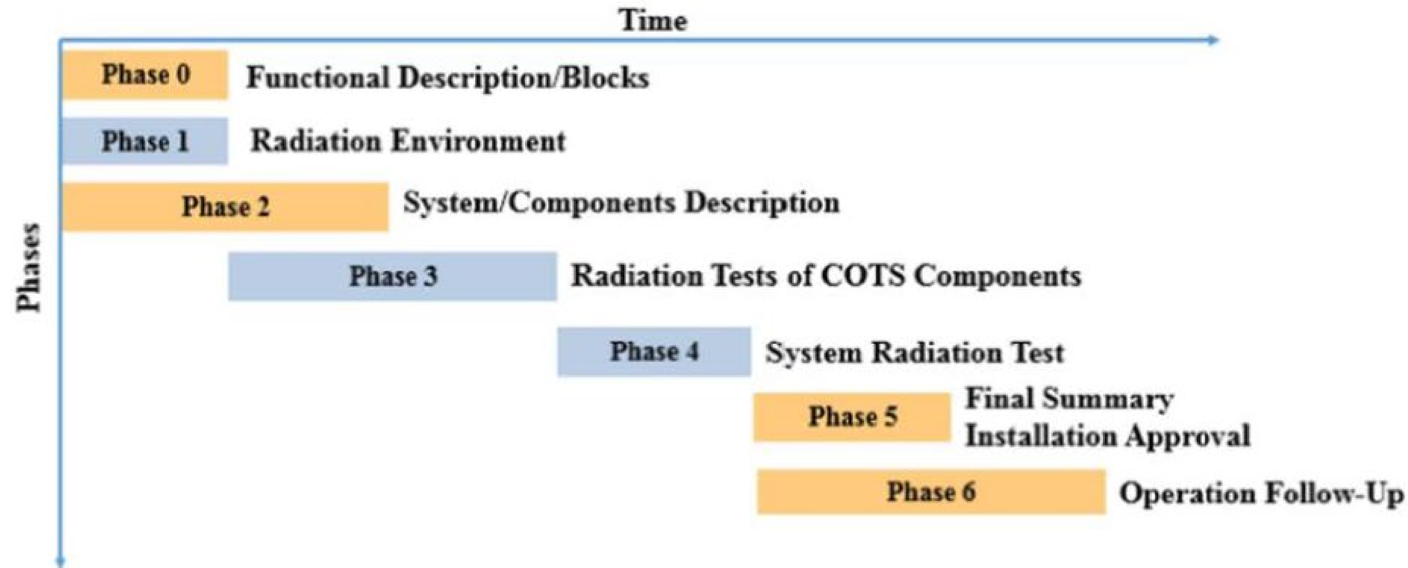
Key systems point: We've gone from:
- **High cost "has to work" to**
- **Optimized cost trading mission "-ilities" with radiation hardening.**

"Better is the enemy of good enough"

Courtesy of Ruben Garcia Alia, G-Rad 2020

RHA for COTS-based systems



- *Considering radiation tolerance constraints at very early stage of design*
- *Validation of radiation tolerance at system level before final production*

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Courtesy of Ruben Garcia Alia, G-Rad 2020

RHA for COTS is now commonplace and promulgating. ***Recommendation is always to perform radiation tasks (testing) as early as possible in a mission (or product development) lifecycle.*** ***System tests are now being included.***

SEE for Systems and Complex Devices- Diatribe on Changing Metrics - 1

- Traditionally, radiation and semiconductor folks don't think like systems folks.
  - In the early days when the upsets/bit-day (u/b-d) metric became "the standard", the test vehicles were SRAMs – a homogenous array usually being tested in a static mode. This made sense.
- However, we're now talking about devices that are neither homogenous, nor static. They have:
  - Heterogeneous integration: Memory structures (configuration and internal user areas - usually SRAM-like), configurable logic blocks, a variety of other I/O and IP as well as embedded control or processors, analog functions like voltage regulators and charge pumps, and so on
  - High operating speeds with a large number of operating state possibilities (state-space) – 2^n
  - Different transistor designs and even feature size design rules, … You get the drift.

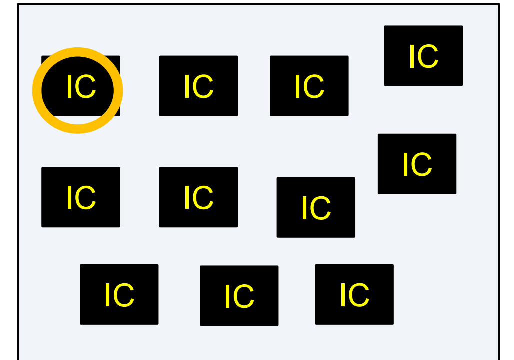
SEE for Systems and Complex Devices- Diatribe on Changing Metrics - 2

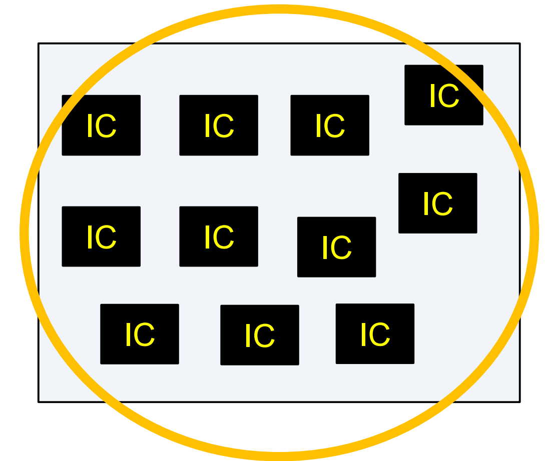
- What systems care about is not if a memory has a bit-flip, but **availability** of the device during mission operation (or specific time windows).
  - So the discussion moves more from the device to the reliability domain (credit: Melanie Berg) where we talk about events and fluence to event
    - Events in this connotation are only events that cause outages (down time) and not those that are either corrected by scrubbing (e.g. memories) or other embedded mitigation.
  - The event reliability will be VERY load dependent (% of memory utilized) and state-space/operating frequency.
    - These events could be divided simply into operational (outages) and data (lost data %) metrics.

Takeaway: from the system perspective, it's really about operational or data availability/reliability in the planned application

I’m Going to Need a Bigger Beam!

- Consider System SEE Testing as a two-step process
  - 1. Test of devices to identify error signatures/dominant event types
    - » Utilize information for device selection and to design SEU tolerance into the system
  - 2. Test of the system to evaluate design/mitigation performance (keeping in mind that it is an ACCELERATED test versus space particle rates)
    - » In essence, this is using the beam as a fault injector
- Step 1 treats the test as we’re used to: irradiate a single IC at a time
- Step 2, however, has options
  - Inject faults into an individual device/module at a time or
  - **Increase beam size to irradiate entire assembly (or portion thereof)**
    - » Currently, NSRL is the only domestic facility with this capability





THE FUTURE OF MODELING (FOR SEE TESTING)

Note: Material for the following 4 modeling charts were graciously provided by Mike Alles and Robert Reed/Vanderbilt-ISDE

Modeling and Simulation

- Like SEE in general, modeling and simulation (M&S) may be broken down into two general categories
  - Physics and timing (circuit simulation)
- Physics relates to the actual particle interaction and energy deposition, while timing is related to circuit operation and sensitive time windows when then energy deposition occurs
  - In other words, where the event occurs (geometry) and when the event occurs (temporally) determine if an observable effect propagates.
- For this talk, the focus will be on the physics and for COTS “black box” devices
  - In particular, the burgeoning challenge related to 2.5/3D structures and new material as it relates to SEE testing
- Consider two perspectives: the tester and the data analyst

M&S – Testers Questions Answered

- Why do I need to model the physics? It revolves around ensuring that the proper ion/energy combination is selected
  - Determine the penetration range and angular test capability based on ion/energy
    - Testability and beam selection to ensure sensitive volumes are traversed and Bragg peak issues are avoided
  - Track structure: will a higher energy beam at same effective LET hit more sensitive nodes?
    - Results comparison between ions/energies at “same” LET but different ion/energies may indicate different sensitivities
    - Increased delta ray production with higher energy creates a wider potential strike area

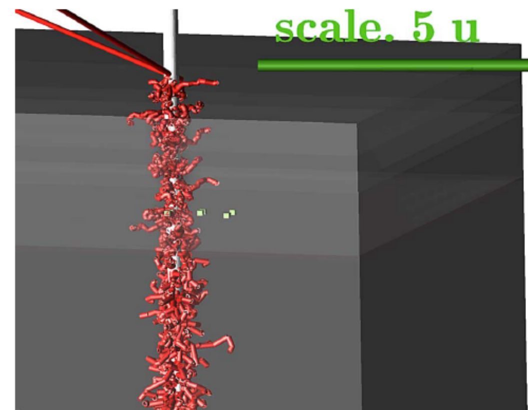


Fig. 6. Simulation of 280 MeV Fe interacting with the simulated SRAM array structure. The solid white tube represents the incident ion track. Red tubes represent generated δ-rays along the ion track. The green structures represent the sensitive volumes of neighboring devices.

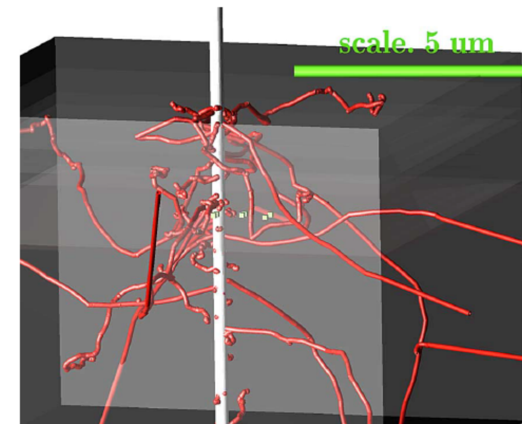
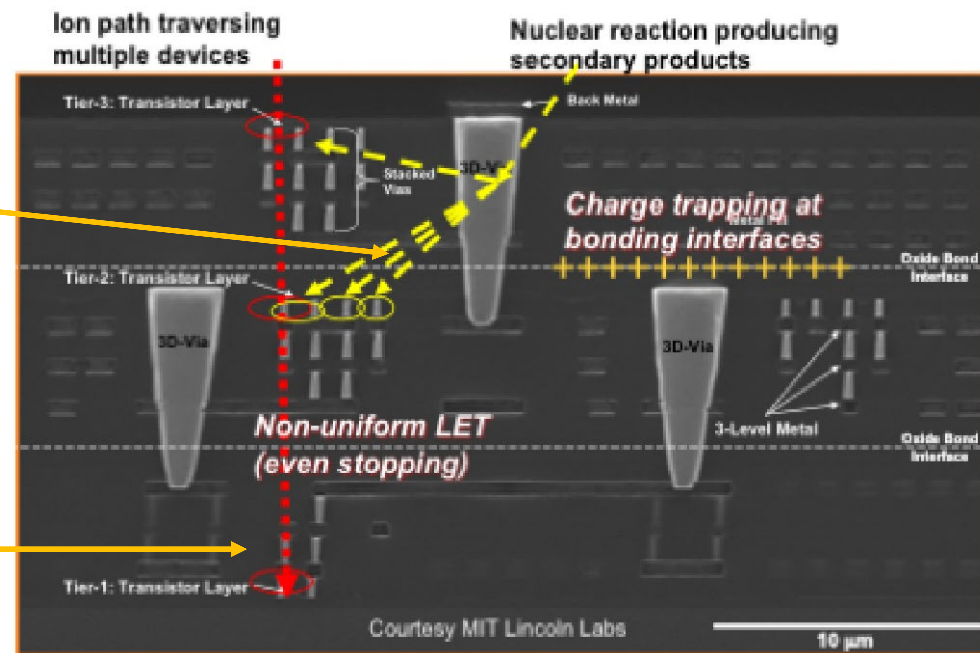


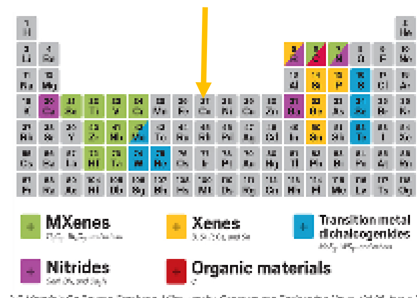
Fig. 7. Simulation of 28 GeV Fe interacting with the simulated SRAM array structure. The solid white tube represents the incident ion track. Red tubes represent generated δ-rays along the ion track. The green structures represent the sensitive volumes of neighboring devices.

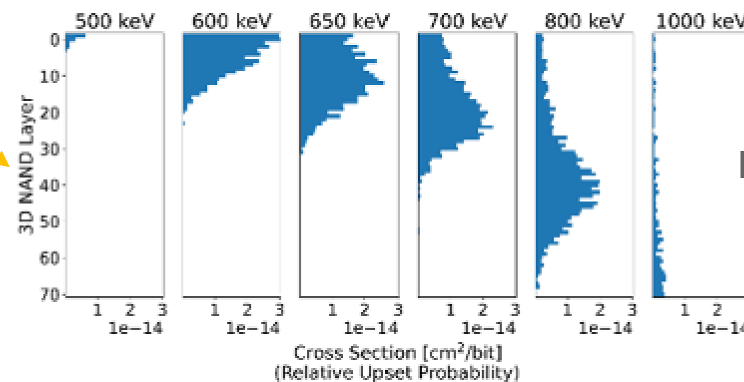
KING et al.: THE IMPACT OF DELTA-RAYS ON SINGLE-EVENT UPSETS IN HIGHLY SCALED SOI SRAMS, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010

M&S – Data Analysts Questions Answered

- Why do I need to model the physics? To interpret the data!
  - Risk of secondaries from material interaction
    - Data inconsistencies for spurious higher LET secondaries
    - Bigger issue as more and more materials are used within the device structure
- Non-uniform LET
  - Different LETs at different sensitive volumes in 3D structure
    - Effects may vary by “layer” within a device
- Outlier: new materials



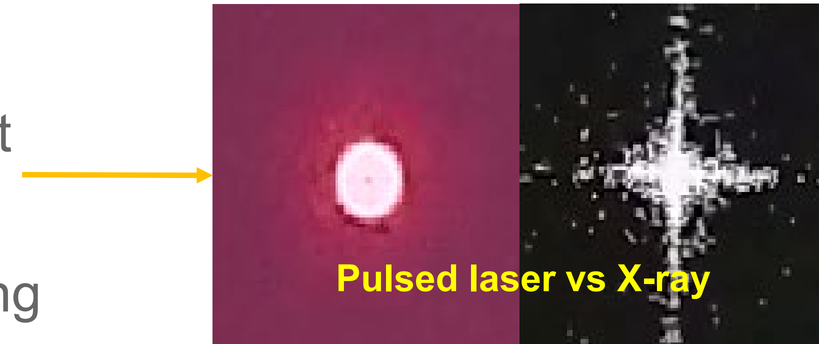




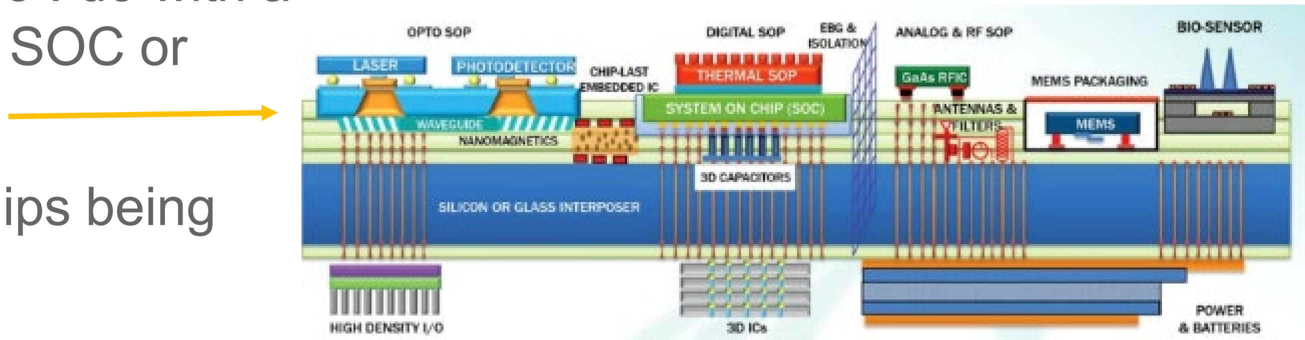
Images courtesy of Vanderbilt University

M&S – Comments

- New consideration: Co-extraction
  - Analyses of response mechanisms from different test conditions and sources
  - How accurate is the Laser/X-Ray, etc in predicting heavy ion response?
- The "timing" tools
  - The big question still stems on what do I do with a complex "black box" such as a COTS SOC or FPGA? (heterogeneous integration)
  - Current tools are great for M&S for chips being designed or simpler (i.e., op amp)…
  - Active (underfunded) area of research



Pulsed X-rays at Aerospace Argonne National Labs facility
Courtesy Vanderbilt-ISDE



Nhanced-semi.com

AND A FEW MORE…

A Few More Future Thoughts…

- Data sharing
  - Reduces test duplication and provides pre-screen for parts selection
  - Caveat emptor
  - Data sharing standards and formats
- Fault Injection
  - A useful tool in the toolbox to flip bits in devices that can be reached via software/operational means.
  - Not a complete SEE tool due to propagation and operational timing
- Functional safety
  - Popular in fields such as automotive, in essence, it’s the ensuring that faults don’t cause safety issues
  - Useful article: https://semiengineering.com/mitigating-the-effects-of-radiation-on-advanced-automotive-ics/
- Data analysis
  - Means of automating and interpreting in a more efficient manner
- WBG requires it owns separate set of discussions…

Summary

- The Future continues to evolve with a myriad of considerations ranging from device complexities and technologies to facility access and capability challenges to testability questions
  - Presented herein are some of those considerations
- Bottom line
  - Heavy Ion SEE testing isn't going away and is expected to have increasing demands
    - TAMU is still the prime facility for access and cost-efficiency, but increased needs for higher energy facilities should be considered

BACKUP