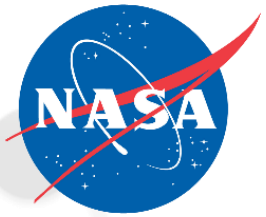

SEE Test Planning

Module 6a

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Acronym List

- dSEE: Destructive Single-Event Effect
- ESD: Electrostatic Discharge
- LDC: Lot Date Code
- LET: Linear Energy Transfer
- P/N: Part Number
- QML: Qualified Munitions List
- SEE: Single-Event Effect
- SEFI: Single-Event Functional Interrupt
- SEL: Single-Event Latchup
- SET: Single-Event Transient
- SEU: Single-Event Upset
- SoC: System on Chip
- SRAM: Static Random Access Memory
- TAMU: Texas A&M University
- TSOP: Thin Small Outline Package

Module 6: Test Planning and Preparation

1. Introduction to Bootcamp
2. Environments
3. Basics of SEE
4. Cyclotron Overview
5. Requirements and Goals
6. ***Test Planning (6a) and Preparation (6b)***
7. Test Execution Refined
8. Facility Considerations and Differences
9. Data Analysis and Interpretation
10. Data Put to Use
11. The Shape of Things to Come
12. Common Mistakes

Outline

1. Starting Point for Module 6a (comparison to 6b)
2. Practical Early Questions
3. Notional Test Planning Case Studies
4. Planning a Beam List
5. Planning Nuances
6. Planning Logistics (Travel, Shipping, Personnel, Safety Training)
7. Cheat Sheet and Final Thoughts

How do modules 6a and 6b relate?

- Test planning (6a) and preparation (6b) are closely related in practice, sometimes done by the same person, and sometimes not.
- They may be done in sequence or in parallel depending on practical considerations (lab space?), funding availability ($ for paperwork but not for hardware) and test complexity (hard stuff needs more planning).
- Loosely, test planning is taking requirements and developing a series of actions that must be performed to verify a part meets requirements (*WHAT are you going to do?*). Test preparation is taking requirements and/or a plan and developing a means to execute a test (*HOW are you going to do it?*).

Starting Point for Module 6a

- **We will work the three case studies introduced in Module 5, and develop them for eventual testing in Module 7**
- **In general, you are at a place where you have been instructed to plan a specific type of test on a specific part, ideally with requirements in place:**
  - "Test a generic lot of AD1234X for single-event latchup, with a fluence of at least $1x10^7/cm^2$ at an effective LET of at least 75 MeV·cm^2/mg."
  - "Test the flight lot of IRHF1234 for destructive SEE to a normal-incidence LET of at least 37 MeV·cm^2/mg and a drain voltage of at least 100 V, starting at 40 V and increasing in 10 V steps. Find the highest voltage at which at least 3 parts pass to $1x10^6/cm^2$."
  - "I need a SEU test of the SRAM from Planet Explorer II. I think it's a parallel memory, but I'll get back to you."

Where we hope to end this module

- ✓**We have a plan to meet our requirements.**
- ✓**Our plans are written (and approved, if applicable).**
- ✓**We've thought through our Plan A and Plan B and are comfortable making decisions on the fly.**

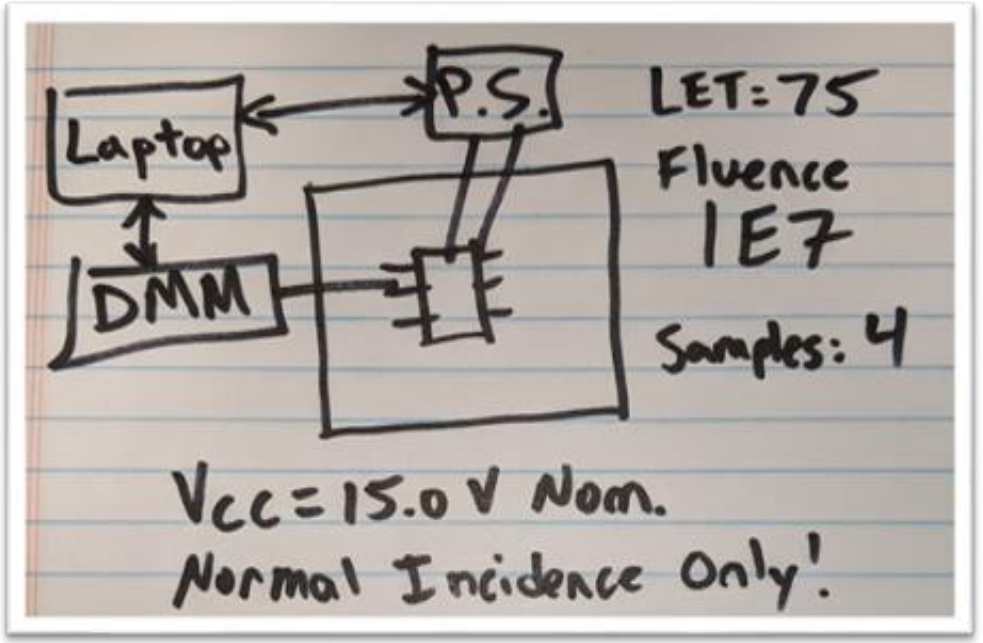
From a TAMU SEE Bootcamp standpoint, we hope to end with an idea of what an SEE test plan looks like, and the processes involved in generating one.

Practical Early Questions (Test Plans)

- Before we commit significant effort, what's going to drive the planning?
  1. **Is this a simple device that I understand?**
     - I know what a voltage reference does and how to describe an SEE test.
     - I do not know everything a processor can do, especially for a given application.
  2. **Do I have a known test facility and time allocation?**
     - You can plan an SEE test with unknowns, but obviously that will impact decisions
     - If you have flexibility to choose when and where and how long, you can plan the test YOU want or need
  3. **Have I been given clear requirements and, if applicable, application usage?**
     - Here's where research vs. flight vs. qualification is very different
  4. **Do I have parts yet? Can I get them? How many can I get? Have I talked to a test engineer?**
     - These will all drive decisions about what kind of testing is possible, how many iterations are achievable, and what sort of data output I should expect.
  5. **What resources are available? Budget? Labor (both $ and people)?**

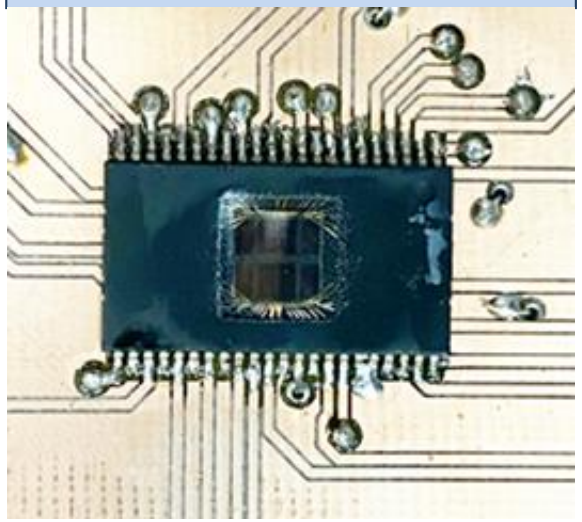
A Notional Test Plan

- Early on, the test planner must identify:
  1. **What am I trying to find out?**
  2. **How will it be irradiated?**
     - ➢ Power on/off, temperature, duration, vacuum, angle, nominal vs min/max, etc
  3. **What beams are desired or required?**
     - » LET, range, angle, energy, flux, fluence, etc.
     - » Includes facility-specific details as available
  4. **What measurements will be performed?**
     - » Digital data capture, current measurement, transient waveforms, etc
  5. **What does the test flow look like?**
     - » How will the part be operated for each run (voltages, data rate, pattern, mode, etc)
     - » List all combinations needed, potentially with a decision tree



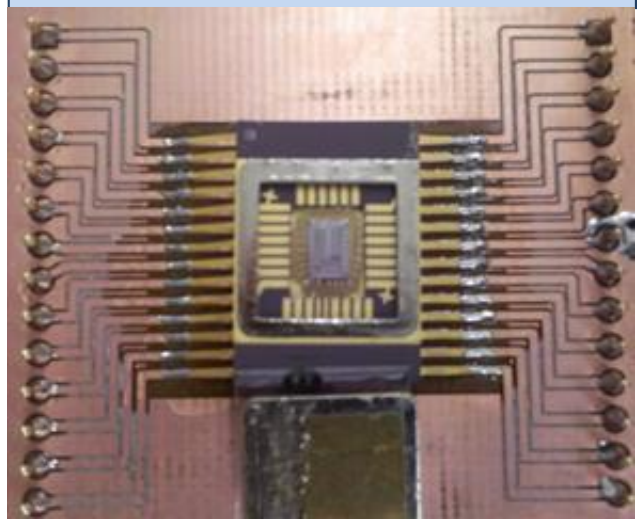
Case Studies: Three Devices (from Module 5)

TSOP SRAM



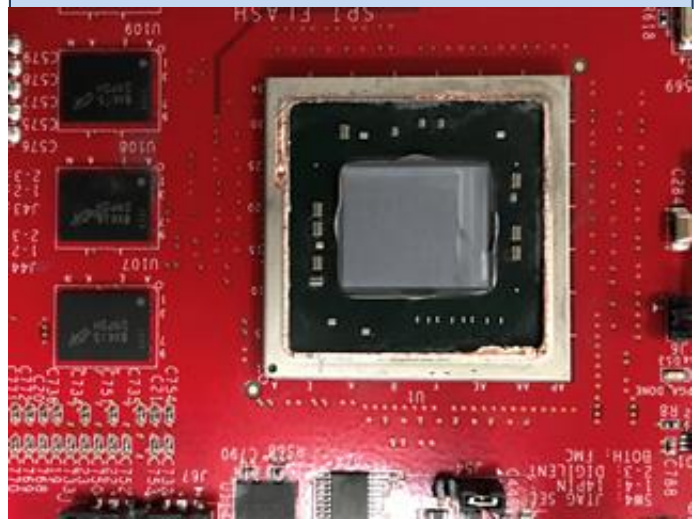
- Understood that there will be SEU/SBU
- Want to “screen” for SEL

QML Amplifier



- **Already guaranteed to not have DSEE**
- **Want to characterize SET**

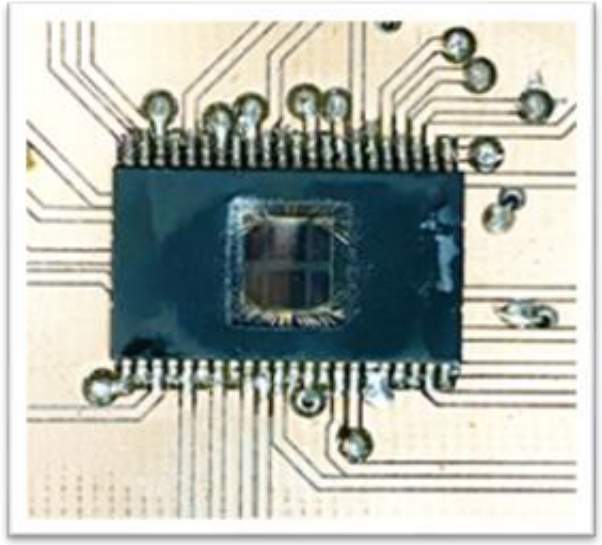
COTS SoC



- **Very little known on radiation response**
- **Want to characterize as many signatures as possible**

Test Case #1 – SEL Test, Commercial SRAM

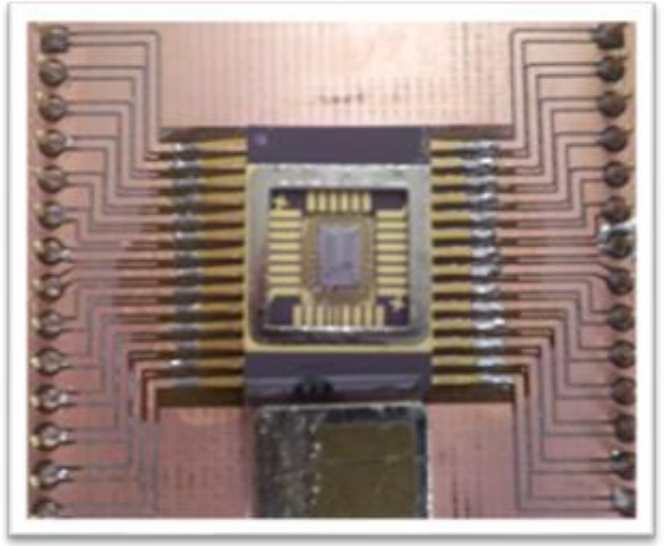
- **What am I trying to find out?**
  - If the device is susceptible to SEL and at what LETs. Ideally we would find a threshold LET for SEL.
- **How will it be irradiated?**
  - The part will be powered on to 110% of nominal supply voltage, heated to 85°C in air, and held in a static mode.
- **What beams are required?**
  - LET > 75 MeV·cm^2/mg at the die surface will meet program requirements for this test.
  - We have been assigned time at Texas A&M. We are going to plan for 15 MeV/amu Au (LET ~80) and we need a fluence of 1x10^7/cm^2 to rule out SEL.
  - We desire several other beams for possible additional testing: 15 MeV/amu Ag (LET ~42) and Cu (LET ~18)
  - Since the part is a standard silicon CMOS device in a wirebond package, we are not *especially* concerned about heavy ion range, though SEL is a factor of depth. Anything close to 100um range will be fine (ask if you don't know)



Test Case #1 – SEL Test, Commercial SRAM

- **What measurements will be performed?**
  - The power supply will continuously log supply current at least twice per second. The supply limits will be set well above normal values (remember, this is a destructive test) so that post-test analysis is not constrained by hardware limits. However, use some sound judgment to avoid destroying your test setup, hardware, or the facility.
- **What does the test flow look like?**
  - Since we are trying to meet flight program requirements, we choose to start with a worst-case "go/no-go test." This will be 85°C at 110% rated voltage and 15 MeV/amu Au (LET ~80). We'll test two parts here and we'll stop immediately upon SEL.
  - If the part latches and beam time remains, we desire to test with lower LET to quantify risk to project. In this case, exposures at an LET of around 37 and 20 are useful to bound rates.
- **What hardware is necessary?**
  - Coordinate this section with the test engineer (which may also be you) prepping the test setup. List all hardware needed, traceability and calibration details, and the manner in which it must be connected on-site.

Test Case #2 – SET Test, QML Amplifier



- **What am I trying to find out?**
  - If the device outputs voltage transients of interest to the flight design, what they look like, and how often they may occur during the mission.
- **How will it be irradiated?**
  - The part will be powered, not heated, in air, and operated dynamically.
- **What beams are required?**
  - An LET > 75 MeV·cm^2/mg at the die surface will meet program requirements to completely write-off the possibility of transients. However, in our experience, parts like this often produce some type of transient waveform.
  - We need low LET beams to look for either a threshold, or at least to measure the most common transients that will drive the rate, and we need a moderate-to-high LET to find those worst-case transients that might break something. We will plan for 15 MeV/amu Ne, Ar, Cu, Ag, Au at TAMU. We have no concerns about range with this part as SETs are created in the thin active layers of devices.
  - We will run tests to a fluence of 1x10^6/cm^2, or until a large number of transients (several hundred) have been captured on a given run.
  - Beam flux will be limited such that our measurement hardware is not overwhelmed with rapid transient captures and our device is not subject to multiple hits during one frame

Test Case #2 – SET Test, QML Amplifier

- **What measurements will be performed?**
  - The power supply will continuously log supply current at least twice per second. An oscilloscope will be set to automatically trigger on voltage transients exceeding 10 mV from normal values. The count of triggers and raw waveforms will be saved.
- **What does the test flow look like?**
  - We need to test at a variety of LETs to compute a rate. It is unlikely the part is SET-immune and our program does not require it to be, so we'll start in the middle with 15 MeV/amu Cu (LET ~18). This is high enough to include the vast majority of particles encountered in space while also serving as a good test of the setup (high enough to likely create SET without excessive tune time).
  - If transients are rare and small (this is judgment) with Cu, we will move up to Ag. If the cross-section jumps several orders of magnitude, then the Cu run may have been near the threshold. We should test something in between. If the cross-section doesn't change, this part is likely just insensitive and we're on the flat part of the curve, so we may look for a threshold at a lower LET.
  - Or, if transients are very common and large with Cu, then we definitely want to move lower. Next beam will be Ar, with the same assessments.

Test Case #2 – SET Test, QML Amplifier

- This plan can get very detailed on paper to account for all possibilities, but is not fundamentally complicated – the idea is to get at least 3, preferably 4-5 points on a cross-section vs LET curve so that a rate can be effectively calculated. They need to be spread across varying LETs and should include at least 2 orders of magnitude of cross-section.

- **What hardware is necessary?**
  - Coordinate this section with the test engineer (which may also be you) prepping the test setup. List all hardware needed, traceability and calibration details, and the manner in which it must be connected on-site.

Test Case #3 – Generic SEE Test, SoC

- **What am I trying to find out?**
  - This is a research project. I want to understand how this system-on-chip responds to a high-radiation environment. This test will largely focus on data corruption (SEU) and functional interruptions (SEFI). We will also check for unexpected destructive SEE.
- **How will it be irradiated?**
  - The part will be powered on to nominal supply voltage, at ambient temperature, in air, and will be tested with many different test routines. We want to test at normal incidence and multiple angles, including multiple directions (facial rotations)
- **What beams are required?**
  - Due to the thickness of the device substrate, **range of at least 200 um** before the Bragg peak is required.
  - Low LET beams will be the focus of the test to characterize particles driving the highest on-orbit rates.
  - We have been assigned time at Texas A&M. We are going to plan for **25 MeV/amu** Ne (LET ~1.7), Ar (LET ~5.5), and Cu (LET 13.3). Tests will be to a variety of fluences, typically to $1x10^6/cm^2$. An additional test with Xe (LET ~40) at 60 degrees incidence is desired to evaluate for any destructive effects.
  - It is likely that low fluxes ($<1x10^3/cm^2/s$) will be required as the device is expected to be very sensitive.

Test Case #3 – Generic SEE Test, SoC

- **What measurements will be performed?**
  - The power supply will continuously log all supply currents at least twice per second. A pair of computers, one running LabVIEW and another running a custom Python script, will interact with the hardware to capture high-speed digital and analog data channels.
- **What does the test flow look like?**
  (author's note – this is highly generic and shortened for time)
  - Since we expect a sensitive device, we will start conservatively to give our test the best chance of completing a beam run without getting "weird." Error signatures are likely to be complex and potentially hidden/delayed. We will run with our lowest LET and a flux of $1x10^3/cm^2/s$ while operating the device in a simple "heartbeat" configuration. Upon unrecoverable error (lack of heartbeat), the test will be terminated.
  - Then, we can begin adding complexity to the test. For this test, we will run a memory testing routine, a loop-back data I/O routine, and an inflight-reconfiguration routine on separate runs and evaluate success or failure while logging statistics on the number of corrected bit errors in internal memory for each run.
  - If a large number of errors is accumulating, or unrecoverable errors are occurring quickly, the flux should be lowered to $1x10^2/cm^2/s$.

Test Case #3 – Generic SEE Test, SoC

- For each beam, testing should be conducted at a 60 degree angle using two perpendicular angles of rotation (e.g. from the top-side and from the right-side of the PCB). These tests will help identify angular effects within the device, particularly the memory structures.
- For each beam configuration, the device should be tested in both nominal and low-voltage modes, and at high and low clock speed.

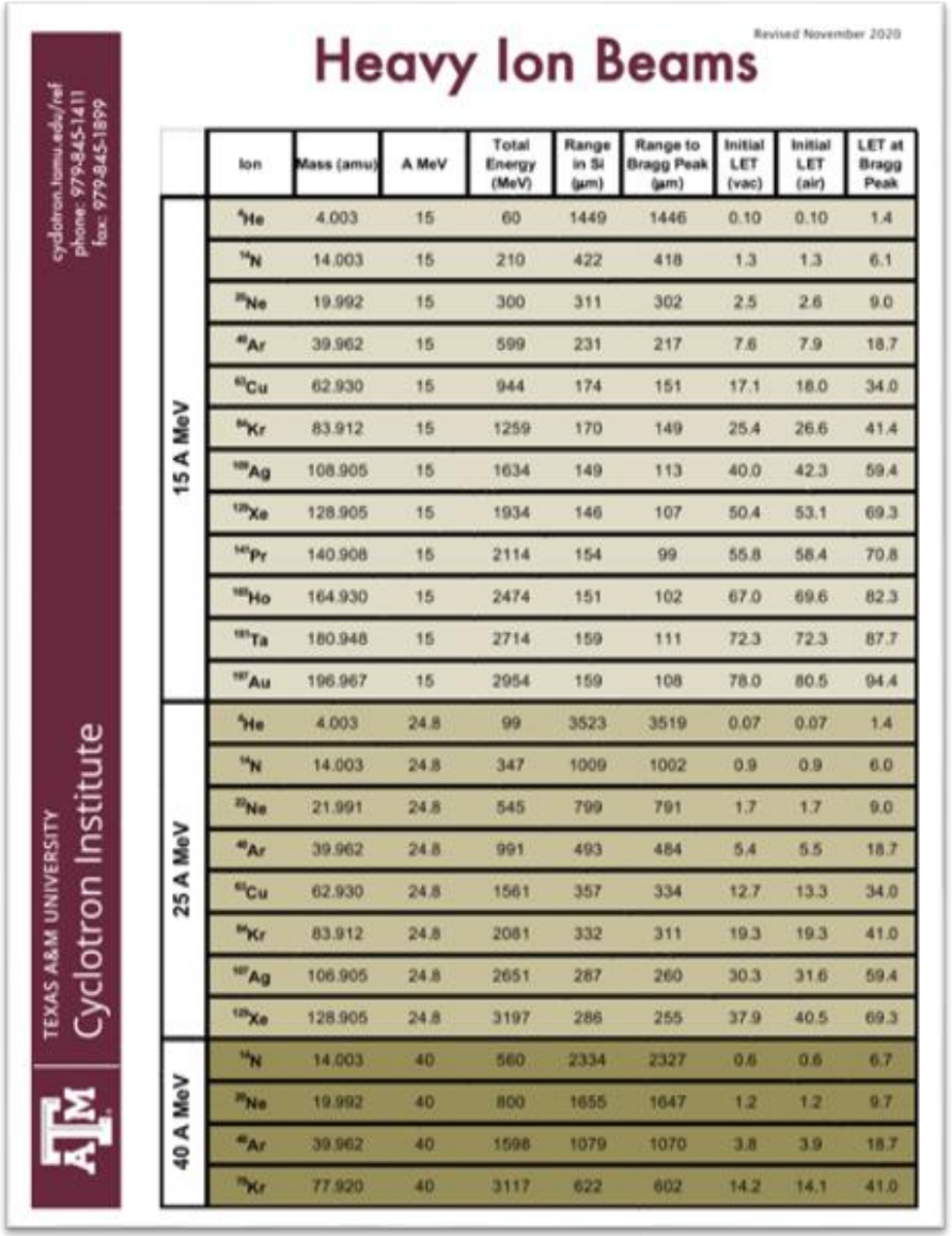
- **What hardware is necessary?**
  - Coordinate this section with the test engineer (which may also be you) prepping the test setup. List all hardware needed, traceability and calibration details, and the manner in which it must be connected on-site. For an SOC, the list of hardware may be substantial just to configure and operate the component on a benchtop.
  - This device is heavy and requires both a custom-built mounting plate and a liquid cooling system to operate without a heat sink. These will require early design and procurement.

Test Planning Tips

- **A test plan *should* stand alone** such that any employee (with experience) can execute the test to your requirements without further input.
- **It is also unrealistic to *expect* that**. Understand that successful test performance requires both thorough planning and the ability to turn on a dime and adapt to facility changes, part failures, time shortages, interesting results, etc.
- However, **a walk-thru of tests planned, possible outcomes, and decision tree** is particularly helpful if test planner/lead will not be on-site.
- **Remember that order of testing matters**
  - If you have limited supply of parts don't run your worst-case test first
  - If you break your only sample, the test is over!
  - If you have a million parts, consider going for that worst-case – you may save a lot of time
  - May need to start with whatever beam/tune is provided by previous team to avoid excessive downtime. Also consider your follow-on team as a courtesy if possible.
  - First runs serve as a baseline for operation of your test setup – find something likely to produce data

Planning a Beam List

- **Most obvious parameter is LET**
  - You need high LET for destructive SEE, and this may drive your choice of tune at the facility
  - You want a variety of LET for non-destructive SEE, and not all tunes will have the same variety of LET available.
  - Certain tests may require very low LET (<1 MeV·cm^2/mg)
- **LET doesn't matter without range**
  - Rarely an issue for traditional, wirebonded, monolithics
  - Very much an issue for flip-chip parts or parts with deep vertical structures (high voltage power components)
  - Extremely problematic for multiple-die packages



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Heavy Ion Beams

Revised November 2020

	Ion	Mass (amu)	A MeV	Total Energy (MeV)	Range in Si (μm)	Range to Bragg Peak (μm)	Initial LET (vac)	Initial LET (air)	LET at Bragg Peak
15 A MeV	^{4}He	4.003	15	60	1449	1446	0.10	0.10	1.4
	^{14}N	14.003	15	210	422	418	1.3	1.3	6.1
	^{20}Ne	19.992	15	300	311	302	2.5	2.6	9.0
	^{40}Ar	39.962	15	599	231	217	7.6	7.9	18.7
	^{63}Cu	62.930	15	944	174	151	17.1	18.0	34.0
	^{84}Kr	83.912	15	1259	170	149	25.4	26.6	41.4
	^{109}Ag	108.905	15	1634	149	113	40.0	42.3	59.4
	^{129}Xe	128.905	15	1934	146	107	50.4	53.1	69.3
	^{141}Pr	140.908	15	2114	154	99	55.8	58.4	70.8
	^{165}Ho	164.930	15	2474	151	102	67.0	69.6	82.3
	^{181}Ta	180.948	15	2714	159	111	72.3	72.3	87.7
	^{197}Au	196.967	15	2954	159	108	78.0	80.5	94.4
25 A MeV	^{4}He	4.003	24.8	99	3523	3519	0.07	0.07	1.4
	^{14}N	14.003	24.8	347	1009	1002	0.9	0.9	6.0
	^{22}Ne	21.991	24.8	545	799	791	1.7	1.7	9.0
	^{40}Ar	39.962	24.8	991	493	484	5.4	5.5	18.7
	^{63}Cu	62.930	24.8	1561	357	334	12.7	13.3	34.0
	^{84}Kr	83.912	24.8	2081	332	311	19.3	19.3	41.0
	^{107}Ag	106.905	24.8	2651	287	260	30.3	31.6	59.4
	^{129}Xe	128.905	24.8	3197	286	255	37.9	40.5	69.3
40 A MeV	^{14}N	14.003	40	560	2334	2327	0.6	0.6	6.7
	^{20}Ne	19.992	40	800	1655	1647	1.2	1.2	9.7
	^{40}Ar	39.962	40	1598	1079	1070	3.8	3.9	18.7
	^{78}Kr	77.920	40	3117	622	602	14.2	14.1	41.0

Planning a Beam List

- **My personal process for destructive SEE:**
  - If I am planning a go/no-go test, or have strong reason to believe the part will pass, I start with my worst-case test and see what happens.
  - *This is not smart if you have 1 or 2 samples*, but can save time. Beam time is scarce resource.
  - If it breaks, move down significantly before coming back up in LET (or pack up the test if failure is the only result you needed). Parts that latch at 75 often latch much lower.
- **Angles and degraders can change our effective LET, but both have tradeoffs, especially for dSEE.**
  - Angles increase effective LET for relatively flat RPPs (pancakes) but are not worst-case for some parts (most vertical power MOSFETs or Schottky diodes)
  - Angles can increase error counts for other reasons too (MBU)
  - Face angle matters, occasionally.
  - Degraders can reduce energy to increase LET, but decrease range and add spread and uncertainty to the LET

Planning a Beam List

- **My personal process for non-destructive SEE on ~simple devices**
  - Start with a mid-LET beam (~15-20 MeV·cm^2/mg)
  - Less chance of destructive event or so many errors that your data is saturated, but allows for identification of error signatures AND early verification that you have a functioning setup.
  - Then, move up or down to find a threshold LET
  - Soft error rates are usually dominated by low LET particles, so higher LET cross-sections add less value. The threshold is critical.
- **For non-destructive SEE on complex devices**
  - Likely need to start lower and stay low while characterizing effects to avoid masking sensitive errors (which will be common) with larger, rarer events. It's good to have a baseline where we can complete a test to the targeted fluence.
  - But, this is really a subject all its own! Always look for a subject matter expert or veteran tester for advice if you can't describe everything a part can do.

How much time do I need?

- **Beam time is neither cheap nor abundantly available.**
- As your test plan develops, try to estimate the amount of time necessary to setup your test in the chamber, run your tests, change parts, and tear down.
- **This takes experience** to understand how slow your tests will be compared to the bench top!
- As a **rough** estimate, an SEL test of a 1 or 2 parts can be done in 4-6 hours if all goes well. An SEU or SET test over multiple ions and operational modes can take 8-24 hours. A characterization of a new SoC or FPGA can be multiple 24 hour shifts!

Planning Nuances

- **For all the obvious things to plan, you'll spend lots of time dealing with the not-so-obvious**
  - Is the facility expecting us, and do they know who is coming and when?
  - The previous team running the beam may leave you with a difficult beam tune. Coordination prior team and the next team to minimize beam waste is important, and you may be able to plan this out ahead.
  - LET/Angle/Degraders/Range (addressed more in module 7): Not all LETs are the same. If you don't know, ask!
    - » Note that even angles are not all the same. Some devices are more susceptible from one axis vs. another.
  - Time/automation control: Not all fluences are the same
    - » Manually-aborted runs will have error bars determined by user response time, and your computed error rates will be lower than reality if an error occurred at t = 1 ms and you didn't hit "STOP" until t = 1.5 s. Plan realistic test abort conditions.
    - » Fluence to failure is hard to compute after the fact. If you see something, just stop the run and figure it out then. Plan for many runs if you are testing SEFI.

Formalizing the Plan and Planning for Success

- **Ok, so you wrote a test plan. Are you done?**
  - Travel
  - Shipping
  - Personnel scheduling
  - Safety Requirements

Planning Logistics: Travel

- **Contact the facility about arrival procedures (badging requirements?)**
- **Plan a realistic travel schedule and alert travelers early**
  - Get dates blacked out on personnel schedules asap
  - Consider likelihood of flight delays w.r.t. your test schedule
- **Plan a realistic operational schedule and get staff buy-in**
  - You may like 24 hour shifts but not everyone does, and a tired assistant is dangerous!
- **Schedule arrivals** in time to rest before long shifts, **test your setup**, and make fixes as necessary.
  - Very risky to arrive same day and start testing right away.
- **Schedule departures** late enough to close out with facility, ship hardware, and comfortably make flight.

Planning Logistics: Shipping

- **Shipping time at YOUR workplace**
  - Investigate where your crates need to go and when
- **Receiving time at TEST facility**
  - Some facilities receive directly to the cyclotron loading dock, others have delays for internal receiving/delivery (ask them!)
- **Proper protection of hardware during shipping**
  - If your organization does not regularly ship, you may need to acquire robust crates
  - Don't overfill, and don't assume it won't be tipped.
  - Don't let your parts get squashed by a 90 lbs power supply.
- **Occasionally you may not be able to return hardware immediately.**

Planning Logistics: On-site Personnel

- **Bring a variety of personnel to the test**
  - Someone will need to solder, tinker with software, etc.
- **If you have more than one test planned, someone in your organization should maintain a master schedule for your trip**
  - Include facility needs (ions and tunes) and personnel on the schedule
- **Schedule time for breaks, meals, repairs/modifications**
  - Interleaving 12 on & 12 off works pretty well. An 8 hour break is not sufficient after a long day once you include commute, meals, and getting ready for the next test.

Planning Logistics: Safety

- **Personnel Radiation Safety**
  - Your organization may have its own rules - Check with your RSO
  - If it's a new facility, ask about paperwork, advance training, or on-site training requirements. Yes, you may get turned back at the gate if you forget….
  - Personal dosimeters are common, but significant exposure is not (especially at heavy ion facilities). Still, plan to perform work outside of the "cave"
- **Hardware Safety**
  - Check for facility limitations if you're doing anything remotely non-standard
    - » 50V and up worth asking about. Facilities do have their own HV rules.
    - » Cryogens will require advance notice and possible training
    - » ESD accommodations vary – bring your own wrist straps, mats, and monitors.

Test Plan Cheat Sheet

This isn't exhaustive, but if you can answer these, you probably have a decent plan.

- **Who, what, when, where, why?**
  - WHERE: Facility details
  - WHEN: Dates
  - WHO: Intended personnel, or at least skill sets
  - WHAT: Part description and traceability (P/N, package, LDC) and equipment list including S/N and calibration data if applicable. Include photos if able.
  - WHY: Type of testing planned and requirements
- **How?**
  - Intended beam list (ions, energies, and ranges)
  - Part configuration (Jumpers? Connectors in use? Wiring diagram)
  - Power configuration - Including elevated voltage levels, expected nominal currents
  - Stimulus - AC/DC inputs, frequencies, signal shapes
  - Measurements - Error rates, SEL current thresholds/limits, hardware settings, cable types, estimated oscilloscope channel and trigger settings
  - Plans for data collection and storage
  - Temperatures for testing

Plan to Standards and References

- **JESD57A** - TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION
- **ESCC Spec 25100** - SINGLE EVENT EFFECTS TEST METHOD AND GUIDELINES
- **ASTM F1192** - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices
- Various **RHA / Test Method Guideline Documents** (NEPP, NASA, ESA)
- **JESD89A** - MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

Module 6a: Final Thoughts

- **Test planning in the real world can take so many different forms…**
  - Years-long efforts to design and qual a rad-hard processor or power converter
  - Quick screens on commercial parts with nothing more than a power supply attached
  - Board-level proton testing, part-level heavy-ion testing, transistor-level laser testing
- **Ultimately you are planning a test that will provide enough information to answer some question.**
  - You must understand the part to be tested
  - You must understand the test requirements or expectations levied upon you
  - You must collect sufficient data to make quantitative and qualitative assessments of the test
  - You need to be able to pack everything, ship it, reassemble in a day and test in a few hours/days.
- **It takes time and practice to get good at this. Learn from others, and learn from your own experience.**