

SEE Test Preparation

Module 6b

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Acronym List

- dSEE: Destructive Single-Event Effect
- ESD: Electrostatic Discharge
- LDC: Lot Date Code
- LET: Linear Energy Transfer
- P/N: Part Number
- QML: Qualified Munitions List
- SEE: Single-Event Effect
- SEFI: Single-Event Functional Interrupt
- SEL: Single-Event Latchup
- SET: Single-Event Transient
- SEU: Single-Event Upset
- SoC: System on Chip
- SRAM: Static Random Access Memory
- TAMU: Texas A&M University
- TSOP: Thin Small Outline Package

Module 6: Test Planning and Preparation

1. Introduction to Bootcamp
2. Environments
3. Basics of SEE
4. Cyclotron Overview
5. Requirements and Goals
6. ***Test Planning (6a) and Preparation (6b)***
7. Test Execution Refined
8. Facility Considerations and Differences
9. Data Analysis and Interpretation
10. Data Put to Use
11. The Shape of Things to Come
12. Common Mistakes

How do modules 6a and 6b relate?

- Test planning (6a) and preparation (6b) are closely related in practice, sometimes done by the same person, and sometimes not.
- They may be done in sequence (in either order) or in parallel depending on practical considerations (lab space), funding availability (\$ for paperwork but not for hardware) and test complexity (hard stuff needs more planning).
- Loosely, test planning is taking requirements and developing a series of actions that must be performed to verify a part meets requirements (WHAT are you going to do?). Test preparation is taking requirements and/or a plan and developing a means to execute a test (HOW are you going to do it?).

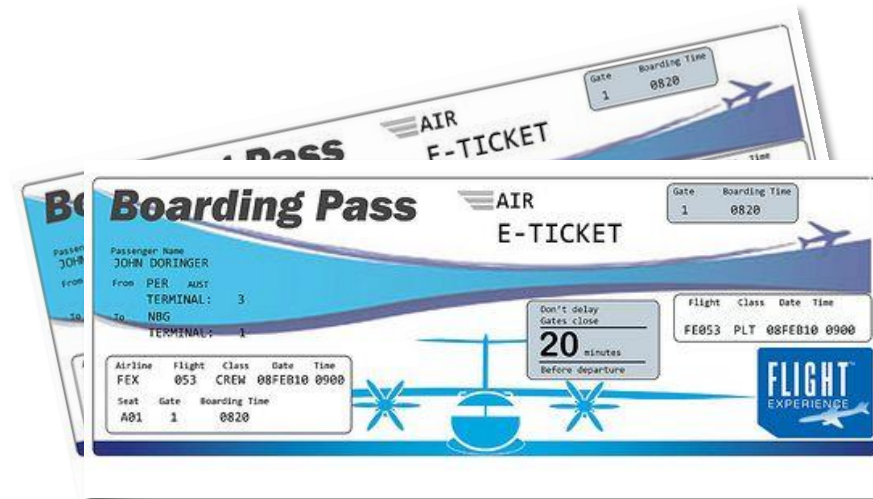
Starting Point for Module 6b

- **Again, we will work the case studies from Module 5 and prepare the parts and their physical test setups for testing.**
- **You are the test engineer assigned to this test, and you have been instructed in any of the following ways:**
 - “Get those AD1234X ready for single-event latchup testing. We need to test them at elevated temperature and under a static DC bias.”
 - “Here’s the test plan I drafted for the IRHF1234. The project office delivered decapsulated parts yesterday. Can you handle the rest of the test prep? We’re probably travelling in four weeks.”
 - “I need a SEU test of the SRAM from Planet Explorer II. I’m slammed over here; can you help me out?”

Where we hope to end this module

- ✓Parts are ready for irradiation
- ✓Tests have been demonstrated successfully
- ✓Equipment has shipped

This is not a EE degree in an hour. Your skills, experience, and judgement will all be needed to prepare an effective test setup!



Practical Early Questions (Test Prep)

- Before we commit significant effort, look for hardware show-stoppers:

1. Can I get beam on silicon?

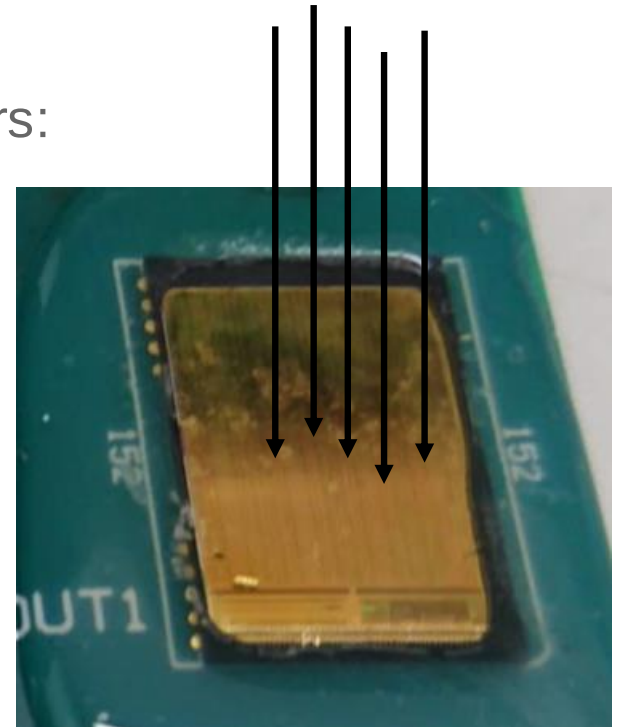
- Flip chip parts may need thinning
- Plastic parts need etching
- Heat sinks may be in the way
- Power devices may have protective coatings
- Hybrid parts may have components blocking other components

2. Can I conceive a test board that will work?

- A breakout board for a voltage regulator is “easy” to put in front of a beam
- A PC motherboard or assembled instrument box is not
- Manufacturer demo/eval boards are very convenient, not always perfect

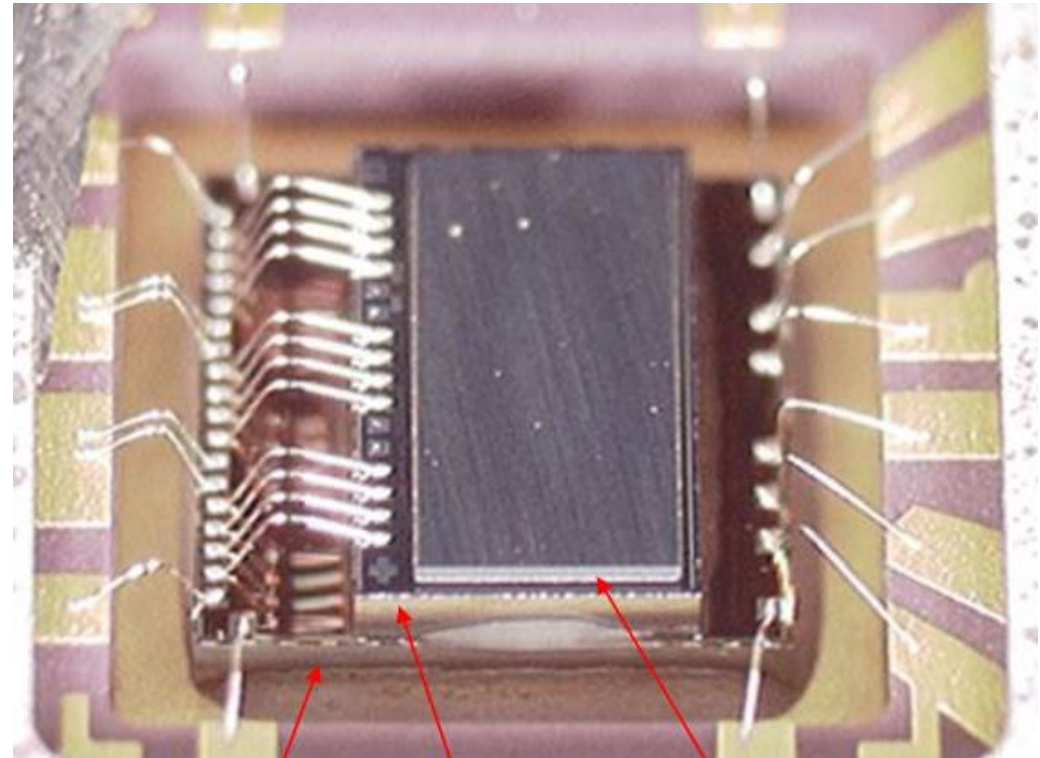
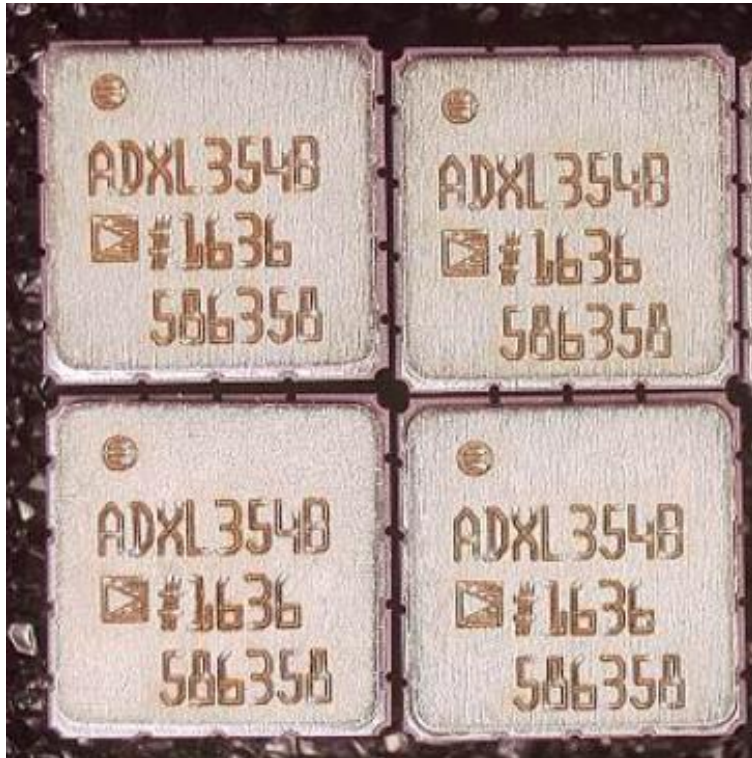
3. Can I get all of my signals in/out of a test chamber if needed?

- For vacuum chambers, DC to ~1 GHz is easy.
- Low power is easy. RF or high power is harder.
- Other facilities have cable run concerns (100' for medical protons) that you need to know about



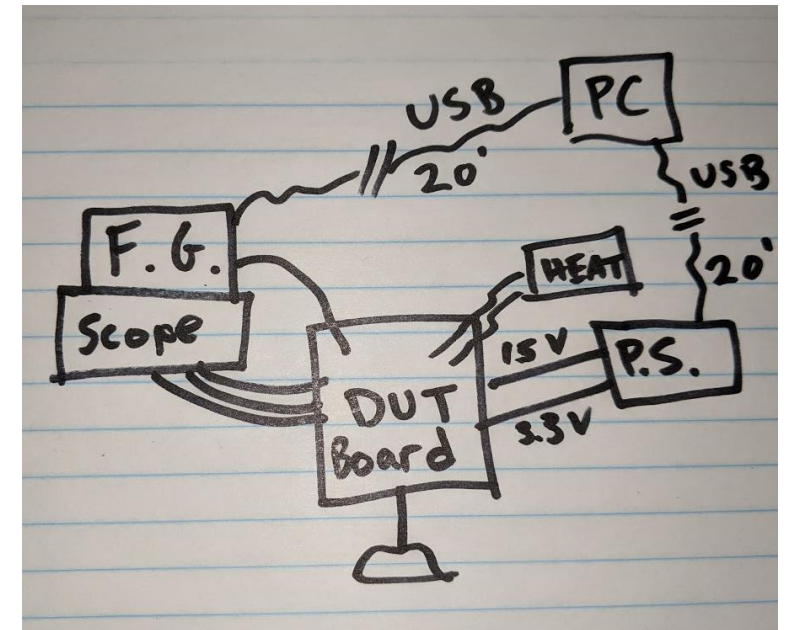
What's a hard part look like?

- Sometimes it's obvious. Sometimes it's a surprise. Typical heavy ion facilities do not have the range to blast through covers or die stacks. There are options, but they are not trivial.



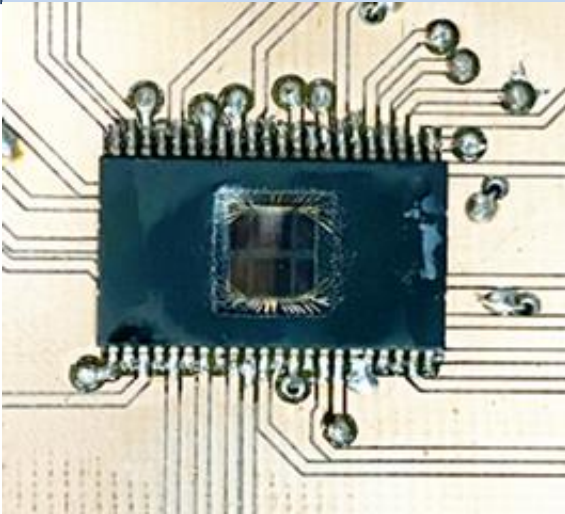
Sketching a Notional Test Setup

- To prep a test, the test engineer must identify:
 - **What am I expected to test, and how does it work?**
 - » Start with a datasheet, previous test report, application engineers, Google, etc.
 - **How will the part will be mounted and operated in beam?**
 - » Facility and test specific
 - » Includes physical, electrical, and radiation issues
 - **What measurements are needed?**
 - » What are your requirements?
 - » Talk to system designers, research lead, or other stakeholders
 - **How will I obtain those measurements?**
 - » What hardware? What cabling? What settings?



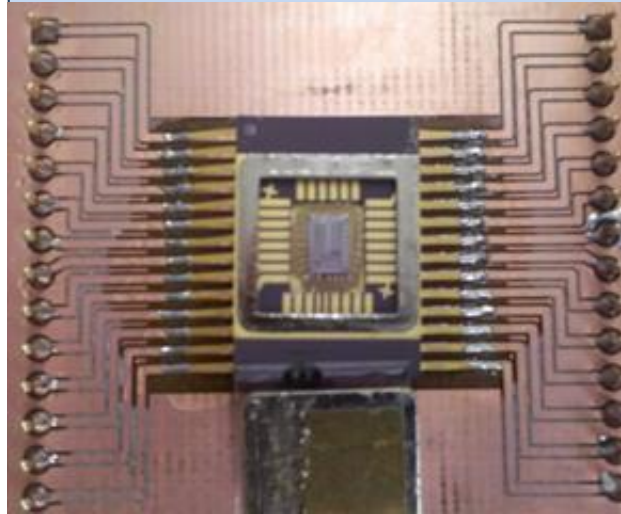
Case Studies: Three Devices (from Module 5)

TSOP SRAM



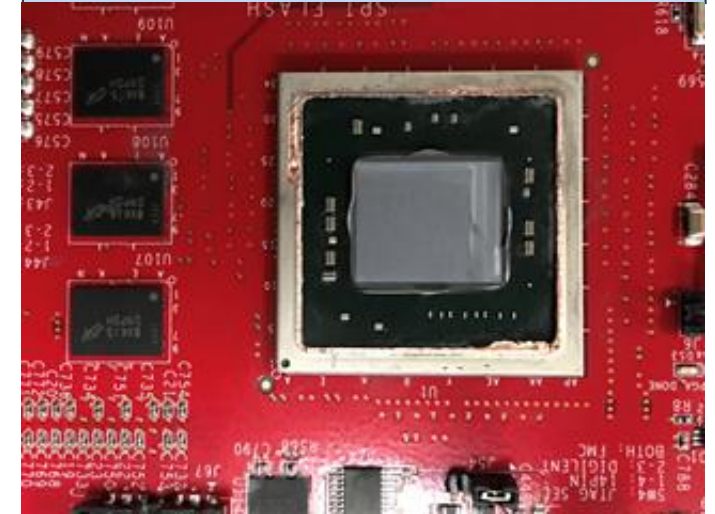
- Understood that there will be SEU/SBU
- Want to “screen” for SEL

QML Amplifier



- Already guaranteed to not have DSEE
- Want to characterize SET

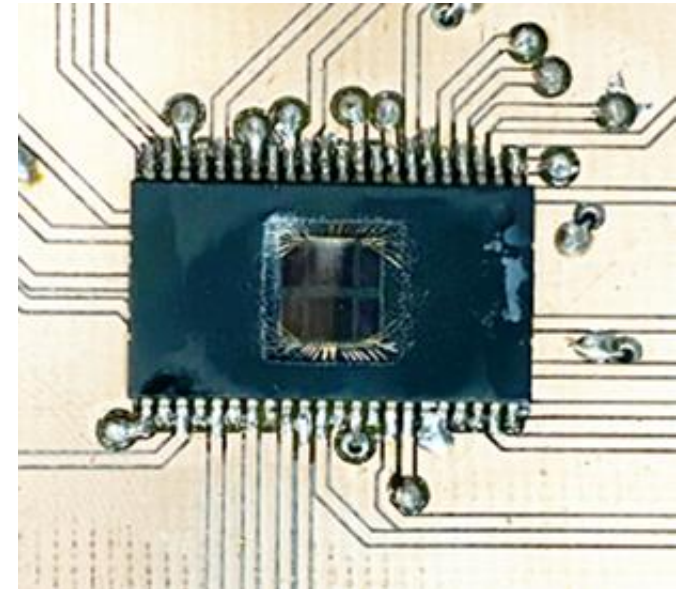
COTS SoC



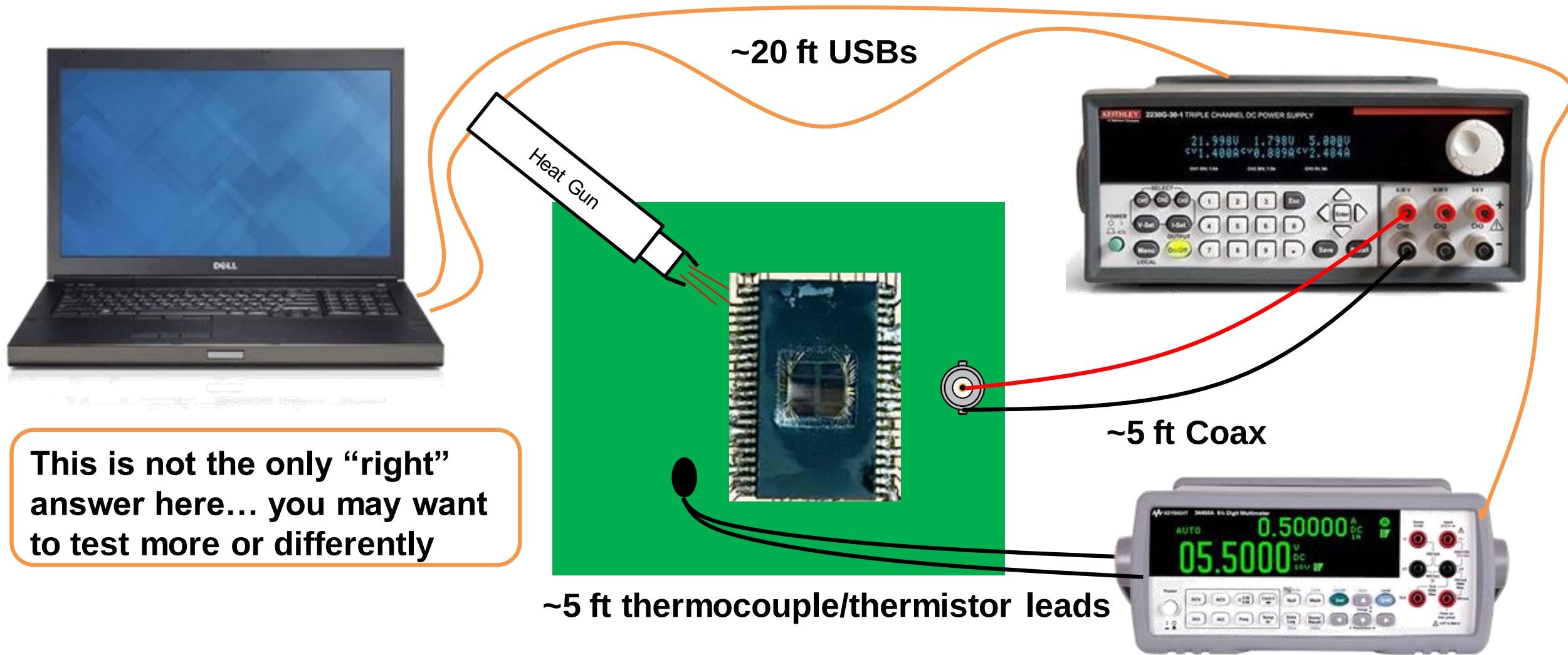
- Very little known on radiation response
- Want to characterize as many signatures as possible

Test Case #1 – SEL Test, Commercial SRAM

- *An SEL test of a commercial SRAM*
- **What am I expected to test?**
 - That the supply current does not abruptly increase during irradiation in a high-voltage, high-temperature configuration.
- **How will the part be mounted and operated in beam?**
 - The part will be on a small PCB, with plastic lid etched away and die exposed to beam line.
 - It will need a steady DC power supply, but no active I/O signals are required. We need to control and monitor case temperature.
- **What measurements will be performed?**
 - The power supply will continuously log supply current.
- **What hardware is necessary?**
 - A power supply capable of appropriate I/V and automated logging (or a separate DMM)
 - A computer to control the power supply and log data
 - A basic circuit board to provide power and terminate/bias other pins appropriately.
 - A thermocouple, thermistor, or IR gun and some kind of heating apparatus.

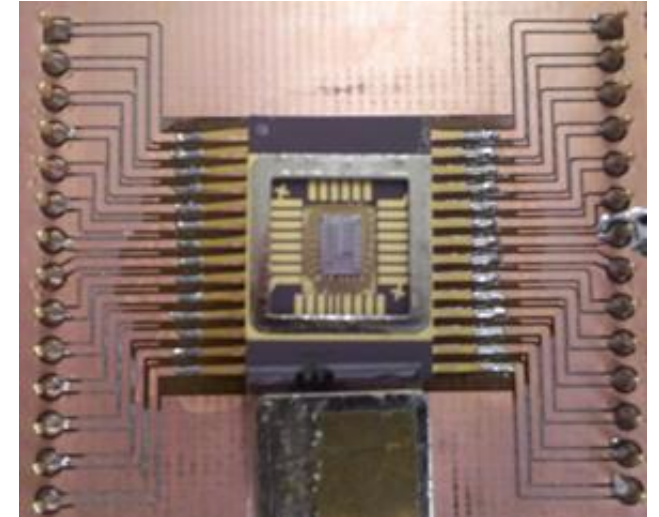


Test Case #1 – SEL Test, Commercial SRAM



Test Case #2 – SET Test, QML Amplifier

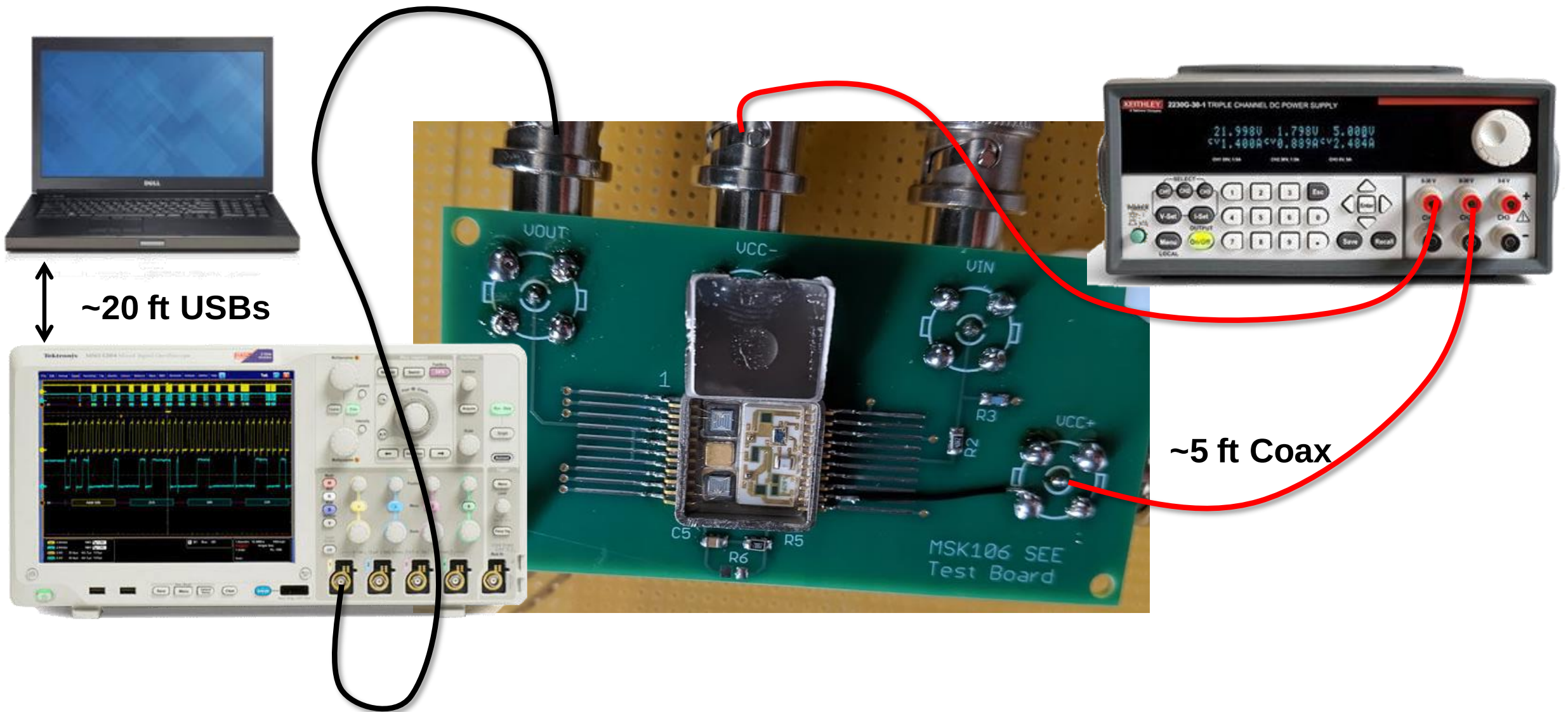
- *An SET test of a space-grade amplifier*
- **What am I expected to test?**
 - What kind of output transients exist, and how sensitive is the device?
- **How will the part be mounted and operated in beam?**
 - The part will be on a small PCB with high quality RF traces, with ceramic lid removed and die exposed to beam line.
 - It will need multiple DC power supplies, but no dynamic input signals are required. It will operate with a selectable gain of 1 or 100 via jumpers and the nominal output will be steady state.
- **What measurements will be performed?**
 - The power supply will continuously log supply current. An oscilloscope combined with LabVIEW software will count and capture transients that deviate from nominal output by +/- 10 mV.



Test Case #2 – SET Test, QML Amplifier

- **What hardware is necessary?**
 - A power supply capable of appropriate I/V and automated logging (or a separate DMM)
 - A real-time oscilloscope with at least 1 GHz bandwidth
 - A computer to control the power supply, log data, and save scope captures
 - A basic circuit board to provide power, terminate/bias other pins appropriately, and provide a clean signal path for the output to oscilloscope.

Test Case #2 – SET Test, QML Amplifier



Test Case #3 – Generic SEE Test, SoC

- *A research study of a new system-on-chip device*
- **What am I expected to test?**
 - How does this part behave in a radiation environment?
 - What types of SEE do we see, what dominates, and how tolerant is the system to errors?
- **How will the part be mounted and operated in beam?**
 - A manufacturer's evaluation board will be used, with the device de-lidded and thinned. A custom aluminum frame will support the board in the beamline.
 - It will need multiple DC power supplies, USB to communicate with host PCs, JTAG for debugging
- **What type of measurements will be performed?**
 - The power supply will continuously log supply current. The test PC will save all digital output from a virtual COM port (over USB). An additional PC will be used for programming the SoC before each run.

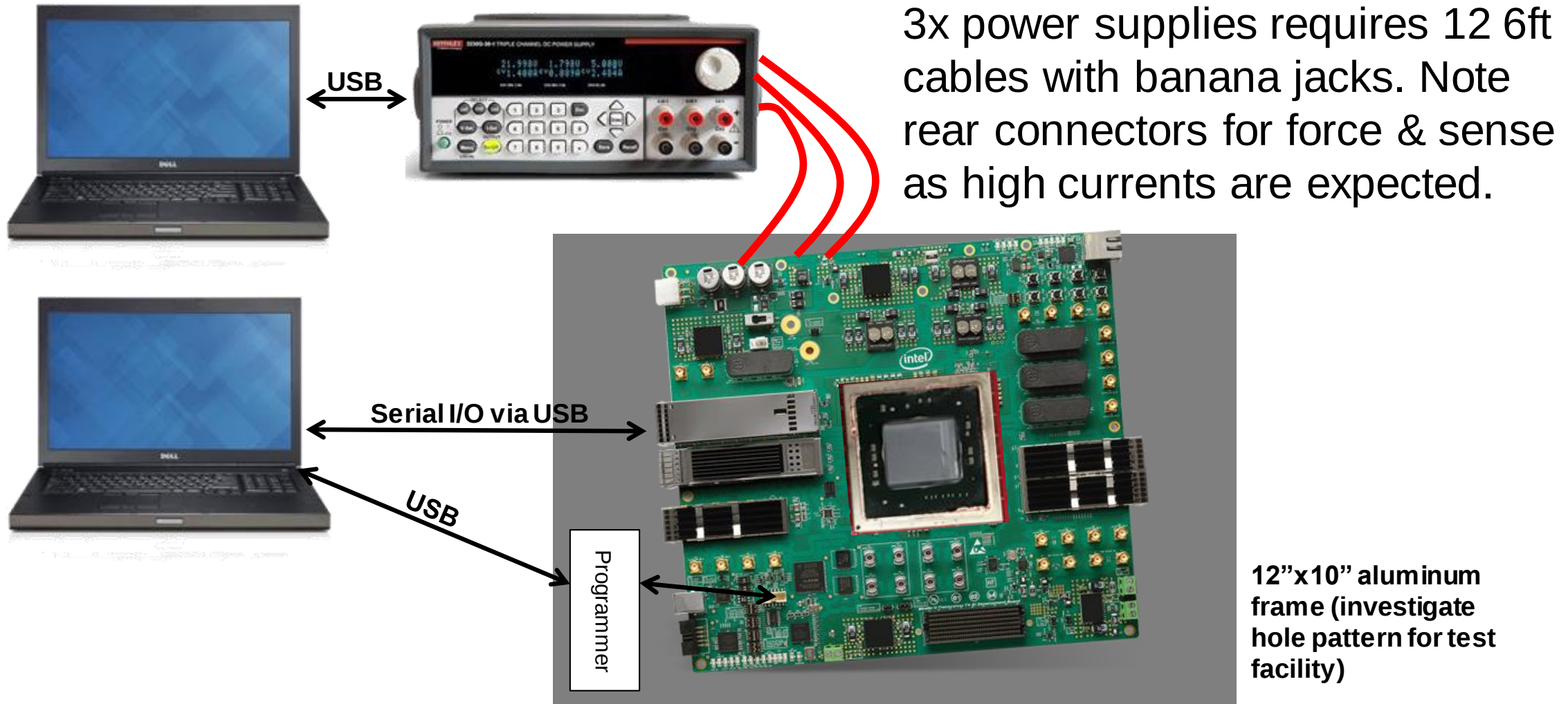


Test Case #3 – Generic SEE Test, SoC

- **What hardware is necessary?**

- A power supply capable of appropriate I/V and automated logging (or a separate DMM)
- A laptop to control the power supply and program the SoC, and a separate laptop to communicate with and log the test software
- A manufacturer's evaluation board (several copies desired)
- An aluminum mounting platform to hold the board and cabling in front of the beam
- Possibly a liquid cooling system as the part dissipates a large amount of heat and normally operates with an integrated heat sink which must be removed for testing.

Test Case #3 – Generic SEE Test, SoC



Moving to Detailed Test Preparation

- We have a viable concept; how to do we implement in detail?
 - **Design and build the test setup**
 - » How is the part operated during test? Flight-like? Broad characterization?
 - » Do we need additional telemetry beyond “normal” feature set?
 - » Can we check operation (inject errors) before the test?
 - **Understand facility operations, hardware limits, physical layout, personnel safety restrictions, etc**
 - » Must be sure our “benchtop” test setup is testable and relevant to application
 - **Prepare part(s) for actual testing**
 - **PLAN what we’re going to do before we show up! (see Module 6a)**
 - **Arrange logistics for hardware and personnel**

Test Setup (Schematic/Design Phase)

- **How will the part function in the beam?**
 - Ask for application details from designers, board leads, radiation engineers...
 - Test planning and requirements definition should give you specifics, but your test setup must be capable of implementing things like:
 - » MOSFET worst case VDS/VGS (consider your hardware physical limitations)
 - » op-amp rail voltages and gain configurations (consider if you can reconfigure easily)
 - » flip-flop data rate (consider cabling length and bandwidth limits)
 - » FPGA designs, processor software very difficult to make “flight-like” but your physical test should allow as much “reality” as possible and avoid artifacts of ground testing

Test Setup (Schematic/Design Phase)

- **Part function and intended test modes HAVE to drive test setup design**
 - » Cannot* build a test setup and then figure out how to get test data
 - » For example, you cannot wire up a high-speed amplifier on a breadboard and expect to get good transients at an oscilloscope 10 feet away
 - » You may not be able to buy an off-the-shelf FPGA demo board and have access to the right I/O or configuration pins to test the part appropriately
 - » Learn what the part is going to do, then make it happen
- **Desired failure mechanism must also drive test setup design**
 - » If we “want” a power MOSFET to blow up, we need to provide a power supply and extra capacitance sufficient to do so. Don’t let the test setup hide the effect you’re looking for!
 - » If we “want” to characterize SETs, we can’t have excessive filtering on the output (unless testing a specific application circuit)
- **Must be able to reset or abort testing live, without access to the part.**

***it happens.**

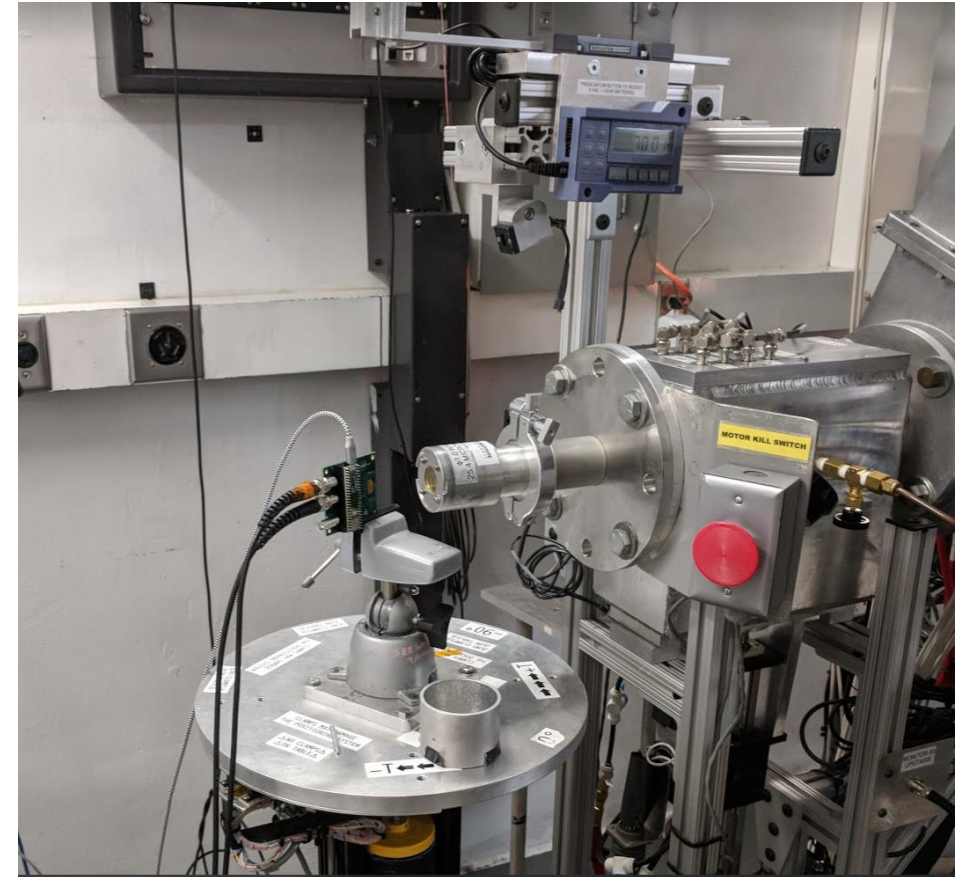
Common Operating Modes

- Typically, a given SEE test type is associated with certain modes of operation that will be relevant to test prep:

	Unpowered	Static with power	Dynamic
SEU	Yes, for non-volatile memories	Common for memories/latches	Common for clocked logic
SET	No	Common, but size and shape may be dependent on output	Common, but may be hard to extract from complex waveform
SEL	No	Common	Common, especially when not all device circuitry is active in a static mode
SEFI	No	Yes, but hard to identify until test ends	Yes
SEB/SEGR	No, though some microdose degradation can occur	Yes	Yes, especially for GaN

Test Setup (Physical Design Phase)

- **Before cutting materials, we need to ensure compatibility between designs and the intended test facility(ies)**
- **Mounting and Positioning Systems**
 - Investigate if facility provides a mounting platform, movable stage, or similar mechanism and what the hole pattern is (or is supposed to be...)
 - Can I move my test in an automated fashion to achieve angular irradiations or multiple devices without re-entering the “cave?”
 - What’s the range of motion, and how will all of this affect my cabling?
 - How close am I to the beam line? Design to keep area near DUT clear of obstructions



Test Setup (Physical Design Phase)

- **Hardware Placement and Cable Runs**

- Can test hardware be next to the part? On the outside of a vacuum chamber? Farther away (protons)
- What are the cable runs from Hardware-to-Engineer?
 - » Likely 15-20 ft for heavy ions,
100+ ft is possible at proton facilities
- Think about SIGNAL/POWER INTEGRITY

- **Vacuum vs. In-Air**

- Will your test be required to operate in vacuum?
- Is it possible to operate in air, but with tradeoffs (or vice-versa)?
- Think about THERMAL ISSUES and CONNECTORIZATION



Additional Test Prep Issues

- **Internet Access**

- Unlikely to drive the test setup itself, but may be critical for test debug (where'd that software go? I have to download it again??)
- Also relevant for **license servers**, email access, online datasheet retrieval, collaboration with off-site personnel

- **Power Availability**

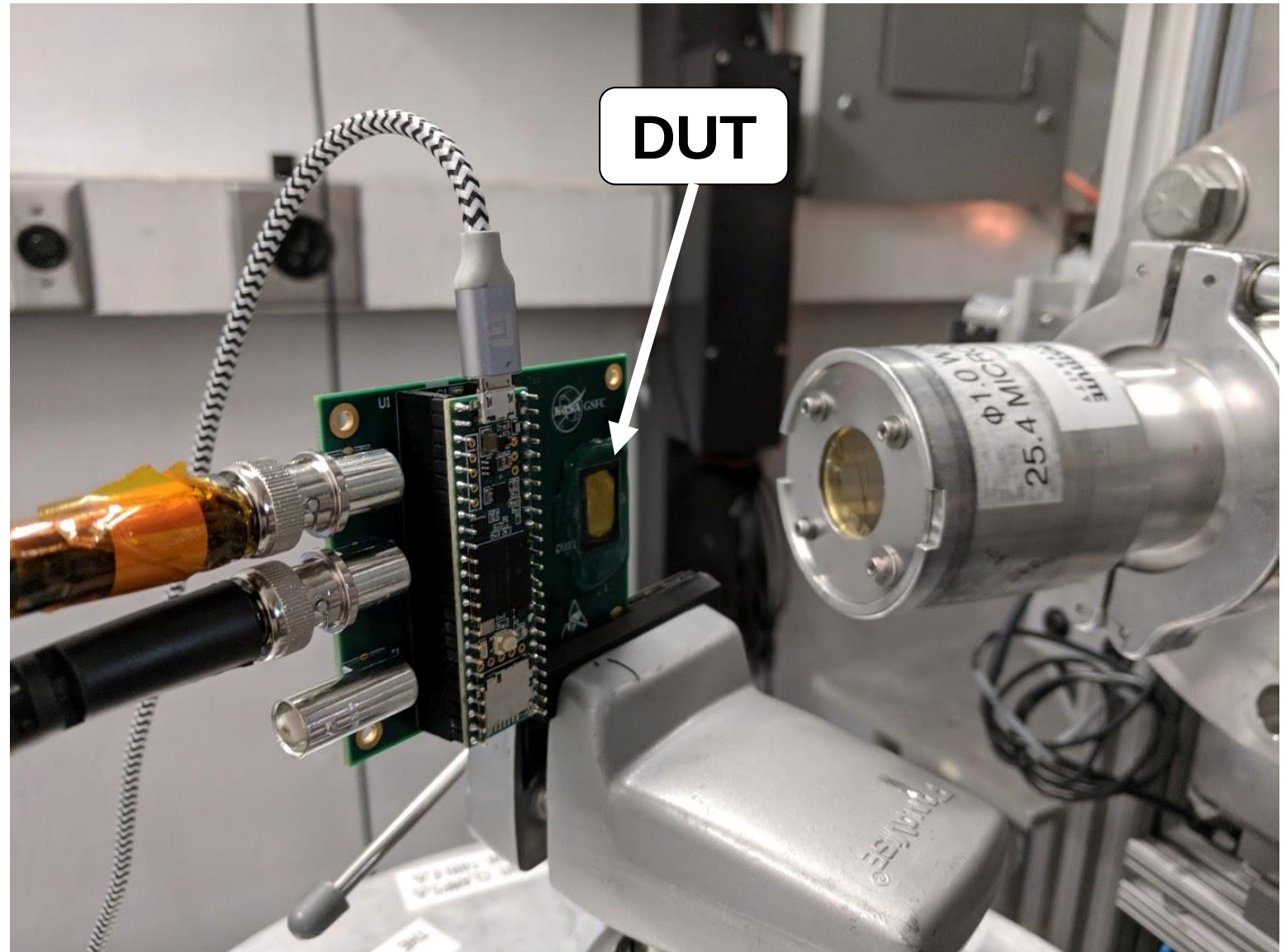
- Sounds trivial, but sufficient AC outlets may not be near the test stand or the test operations area and, for sensitive tests, power may be noisy

- **Bring all your support equipment!**

- ESD mats and monitors and wrist straps. Bring a soldering iron, wire, and spares. Bring schematics, diagrams, and sourcecode.

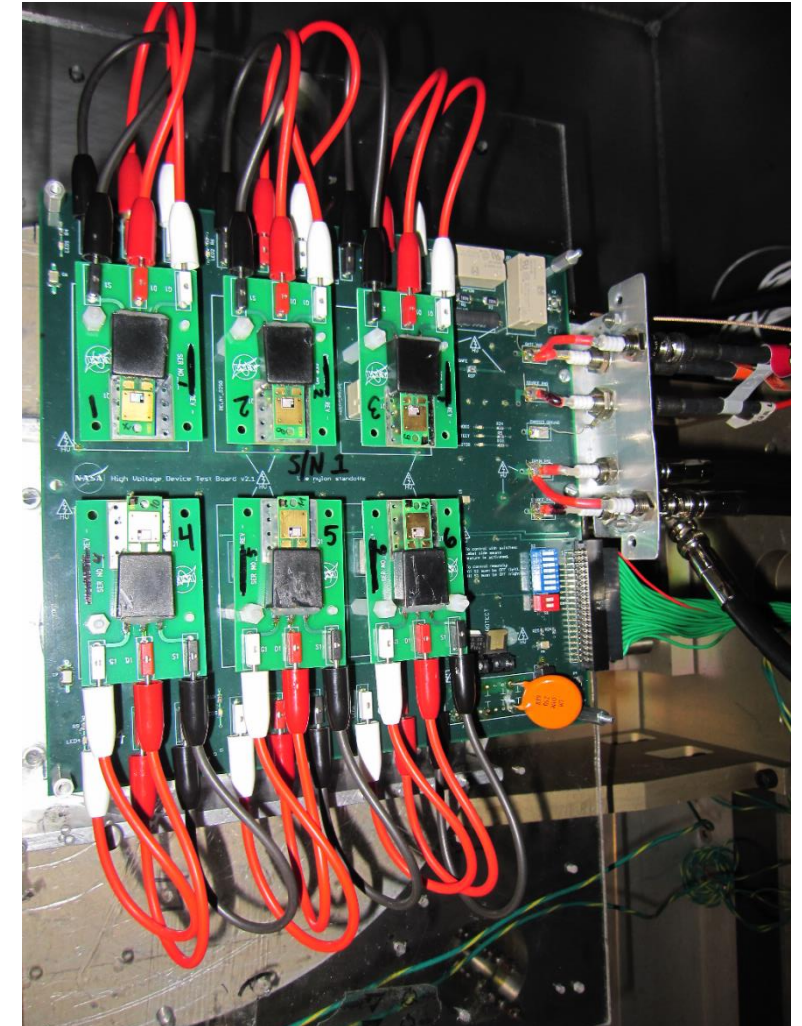
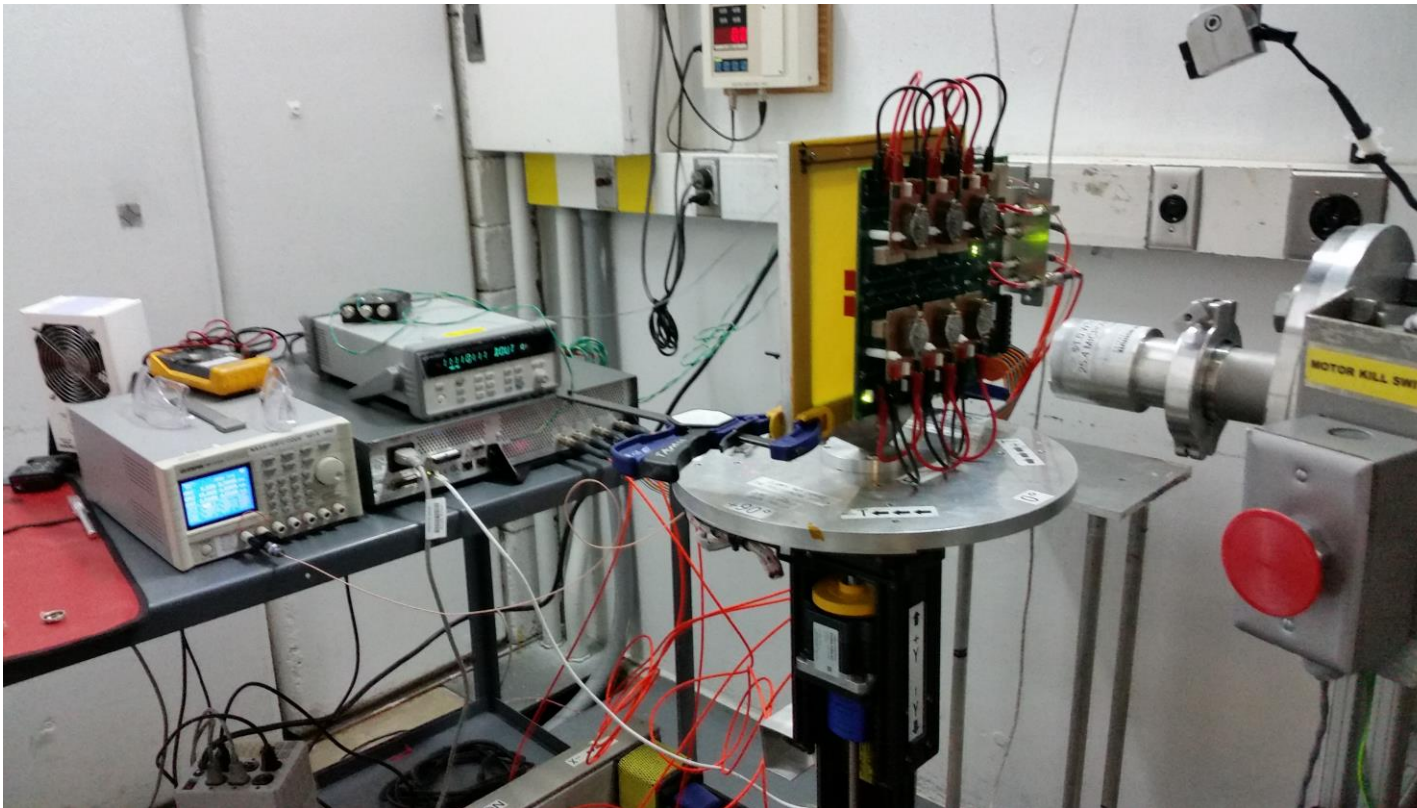
Physical Test Setup Example - SEU

- One side is **free of obstructions** for angular irradiation
- No cabling coming out of front-side to hit the **beam line**
- Plastic part **decapsulated** and moved close to beam line

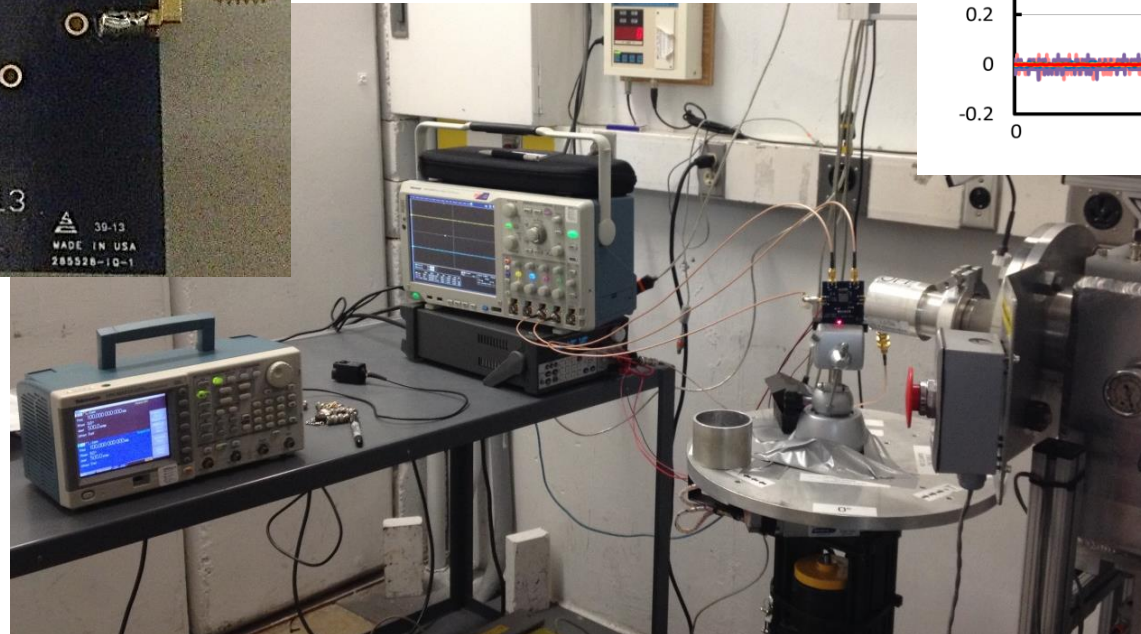
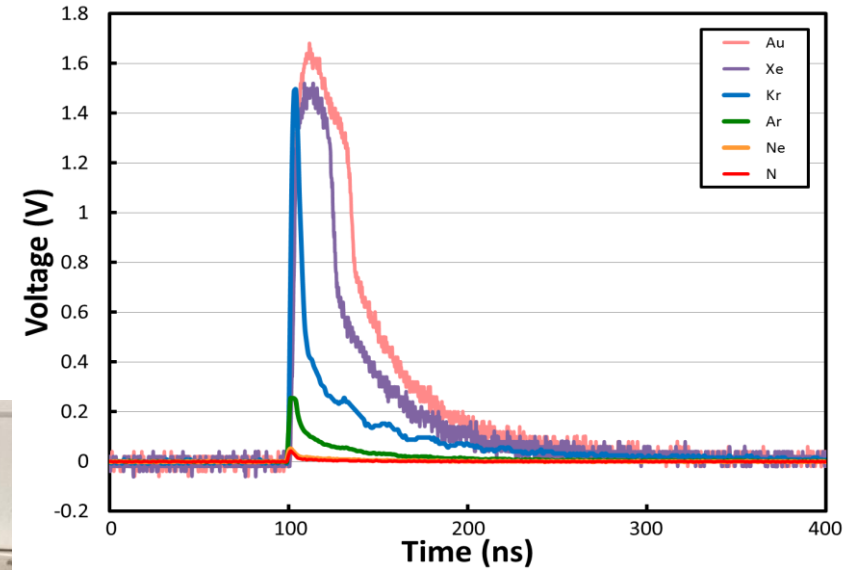


Physical Test Setup Example – SEB (with positioner)

GSFC power MOSFET / diode test board
Six test locations relay-switched



Physical Test Setup Example - SET



Physical Test Setup Example – High rate of SEL

- Unusual test to automate a large number of SEL tests to verify functionality of mitigation circuitry:

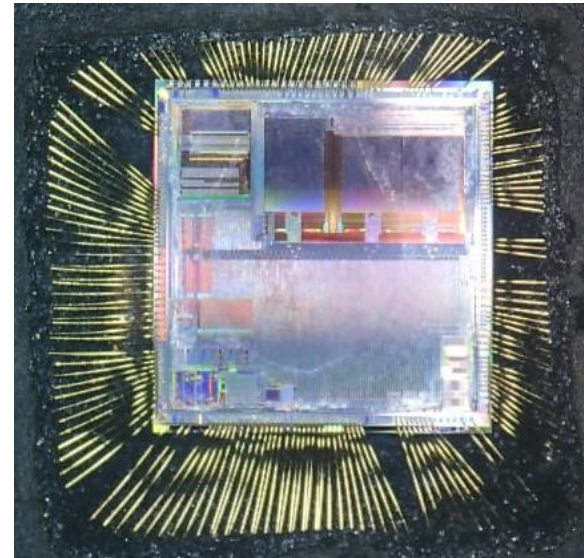
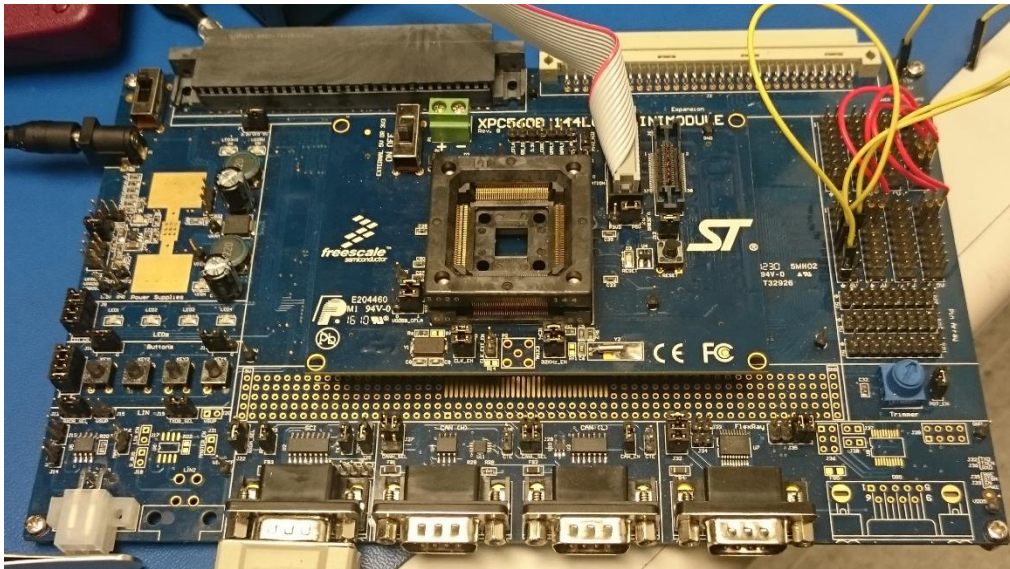


Using Commercial Evaluation Boards

- **Custom-made test boards are not the only way**
- Commercial evaluation/demo boards may save significant time and money, especially when parts require peripheral circuitry or highly-tuned transmission lines
- **The downside is you get what you get**
 - Limited access to debug ports
 - Limited ability to control power supply levels (may need to cut traces)
 - No control of board size or DUT location

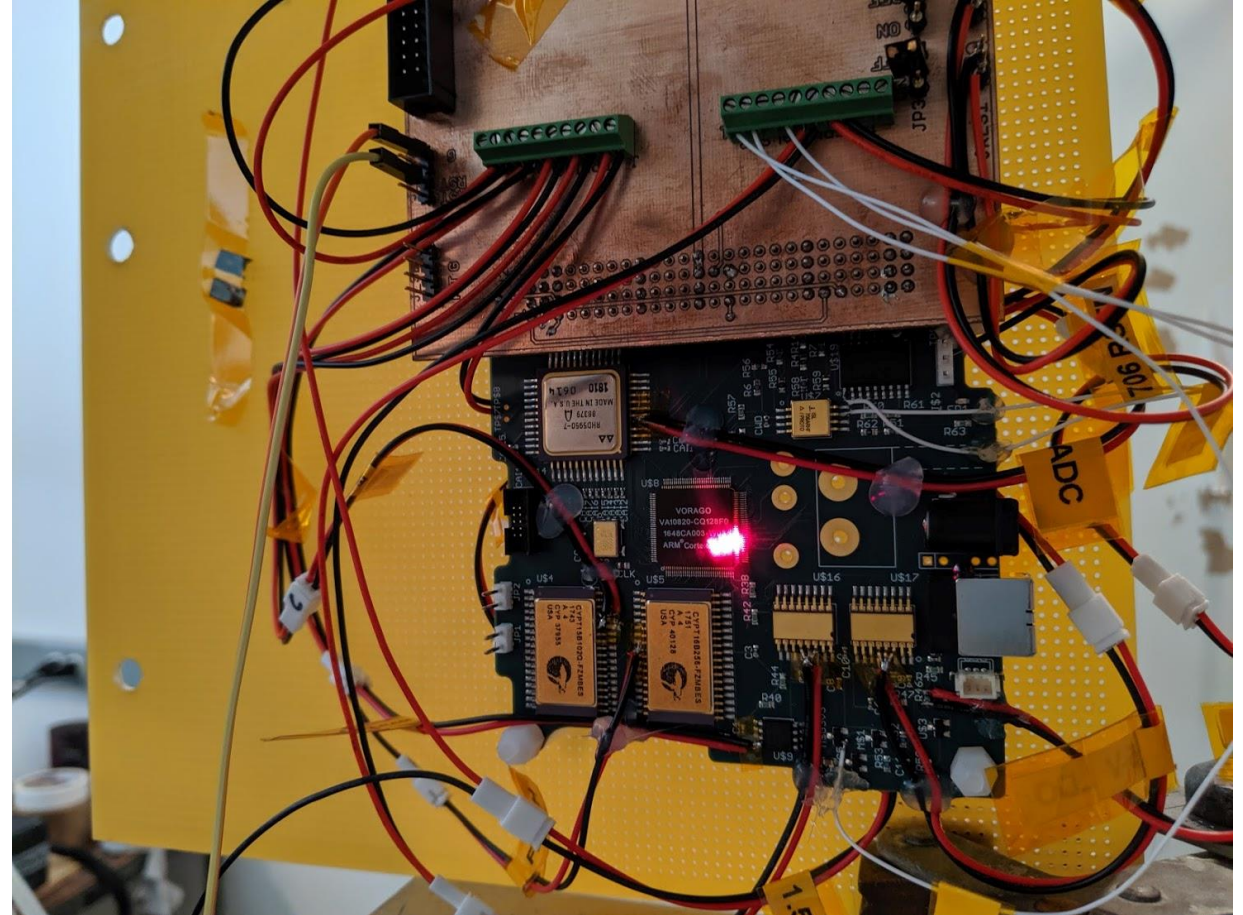
Eval Board Example: Microcontroller

- Here's a commercial evaluation board being used to test a 32-bit microcontroller
- Very easy setup (just power in, JTAG programmer, and serial I/O)
- But that means very limited data unless we add in a lot of additional monitoring circuitry



Eval Board Example: Single Board Computer

- This was a [proton] test of a **single-board computer**, so testing at the board level was the objective.
- But, we still needed to tear up the board to access various power lines and control pins.



Test Hardware

- **You are the best person to determine what hardware you need**
- **Consider**
 - Connectivity (force/sense, USB, GPIB, probes, etc)
 - Capability (current, voltage, frequency, resolution, etc)
 - Scarcity (can you ship that item away for a few weeks?)
 - Familiarity (can you debug it at 2AM?)
 - Portability (you may be carrying it yourself)
- **Depending on test and your institution, calibration and verification may be required before or after testing**
- **Try whenever possible to debug, demo, and test with the same S/N**

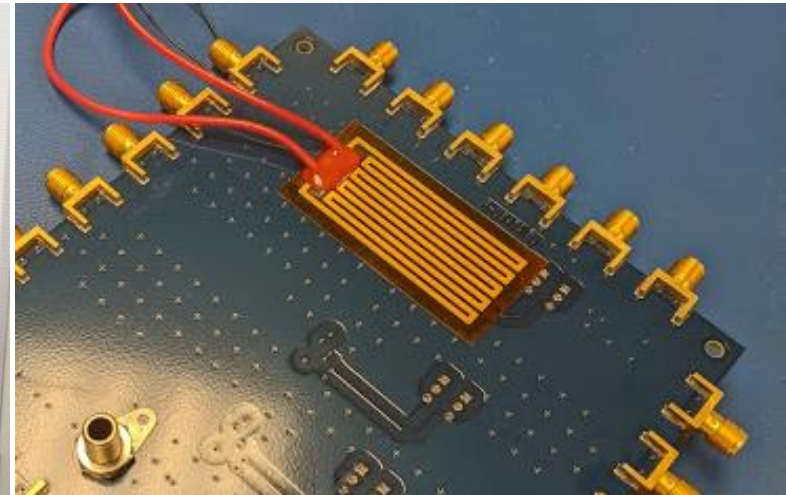
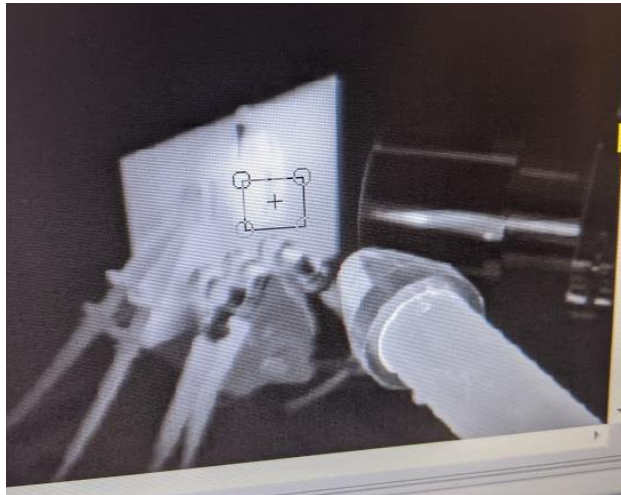
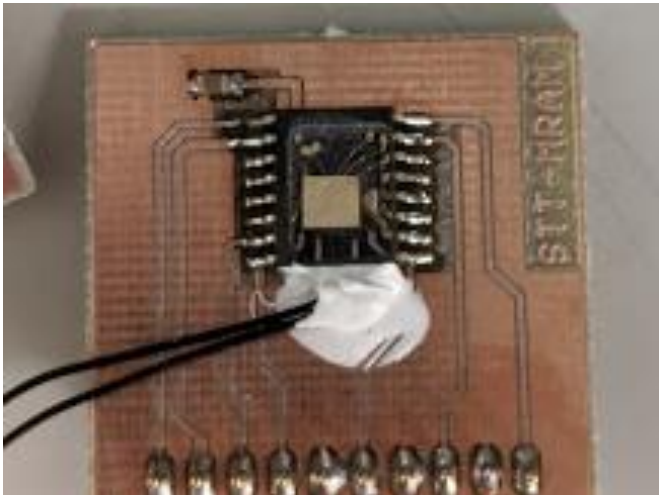
Test Control

- Don't forget about your **remote control of the test hardware**. Can everything be controlled from 15+' away? Can you debug from afar?
- Remote shutdown and **remote reset** are necessary!
- **Use the same gear for final debugging if at all possible.**
- **Complex test setups can drive logistical challenges.**
 - Faster test execution if a couple of engineers split duties, but this will break down quickly for large # of people in a small room.



Implementing Temperature Control & Monitoring

- **Testing at elevated temperature is common, especially for SEL**
- **With facility support, this can be a test execution concern (e.g. TAMU's heat gun / IR camera approach)**
- **With no facility support, this must be prepared in advance**
 - Thermocouple, thermistor epoxied/pasted to DUT, or internal temperature monitor, or borrow an internal diode
 - Resistive heaters below DUT or back of board (harder, and leave space for it!)



Part Preparation

- **For heavy ion testing, you probably need to expose the die surface directly (and completely)**
- **First Rule of Part Prep is: Don't wait until the last minute**
 - Your day can be ruined by devices with impenetrable lids, “goop” on the die, copper wirebonds, unexpected metal, die orientation, etc.
- **Quantity: How many parts do you want to request, prep, ship, and test? (likely all different numbers)**
 - Common to request more if they're cheap, but *in general* I will:
 - » Request 6, prep 5, ship all that work, and test 2-3
 - If you need statistics on destructive SEE, you need lots of parts
 - For \$\$\$\$ parts you may have 1 sample (\$100k FPGA, \$30k DAC, priceless detectors, etc)

Part Preparation Methods

- **Chemical Decapsulation**

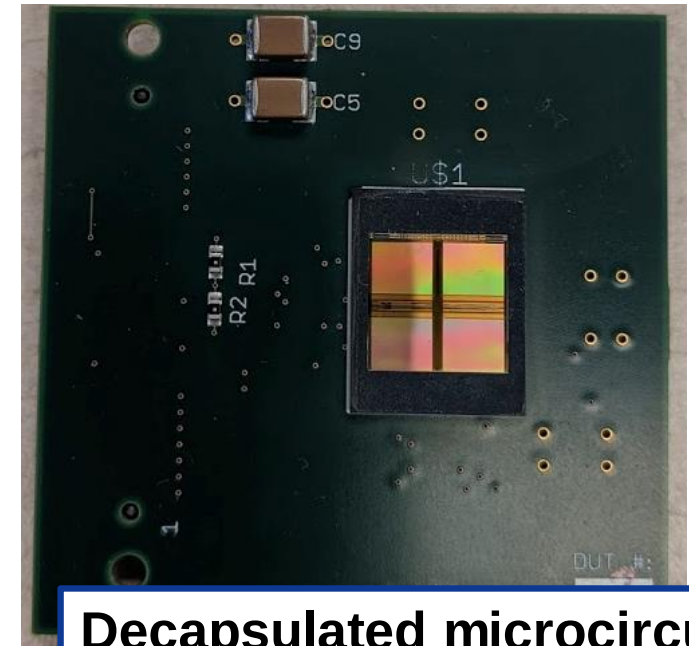
- Most heavy ion SEE beams have range $< 300\text{ }\mu\text{m}$, and we don't want to use it all – the LET becomes non-uniform as we approach the Bragg Peak
- Plastic parts need to be *decapsulated*, commonly with acid or laser/acid combination. This is not a 100% yield operation.



Nisene JetEtch Pro



Control Laser FALIT

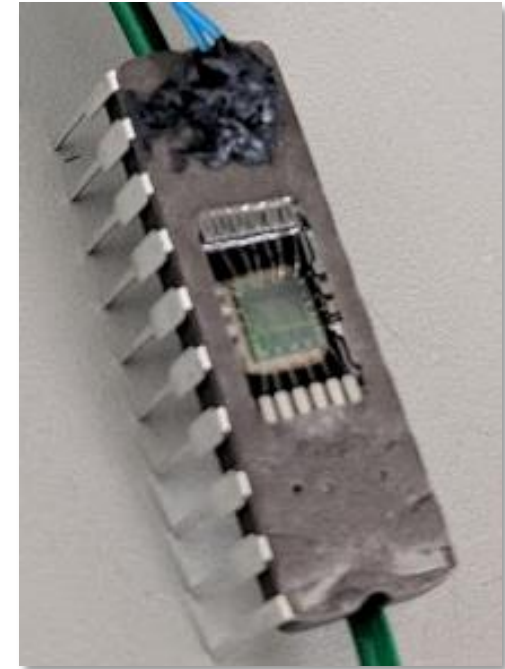
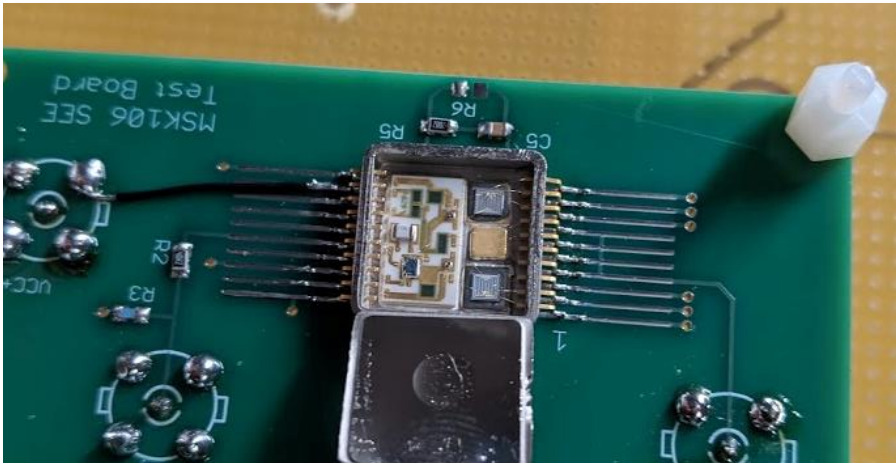


Decapsulated microcircuit

Part Preparation Methods

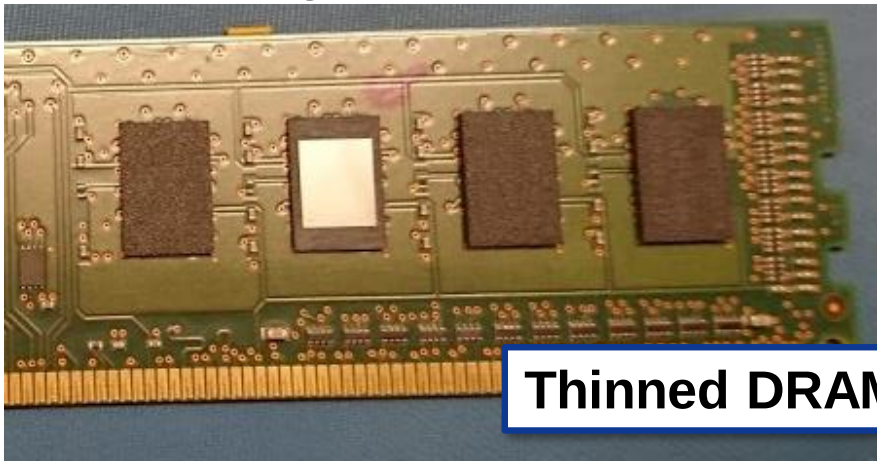
- **Mechanical Delidding**

- **Ceramic parts need to be de-lidded, potentially by “cracking” the seal**
 - » This is <100% yield
- **Ceramic/metal parts with metal lids need to have the lid peeled back**
 - » Hammer an xacto knife into the gap (seriously, be safe...)
 - » Heat until glue/solder softens
 - » Dremel off a corner (careful of debris!) and pry away

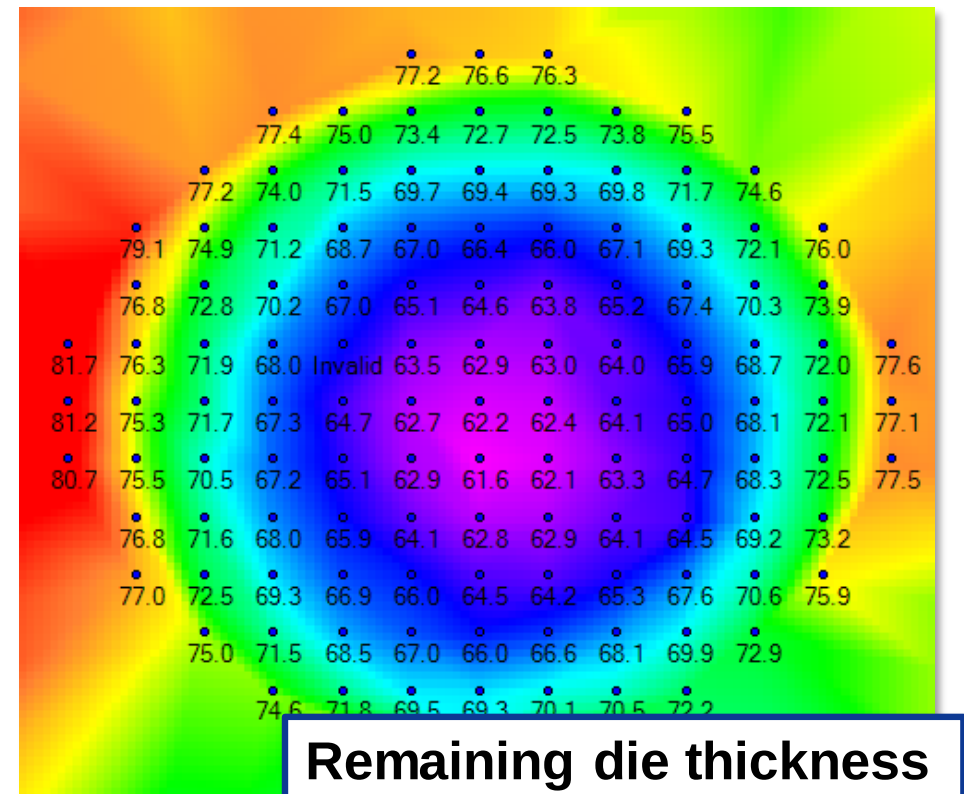


Part Preparation (Backside Thinning)

- Thick flip-chip packages (FPGAs, processors, some memories) need to reduce backside silicon substrate thickness due to limited range at ground test facilities
- Can also remove plastic encapsulant (only on flip-chips)
- Requires knowledge of die thickness or characterization. Results will not be uniform and LET will vary somewhat.



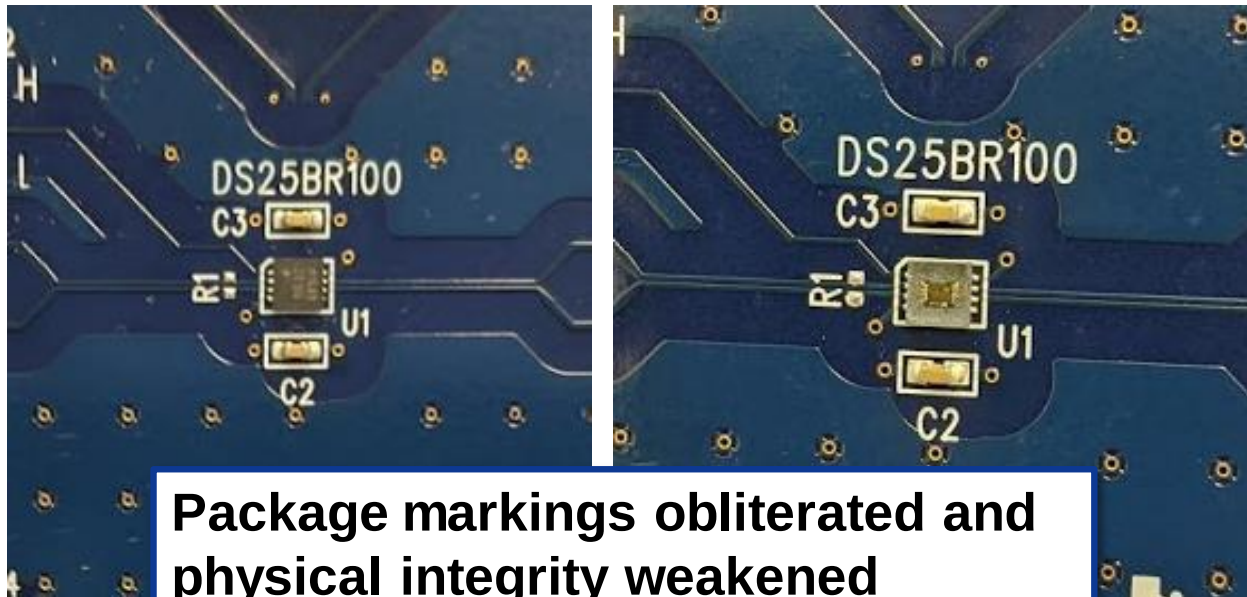
Thinned DRAM



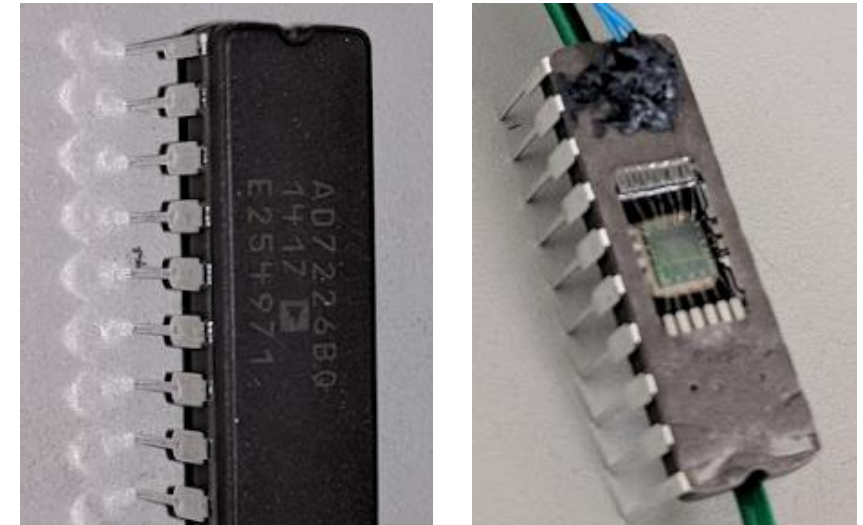
Remaining die thickness (SRAM test chip)

Part Preparation and Mounting

- **Photograph your parts prior to decap, and remember that acid, acetone, or alcohol may wipe markings (including your own).**
 - Note orientation!! You may etch away that “pin 1” dot
 - Note part number/date code!!
- **Think about any special concerns (two date codes?) before decap**
- **It may be better to decapsulate small parts *after* soldering in place**



Package markings obliterated and physical integrity weakened



Pin 1 orientation not always clear

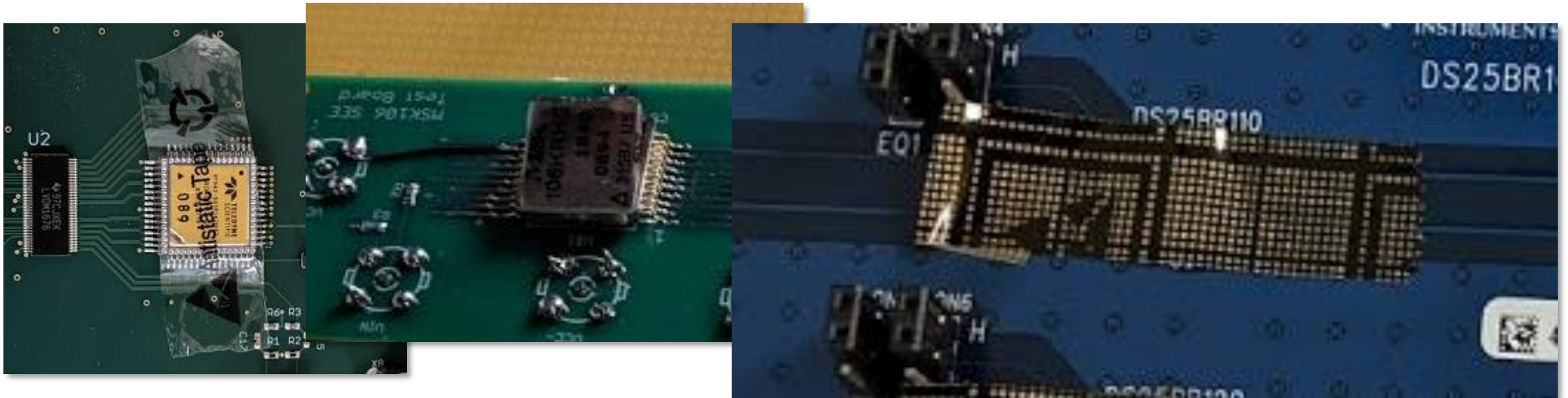
A note on Part Preparation

- **You don't have to do it yourself.**
 - There are companies that can do this for you, and possibly resources in your organization. It takes skill to break a ceramic part in half or acid etch a plastic part with copper bonds.
 - Vendor probably can't "guarantee" it still works
- **With a technician or external vendor, be clear on expectations**
 - "Thin it to 50 um" ← What does this mean? Is that the min, avg, or max?
 - "Etch away the plastic" ← Does the technician know the part still must work?
- **Are there any handling requirements for a third party?**
 - How hot can they take the part? Are there are especially sensitive components on a board? Can it get wet?

Protect Your Parts

- **Protection during pre-tests/shipping**

- Parts have lids/encapsulant for a reason. Large, expensive parts with hundreds of bond wires are very easy to ruin with a thumb, solder tip, or carelessly draped wire.
- It's not too difficult to cover a part (cheap solution: flip inverted and tape to an old PCB) or leave one side of lid attached.



Pre-Test Checkout / Demo

- **Try to demo your test end-to-end, including cable lengths, feedthroughs and specific hardware if available**
- **Use some sort of fault injection to verify that your setup can capture errors**
 - Camera flash / strobe light works for many parts
 - Software / hardware fault injection
 - The screwdriver fault injection test (short something safely)
- **Depending on your organization, goals, and experience, anything from a formal Test Readiness Review to a casual “here’s the setup” demonstration may be prudent**
 - Engage with stakeholders to understand their expectations here

Module 6b: Final Thoughts

- **No two tests are the same. Nearly everything is a custom job.**
- **Understand the big picture, rather than just preparing one part for one test.**
- **Build a test that provides high-quality data.**
- **Ultimately you are building a system that operates a part as it would in a high-radiation environment, AND**
 - You need to collect sufficient data to make quantitative and qualitative assessments of the performance
 - You need to be able to pack everything, ship it, reassemble in a day at a new facility and test in a few hours/days.