

Effect of High- κ Dielectric Layer on $1/f$ Noise Behavior in Graphene Field-Effect Transistors

Yifei Wang,^{1†} Vinh X. Ho,^{1†} Zachary. N. Henschel,¹ Michael P. Cooney,² and Nguyen Q. Vinh^{1*}

¹ Department of Physics and Center for Soft Matter and Biological Physics, Virginia Tech, Blacksburg, VA 24061, USA

² NASA Langley Research Center, Hampton, Virginia 23681, USA

[†]Yifei Wang and Vinh X. Ho contributed equally to this work.

* Corresponding author: vinh@vt.edu; phone: 1-540-231-3158

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ABSTRACT

We report the $1/f$ noise characteristics at low-frequency in graphene field-effect transistors that utilized a high- κ dielectric tantalum oxide encapsulated layer (a few nanometers thick) placed by atomic layer deposition on Si_3N_4 . A low-noise level of $\sim 2.2 \times 10^{-10} \text{ Hz}^{-1}$ has been obtained at $f = 10 \text{ Hz}$. The origin and physical mechanism of the noise can be interpreted by the McWhorter context, where fluctuations in the carrier number contribute dominantly to the low-frequency noise. Optimizing fabrication processes reduced the number of charged impurities in the graphene field-effect transistors. The study has provided insights into the underlying physical mechanisms of the noise at low-frequency for reducing the noise in graphene-based devices.

INTRODUCTION

The outstanding electrical properties of graphene (a single atomic layer) have received considerable attention for future electronics including high speed transistors, photodetectors, components of integrated circuits, flexible and wearable devices, touch screens, ultrasensitive sensors.¹⁻³ In these applications, the flicker or low-frequency $1/f$ noise ($f < 100$ kHz) is the key factor of the device performance. The amplitude of the flicker noise defines the limit of the operation of electronics devices.⁴⁻⁸ Therefore, to enhance the performance of graphene devices, several configurations have been realized to scale down the flicker noise. Graphene field-effect transistors (GFETs) containing a few graphene layers helped reduce noise level.⁹ GFETs with the graphene channel on h-BN or encapsulated by two h-BN layers, which reduce charged impurities and trapping sites, can suppress the flicker noise by a factor of 5 to 10 times compared to that of graphene on Si/SiO₂ substrates.¹⁰⁻¹² The noise at low-frequency of graphene devices can be reduced through irradiation.^{5, 13} Another approach is to employ a high- κ dielectric layer that can protect graphene from exposure conditions to prevent the increase of the noise. Nevertheless, the mobility degradation in graphene can occur when the dielectric layer is grown atop graphene. The flicker noise in GFET devices with an HfO₂ high- κ dielectric thin film grown by atomic layer deposition (ALD) has been realized.¹⁴ A reduction of the low-frequency noise with a top-gated GFET using Al₂O₃ as gate-dielectric has been reported.¹⁵ However, a high dark current in the milliampere scale of such GFETs is an obstruction for many applications. For example, the high dark current in GFET photodetectors causes a high shot noise, and thus, sets a high-level noise floor of these devices. These reports mostly focused on GFETs under the voltage control of the top-gate. However, the back-gated FETs are the backbone for a variety of electronic applications. Therefore, it is essential to improve GFETs with low noise in the back-gated configuration, which is covered by a high- κ dielectric thin film with a few nanometers thick. Among various high- κ dielectric materials, we have focused on the tantalum pentoxide (Ta₂O₅) with high dielectric constant ($\kappa = 25 - 40$) and good chemical and thermal stability. The material has been used in many applications in solar energy conversion as well as microelectronics, including photocatalytic materials,¹⁶ charge-trapping for nonvolatile resistive random access memories,¹⁷ atomic switches,¹⁸ capacitors, insulators,¹⁹ thin-film electroluminescent devices,²⁰ and high-speed elements.²¹

Here, we report the reduction of the flicker noise in GFETs by engineering the high-quality dielectric tantalum oxide (Ta₂O₅) layer grown by ALD on Si₃N₄. The back-gate bias dependence of the flicker noise on the graphene channel size with the source-drain distance varied from 10 to 200 μm has been investigated systematically. The noise magnitude has been observed to be a factor of 10 times lower in comparison with that in recent reports. The normalized noise-power spectral density of $\sim 2.2 \times 10^{-10}$ Hz⁻¹ at $f = 10$ Hz has been obtained. The noise mechanism can be explained by fluctuations of the carrier number, which are originated from the carrier trapping and de-trapping processes.

RESULTS AND DISCUSSION

To investigate the flicker noise, we fabricated GFETs on different substrates (Si/SiO₂ and Si/Si₃N₄) with and without an encapsulated high- κ dielectric layer (Ta₂O₅). A highly *p*-doped Si wafer (1 – 10 Ω .cm) and a 300-nm SiO₂ (or 300-nm Si₃N₄) layer are employed as the back-gate and dielectric layer, respectively. Graphene transistors were prepared in following steps. First, photolithography, electron-beam deposition and lift-off processes were employed to form metal contacts of Cr (3 nm) and Au (100 nm) for source, drain and back-gate. Second, a single graphene sheet was transferred onto the SiO₂/Si or Si₃N₄/Si substrate. A Ta₂O₅ dielectric layer has been grown on top of graphene for some GFET devices in two steps, including growing a 2-nm Ta₂O₅ seed layer by electron beam evaporation and an 18-nm Ta₂O₅ film by ALD.²²⁻²³ Photolithography and dry etching steps were employed to determine the active size of the devices. The distances between source and drain (length), L , are 10, 20, 30, 50, 75, 100, 150, 200 μ m, and the ratio between the width and length, W/L , of the active area is fixed at 2. The detail of the fabrication is provided in the Supplementary Information. A diagram of fabrication steps is illustrated in Figure S1. A surface image of a graphene sheet on Si₃N₄/Si using atomic force microscope (AFM) is provided in Figure S2.

The current – voltage (I-V) behavior was characterized by two Keithley source-meters units. A Keithley 2400 was employed to vary the back-gate voltage, V_{BG} , while a Keithley 2450 was used to set a constant voltage between drain and source contacts, V_{DS} , and to measure the drain current, I_D . Our electrical measurements were performed at room temperature. The I-V characteristics of a GFET covered by an ALD Ta₂O₅ film on Si₃N₄ ($L = 10 \mu$ m, $W = 20 \mu$ m) under $V_{DS} = 0.1$ V is provided as an example in Figure 1, inset. Details of the setup and I-V characteristics at different V_{DS} are illustrated in Figures S3 and S4.

To accurately determine the mobility, μ , of carriers in graphene, the contact resistance, R_c , on a level with the graphene channel resistance, R_{ch} , is estimated from the total device resistance, $R = V_{DS}/I_D$. The mobility of carriers in the graphene device can be extracted by fitting the resistance – voltage (R-V) characteristic curve (Figure 1) in the following form.²⁴⁻²⁶

$$R = 2R_c + R_{ch} = 2R_c + \frac{L}{Wq\mu\sqrt{n_0^2 + n_g^2}}, \quad (1)$$

where q is the charge of electron, n_0 is the carrier density resulting from charged impurities at the interface between dielectric layers and graphene or in the dielectric layers, $n_g = \frac{C_G}{q}(V_{BG} - V_D)$ is the density of charged carriers generated by a voltage on the back-gate away from the charge neutrality point voltage, V_D , (the Dirac point), $C_G = \frac{\epsilon\epsilon_0}{d}$ is the areal capacitance of the gate, with d being the thickness of the Si₃N₄ dielectric material ($d = 300$ nm), ϵ_0 is the vacuum permittivity, and $\epsilon \sim 6$ is the dielectric constant of

Si₃N₄.²⁷ The capacitance of the 300-nm Si₃N₄ dielectric layer is ~17 nF/cm². The red curve in Figure 1 presents the best fit to the R-V characteristic data using Eq. 1. We obtained the contact resistance at each electrode of ~209 Ω. The carrier density generated by charged impurities is ~2.4 × 10¹¹ cm⁻² at Dirac point. A high carrier mobility has been obtained in the GFET of ~5080 cm²/(V·s).

The level of the flicker noise is the key point for the performance of graphene devices. The 1/f noise was identified using a 100 kHz FFT spectrum analyzer (SR770) at room temperature. A current amplifier (FEMTO DLPCA-200) was employed to amplify the drain current. At a fixed back-gate voltage, the drain current was varied by adjusting drain-source voltage, V_{DS} , from 20 mV to 0.5 V. The noise-power spectral density can be described as,

$$S_I = \frac{AI_D^2}{f^\gamma}, \quad (2)$$

where A is the amplitude of the noise and follows the empirical relation, $A = \alpha_H/n$, with α_H being the Hooge's noise parameter to evaluate the magnitude of the flicker noise,⁴⁻⁵ n is the total amount of carriers passing through the conducting area, $\gamma \approx 1$ is an experimental value.^{5,7}

The noise-power spectral density of GFETs on Si₃N₄ ($L \times W = 10 \times 20 \mu\text{m}^2$) with the ALD Ta₂O₅ encapsulated layer was investigated under different drain current from 6.18 to 156.8 μA, and the voltage of the back-gate was fixed at Dirac point ($V_{BG} = V_D = 1 \text{ V}$). A typical noise-power spectral density under $V_{DS} = 0.1 \text{ V}$ is shown in Figure 2a (upper inset). This plot follows the 1/f dependence (namely, $\gamma = 1$), and the noise-power spectral density, S_I , is ~10⁻¹⁸ A² Hz⁻¹ at 1 Hz. The absence of bulges on the noise-power spectral density in this GFET device indicates that traps with a specific time constant are not dominated in the spectrum. Note that a few bulges have been reported in GFETs on Si/SiO₂. The bulges come from the generation-recombination (G-R) noise indicating fluctuation processes with well-defined frequencies.⁵ When the drain current, I_D , was varied from 6.18 to 156.8 μA, the noise-power spectral density increases with a square function from 3.2×10^{-19} to 7.7×10^{-17} A² Hz⁻¹ at $f = 1 \text{ Hz}$ as plotted on a linear scale (Figure 2a) and a log-log plot (Figure 2a, lower inset). The noise-power spectral density proportional to I_D^2 is also reported in previous reports for graphene devices on SiO₂.^{5,10}

To evaluate the noise of GFETs on different insulator/dielectric layers, we determine the normalized noise-power spectral density, in which the noise is normalized with current, S_I/I_D^2 , or the noise behavior independent of the drain current flowing through the device. The experiments performed under $V_{DS} = 0.1 \text{ V}$ and $V_{BG} = V_D = 1 \text{ V}$ for graphene devices on SiO₂, Si₃N₄, and on Si₃N₄ with the ALD Ta₂O₅ encapsulated layer (Figure 2b). These devices were fabricated under the same conditions and graphene channel size of $L = 10 \mu\text{m}$ and $W = 20 \mu\text{m}$. The noise level at $f = 1 \text{ Hz}$ of the graphene device on SiO₂ without the ALD Ta₂O₅ layer is $1.8 \times 10^{-8} \text{ Hz}^{-1}$, which is similar to previous reports.^{10, 12} The graphene on Si₃N₄ device without the ALD Ta₂O₅ layer shows a lower noise level of $0.8 \times 10^{-8} \text{ Hz}^{-1}$, which is about 2 times lower

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3 than that of graphene on SiO₂ device. However, the graphene device covered with the high- κ Ta₂O₅
4 dielectric layer on Si₃N₄ shows a noise level of 2.5×10^{-9} Hz⁻¹. At $f = 10$ Hz, the normalized noise-power
5 spectral density, S_I/I_D^2 , of this device is equal to 2.2×10^{-10} Hz⁻¹, indicating a reduction of the $1/f$ noise by
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8 5 and 50 times as compared to that of graphene devices on h-BN and SiO₂, respectively.¹⁰⁻¹²
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10 The gate-bias characteristics of the noise-power spectral density normalized with current were further
11 examined for the graphene device on Si₃N₄ with the ALD Ta₂O₅ layer under different back-gate voltage.
12 The normalized noise-power spectral density, S_I/I_D^2 , and together with the amplitude of the noise, $A =$
13 $(1/M)\sum_{m=1}^M f_m S_{Im}/I_m^2$, as function of gate voltage, $(V_{BG} - V_D)$, for graphene devices on SiO₂, Si₃N₄, and
14 on Si₃N₄ with the ALD Ta₂O₅ encapsulated layer at $f = 1$ Hz are illustrated in Figures 3 and S5,
15 respectively. Note that the noise amplitude is an average over several frequencies, thus, is the same as the
16 noise-power spectral density normalized with current, S_I/I_D^2 . As shown in Figure 3, M-shape behaviors
17 of the noise-power spectral density normalized with current have been observed in devices with graphene
18 on SiO₂ and Si₃N₄ with local minimum at $V_{BG} = V_D$. The observation of the noise behavior agrees with
19 previous reports,^{10, 12, 28} indicating that the noise at low-frequency in our devices on SiO₂ is typical for
20 graphene. The characteristic is related to the presence of the spatial charge inhomogeneity as well as
21 electron-hole puddles in graphene devices on SiO₂.²⁸ In contrast, the behavior is not observed in graphene
22 devices on Si₃N₄ with the ALD Ta₂O₅ layer. The noise-power spectral density normalized with current
23 together with the amplitude of the noise are more than one order of magnitude lower in the graphene
24 device on Si₃N₄ with the ALD Ta₂O₅ encapsulated layer compared to that on SiO₂. A Λ -shape instead of
25 an M-shape has been observed in the device (Figure 3). The noise level is lower when voltage applied to
26 the back-gate is further away from Dirac point voltage. Graphene devices without a dielectric layer
27 (Ta₂O₅) can absorb water vapor or organic contaminations under environmental exposures, which leads
28 to a high noise level.^{12, 29-30}
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40 We now address the origin and physical mechanism of the flicker noise behavior in our devices. From
41 a relation between the drain current, mobility and the number of charge carriers ($I_D \propto q\mu n$) in Eq. 1,
42 fluctuations in the drain current can be described as $\delta I_D \propto qn\delta\mu + q\mu\delta n$.⁵⁻⁶ The flicker noise in FET
43 devices typically originates from fluctuations in the carrier mobility or the number of charge carriers, or
44 both.³¹ In the context of the fluctuations in the carrier mobility described by Hooge model, the carrier
45 mobility in graphene is typically affected by long-range Coulomb scatterings associated with charged
46 impurities, and short-range disorder scatterings related to intrinsic defects, cracks, or boundaries of
47 graphene.²⁹⁻³⁰ Other scattering processes including ripples, phonons, mid-gap states generate fluctuations
48 in the carrier mobility similar to that expected from the long- and short-range scatterings.^{1, 32-36} Thus, we
49 will analyze the fluctuations in these two scattering sources separately. The carrier mobility limited by
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3 the long-range Coulomb scattering does not exhibit gate-bias dependence, whereas the mobility
4 associated with the other scattering depends on the gate-bias.¹ The behavior of the noise will be
5 determined by which scattering mechanism contributes dominantly. In the viewpoint of fluctuations in
6 the carrier number expected from the McWhorter's relation, the fluctuations are induced by the number
7 of charge carriers passing through graphene layer due to the trapping/de-trapping processes near
8 graphene-dielectric interfaces. The efficiency of these processes is defined by the density of empty as
9 well filled states near the Fermi level.

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11 Our observation of an M-shape behavior in graphene on SiO₂ and Si₃N₄ devices (Figure 3) is
12 consistent with previous reports of non-encapsulated GFET structures on SiO₂.^{10, 29-30} In these structures,
13 molecules from the air (i.e., water-like contaminants) trapped on graphene are likely adding to the source
14 of the charge-density inhomogeneity (or charge puddles) near Dirac point, which arises the long-range
15 Coulomb scattering across the graphene channel.³⁵⁻³⁶ Transforming from the M- to V-shape after
16 annealing these devices was assigned to the suppression of the long-range scattering by removing
17 absorbed molecules, thus, reducing the fluctuations in the carrier mobility.²⁹ On the other hand, the M-
18 shape noise behavior can also originate from the high trap density in the device fabrication process.²⁸
19 These traps cause trapping/de-trapping processes of charged carriers near the graphene - SiO₂ interface
20 that induces the fluctuations in number carrier.

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22 The unexpected gate-bias behavior of the flicker noise in graphene on SiO₂ reported in several
23 observations complies with the Hooge approach.³⁷ The measured noise can be interpreted by an empirical
24 relation between the Hooge's noise parameter, α_H , the mobility, μ , and a network of resistors.³⁰ While
25 carrier mobility associated with the long-range Coulomb scattering is independent of the gate-voltage
26 (i.e., $\mu_L = 1/C_L$), the carrier mobility related to the short-range scattering is inversely proportional to
27 voltage applied on the back gate, $\mu_S = 1/(C_S(V_{BG} - V_D))$, where C_L and C_S are the long- and short-range
28 scattering constants.³⁸⁻³⁹ Following the dependence of the Hooge parameter (i.e., $\alpha_H \approx (1/\mu)^\delta$) on the
29 carrier mobility³⁰ and Matthiesen's rule (i.e., $1/\mu = 1/\mu_L + 1/\mu_S$), the dependence on the gate bias of
30 normalized noise-power spectral density is expressed as,³⁰

$$\frac{S_1}{I^2} = \frac{\alpha_H}{nf^\gamma} \approx \frac{(C_S(V_{BG} - V_D) + C_L)^\delta}{(V_{BG} - V_D)f^\gamma}, \quad (3)$$

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32 where the $\delta \approx 3$ is experimentally determined for graphene on a substrate device.^{30, 40} The $1/f$ noise is
33 contributed by both the short- and long-range carrier scattering. The transport property of carriers near
34 Dirac point in graphene channel is governed by spatial charge inhomogeneity which is related to the
35 presence of electron-hole puddles in graphene, resulting in an increase in fluctuations.²⁸ The V-shape
36 have been observed. For voltage applied on the back-gate away from Dirac point, fluctuations are
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3 governed by long-range Coulomb scattering, thus, the $1/f$ noise decreases with increasing V_{BG} .³⁰ The M-
4 shape behavior has been observed in our graphene device on SiO_2 .

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6 To improve the device performance as well as to reduce the flicker noise in our graphene devices, we
7 have employed a high- κ dielectric material, Si_3N_4 , for the insulator gate, and encapsulated graphene with
8 an ALD Ta_2O_5 layer. As mentioned above, the normalized noise-power spectral density is more than one
9 order of magnitude lower in the graphene device on Si_3N_4 with the ALD top layer as compared to that on
10 SiO_2 . The observed $1/f$ noise behavior in these devices presents the Λ -shape dependence (Figure 3). The
11 short-range disorder scattering does not primarily attribute to the flicker noise of our devices. Therefore,
12 the carrier-mobility fluctuations in the short- and long-range scatterings associated with the Hooge model
13 do not contribute dominantly to the flicker noise, whereas the fluctuations in the carrier number associated
14 with the McWhorter approach have a major role in the flicker noise of these devices.

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16 The decrease of impurities in graphene devices on Si_3N_4 with an ALD Ta_2O_5 encapsulated layer is
17 expected from our fabrication process. Although our devices are not annealed to remove atmospheric
18 contaminants, the $1/f$ noise reduction and Λ -shape behavior have been obtained. Typically, metal contacts
19 were implemented by depositing metals on top of graphene on a substrate. This method caused the
20 contamination of photoresist residues on graphene during the photolithography process. In contrast, our
21 fabrication process starts with a well-prepared structure of $\text{Si}/\text{Si}_3\text{N}_4/\text{metal-contacts}$, and a single graphene
22 sheet is transferred onto this structure. Graphene surface is not covered by polymer at any stage of the
23 fabrication, reducing the number of traps at interfaces of graphene/metal contacts and graphene/ Si_3N_4 .
24 The reduction of photoresist residuals on graphene surface before growing the ALD Ta_2O_5 layer was
25 confirmed by AFM image (Supplementary information, Figure S2).

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27 In order to reduce the fluctuations in the carrier mobility, the high- κ ALD Ta_2O_5 dielectric layer has
28 been deposited on the top of our graphene devices to suppress the long-range Coulomb scattering as well
29 as protect the graphene surface. Although a degradation of the carrier mobility in graphene could happen
30 when the dielectric layer was grown on top of graphene, this dielectric layer with high quality could
31 protect graphene from exposure conditions to prevent the increase of $1/f$ noise.¹⁴ The dielectric screening
32 effect of the high- κ Ta_2O_5 dielectric material can minimize the long-range Coulomb scattering
33 efficiently.⁴¹ On the other hand, to achieve a uniform deposition of the ALD layer on graphene, a 2-nm
34 Ta_2O_5 seed layer was deposited by electron beam evaporation. The samples were loaded into a vacuum
35 chamber (3×10^{-6} Torr), which significant reduced contaminants on the surface of graphene before
36 growing the 2-nm Ta_2O_5 seed layer. During the evaporation step, the 2-nm Ta_2O_5 layer contains oxygen
37 vacancies, acting as carrier traps at the interface between graphene and the seed layer. The oxygen
38 vacancy-related traps can generate fluctuations in the carrier number through random trapping/de-
39 trapping processes of carriers. Thanks to H_2O pulses during the first few cycles of the ALD process at
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300 °C, the 2-nm TaO_x seed layer is fully oxidized, resulting in a low number of carrier traps in the seed layer. Consequently, the suppression of the long-range scattering as well as fewer effective trap states at the interfaces between graphene and oxide resulted in the reducing of the noise and produced the Λ -shape gate-bias behavior. Note that by varying the voltage applied on the gate, we can control the carrier number in the active area. As mentioned before, the normalized noise-power spectral density does not follow the simple $1/(V_{BG} - V_D)$ dependence as expected from the Hooge approach (Figure 3). The Λ -shape gate-bias behavior suggests that another physical mechanism for the flicker noise of the drain current dominates in our GFETs.

To shed light on the mechanism of the flicker noise, we further investigated noise characteristics with different device area. The active area, $L \times W$, is varied in a wide range from 200 to 80000 μm^2 , where the lengths, L , are 10, 20, 30, 50, 75, 100, 150, 200 μm , and the ratio of W/L is fixed at 2. The voltage between source and drain, V_{DS} , was fixed at 0.1 V. For the device with $L \times W = 200 \times 400 \mu\text{m}^2$, at Dirac point ($V_{BG} = V_D$) and $f = 10$ Hz, a maximum value of $\sim 1 \times 10^{-12} \text{ Hz}^{-1}$ has been observed for the normalized noise-power spectral density (Figure S6). The value is several orders of magnitude lower than that in devices on SiO₂ reported in the literature.¹⁰⁻¹² To compare the flicker noise behavior in the graphene devices with different active area, we employ the area-normalized noise-power spectral density, $\beta = (S_I/I_D^2)(L \times W)$.¹⁰⁻¹¹ Figure 4 shows plots of β parameter at $f = 10$ Hz, ranging between 1×10^{-9} to $5 \times 10^{-9} \mu\text{m}^2 \text{ Hz}^{-1}$ for the length, L , of $< 50 \mu\text{m}$. In the micrometer scale, the flicker noise in these devices was reduced by a factor of 5 as compared to that in graphene devices encapsulated by two h-BN layers,¹¹ a HfO₂ dielectric gate¹⁴, or on h-BN¹⁰ with β reported from 5×10^{-9} to $10^{-7} \mu\text{m}^2 \text{ Hz}^{-1}$ at $f = 10$ Hz. The value is the same order with multiple graphene layers on a substrate.⁴² However, the mobility of carrier decreases with adding graphene layers,⁴²⁻⁴³ thus, reducing the performance of the devices. Note that under identical conditions including gate-bias and temperature, the carrier number is proportional to the active area.¹² As illustrated in Figure 4, the area-normalized noise-power spectral density does not scale inversely proportional to the device area (namely, the simple $1/n$ dependence or the graphene sheet resistant).⁴⁴ This suggests that the reduction of the noise and the Λ -shape behavior of the devices covered with the ALD Ta₂O₅ dielectric layer cannot be explained with the Hooge's model.

To provide insight into the Λ -shape behavior, we employed the framework of the McWhorter approach based on the fluctuations in the carrier number of single-layer graphene in field-effect transistors. The amount of charged carriers in the active area can be varied by sweeping the back-gate voltage further away from Dirac point, and this value is proportional to the gate voltage, V_{BG} (see Eq. 1).²⁴ In the McWhorter model, normalized noise-power spectral density, S_I/I_D^2 , reduces with the $1/n^2$ dependence, thus, the β parameter is proportion to $1/n$ or $1/V_{BG}$.¹² The carrier tunneling to/from the

graphene channel through the trapping/de-trapping processes gives rise to the fluctuations in the carrier number in the graphene channel, which mainly contributes to the $1/f$ noise. The inset of Figure 4 shows the β parameter is scaled down with the back-gate bias, V_{BG} . The noise characteristic in our devices can be explained by the McWhorter model, in which the fluctuations in the carrier number are the dominant source for the flicker noise.

Following the McWhorter approach, we can estimate the effective trap density, D_{eff} , at Fermi level from normalized noise-power spectral density:⁴⁵

$$\frac{S_I}{I^2} = \frac{k_B T D_{\text{eff}}}{f L W n_c^2 \ln(\tau_{\text{max}}/\tau_{\text{min}})}, \quad (4)$$

where T is the temperature, τ_{min} and τ_{max} are the minimum and maximum time for carrier tunneling, respectively, and k_B is Boltzmann's constant. The carrier concentration in the active area can be estimated from the charged carrier density, $n_c = \sqrt{n_0^2 + n_g^2}$. The approach has been used to analyze the low-frequency noise in metal-oxide-semiconductor field-effect transistors based on Si or GaAs.⁴⁵ To estimate D_{eff} , we fit the experimental results to the McWhorter model (Eq. 4) with $\ln(\tau_{\text{max}}/\tau_{\text{min}}) = 4$,^{15, 45} (the red line in Figure 2b). Under $V_{DS} = 0.1$ V, the effective trap density, D_{eff} , is $\sim 1.14 \times 10^{10}$ cm⁻² eV⁻¹ at Dirac point (i.e., $V_{BG} = V_D$), which is a factor of 10 times lower than that of GFETs on the SiO₂/Si substrate.^{32-33, 46}

CONCLUSIONS

In summary, we have carried out measurements of the low-frequency $1/f$ noise on graphene field-effect transistors covered by the high- k dielectric Ta₂O₅ layer (a few nanometers thick) on Si₃N₄. A low noise level of $\sim 2.2 \times 10^{-10}$ Hz⁻¹ has been obtained at $f = 10$ Hz. The dependence on the channel graphene area of the noise was also investigated systematically. The origin and physical mechanism of the noise can be interpreted by the McWhorter model, in which the tunneling of carriers from/to the graphene channel via the trapping/de-trapping processes in dielectric layers processes is the determining factor. The considerable suppression of flicker noise can offer guidance on practical implications.

ASSOCIATED CONTENT

Supporting Information: The Supporting Information is available free of charge on the ACS Publications website at xxx. Details for GFET fabrication, atomic force microscopy images, electrical setup, I-V transfer characteristics, noise amplitude, normalized noise-power spectral density.

AUTHOR INFORMATION**Corresponding Author**

*E-mail: vinh@vt.edu

ORCID

V. X. Ho: 0000-0001-5413-9030

N. Q. Vinh: 0000-0002-3071-1722

Author Contributions

[†]Y. Wang and V. X. Ho contributed equally to this work.

Notes

The authors declare no competing financial interest.

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Figure captions

Figure 1: Resistance – voltage transfer characteristics of a graphene device covered by an ALD Ta₂O₅ film on Si₃N₄ ($L = 10 \mu\text{m}$, $W = 20 \mu\text{m}$) at room temperature under $V_{\text{DS}} = 0.1 \text{ V}$. The left inset provides a schematic of our graphene device, and the right inset shows the original current – voltage transfer curve.

Figure 2: The flicker noise in GFETs ($L = 10 \mu\text{m}$, $W = 20 \mu\text{m}$) at Dirac point voltage (mainly, $V_{\text{BG}} = V_{\text{D}} = 1$) and under $V_{\text{DS}} = 0.1 \text{ V}$. **(a)** The noise-power spectral density at $f = 1 \text{ Hz}$ increases with a square function of the drain current. Upper inset provides the noise-power spectral density, while lower inset presents the noise-power spectral density at $f = 1 \text{ Hz}$. **(b)** The noise-power spectral density is normalized with current in graphene on SiO₂, Si₃N₄, and on Si₃N₄ with the ALD Ta₂O₅ encapsulated layer.

Figure 3: Normalized noise-power spectral density as function of back-gate voltage ($V_{\text{BG}} - V_{\text{D}}$) for graphene on SiO₂, Si₃N₄, and Si₃N₄ with the ALD Ta₂O₅ encapsulated layer at $f = 1 \text{ Hz}$.

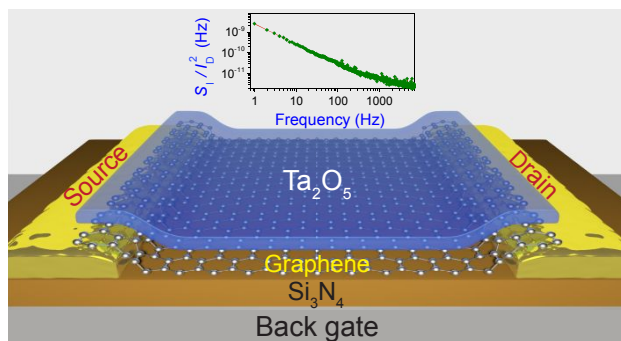
Figure 4: Area-normalized noise-power spectral density, $\beta = (S_I/I_D^2)(L \times W)$, at $f = 10 \text{ Hz}$ plots against the back-gate voltage ($V_{\text{BG}} - V_{\text{D}}$) for graphene devices on Si₃N₄ with the ALD Ta₂O₅ encapsulated layer. Inset shows the data on the log-log scale.

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Table of Contents graphic:

Schematic of graphene devices including back-gate, graphene, dielectric layers (Si₃N₄, Ta₂O₅), and 1/*f* noise.

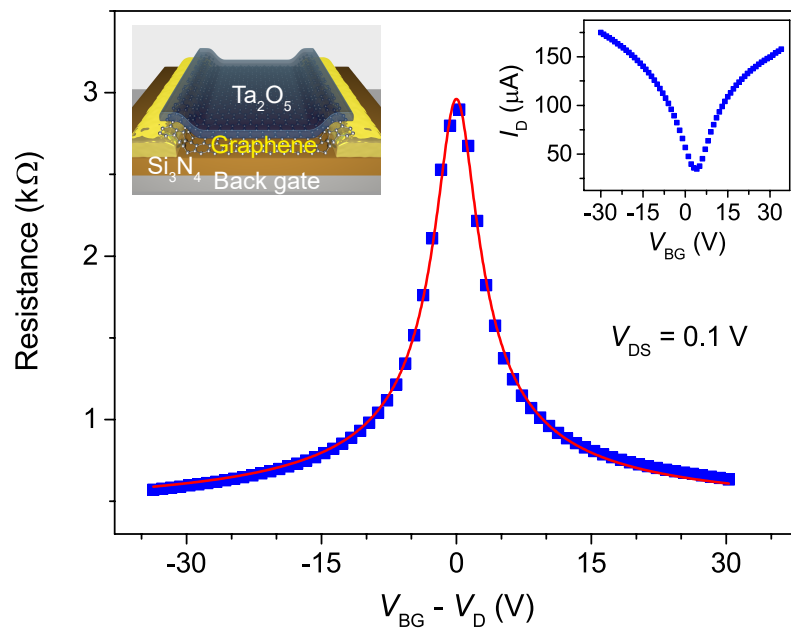


Figure 1

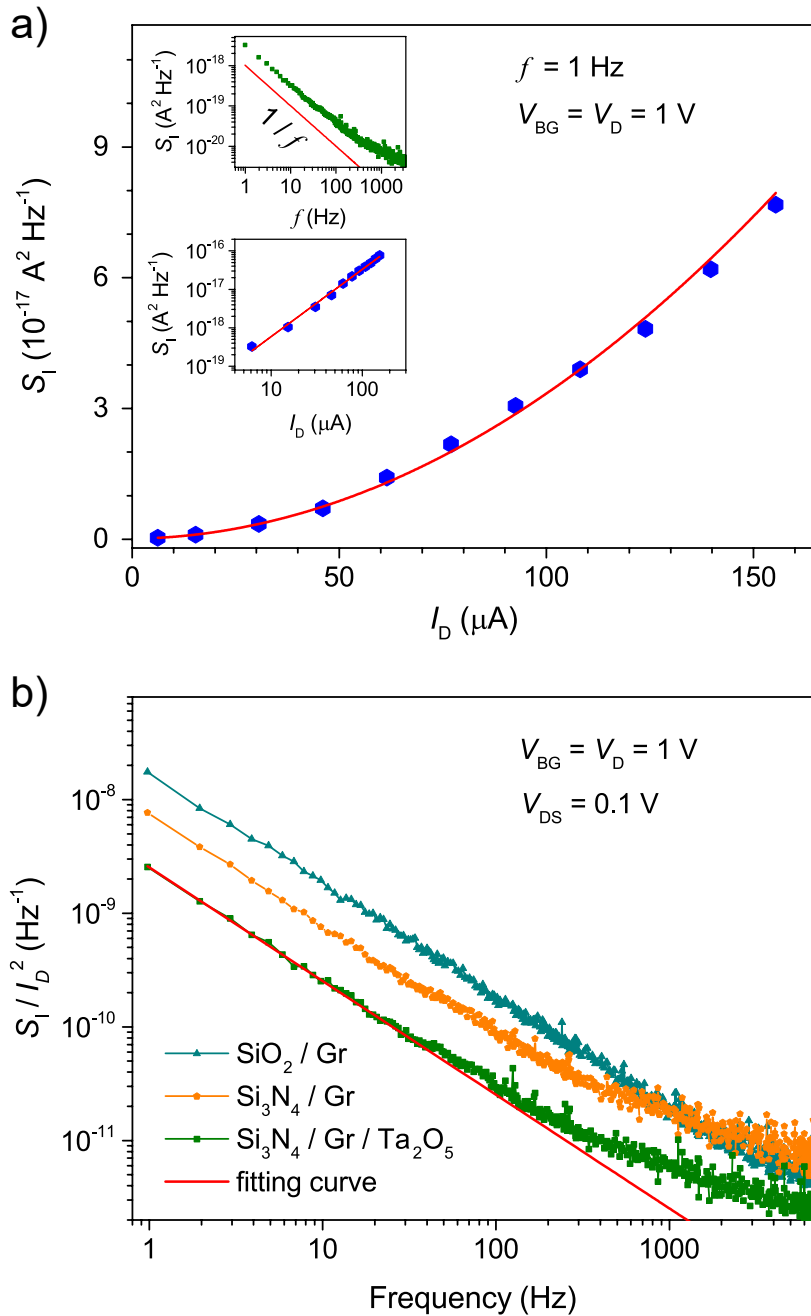


Figure 2

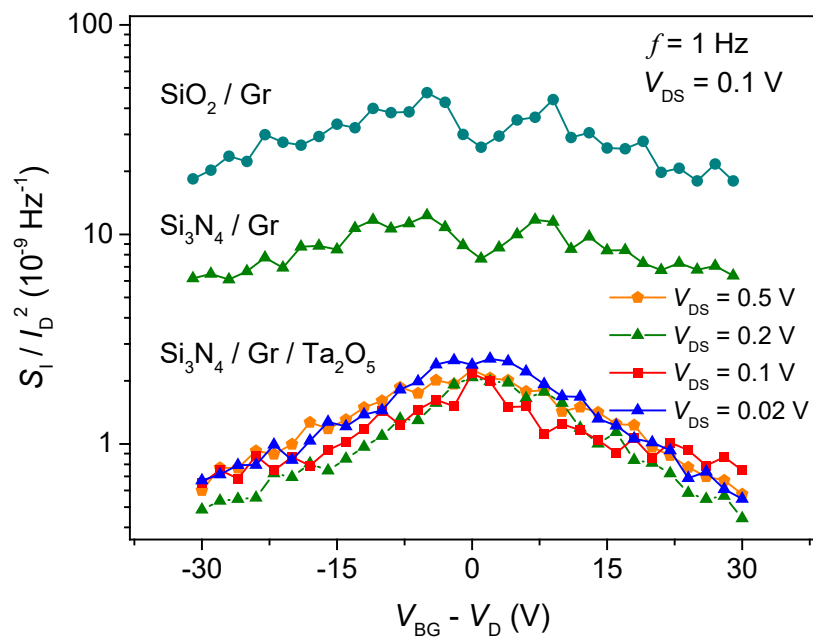


Figure 3

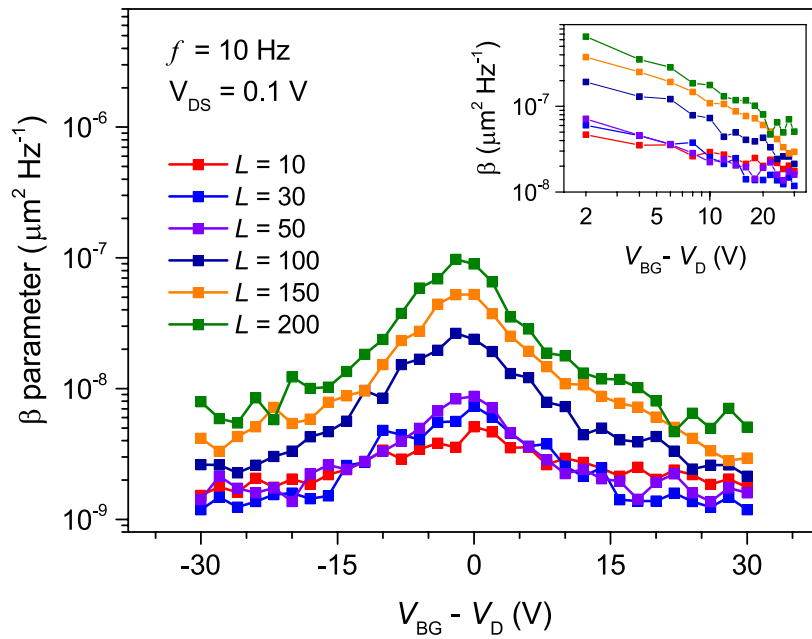


Figure 4