Upscaling of 500 °C Durable SiC JFET-R Integrated Circuits

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Abstract
At HiTEC 2018, NASA Glenn Research Center reported the first demonstration of yearlong 500 °C operation of ceramic-packaged "Generation 10" ~200-transistor integrated circuits (ICs) based on two-level interconnect silicon carbide (4H-SiC) junction field effect transistors and resistors (JFET-R). This HiTEC 2021 submission updates on-going efforts at NASA Glenn spanning two subsequent prototype IC generations "11 and 12" to increase both complexity and durability of these ICs. Increased chip complexities of around 1000 transistors/chip for Gen. 11 and near 3000 transistors/chip for Gen. 12 are made possible by reductions in minimum layout feature sizes (including resistor width shrinkage from 6 µm to 2 µm) coupled with enlarged die size (from 3 x 3 mm to 5 x 5 mm). Gen. 11 ICs electrically tested to date include an 8-bit delta-sigma analog to digital converter (ADC) as well as upscaled random access memory (RAM) and nearly 1 kbit read only memory (ROM). However, Gen. 11 prototype ICs exhibited significantly lower yield and durability than Gen. 10 ICs. Development of revised processing is being investigated towards mitigating these issues in subsequent Gen. 12 fabrication run currently in progress.

Key words
Integrated Circuit, JFET, SiC, Analog-to-Digital, Memory, 500 °C

I. Introduction
Operational lifetime is obviously an essential consideration to designers contemplating infusion of high temperature electronics towards enhancing the performance of systems. Circuit parts that are incapable of predictably prolonged operation at desired high temperature application environments are unlikely to support reliable device operation necessary to achieve widespread beneficial deployment. As such, NASA Glenn Research Center has focused its high temperature electronics development efforts on greatly expanding the temperature envelope for durable semiconductor integrated circuit (IC) operation from below 300 °C to at least 500 °C.

At HiTEC 2018, NASA Glenn reported the first ICs to demonstrate more than a year of stable operation at 500 °C [1]. These "Generation 10" prototype ICs are based upon highly robust silicon carbide Junction Field Effect Transistor & Resistor (SiC JFET-R) devices interconnected by two-level $TaSi_2$ interconnect metallization passivated with SiO_2/Si_3N_4 dielectric stack. While these SiC JFET-R chips can perform important electronic functions (such as high-T sensor signal amplification), far broader circuit capabilities and benefits will be enabled by upscaling chip complexities. This work details results from the experimental fabrication of the "Generation 11" NASA Glenn prototype SiC JFET-R chipset.

II. Gen. 11 Experimental

A. Chip Complexity
Using Random Access Memory (RAM) as a benchmark, Fig. 1 illustrates the upscaling undertaken in the Gen. 11 chip designs compared to the Gen. 10 chips. Chip designs prototyped in the Gen. 11 run included a 998 bit Read Only Memory (ROM) chip, a 10-bit synchronous counter chip, and an 8-bit sigma-delta analog to digital converter (ADC), along with other circuits with capabilities well beyond the

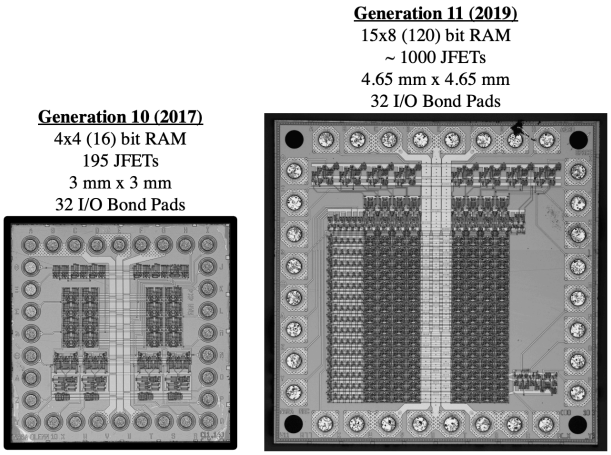

Fig. 1. Illustrative comparison of Gen. 10 and Gen. 11 SiC JFET-R RAM chips.

ICs demonstrated in the Gen. 10 chipset. An increased Gen. 11 circuit density was primarily facilitated by halving the SiC resistor width dimension to 3 µm and increasing the die size to 4.65 x 4.65 mm as shown in Fig. 1.

B. Chip Fabrication

Gen. 11 JFETs and resistors were fabricated by etching and ion implantation as described for prior NASA Glenn IC generations, as were the high-T durable Iridium Interfacial Stack (IrIS) wire bonding pads [1-3]. However, modified Gen. 11 interconnect processing was attempted in an effort to alleviate dielectric crack formation as the primary long-term failure mechanism of these ICs. As detailed in [4], the attempted interconnect process modifications resulted in substantially inferior IC yield and 500 °C durability than achieved for Gen 10. Some chip designs had zero yield due to their physical placement in wafer regions within ~2 cm of the outer edge that suffered from de-lamination of large Metal 1 power bus traces. Fortunately, this de-lamination was did not occur in central wafer regions which permitted shorter-term functional oven-testing of a few Gen. 11 prototype IC designs from 25 °C to 500 °C described in Section III. However, even in central wafer regions the 25 °C probe-test yield of the complex ICs was less than 25%.

Major process refinement goals for the Gen. 12 prototype fabrication run (which has been delayed a year due to COVID-19 related NASA Glenn SiC lab closure) will be to simultaneously correct and eliminate dielectric metal stack crack formation and de-lamination while recovering to functional circuit yields achieved in Gen. 10 in excess of 70%.

C. High-T Packaging

All ICs were probe tested at 25 °C prior to dicing and placement into custom-manufactured High Temperature Co-Fired Ceramic (HTCC) packages which in turn were mounted onto alumina circuit boards [5]. The high temperature packaging process employed for Gen. 11 chips is a modification of the prior-generation packaging procedures detailed elsewhere at this conference [6]. Gold wires with fiberglass sleeve insulation facilitated connections between chips in the ovens and computer-controlled electrical measurement instruments residing outside of the ovens.

III. Gen. 11 Electrical

This section presents results from three Gen. 11 chips that were high-T packaged and oven-tested just prior to closure of NASA Glenn SiC laboratories due to COVID-19. Consistent with our previous reports of SiC JFET-R ICs [1,2], these results were obtained following more than 24 hours of 500 °C burn-in with input/output signal voltages in the range of 0 to -10V, and +VDD and -VSS power supply voltages near ±25 V. It is important to note that none of these chips attained 1000 hours of operation above 460 °C. It is surmised that this notable degradation in durability is due to the processing issues we describe in Section II.B and [4]. However, COVID-19 related SiC lab closure has delayed post-testing inspections of these electrically oven-tested Gen. 11 IC chips.

A. Analog to Digital IC

Fig. 2 shows the electrical block diagram of the tested 8-bit ADC chip. Fig. 3 shows an annotated optical micrograph of the core ADC IC prior to packaging. When the external jumper for delta-sigma mode operation (highlighted in grey) connects the Comparator output to the Pulsed Width Modulation (PWM) Up/Down Control input that controls direction of the Counter, the ADC functions in delta-sigma mode with chip-generated Analog Out signal tracking the Analog In signal. Without this jumper, the ADC can output a PWM signal with the 8-bit counter either always increasing

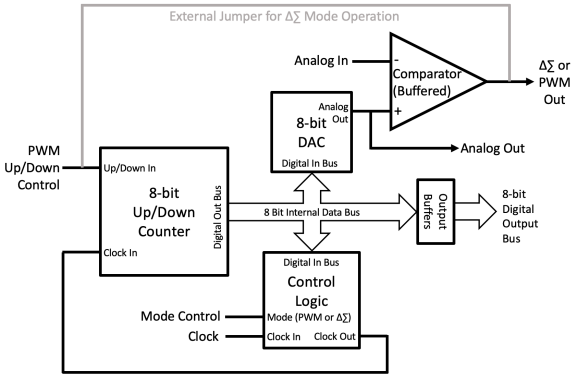

Fig. 2. Functional block diagram of the Gen. 11 8-bit ADC circuit. The chip can be connected to function in either delta-sigma tracking mode or PWM mode.

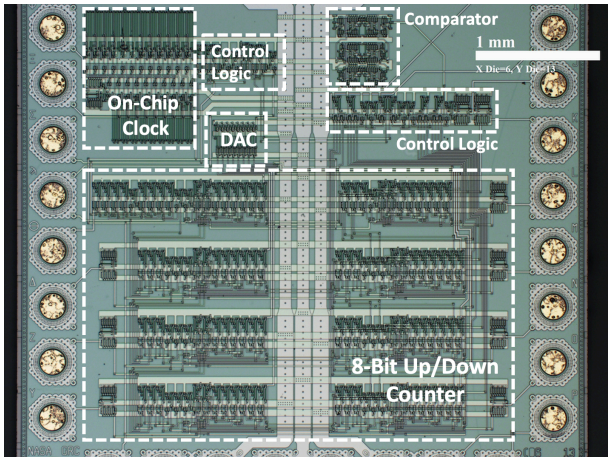

Fig. 3. Annotated microscopic photo of the Gen. 11 Analog to Digital (ADC) IC taken prior to packaging and testing.

or decreasing depending upon the logic signal applied at the PWM Up/Down Control input. The Digital to Analog (DAC) block is implemented using integrated SiC resistor "R2R" ladder circuit architecture [7].

Experimentally measured waveforms demonstrating basic delta-sigma mode digitization of low-frequency sine wave analog input signal at 460 °C are shown in Fig. 4. While the ADC chip design also contains its own on-chip ring oscillator subcircuit for generation of clock signal, a localized absence of metal interconnect from particle defect during photolithography rendered this chip's oscillator non-functional. Therefore, instrument-generated external clock signals were employed for testing of this chip. As expected for delta-sigma mode of operation, the Analog Out

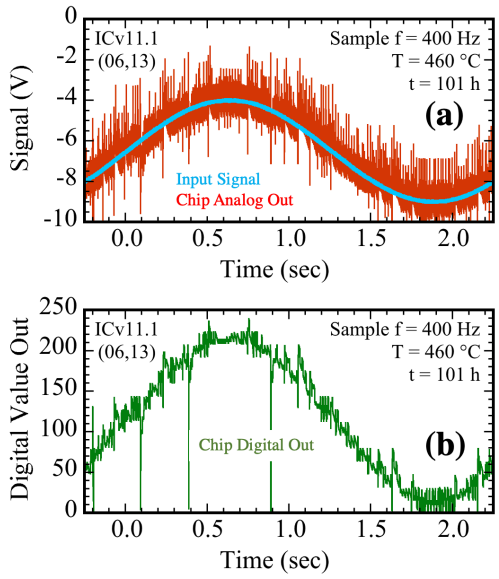

Fig. 4. 460 °C waveforms demonstrating basic delta-sigma mode operation of the Gen. 11 ADC chip digitizing a 0.5 Hz sinewave input signal (see text).

diagnostic signal in red follows the Analog In signal shown in blue in Fig. 4a. The Fig. 4b green trace shows the corresponding digital value waveform constructed from monitoring the 8-bit Digital Output Bus during the test. The roughness of the Fig. 4b digital value waveform suggests that this chip was not functioning at full 8-bit digital resolution at 460 °C. Further testing of the ADC operating in the PWM mode, wherein the counter output increments continuously, confirmed that the two least significant counter bits were indeed malfunctioning. At least some of the substantial noise observed on the red Analog Out diagnostic signal of Fig. 4a are glitches known to be produced by R2R ladders during counter state transitions [7]. Additional circuitry can be added to future versions of this ADC to achieve de-glitched Analog Output signal.

B. Memory ICs

The other two Gen. 11 prototype JFET-R ICs packaged and oven-tested prior to COVID-19 lab closure were a Read-Only Memory (ROM) chip and a Random-Access Memory (RAM) chip. Whereas the Gen. 10 memory chips relied on separated read and write data busses, both Gen. 11 memory ICs implemented high-impedance tri-state buffers and "chip select" control signal that permits both read and write operations as well as multiple memory chips to be combined onto the same data bus. To achieve adequate bus isolation of de-selected chips using depletion mode pass transistors, the shared data bus functions at shifted logic levels slightly above 0V for logic low and near +25V for logic high, similar to the basic approach used to isolate/access memory cells from bit lines inside the RAM chip itself [1]. Each Gen. 11 RAM bit is of the identical 6-JFET schematic circuit design as implemented on Gen. 10, but at 37% less cell area (208 µm x 159 µm). Combined with the larger die area (Fig. 1), single-chip data capacity increased 7.5X over the Gen. 10 prototype RAM chip.

None of the Gen. 11 RAM chips yielded all 120 bits functional at 25 °C. However, a RAM chip with over 90% of its bits working (Fig. 1) was packaged and oven-tested prior to COVID-19. Fig. 5 details the 500 °C measured waveforms from a properly functioning data column of this chip recorded during reading and writing of a "checkerboard" test data pattern of alternating 0's and 1's. It should be noted that a silicon-based test circuit outside the oven with tri-state output buffers custom-built to function at 0 V to +25 V data bus voltages was employed for this test. The address and control signal chip inputs use standard -10 V to 0 V SiC JFET-R logic levels. This and similar additional testing of functional RAM data columns experimentally verified all aspects of the Gen. 11 RAM circuit design as operational from 25 °C to 500 °C [8].

Each bit of the ROM is mask-programmed during fabrication by the presence or absence of a single transistor, which facilitates much higher bit density and memory capacity

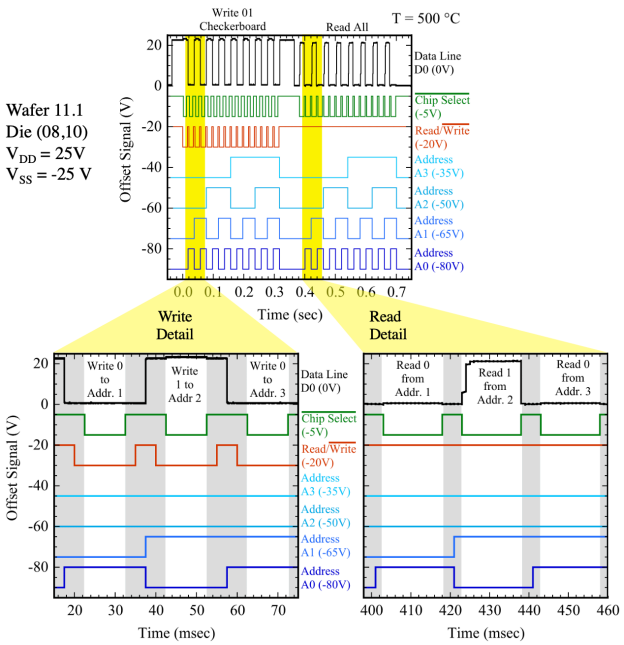

Fig. 5. Measured waveforms detailing 500 °C write and read of checkerboard test pattern for a single 8-bit column of the Gen. 11 RAM chip.

compared to RAM. The interior ROM array is 32 columns by 31 rows that is 4:1 multiplexed into 124 8-bit output words. As reported elsewhere [8], all 992 bits of the oven-tested ROM chip functioned at 25 °C and 500 °C.

C. Venus Lander ICs

Additional Gen 11 prototype chip designs were also fabricated towards demonstrating engineering prototype "long-life" Venus lander electronics [9]. These included 12-bit shift registers, 8-bit and 10-bit counters, comparators, sensor amplifiers, and other circuits customized for implementing all-SiC lander electronics. A multi-chip HTCC circuit board was constructed from these chips in preparation for testing in caustic 92 atmosphere 460 °C environment inside the NASA Glenn Venus environment chamber (GEER). As reported in [8], the circuit board demonstrated basic functionality at 25 °C prior to COVID-19 related suspension of NASA Glenn SiC lab activities.

IV. Gen. 12 Development

NASA Glenn prototype IC Gen. 12 run has been designed to further advance the capabilities of SiC JFET-R ICs. Table I shows the evolution in relevant IC benchmarks for Gen. 10, 11, and 12 developmental prototype generations of NASA Glenn JFET-R chips.

Since accessibility and commercialization are key to technology infusion, NASA Glenn has entered formal partnerships to prototype limited numbers of developmental SiC JFET-R IC chips. Likewise, basic device/circuit models and mask layout design guidelines are publicly available online [10] and a basic device process development kit (PDK) was implemented for the design phase of the NASA Glenn JFET-R IC Gen. 12 wafer run. Potential users can thus explore circuit capabilities and possible benefits via design and simulation of their own application-specific JFET-R ICs. SiC JFET-R IC design services are also commercially available [11]. Under negotiated technology transfer and licensing agreements, a number of outside-user device designs have been prototyped in NASA Glenn SiC JFET-R wafers starting with IC Gen. 11. The next opportunity for prospective users to have devices fabricated on NASA Glenn developmental wafers will be the IC Gen. 13 SiC JFET-R prototype run slated to start in 2022.

TABLE I
MAJOR DESIGN METRICS FOR RECENT GENERATIONS OF EXTREME ENVIRONMENT DURABLE SIC JFET-R ICS

	Gen. 10	**Gen. 11**	**Gen. 12**
Gate Length	6 µm	6 µm	3 µm
Res. Width	6 µm	3 µm	2 µm
Contact Via	6 µm	6 µm	3 µm
JFETs/Chip	~ 200	~ 1000	~ 3000
Die Width	3 mm	4.65 mm	5 mm
Year	2017	2019	2022*

* Delayed by COVID-19 NASA Glenn lab closure.

With modest adjustments, the SiC JFET-R fabrication process is compatible with semiconductor mass-production tools and materials. Towards this end, the processing that forms the SiC JFETs and resistors (without interconnect) for the IC Gen. 12 prototype IC run was recently competitively outsourced [12]. The development of revised interconnect processing followed by completion of the IC Gen. 12 fabrication run (i.e., implementation of interconnects and bond pads) is anticipated to resume in the first half of 2021 following the prolonged closure of the NASA Glenn SiC microfabrication laboratory arising from the COVID-19 pandemic.

V. Conclusion

Successive learning cycles of designing, implementing, and testing prototype SiC JFET-R chips are demonstrating important expansion of application-relevant extreme temperature electronics capability. The NASA Glenn SiC JFET-R Gen. 11 run demonstrated significantly upscaled circuit complexity compared to Gen. 10. However, Gen. 11 interconnect process changes intended to eliminate dielectric cracking resulted in reduced yield and degraded durability compared to Gen. 10. The Gen. 12 prototype is seeking to demonstrate higher yields and durability than Gen. 10 at even higher levels of integration than Gen. 11.

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