Alternative Setup for Long-Duration Low-Duty-Cycle 600°C Ambient Testing of SiC Integrated Circuits

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Abstract

A scalable, compact oven testbed system for simultaneously evaluating a multitude of high temperature integrated circuits (ICs) for prolonged operating times of up to 600 °C has been prototyped. The new testbed system enables long-duration high temperature testing in sufficient statistical quantities consistent with standard aerospace electronics engineering standards. This setup is comprised of multiple compact ovens housing chips or packages mounted to ceramic circuit boards. Each oven is a compact 15.2 cm length by 15.2 cm width by 12.7 cm depth with a maximum 400 Watts of heating power. The custom-made silicon oxide ceramic heating block inside each oven is based on a 3D printed design adapted for the easy insertion of the IC device under test (DUT). This innovative design provides the quick insertion of ICs with or without a ceramic package into a 600 °C environment by utilizing a movable 11.43 cm long ceramic substrate with electrical traces extending from the oven hot zone to external standard plastic-based board connectors. Another key oven design feature is the minimization of the DUT exposure to electromagnetic interference (EMI) by utilizing a filtered DC power source to reduce heating element noise. Additionally, the ovens can be configured in a parallel arrangement allowing global data monitoring over a single industrial RS422 serial port. This feature is important for scaling up to test multiple ICs semi-simultaneously. A USB serial port is provided to independently control the operating parameters of each oven such as the oven target temperature and oven ramp rate. The oven temperature can reach up to 600 °C with a confirmed +/- 4 °C maximum deviation across the test zone region. The ramp rate can be programmed from 1 °C/minute up to 10 °C/minute. Furthermore, a programmable switchboard is used to interface with the DUT. This switchboard comprises a National Instruments Peripheral Component Interconnect eXtension for Instrumentation (NI PXI) system and a breakout board to send and receive power, analog or digital test signals. By using this unique oven testbed system, a variety of ICs can now be tested in parallel using the same test components configured for a diverse set of requirements.

Key words

DC Powered Oven, High Temperature Oven, Programmable Ramp Rate Oven, Software Routable Electrical Connections.

I. Introduction

NASA has long been interested in exploring and understanding the planet Venus. On the surface, this planet's average temperature is around 460 °C with an atmosphere made up with a reactive gas chemistry and over 90 atmosphere pressure. This harsh environment requires specialized high temperature electronics to enable the acquisition and transmission of science data for weeks or months of lander mission duration [1]. Currently, these specialized electronic integrated circuits (ICs) are in development and are Silicon Carbide (SiC) based. Prior to flight and landing on Venus however, these SiC integrated circuits must undergo long-duration high temperature testing in sufficient statistical quantities consistent with standard aerospace electronics engineering standards [2]. However, commercial off-the-shelf (COTS) ovens used to date for

prolonged 460 °C – 500 °C SiC prototype chip testing are physically large in comparison to the ICs and require complex cabling and instrumentation that varies with each IC. Fig. 1 illustrates this previous oven testing setup employed for long-term 500 °C. A number of aspects of this setup render it impractical for achieving large statistical sets of long-term IC testing.

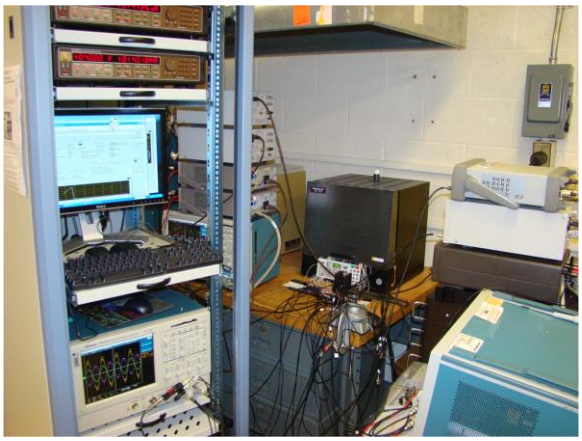
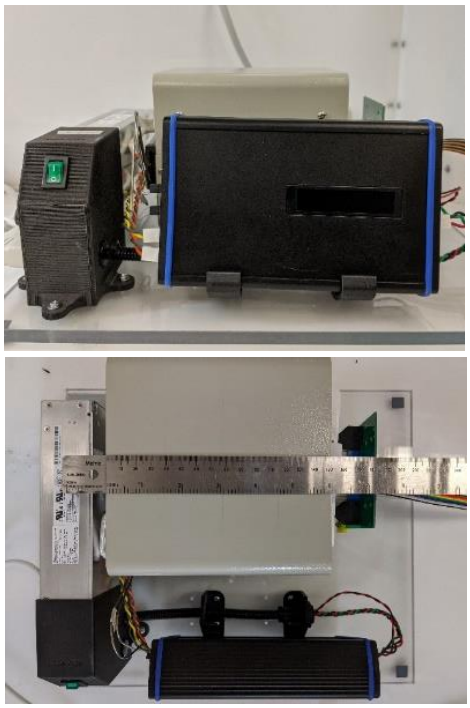


Fig. 1: Photograph of the previously employed NASA Glenn 500 °C IC testing setup.

II. Setup Overview

Since the COTS ovens were considerably larger than required for the IC testing, a much smaller oven was designed and implemented from commercially available parts. Fig. 2 shows the size comparison of the prior large COTS oven compared to the built-up compact oven. The COTS ovens had built-in temperature and step control under the oven housing whereas the compact oven electronics are physically separated as shown in Fig. 3. Each compact oven resides on a small acrylic platform that contains the oven, an oven controller, power supply, and sample board slide assembly.

Fig. 2: Oven Size Comparison of COTS oven (left) and compact oven heating enclosure



(a)

(b)

Fig. 3: Compact oven assembly including heating enclosure, power electronics, and control electronic boxes mounted together on acrylic platform. (a) Front View, (b) Top View

Fig. 4 illustrates the setup with a SiC IC chip at the end of the horizontal ceramic substrate board ready to be slid into the entrance slot of the compact oven. The details of the horizontal ceramic circuit board are covered in a later section of this paper. However, it is important to note at this juncture that this board is designed such that it can hold either an unpackaged SiC chip that is directly attached and wire bonded to the board (as depicted in Fig. 4), or alternatively hold a ceramic chip package of the type described in [3] with

Fig. 4. Illustration of SiC chip compact oven electrical connection and insertion hardware.

wire bonded SiC chip residing therein. Even with the chip inserted fully into the oven at 500 °C, the outside-oven end of the horizontal ceramic substrate circuit board remains cool enough that it mounts into a conventional (plastic) edge connector mounted on the vertical conventional printed circuit board (PCB) shown in Fig. 4. The lower end of the vertical PCB anchors to a rail slider that guides the board insertion and extraction from the slot in the compact oven.

To replace the large rack of instrumentation seen in Fig. 1, a National Instruments Peripheral Component Interconnect eXtensions for Instrumentation (NI PXI) system was procured for a smaller form factor in testing the ICs. This unit compactly integrates individual measurement instrument units like power supplies, oscilloscope, source measurement units (SMUs), and analog inputs and outputs. In addition to customizing the testing rig for particular ICs, the NI PXI system handles the electronic routing of test signals for different chip designs via software-programmed switching relay matrices instead of wires. Fig. 5 presents a simplified schematic of how multiple oven setups are connected in parallel to facilitate simultaneous long-term testing using a single PXI chassis system.

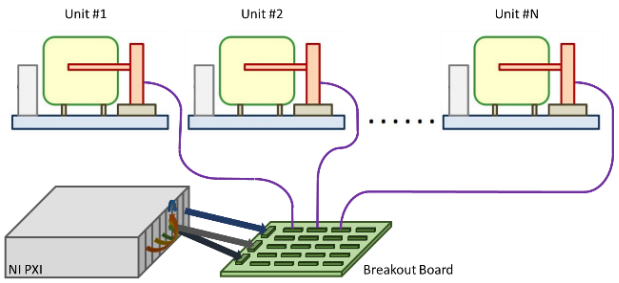


Fig. 5: Simplified schematic depiction of the setup's multiple parallel oven configuration. All wiring connections shown in this figure are ribbon cables.

The PXI connects via ribbon cables to a breakout board that contains passive connections to each chip under test (Fig. 6). The testing setup is capable of running up to 32 ovens with up to 16 test signals per oven, wherein each oven contains one or more SiC ICs.

III. Oven Enclosure Design and Testing

A. Mechanical Construction

Each oven frame is a compact 15.2 cm x 15.2 cm x 12.7 cm COTS empty metal box. The box contains a custom ceramic heater cavity assembly and high temperature insulation. There are a few custom cuts on the COTS empty metal box for electrical connections to the COTS high temperature-heating coils located in the custom ceramic heater cavity assembly in the back and a slot opening in front for the DUT.

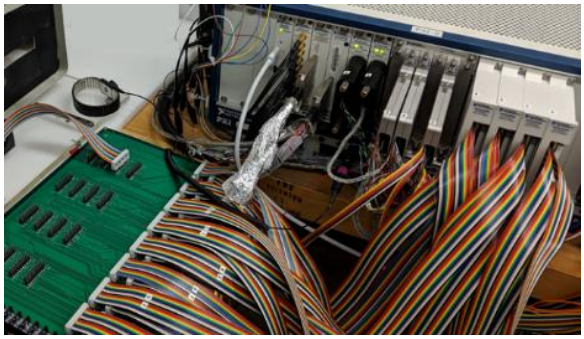


Fig. 6: PXI chassis with instrument and relay matrix system connected to breakout PCB via ribbon cables. The open connectors on the left of the breakout board are for ribbon cables running to each compact oven setup.

The function of the COTS metal box is to center the custom ceramic heater cavity assembly on and around thick high-temperature insulation.

There are two types of high temperature insulation used: a hard 1.5 inch thick insulation and a soft 0.5 inch thick insulation. The hard high temperature insulation provides a solid cover for the custom ceramic heater cavity's heat. Due to the insulating properties of this insulation, the metal box housing is ~41 °C as measured when the oven interior is 550 °C or about 20 °C warmer than room temperature under an exhaust system. However, the hard high temperature insulation produces an abundant amount of undesirable dust that could harm the DUT and electrical connections. In contrast, the soft high temperature insulation produces substantially less dust. Therefore, this insulation primarily surrounds the ceramic heater at the opening and in the back where electrical connections reside as well as fill the gaps between the thick high temperature insulation and COTS metal box.

The Silicon Oxide based custom ceramic heater cavity's assembly shown in Fig. 7 is configured as an open box for insertion of the substrate into the middle cavity space. It houses two COTS quartz plates and two COTS high temperature-heating coils, one above and one below the cavity, to support improved temperature uniformity around the SiC chip/DUT. The COTS quartz plates were cut to specific dimensions and serve the specific purpose of minimizing particles that undesirably fall on the horizontal ceramic substrate board and chip/package. These plates can be unpolished or polished because their properties are equivalent for our application. For a future design of the ovens, a transparent polished quartz window is under consideration. As such, testing with the polished COTS quartz plate properties versus unpolished was conducted. Each COTS high temperature-heating coil ends are crimped to 18 AWG wires and fed through the COTS metal box frame. The high temperature-heater coil supply wires are then twisted into a pair and connected to the oven controller's DC power supply.

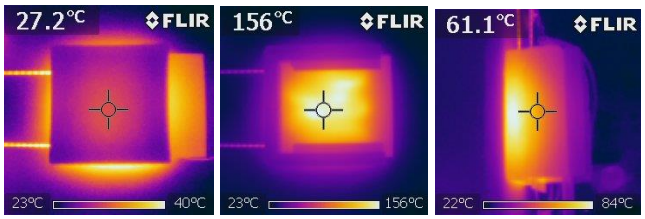
Fig. 7: Side view and bottom view of the custom ceramic heater cavity assembly with COTS quartz plate inserts for reducing particle fallout.

Due to the COTS parts in the custom ceramic heater cavity assembly, the ceramic heater cavity required a custom design made from Silicon Oxide ceramic material. To create this custom ceramic heater cavity shown in Fig. 7 from the Silicon Oxide, a 3D printed plastic model was designed and constructed based on the substrate dimensions of SiC ICs and the COTS parts. After the final design iteration of the custom ceramic heater cavity in 3D printed plastic, a flexible silicon based RTV product was used to surround the 3D printed plastic pieces to create the inverse molds. Once the silicon based RTV hardened, the plastic pieces were removed from the mold and the Silicon Oxide ceramic material was used to fill the new RTV mold. During the ceramic curing process, vibration, tapping, and poking holes were techniques used to prevent air bubbles from forming. After fully hardening, the pieces were taken from the flexible silicon molds and put in a furnace. The furnace heated the ceramic components relatively fast up to ~110 °C to evaporate any water. After holding that temperature for around 4 hours, the parts were slowly heated to 650ºC for hardening and then allowed to cool. Once the parts reached room temperature, they were assembled. A high temperature paste [4] was applied between the custom ceramic heater cavity pieces. Some key lessons learned in the oven fabrication steps were:

1. Apply mold release agent on the 3D parts so they do not stick to the silicon mold when it "hardens",
2. Make sure the molds are leveled for the ceramics, if not, assembly of the parts might not fit together,
3. Do not keep the ceramic pieces in the silicon mold for longer than directed in the manufacturer's instructions or there is a chance of harming the ceramic part during the removal process.
4. The full custom ceramic heater cavity was broken into three different molds (i.e. coil housing, side, and back) for easier removal of the actual hardened ceramic from the silicon mold.

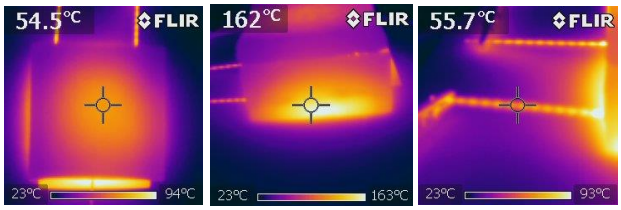
B. Thermal Characterization

The infrared (IR) pictures taken of the ceramic heater assembly without insulation are presented in this section and were recorded using a FLIR i7 thermal imaging camera. IR images presented are shown with the oven core near 150 °C (Fig. 8) and 500 °C (Fig. 9). For clarity of studying the temperature uniformity of a single heating element, the top coil of the ceramic heater assembly was omitted leaving the bottom element as the sole heat source.



(a) (b) (c)

Fig. 8: Infrared camera images of a heater assembly powered by only a lower heating element recorded with the cavity near 150ºC. (a) Top view with top quartz and ceramic cover in place (b) Top view with top ceramic and quartz removed, focused on the bottom quartz plate (c) Side view top quartz and ceramic cover in place.



(a) (b) (c)

Fig. 9: Infrared camera images of a heater assembly powered by only a lower heating element recorded with the cavity near 500ºC. (a) Top view with top quartz and ceramic cover in place (b) Side view top quartz and ceramic cover in place (c) Coil Leads

The oven has been tested to reach up to 600ºC with a +/- 4 °C error across the region where the IC resides. This +/- 4 °C error is dependent upon the level of exposure of the oven cavity to the outside room temperature. Furthermore, if the oven cavity is wide open, the heater does not have enough power to reach 500 °C with the current oven controller's configuration. The current oven controller configuration for the heater coils are in parallel, which limits its maximum power. Originally, a series arrangement was used but abandoned due to the controller providing more power than needed for nominal operation. Therefore, when operating with the DUT and the DUT's edge platform, the heater substrate needed to have some insulation to maintain temperature. Using the soft insulation proved to be marginally acceptable because the internal heat test results varied widely and the substrate connector got excessively hot. Consequently, the hard insulation with a slit opening for the substrate was used for subsequent heating tests. This hard insulation provided repeatable results unlike the soft

insulation. The error also depends on the ramp rate. If the ramp rate is 10 °C/minute, the temperature will drag behind at higher temperatures. The error is considerably smaller when the ramp rate is the 1 or 3 °C/minute. This is perfect for the SiC ICs since a ramp rate of 3 °C/minute to 500 °C is used.

To test the internal temperature gradients, thermocouples were placed in various spots along the substrate. Fig. 10 shows how one of these tests was done. Testing started with the DUT in the middle of the ceramic heater. The results with the ceramic substrate in the middle showed that the bottom heater fed its heat to the top of the substrate. Therefore, the next tests were with the substrate pushed fully in, touching the back of the oven heater. In this configuration, an improved heat distribution between the top and bottom of the substrate was observed. The variation from the top and bottom chip middle was less than 5 °C soaked instead of over 10 °C variation when the board was in the middle of the oven heater. However, still the farthest edge sees the most heat. Fig. 11 shows the temperature gradient of an oven test with the board completely in at 500 °C.

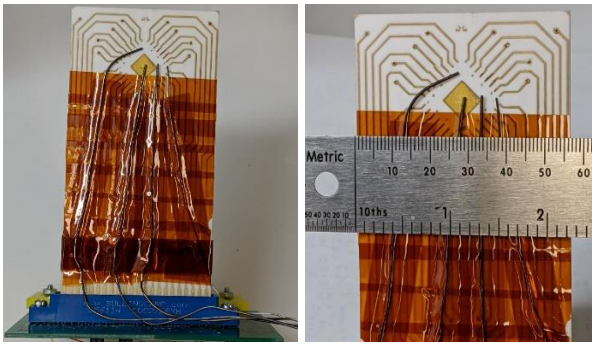


Fig. 10: Photographs illustrating of the thermocouple configuration on the ceramic substrate used for the heat gradient test.

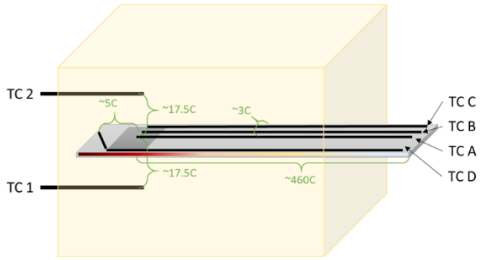


Fig. 11: Annotated illustration of thermocouples and measured temperature differences within the oven cavity at 500 °C and ceramic board fully inserted.

Fig. 12 shows the temperature versus time on a slow ramp of 1 °C/minute and a fast ramp down with 5% heat continued in conjunction with the thermocouple placements shown in Fig. 10 and 11. Fig. 13 shows the temperature versus time on a fast ramp of 20 °C/minute and an uncontrolled ramp down, 0% heat. For these tests, the oven controller was set to 550 °C. The thermocouples on the substrate see both sides of heater and, therefore, are hotter than the two thermocouples above and below.

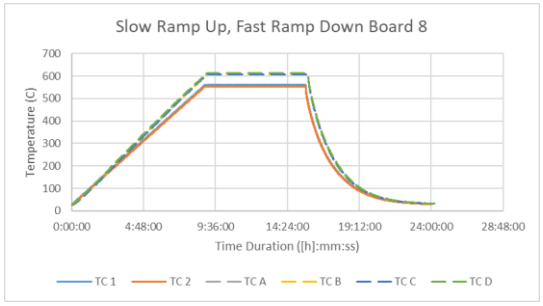


Fig. 12. Plots of thermocouple measurements vs. time for slow (1 °C/minute) ramp up, soak at 550 °C, and power-off cool down.

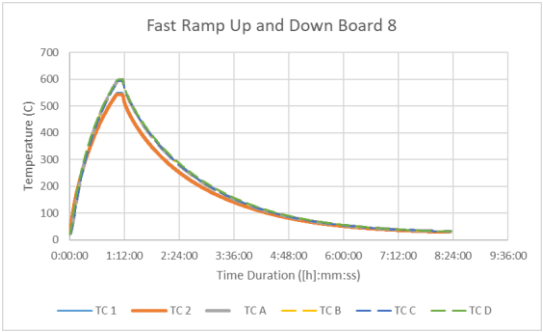


Fig. 13. Plots of thermocouple measurements vs. time for fast (20 °C/minute) ramp up followed by power-off cool down.

C. Oven Controller

Each oven controller typically supplies 120 Watts of power for a rate of 4 °C/minute but can supply up to 400 Watts of power. The oven controller has a DC 48V line for heating the ovens and a 5V line for the control, thermocouples, and communication electronics. See Fig. 14 for a block diagram of the oven controller. The control utilizes a PIC18F46K22 microchip microcontroller, which is programmed to control oven target temperature and oven ramp rate independently. The oven ramp rate can be programmed from 1ºC/minute up to 10ºC/minute. It is possible for a higher ramp rate but the oven power is limited because the two heaters are in parallel configuration.

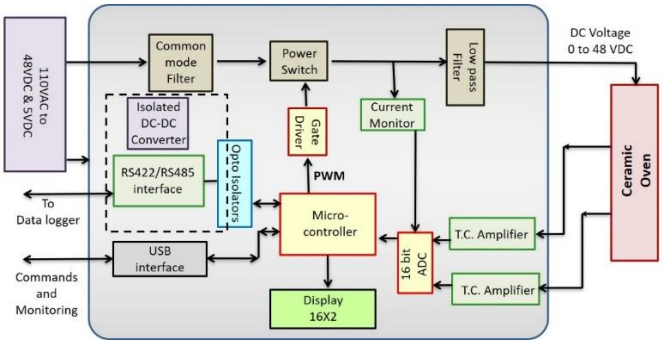


Fig. 14: Block diagram of oven control electronics.

Using DC instead of AC reduces the EMI radiating from the heating elements within the oven. The PIC18F46K22 microcontroller within the oven controller utilizes one of its pulse width modulation (PWM) channels to drive a LM5109 half bridge gate driver that has its upper rail tied to the 48 V bus. This construct generates a 48 V peak-to-peak square wave with a varying duty cycle that is run through a low pass filter to remove the primary and higher order frequency components of the PWM signal. The filtered PWM signal provides an adjustable DC voltage that supplies the power required to heat the ovens. A quirk of the PIC18F46K22 PWM peripherals is that the duty cycle cannot be fully off or fully on. It is limited to anywhere between a 5% and 80% duty cycle. Therefore, when the oven requires the heat to be off, the controller still provides 5% heat. Results show that this 5% does not slow down the ramp down curves but will not allow the oven to sit at room temperature. It will be about 5 °C warmer than room temperature.

There is a USB port for setting up the individual oven controller parameters such as temperature set points and ramp rates. There is also a second RS-422 communication port for networking multiple ovens together, see Fig. 15. This feature allows a single monitoring computer system to observe and record the real time temperature in multiple ovens on one RS-422 channel by using an oven's specific identification number. To link each oven together it goes through a daisy chain communication board. Each board connects to the previous chain, an oven, and the next board if applicable. This feature is crucial for testing multiple ovens at once.

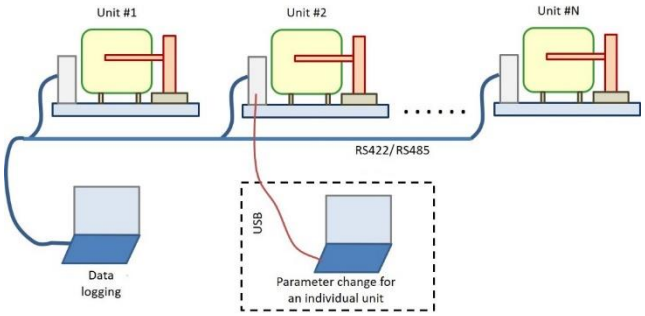


Fig.15: Simplified illustration of oven communication network.

IV. Measuring ICs in the Oven

The ICs, whether in a ceramic package or open, are placed on a movable 11.43 cm long Al_2O_3 substrate. The chip containing one or more ICs resides on the gold square on the ceramic substrate. The wire bonding connects the pins on the chip to certain pads on the substrate giving access to inputs and outputs of particular ICs. Fig. 16 shows two versions of the chip pad placement. Fig. 16a moves the pin to the specific pad near the pin whereas the other, Fig. 16b can jump pin(s) to another location pad. This gives flexibility for the wire bonding. The line traces on the substrate are 22 mils thick with a minimum spacing of 47 mils. The pitch near the onboard SiC chip is 70 mils whereas the pitch near the plastic edge connector is 80 mils.

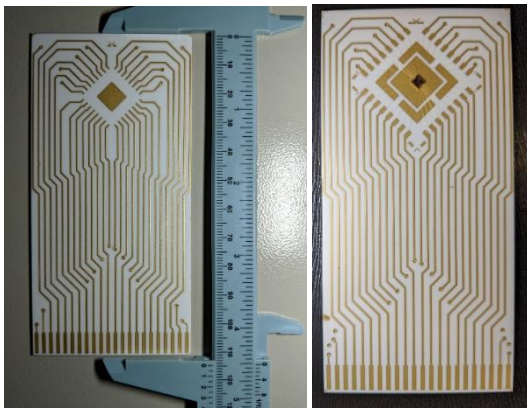


Fig.16: (a) Plain Substrate (b) Substrate with Chip

At 500ºC, the substrate dissipates enough heat to allow a room temperature end connector. This creates the ability to connect to the IC(s) without requiring high temperature wires and their connectors. Therefore, the substrate slides into a room temperature connector on a fixture board.

The fixture board is the only board that contains hand customization to connect the ICs traces to either power or signal pins that go to the NI PXI system. This customization is required due to the limitations of both sides: the IC(s) location pins, wire bonding, and the PXI reed relay multiplexer pinout. The wire bonding is limited to a pad nearby the pin on the chip because the wires cannot touch. The PXI system requires the first 16 signals of an 18-pin connector to be the changeable signals (either supply or measurement). The next two pins of the 18-pin connector are the designated VDD and VSS power bus followed by the two grounds. The power and grounds are split from the 16 signals to provide IC power.

There is an additional switch board between the fixture board and the NI PXI system. This board is called the breakout board that was shown in Fig. 5. The purpose of the breakout board is to connect the NI PXI system to one of the 32 oven possibilities when that specific chip is ready to be measured. The pads of the substrate connect to the NI PXI system's designated signal pins (the first 16 pins) which are the rows

to a NI SwitchBlock matrix of options within NI's software. These options include oscilloscope probes, analog inputs and outputs, DC power and source measuring units. The NI PXI system also contains Reed Relay Multiplexer modules that allow switching per test to different ICs in multiple or the same oven. By using the NI PXI system, testing became less complex and allows various ICs to be tested with the same components.

V. Conclusion

A smaller footprint and scalable testing rig for high temperature electronics was designed and tested. The oven footprint is now a fraction of the size allowing for more ovens and is scalable up to 32 ovens. Since multiple ovens are possible, a networking connection was created by RS422 bus. The ceramic heating block can reach up to 600 °C, which is higher than Venus's surface temperature. The oven control uses a designated temperature and a designated ramp rate to increase the temperature within the oven. The system connects the traces on the substrate to a NI PXI system that allows changing the measuring and/or source pins depending on the LabVIEW test program.

This work is still advancing and being fine-tuned. Capabilities in the process include a ramp down cooling rate, zone heating, and display. The future breakout boards will need to be able to connect up to 70 pads to pins to test next generations of SiC ICs.

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