Processing Choices for Achieving Long Term IC Operation at 500° C

D. Spry and P. Neudeck

NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, OH 44135, david.j.spry@nasa.gov, 216 433-3361

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Abstract: The prospects for beneficial infusion of integrated circuits (ICs) into previously inaccessible extreme-temperature application environments has increased with recent NASA Glenn demonstrations of 4H-SiC Junction Field Effect Transistor & Resistor (JFET-R) chips functioning for over a year at 500 °C in air ambient [1]. This paper focuses on fabrication process choices believed key to demonstrated 500 °C durability that must be considered when porting this uniquely durable IC capability into commercial foundry manufacturing.

Introduction

Stable and long-term functionality is a requirement for beneficial integrated circuit (IC) electronics deployment into applications. While it has been known for decades that wide band gap semiconductor's ability to operate near 500 °C would enable worthwhile benefits to aerospace, automotive, drilling, and other applications, there has essentially been no such practical deployments due to lack of stable long-term operation at this temperature. To address this critical gap to enable IC electronics capability to these important applications, the NASA Glenn SiC JFET-R process was developed emphasizing "over-design for durability" prioritized over other IC performance metrics (e.g., circuit speed). To date, ICs prototyped using this process are the only chips ever reported to demonstrate more than one year of stable operation at 500 °C [1].

The fundamental technology cross-section developed is shown in an experimentally realized cross-section in Fig. 1. For the SiC JFET-R process flow, the "front end of the line" (FEOL) process defines inherently durable transistors and resistors in commercially procured 4H-SiC homoepilayers [2]. The FEOL involves reactive ion etching SiC epi to define JFET and resistors devices along with three ion implants (two n-type, one p-type, all activated by the same anneal) that respectively facilitate source/drain contacts, lowered JFET resistance, and suppresses parasitic field inversion conduction [1,3,4]. The FEOL processing steps are sufficiently straightforward and widely practiced in the manufacture of conventional-temperature SiC high-power devices that NASA chose to migrate them into commercial SiC foundry for the most recent (COVID-19 delayed) "Version 12" JFET-R IC run [5].

The arguably tougher challenge to achieving prolonged IC operation at 500 °C resides at the "back end of the line" BEOL that implements two levels of metal interconnect followed by wire bonding pads. This paper explores key durability aspects the BEOL interconnect process, including experimental annealing results and core fabrication philosophies that to this day are crucially guiding the processing evolution of this technology.

BEOL Anneal Experiments

As described previously, the SiO_2 interlayer dielectrics films seen in Fig. 1 are deposited at 720 °C via low-pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) precursor, while $TaSi_2$ "Metal 1" and "Metal 2" films are deposited via close-proximity sputtering (21 mm target to substrate space) in order to minimize void formation over topologic features [1,3].

A series of accelerated age testing experiments provided key insights that foundationally guided BEOL process development choices. A series of individual non-functioning chips from an earlier unsuccessful version of the NASA Glenn JFET IC were each subjected to 30 minute anneals in either N_2 or H_2:N_2 4% forming gas at one of the following temperatures: 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, or 1370 °C. All samples were optical-imaged before and after the anneal and selected samples were then focused ion beam (FIB) cross-sectioned to further document basic material failure points. The four district chip features were in-depth examined as follows: 1) the edge of a wide Metal 2 power bus, 2) the central region of a larger area capacitor, 3) an "IrIS" bond pad [6] capped with 1 µm gold to somewhat mimic the presence of a Au ball wire bond had the chip had been fully packaged [7], and 4) an uncapped IrIS bond pad.

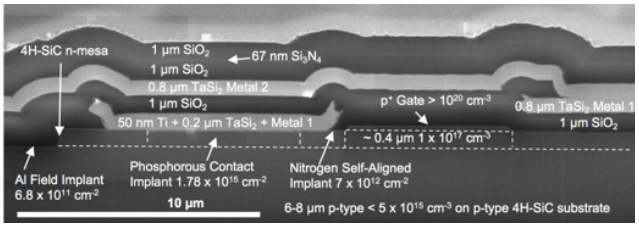

Fig. 1. Scanning electron micrograph cross-section of the source and gate region of an as-fabricated 500 °C durable 4H-SiC JFET with two levels of interconnect from the NASA Glenn Version 10 prototype wafer run [1]

Table I summarizes the major outcomes of this study. Each of the 4 columns of the table corresponds to one of these 4 respective chip features while each row corresponds to the anneal temperature the chip was subjected to. The thicker red lines in the table demarcate the ascertained effective upper temperature limit of the BEOL processing for each respective chip feature studied. As seen in Table I, the bond pads effectively limit the overall chip microstructural durability.

Bond Pad Feature Temperature Limits: As supported by the post-anneal cross-section images collected from 500 °C, 700 °C, and 900 °C annealed IrIS bond pads shown in Fig. 2, the first clear BEOL structural temperature limit is found just above 700 °C. For the Fig. 2a image after 500 °C anneal the IrIS stack has segregated into its planed layers of $TaSi_2$ that contacts the underlying SiC, $PtSi_X$, Ir, Pt and a top Au metal. While the Fig. 2b post 700 °C image of bond pad without Au cap reveals a thickened $PtSi_X$ zone that comes closer to SiC interface, the contact remains a smooth and abrupt interface between $TaSi_2$ and SiC. However, the Fig. 2c image of 700 °C anneal IrIS stack with Au cap shows evidence of oxygen accumulation at the Au/Pt interface which could become a bonding failure point if the Au ball bond attached during chip packaging is not thick enough to prevent oxygen penetration. By 900 °C, the Fig. 2d image shows Pt has reached the SiC interface along with evidence of voiding (white arrow).

Oxide and Metal 2 Temperature Limits: The second clear BEOL structural temperature limit is found at 1200 °C for the LPCVD TEOS SiO_2 and $TaSi_2$. The Fig. 3a, b, and c cross-section images of samples after 1000 °C and 1100 °C anneals all show about the same $TaSi_2$ microstructure and Metal 2 trace shrinkage along the edges of the metal. The largest

TABLE I

EXPERIMENTAL SUMMARY OF ANNEALS ON SELECTED CHIP FEATURES (COLUMNS) AS A FUNCTION OF ANNEALING TEMPERATURE (ROWS)

Anneal T °C	Power Bus	Capacitor	Au Capped Bond Pad	Uncapped Bond Pad
500				Nominal
600				
700			w/Au +oxide	PtSix grows
800				
900				Pt reaches SiC
1000	Nominal			
1000	FMG ~ N2	Metal 1 vs. 2		
1100	~1000			
1200	TaSi2 chg			
1300	3 layers			
1370	1 layer		Au/Pt trees	Pt nano wires

N2:H2 Foming gas 4%
FIB image (not shown)
FIB image shown
SEM image (not shown)
Optical image (not shown)
upper temperature limit

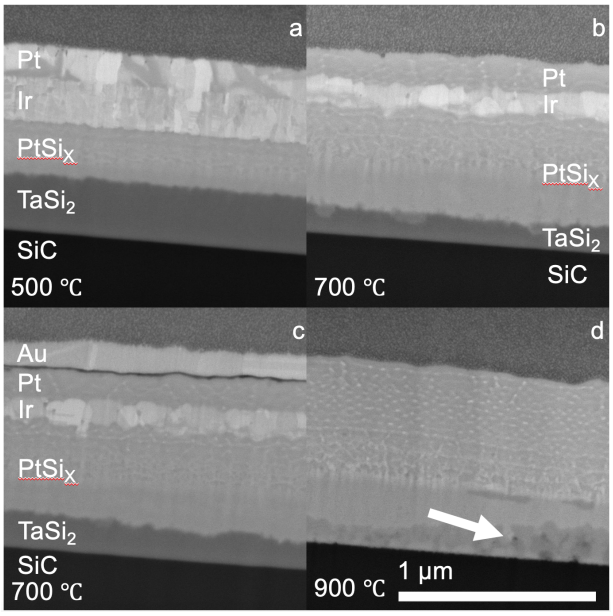

Fig. 2. FESEM images of a FIB cross-section of "IrIS" bond pads, each subjected to single 30 minute anneal in N2 at (a) 500 °C, (b, c) 700 °C, and (d) 900 °C. For the 900 °C anneal Pt has reached the SiC surface and there is onset of void formation as denoted by white arrow.

difference in these images/samples is that samples anneal in FMG exhibits more charging of the dielectric despite the fact that all images were taken under the same field emission scanning electron microscope (FESEM) conditions. For sample subjected to 1200 °C anneal, Figure 3d shows that at 1200 °C the amount of $TaSi_2$ shrinkage increased slightly along with observable change to the $TaSi_2$ microstructure. The top and bottom interfaces of the $TaSi_2$ Metal 2 trace is also roughening. The sample annealed at 1300 °C (Fig. 3e) shows clear relaxation of the dielectric resulting in a large void and substantial restructuring of the $TaSi_2$, yet some of the layered TaSi2 microstructure is still apparent. The Fig. 3f image of the 1370 °C annealed sample reveals a nearly circular relaxation void with evidence of metal redeposition on the interior walls of the void, and there is also no longer layered microstructure evident to the $TaSi_2$.

It is worth noting that no dielectric cracks were observed to form on any of these samples. Dielectric cracks have been observed in subsequent prototype IC generations that added Si_3N_4 layers (e.g., Fig. 1) that function as mitigation against mobile ion contamination circuit effects [1,5].

Comparison of Metal 1 vs. Metal 2: In order to assist ohmic contact formation to SiC, titanium was deposited as the first layer of the Metal 1 Ti/$TaSi_2$ stack in early generations NASA Glenn SiC JFET-R prototype ICs. Fig. 4 shows a cross-sectional image recorded near the horizontal center of a large-area Metal 1 / TEOS SiO_2 / Metal 2 capacitor device following annealing at 1000 °C for 30 minutes in FMG. Note that the Metal 2 $TaSi_2$ layer exhibits more-ordered layer-

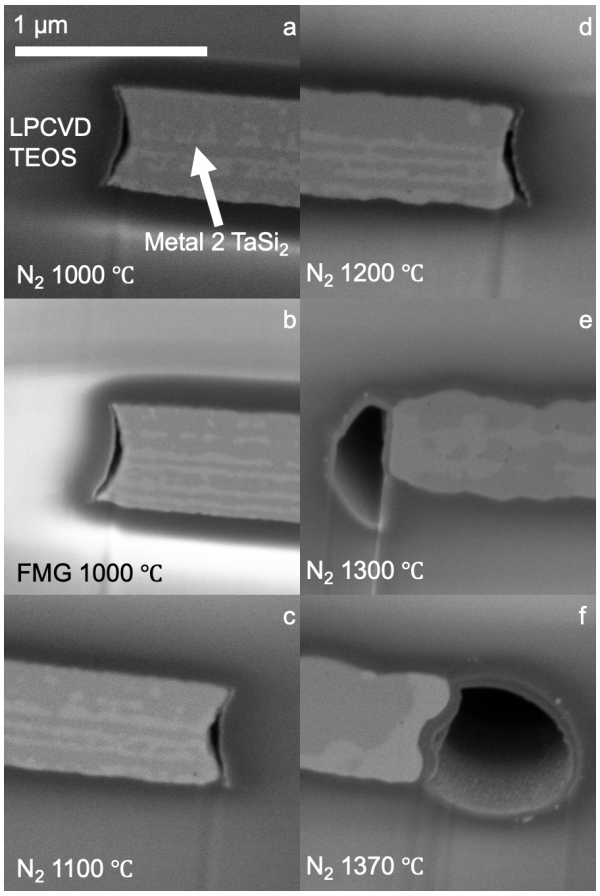

Fig. 3. FESEM images of a FIB cross-section of edges of Metal 2 power bus line feature. All anneals are 30 minutes. (a), (c)-(f), were annealed in N_2. (b) was annealed in N_2:H_2 4% FMG.

structure than Metal 1, and there is also evidence of voids in the Metal 1 titanium layer. It can also be observed in Fig. 4 that Metal 1 is noticeably thicker than Metal 2.

Void formation is mitigated with titanium deposited only inside etched Via 1 areas where SiC ohmic contact is needed using a plug-metal process described in [1,8].

BEOL Process Integration Approach

In addition to the fundamental microstructure thermal behaviors described in the preceding section, this section describes important core process integration approaches adopted to maximize BEOL interconnect and bonding pad long-term 500 °C operational durability.

The first is to take full advantage of the physical hardness of SiC as the foundation for anchoring the highest-stress features. In particular, the "IrIS" metal bond pads are over 100 µm in diameter and physically the largest features on each SiC chip, and they also withstand the largest materials mismatch in Coefficient of Thermal Expansion (CTE) [6]. To withstand the CTE mismatch over the inherently larger than 500 °C range of desired operating temperature, the wire bonding pads

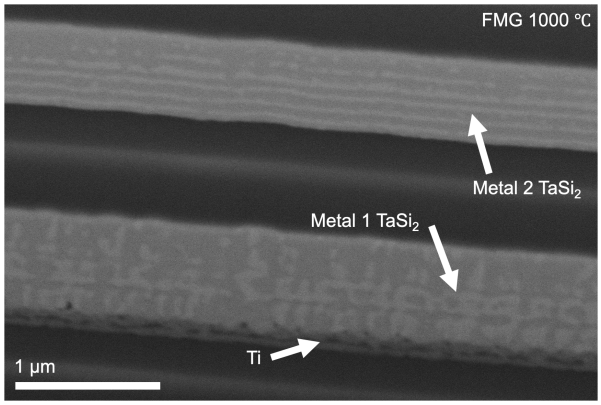

Fig. 4. FESEM images of a FIB cross-section of central region of Metal 1 / TEOS SiO2 / Metal 2 capacitor following 30-minute 1000 °C anneal in N_2:H_2 4% FMG.

are strategically anchored directly to the single-crystal SiC, and they are also location-confined to outer periphery regions of each chip. To further limit/confine stress/damage effects, the bond pads are also physically isolated from any direct attachment of Metal 1 and Metal 2 interconnect traces. Heavily doped SiC serves as the electrical "bridge" of signals between "IrIS" bond pads and Metal 1 interconnect traces [9].

Another major durability-enhancing philosophy is to minimize unique processing steps and their associated processing materials. Instead of employing Cu interconnect traces with $TaSi_2$ (or other material) liners as done for many silicon ICs, 1 µm thick $TaSi_2$ is instead employed as the sole material for both levels of interconnecting metal between on-chip transistors and resistors [1,3]. Close-proximity (21 mm target to wafer spacing) sputtering if $TaSi_2$ is carried out via pulsed-DC or High-Power Impulse Magnetron Sputtering (HIPIMS). Other methods of $TaSi_2$ deposition (e.g., CVD) as well as silicon-rich films may also work, so long as uniformly dense film coverage over ~ 1 µm surface topology features (imposed by underlying features such as etched SiC mesas as seen in Fig. 1) is achieved.

The third key philosophy is to deposit all dielectric layers at the same temperature (720 °C) that is also well above the desired 500 °C designed IC operating temperature. This approach ensures that maximum film stresses occur near room temperature instead of high temperature. SiO_2 dielectric is deposited at 720 °C using Low Pressure Chemical Vapor Deposition (LPCVD) via TetraEthyl OrthoSilicate (TEOS) precursor. Thin stochiometric Si_3N_4 films (again, LPCVD deposited at 720 °C) are sandwiched between SiO_2 layers (as seen in Fig. 1) with startlingly profound impact to high temperature durability reported in [10].

A fourth key philosophy is achieved manufacturability critical to technology adoption and infusion. With modest adjustments, the NASA Glenn 500 °C durable SiC JFET-R fabrication process is compatible with semiconductor mass-production tools. Insulator deposition is carried out using standard LPCVD tube furnace hardware with some non-standard procedures. All materials used in the BEOL

processing are compatible with most silicon IC manufactures except for the bond pad metals of iridium, gold, and platinum, which would require separate equipment and accommodations. Advantageously, the bond pad metal and corresponding via-3 features are large simple features and could even be done in a separate facility with a contact aligner.

Further processing optimizations are actively being investigated. One primary focus/challenge of on-going improvement is to retire dielectric cracking as the predominant high-T failure mechanism [1,3,10] while preserving Si_3N_4 as an impediment to deleterious oxygen and sodium penetration. A second major focus is to shrink all layout feature sizes in order to substantially upscale chip complexity. Towards this end, stepper-based lithography is planned to supplant contact-aligner based lithography in future SiC JFET-R IC runs [11].

The BEOL described here might also be adapted for use with other transistor approaches including planar implanted SiC JFETs or SiC bipolar junction transistors. However, heteroepitaxial transistor technologies (e.g., III-N heterojunction FETs) will face additional obstacles to 500 °C durability including higher CTE mismatch stress and higher reactivity/diffusivity than inherent to the SiC homoepilayer approach.

Conclusion

This paper has summarized important processing and materials aspects of achieving prolonged SiC JFET-R ICs capable of more than a year of 500 °C operation. With modest investment in modified equipment and materials, this technology is portable to commercial foundry manufacturing. Such new capability promises to unlock extreme-temperature IC benefits to a variety of important aerospace, automotive, and deep-well drilling applications.

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Acronyms

BEOL: Back End Of Line
CTE: Coefficient of Thermal Expansion
CVD: Chemical Vapor Deposition
FEOL: Front End Of Line
FESEM: Field Emission Scanning Electron Microscope
FET: Field Effect Transistor
FIB: Focused Ion Beam
FMG: Forming Gas
HIPIMS: High-Power Impulse Magnetron Sputtering
IC: Integrated Circuit
IrIS: Iridium Interfacial Stack
JFET: Junction Field Effect Transistor
JFET-R: Junction Field Effect Transistor & Resistor
LPCVD: Low Pressure Chemical Vapor Deposition
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
NASA: National Aeronautics and Space Administration
SiC: Silicon Carbide
T: Temperature
TEOS: TetraEthyl OrthoSilicate